



Monolithic N-Channel JFET Duals

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Max (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
U5545NL	-0.5 to -4.5	-50	1.5	-50	5
SST/U5546NL	-0.5 to -4.5	-50	1.5	-50	10
SST/U5547NL	-0.5 to -4.5	-50	1.5	-50	15

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 3 pA
- Low Noise
- High CMRR: 100 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

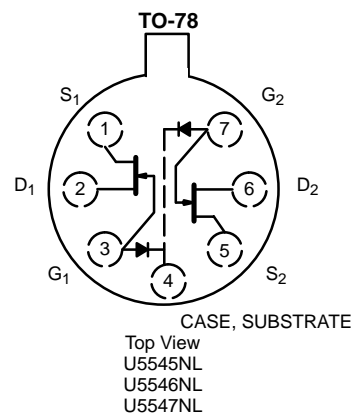
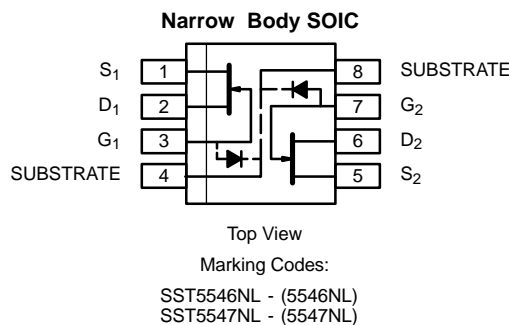
DESCRIPTION

The SST/U5545NL Series are monolithic dual n-channel JFETs designed to provide high input impedance ($I_G < 50$ pA) for general purpose differential amplifiers. The U5545NL features minimum system error and calibration (5-mV offset maximum).

The SST5546NL/47NL in the SO-8 package provide ease of manufacturing. The symmetrical pinout prevents improper orientation. These part number are available with tape-and-reel options for compatibility with automatic assembly methods.

Pins 4 and 8 on the SST series and pin 4 on the U series part numbers enable the substrate to be connected to a positive, external bias (V_{DD}) to avoid latchup.

The hermetically sealed TO-78 package is available with full military processing.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -50 V
 Gate Current 30 mA
 Lead Temperature ($1/16$ " from case for 10 sec.) 300°C
 Storage Temperature -65 to 200°C
 Operating Junction Temperature -55 to 150°C

Power Dissipation : Per Side^a 250 mW
 Total^b 500 mW

Notes
 a. Derate 2 mW/°C above 25°C
 b. Derate 4 mW/°C above 25°C

SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ ^a	Limits						Unit
				U5545NL		SST/U5546NL		SST/U5547NL		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-57	-50		-50		-50		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 15 V, I _D = 0.5 nA	-2	-0.5	-4.5	-0.5	-4.5	-0.5	-4.5	V
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 15 V, V _{GS} = 0 V	3	0.5	8	0.5	8	0.5	8	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -30 V, V _{DS} = 0 V	-10		-100		-100		-100	pA
		T _A = 150 °C	-20		-150		-150		-150	nA
Gate Operating Current	I _G	V _{DG} = 15 V, I _D = 200 μA	-3		-50		-50		-50	pA
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V	0.7							V
Dynamic										
Common-Source Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, V _{GS} = 0 V f = 1 kHz	2.5	1.5	6.0	1.5	6.0	1.5	6.0	mS
Common-Source Output Conductance ^b	g _{os}		2		25		25		25	μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V f = 1 MHz	3.5		6		6		6	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		1.3		2		2		2	
Equivalent Input Noise Voltage	e _n	V _{DS} = 15 V, I _D = 200 μA f = 10 Hz	20		180					nV/ √Hz
Noise Figure	NF	R _G = 1 MΩ	0.1		3.5					dB
Matching										
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 15 V, I _D = 50 μA			5		10		15	mV
		V _{DG} = 15 V, I _D = 200 μA			5		10		15	
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 15 V, I _D = 200 μA T _A = -55 to 125 °C			10		20		40	μV/ °C
Saturation Drain Current Ratio ^c	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 15 V, V _{GS} = 0 V	0.98 ^c	0.95	1	0.9	1	0.9	1	
Transconductance Ratio ^c	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 15 V, I _D = 200 μA f = 1 kHz	0.99 ^c	0.97	1	0.95	1	0.9	1	

Notes

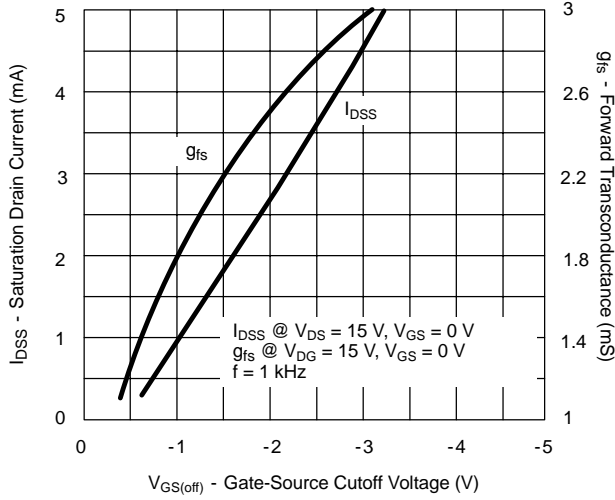
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
- Assumes smaller value in the numerator.

NQP

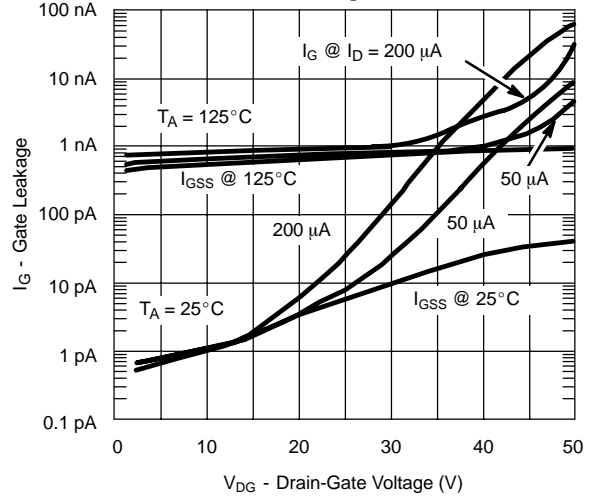


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

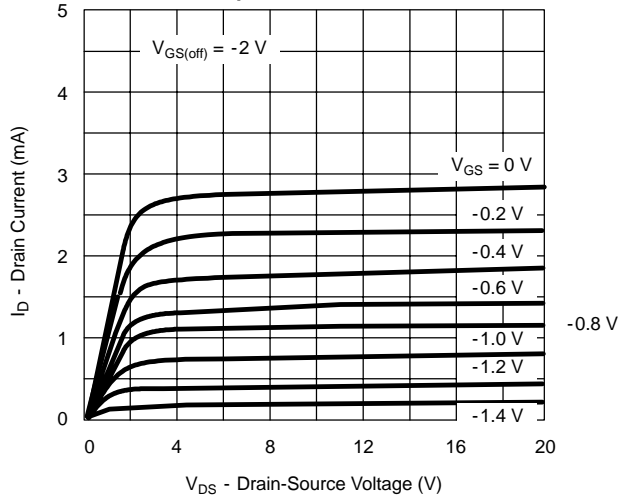
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



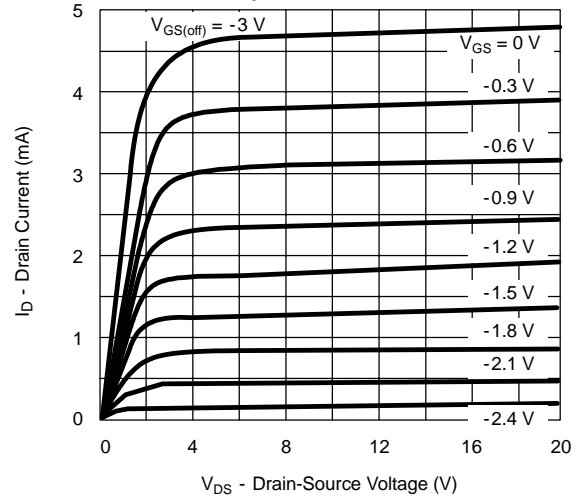
Gate Leakage Current



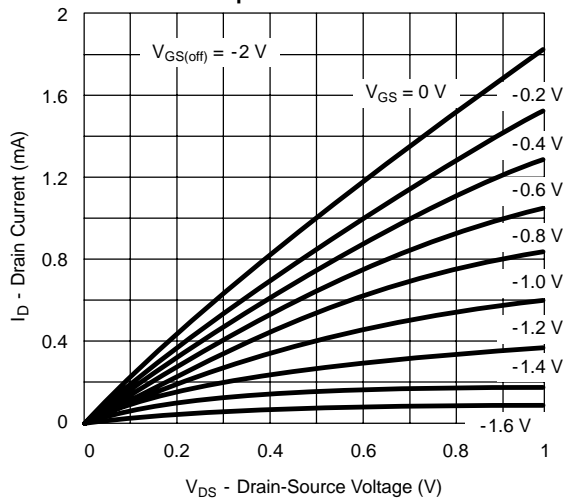
Output Characteristics



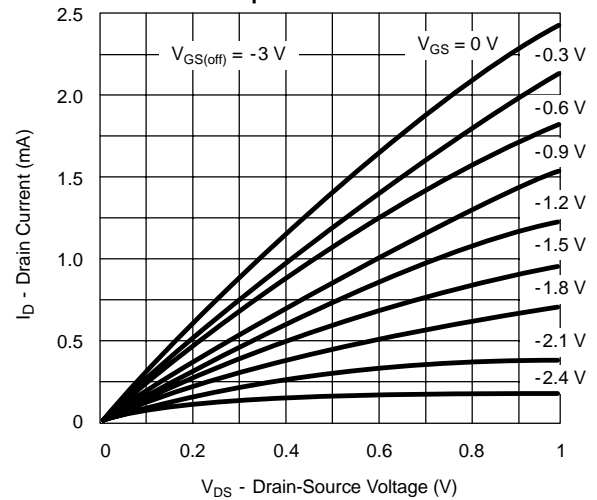
Output Characteristics



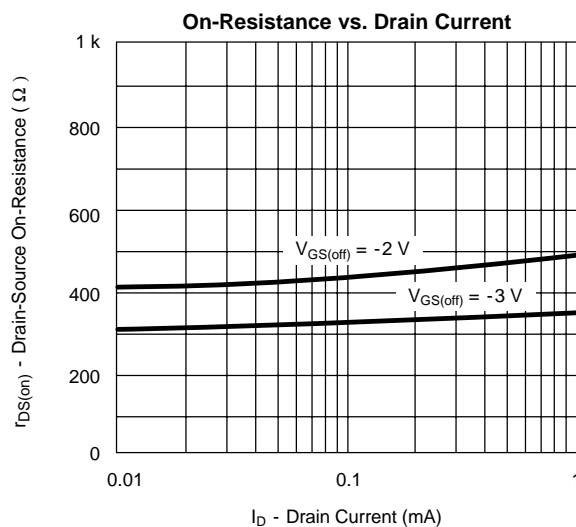
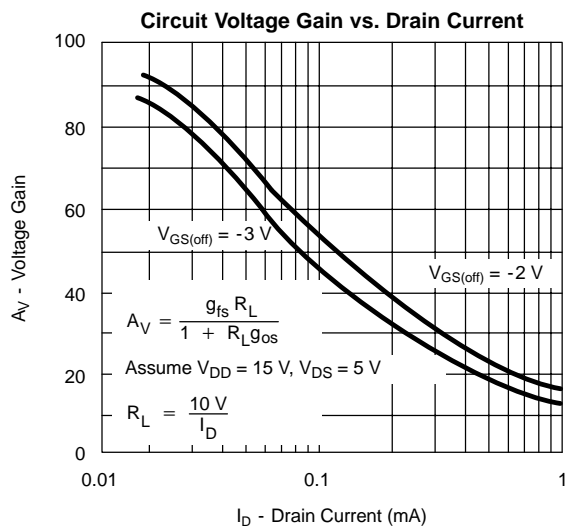
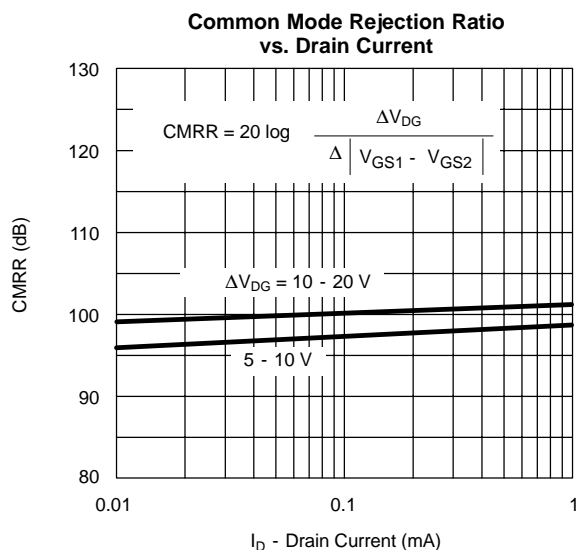
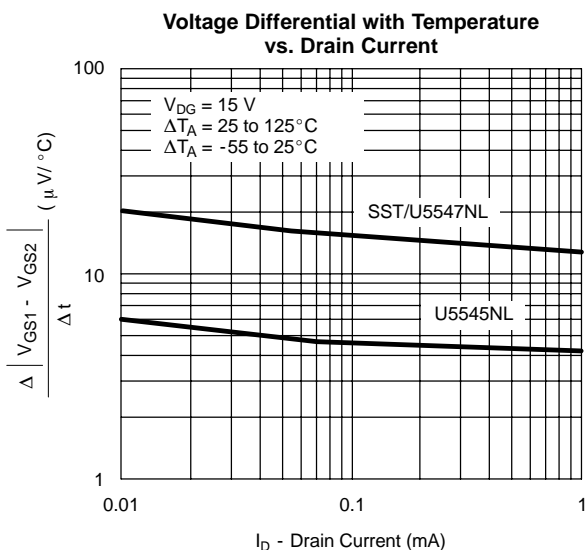
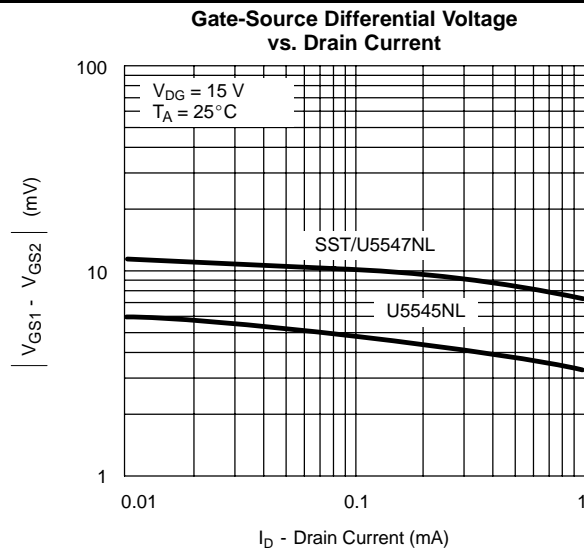
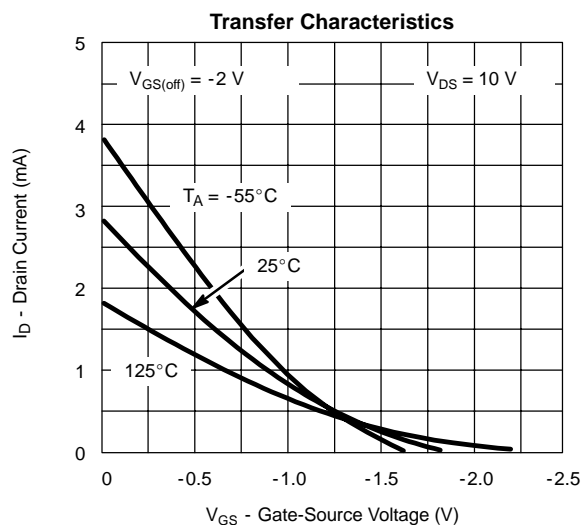
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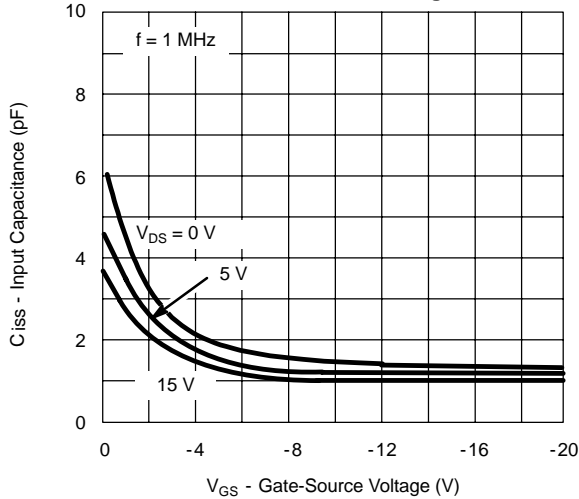


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

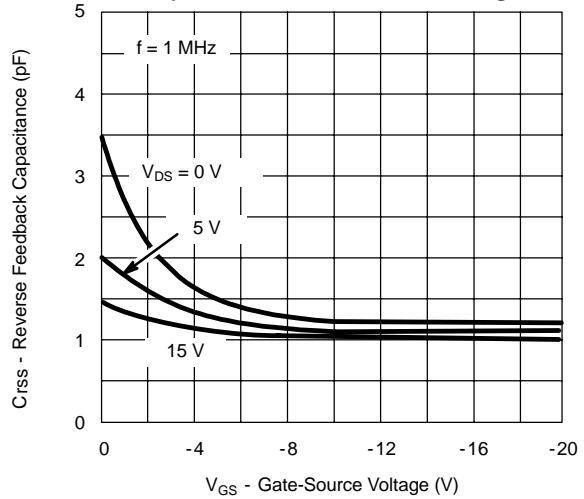


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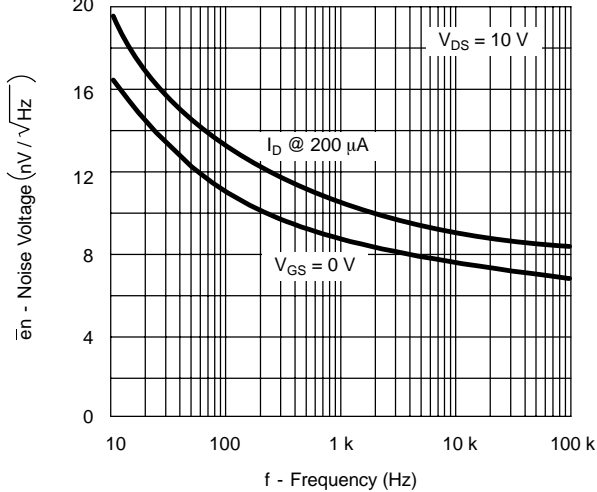
Common-Source Input Capacitance vs. Gate-Source Voltage



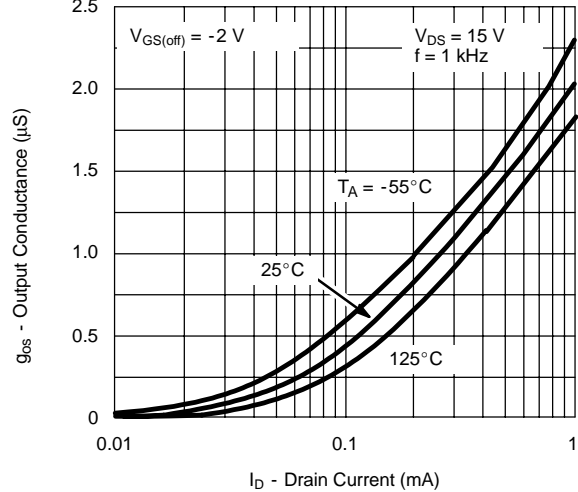
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



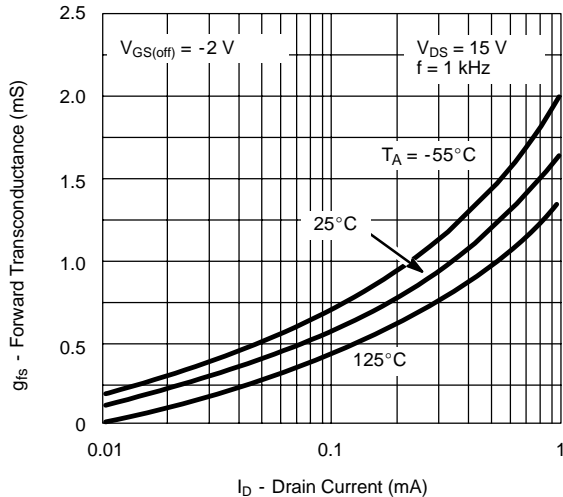
Equivalent Input Noise Voltage vs. Frequency



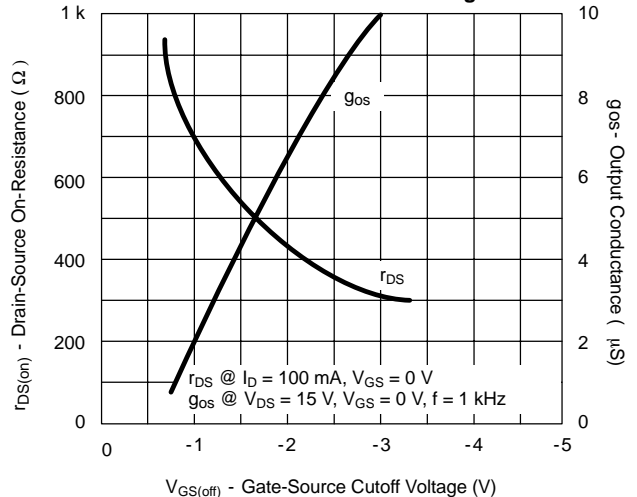
Output Conductance vs. Drain Current



Common-Source Forward Transconductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage





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