



## Monolithic N-Channel JFET Duals

PRODUCT SUMMARY				
$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
-1 to -6	-25	4.5	-1	20

### FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 90 dB

### BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- High-Speed Performance
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

### APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

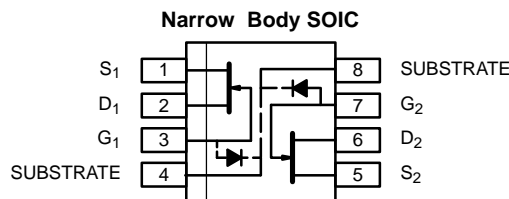
### DESCRIPTION

The SST441NL is a monolithic high-speed dual JFET mounted in a single SO-8 package. This JFET is an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

Pins 4 and 8 on the SST441NL and pin 4 on the U441NL part numbers enable the substrate to be connected to a positive, external bias ( $V_{DD}$ ) to avoid latchup.

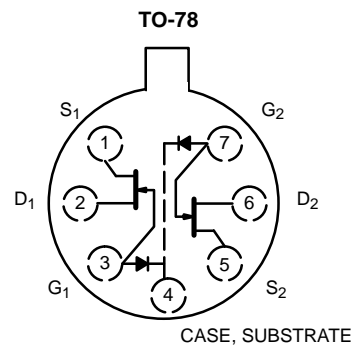
The U441NL in the hermetically sealed TO-78 package is available with full military processing.

The SO-8 package provides ease of manufacturing. The symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.



Top View

Marking Codes:  
SST441NL - 441NL



Top View  
U441NL

### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-25 V
Gate Current	50 mA
Lead Temperature ( $1/16$ " from case for 10 sec.)	300°C
Storage Temperature	-55 to 150°C
Operating Junction Temperature	-55 to 150°C

Power Dissipation:	Per Side <sup>a</sup>	300 mW
	Total <sup>b</sup>	500 mW

- Notes
- Derate 2.4 mW/°C above 25°C
  - Derate 4 mW/°C above 25°C

For applications information see AN102.

SPECIFICATIONS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ <sup>a</sup>	Max	
<b>Static</b>						
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-25	-35		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA	-1	-3.5	-6	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V	6	15	30	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0 V		-1	-500	pA
		T <sub>A</sub> = 125 °C		-0.2		nA
Gate Operating Current	I <sub>G</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA		-1	-500	pA
		T <sub>A</sub> = 125 °C		-0.2		nA
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = 1 mA, V <sub>DS</sub> = 0 V		0.7		V
<b>Dynamic</b>						
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 1 kHz	4.5	6	9	mS
Common-Source Output Conductance	g <sub>os</sub>				20	200
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 100 MHz		5.5		mS
Common-Source Output Conductance	g <sub>os</sub>				30	
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 1 MHz		3.5		pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>				1	
Equivalent Input Noise Voltage	e <sub>n</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 10 kHz		4		nV/ √Hz
<b>Matching</b>						
Differential Gate-Source Voltage	V <sub>GS1</sub> - V <sub>GS2</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA		7	20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA T <sub>A</sub> = -55 to 125 °C		10		μV/°C
Saturation Drain Current Ratio <sup>c</sup>	$\frac{I_{DSS1}}{I_{DSS2}}$	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V		0.98		
Transconductance Ratio <sup>c</sup>	$\frac{g_{fs1}}{g_{fs2}}$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 1 kHz		0.98		
Common Mode Rejection Ratio	CMRR	V <sub>DG</sub> = 10 to 15 V, I <sub>D</sub> = 5 mA		90		dB

## Notes

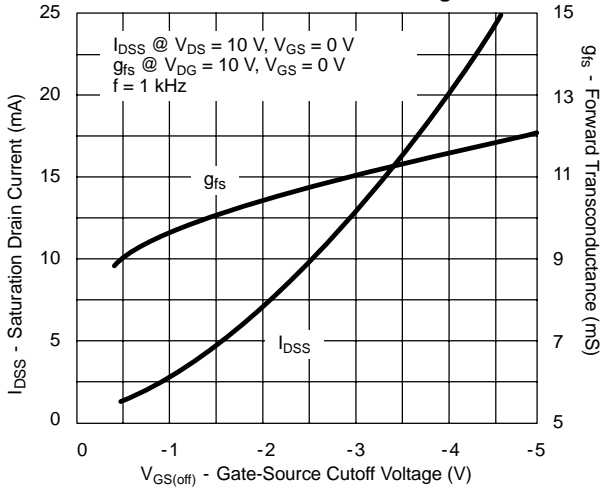
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
 b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.  
 c. Assumes smaller value in the numerator.

NNZ

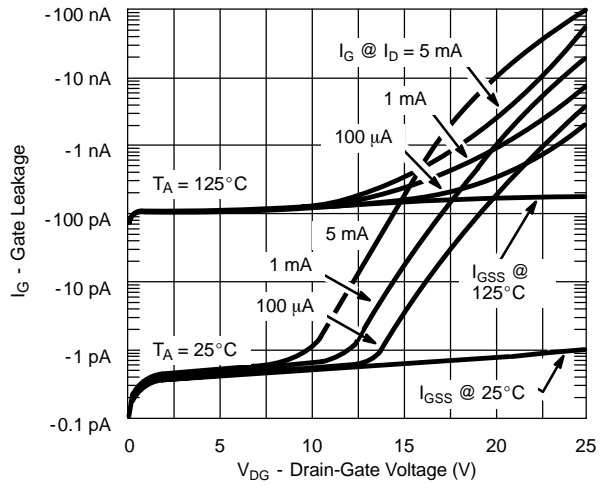


**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

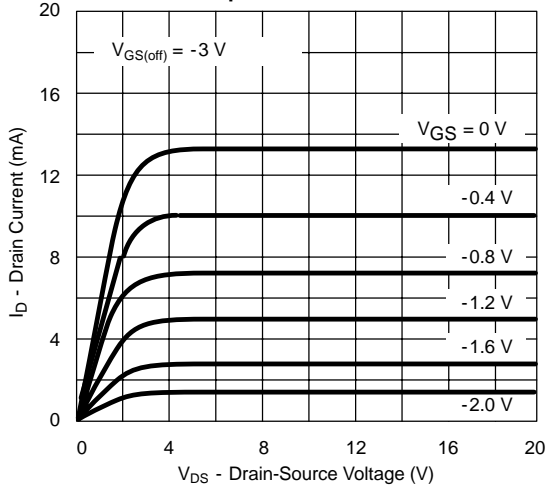
**Drain Current and Transconductance vs. Gate-Source Cutoff Voltage**



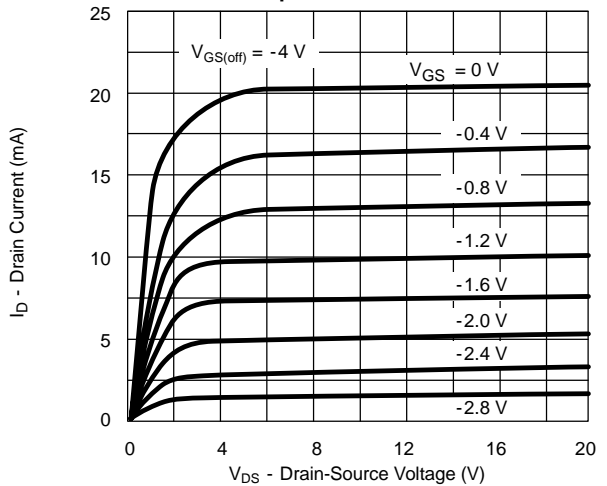
**Gate Leakage Current**



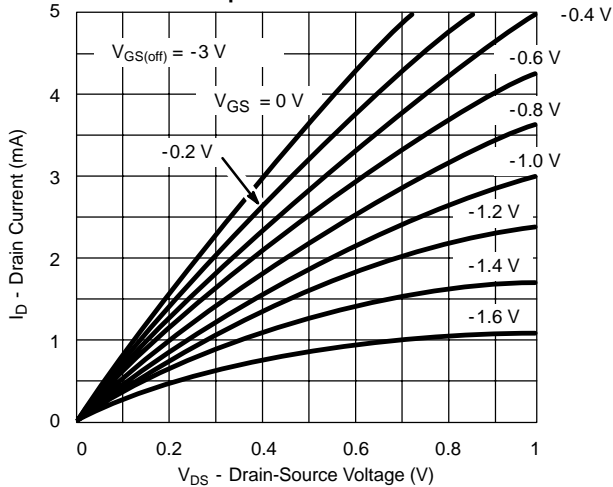
**Output Characteristics**



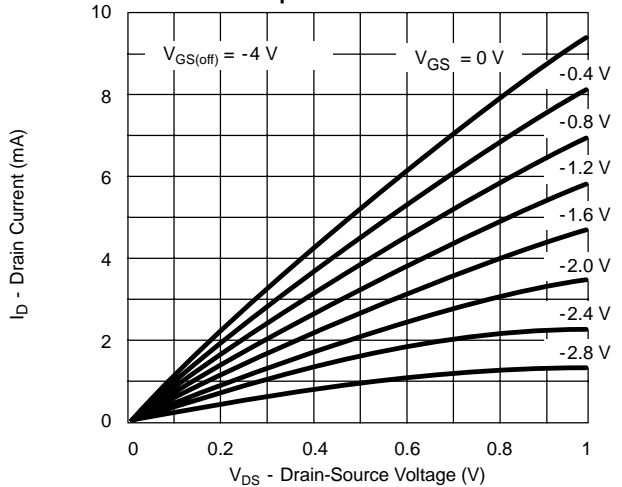
**Output Characteristics**



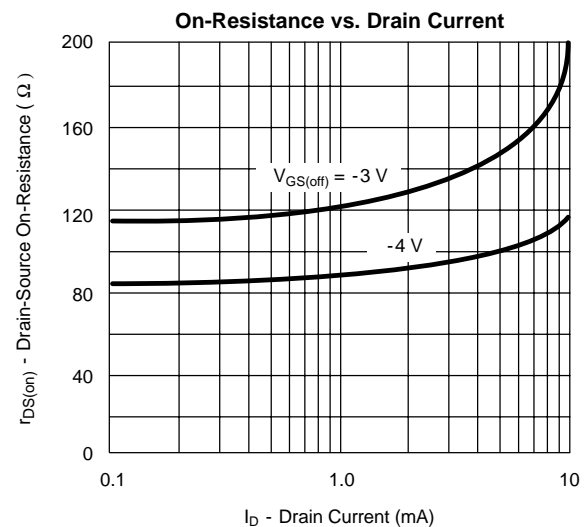
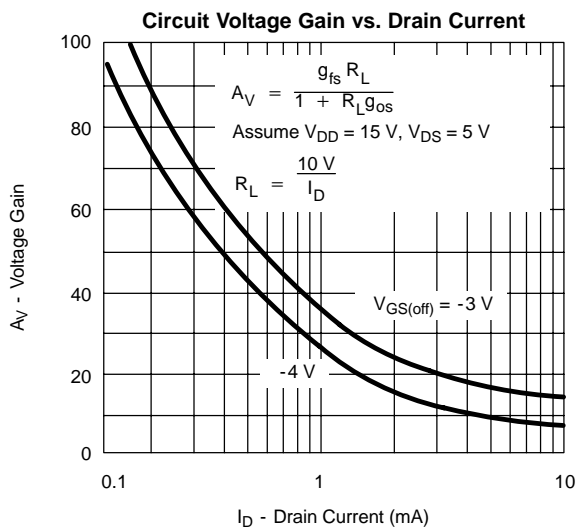
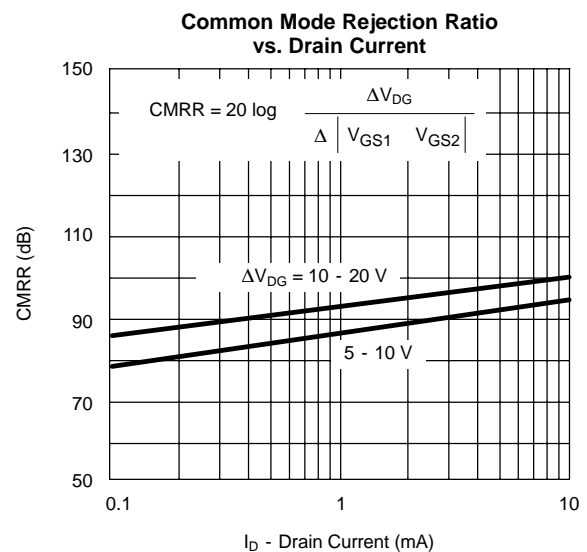
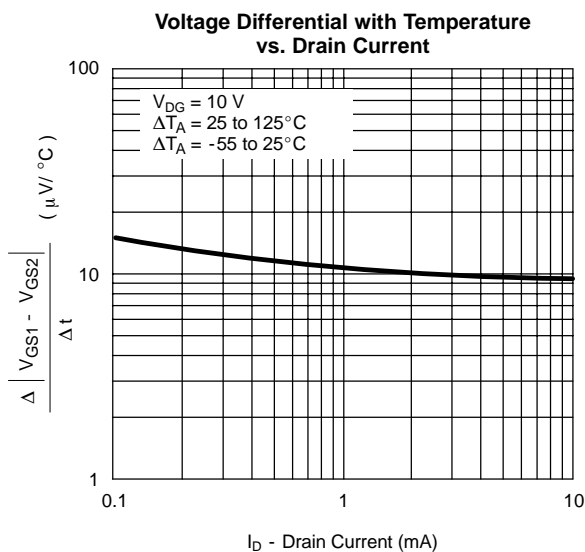
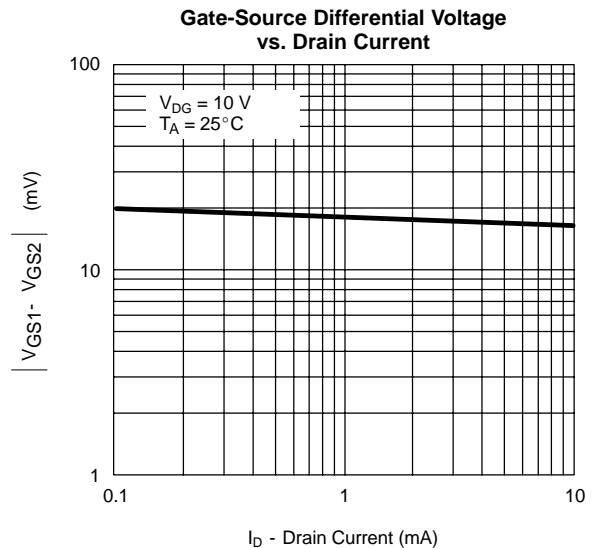
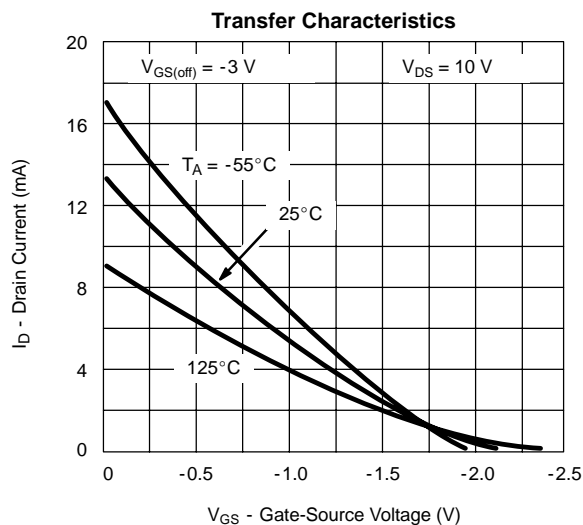
**Output Characteristics**



**Output Characteristics**

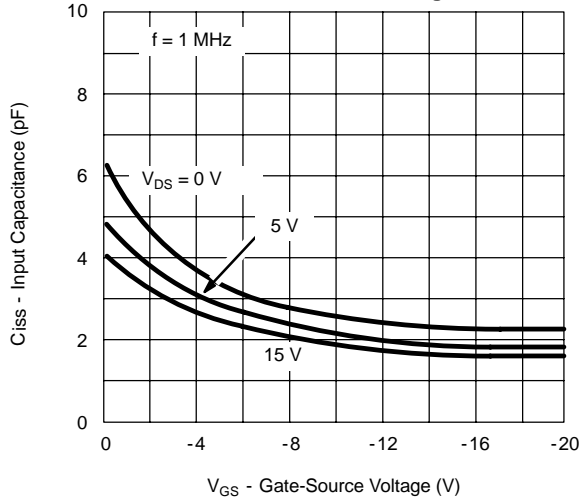


### TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

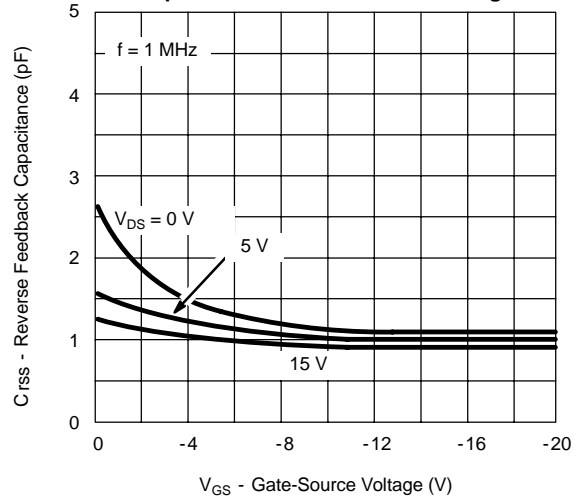


**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

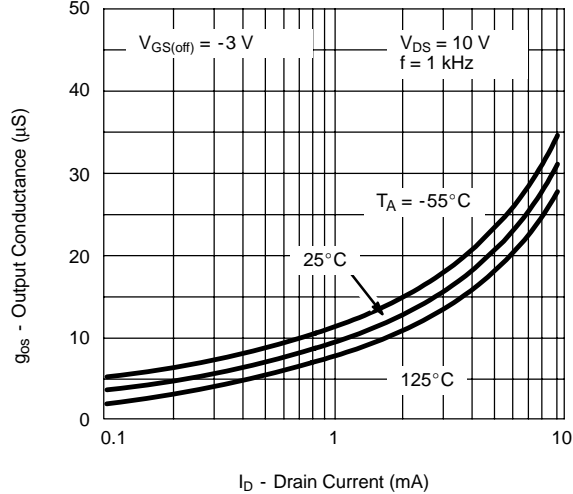
**Common-Source Input Capacitance vs. Gate-Source Voltage**



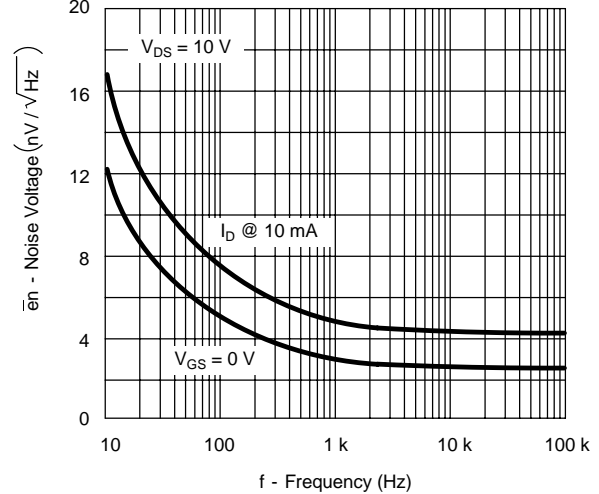
**Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage**



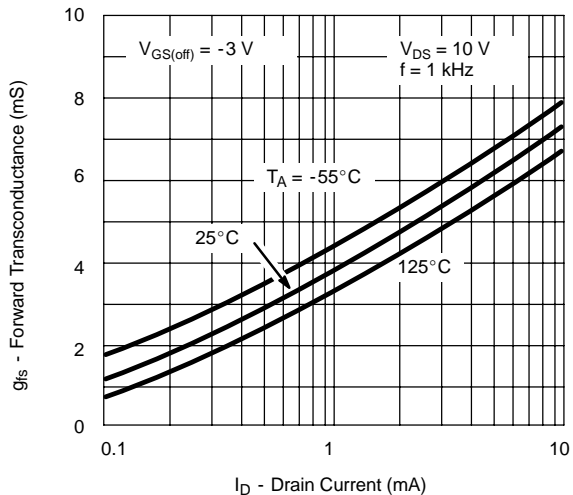
**Output Conductance vs. Drain Current**



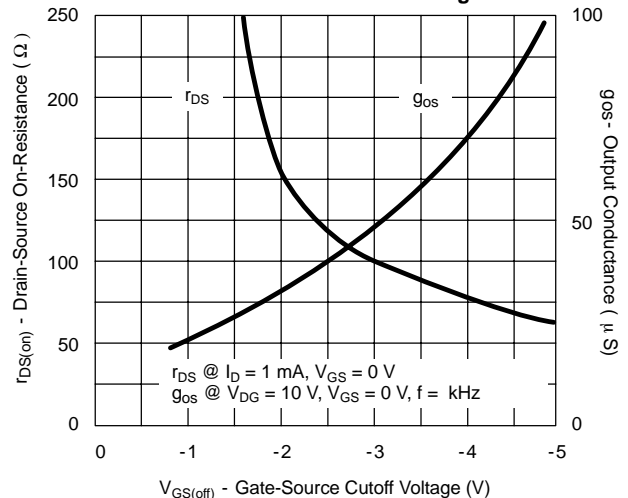
**Equivalent Input Noise Voltage vs. Frequency**



**Common-Source Forward Transconductance vs. Drain Current**



**On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage**





## Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.