Edge7804

133 MHz Quad Pin Electronics Driver and Window Comparator

SEMTECH

TEST AND MEASUREMENT PRODUCTS — PRELIMINARY

Description

The Edge7804 is a quad channel, monolithic ATE pin electronics solution manufactured in a high-performance BiCMOS process.

The Edge7804 operates up to 133 MHz with up to 3V signals, and 100 MHz with 5V signals.

Each channel has a three-statable driver capable of generating 5.4V swings over a –0.2V, +5.2V range. Drivers have independent high and low input levels that are buffered internally. Drivers feature a self-calibrating source impedance, programmable in the range 48Ω to 110Ω. The source impedance of all drivers matches R_{EREF}/100, where R_{EREF} is the external reference resistor. Each channel's dual comparator has a range of –2.0V to +5.5V.

A channel's driver and comparators are connected internally via high voltage switches to the VIO pin. These switches provide a means to disconnect the driver and comparator from the VIO pin.

The Edge7804 contains an independent network of high voltage switches intended to connect an external Parametric Measurement Unit (EPMU) to any channel (or channels) output on the channel's POUT pin. The EPMU can have a range of –4.75V to +9.75V, up to ± 40 mA. Typically, a channel's VIO and POUT pins are connected together externally.

Each channel contains a continuity test circuit (CTC) with a switch to connect it to the channel's POUT pin. This circuit forces a current up to –250 µA, and tests the resulting voltage with a 0 to –2V programmable limit. The result is tested by the channel's comparator.

Each channel contains a 2KΩ pull-up resistor with a switch to connect it to the channel's POUT pin.

The channel's function and connections are programmed using a serial interface. An individual channel's function can be programmed, or a function of any set of channels (of multiple Edge7804s) can be programmed in parallel where each channel can belong to none, one, or more (up to 8) sets.

The Edge7804 features the inclusion of all four channels of pin electronics into a 128 pin package.

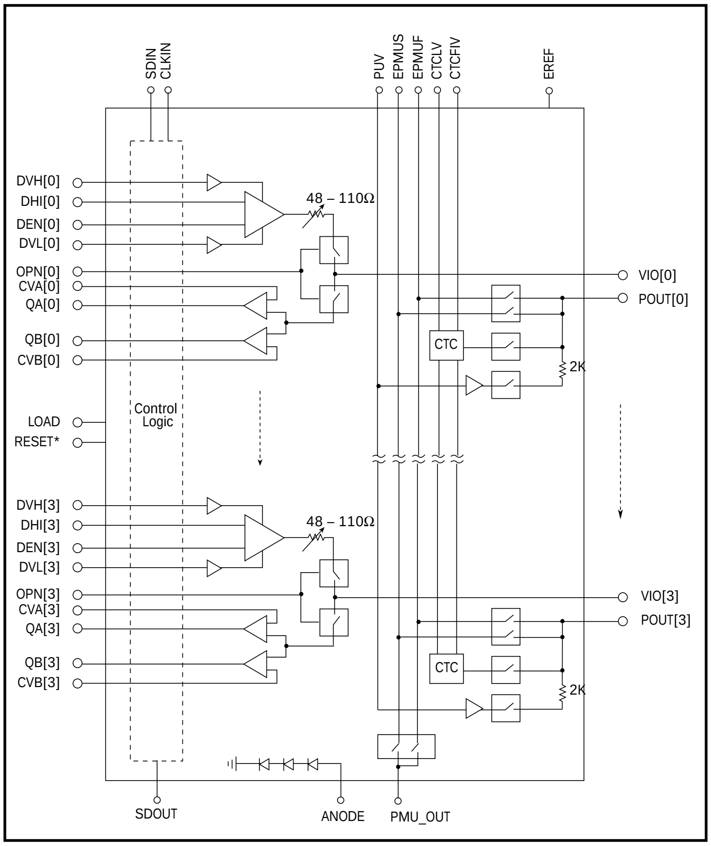
Features

- Four Integrated Three-Statable Drivers and Window Comparators
- Driver Voltage Range –0.2V, +5.2V
- Comparator Voltage Range –2.0V to +5.5V
- Internal Disconnect Switches
- Internal Switches to an External PMU, Range –4.75V to +9.75V, up to ± 40 mA
- Per Pin Pull-Up/Down 2KΩ to (0V to +5V)
- Per Pin Continuity Test (Force Current up to –250 µA, Limit Voltage 0 to –2V)
- Self-Calibrating Driver Source Impedance to an External Reference (48Ω to 110Ω)
- Low Power Dissipation (250mW/channel quiescent)
- 128 Pin MQFP Package (with Internal Heat Spreader)

Applications

- Design for Test/Structural Pins in ATE
- Low Cost
  - Logic Testers
  - Memory Testers
  - ASIC Verifiers
  - Mixed Signal Testers

Functional Block Diagram



PIN Description

[0:3] Refers to Channels 0, 1, 2 or 3

Pin #	Pin Name	Description
Driver, Comparator		
12, 27, 76, 91	OPN[0:3]	LV_TTL input that opens switches that disconnect the driver and comparator from VIO. This input overrides the individual switch register bits non destructively.
15, 24, 79, 88	VIO[0:3]	Device input/output of each channel.
127, 40, 63, 104 128, 39, 64, 103	DHI, DHI*[0:3]	"Flex" differential input digital pins which select the driver high or low level.
1, 38, 65, 102 2, 37, 66, 101	DEN, DEN*[0:3]	"Flex" differential input pins which control the driver being active or in a high impedance state.
126, 41, 62, 105 125, 42, 61, 106	DVH, DVL[0:3]	High impedance analog voltage inputs which determine the driver high and low levels. Connect a 0.22µf capacitor to ground for bypassing reasons.
16, 23, 80, 87 14, 25, 78, 89	DBH, DBL[0:3]	Driver level buffer outputs for high and low levels. Connect a 0.47 µF capacitor to ground for bypassing reasons.
124, 43, 60, 107 123, 44, 59, 108	CVA, CVB[0:3]	Analog inputs which set the A and B comparator thresholds.
10, 29, 74, 93 9, 30, 73, 94	QA, QA*[0:3]	Differential digital outputs of comparator A.
8, 31, 72, 95 7, 32, 71, 96	QB, QB*[0:3]	Differential digital outputs of comparator B.
PMU		
111	PMU_OUT	PMU test point for the anode of the thermal diode string.
5, 34, 69, 98	POUT[0:3]	Parametric Measure Unit input/output of each channel.
110	EPMUF	External parametric measurement for force input.
109	EPMUS	External parametric measurement for sense input.
114	PUV	Pull-up voltage input.
120	CTCLV	Continuity test circuit limit voltage.
118	CTCFIV	Continuity test circuit force current voltage.
Control		
54	RESET*	Active low chip reset. Resets the internal registers. It is an asynchronous input not requiring any CLKIN transitions.
51	CLKIN	Clock for the input data shift register.
50	SDIN	Serial data input.
49	SDOUT	Serial data out.
53	LOAD	Loads input data into central register.

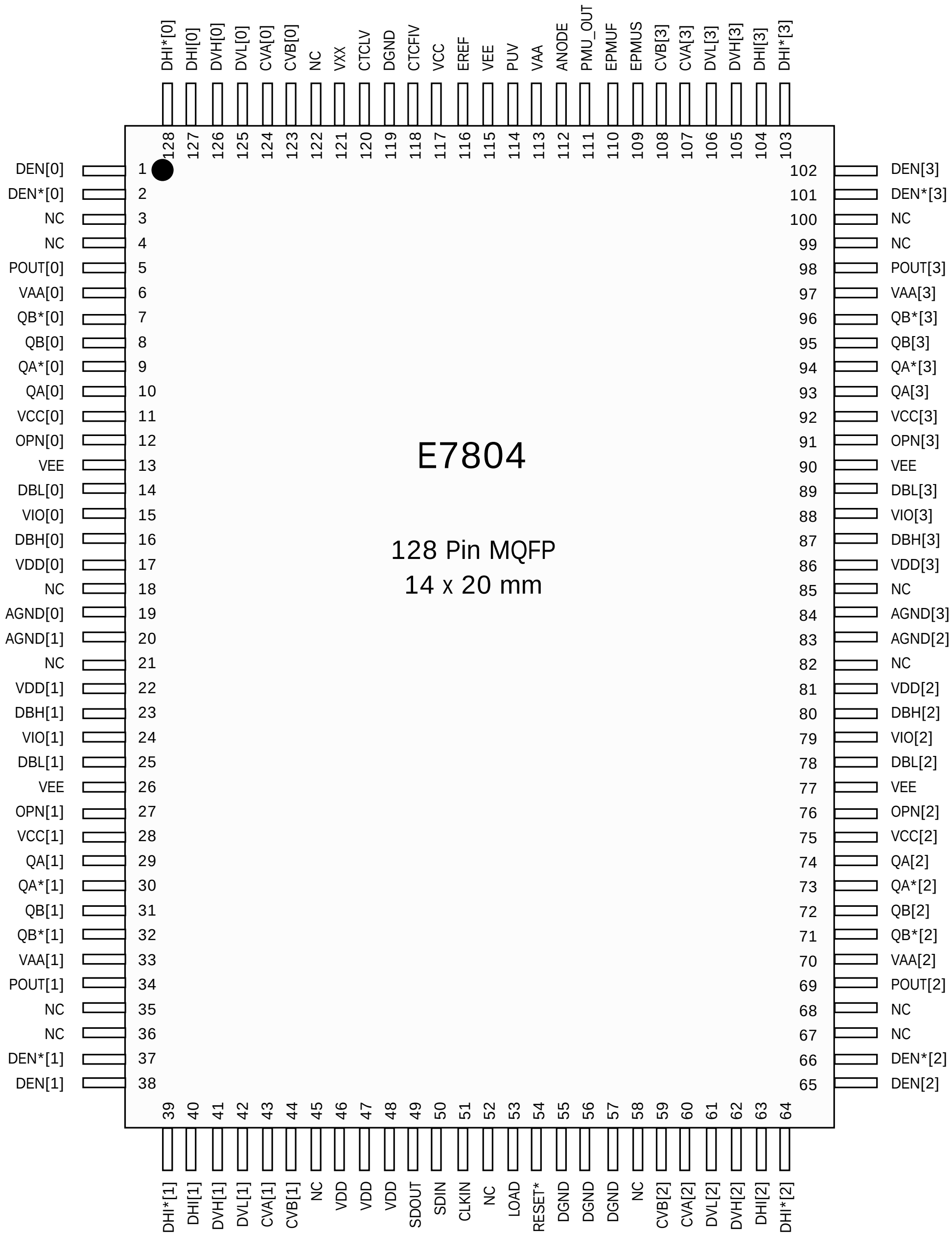
PIN Description *(continued)*

[0:3] Refers to Channels 0, 1, 2 or 3

Pin #	Pin Name	Description
Power Supplies		
11, 28, 75, 92	VCC[0:3]	Analog positive power supply to channel high voltage circuitry (+8.25V).
117	VCC	Analog positive power supply to high voltage circuitry (+8.25V).
6, 33, 70, 97	VAA[0:3]	Analog positive power supply to channel circuitry (+5.0V nominal).
113	VAA	Analog positive power supply to core circuitry (+5.0V nominal).
13, 26, 77, 90, 115	VEE	Analog negative power supply (–5.0V nominal).
17, 22, 81, 86	VDD[0:3]	Digital positive power supply to channel comparator outputs (+3.3V nominal).
46, 47, 48	VDD	Digital positive power supply for core logic (+3.3V nominal).
19, 20, 83, 84	AGND[0:3]	Analog ground for channels.
55, 56, 57, 119	DGND	Digital ground for chip.
121	VXX	Switch positive power supply (VCC to VEE + 15V).
Miscellaneous		
116	EREF	External reference resistor input. R_{EREF} should be connected between EREF and AGND.
112	ANODE	Anode terminal of the on-chip thermal diode string. The pin is ESD protected to VXX, so when measuring the forward drop of the diode string, VXX should be either floating or ≥ 2V. Cathode of diode string is connected to DGND.
3, 4, 18, 21, 35, 36, 45, 52, 58, 67, 68, 82, 85, 99, 100, 122	NC	No connect pin. No connection is made internally. These pins can be connected to a ground plane to assist in heat removal from the package.

PIN Description *(continued)*

128 Pin MQFP Package



NC - No Connect.

Circuit Description

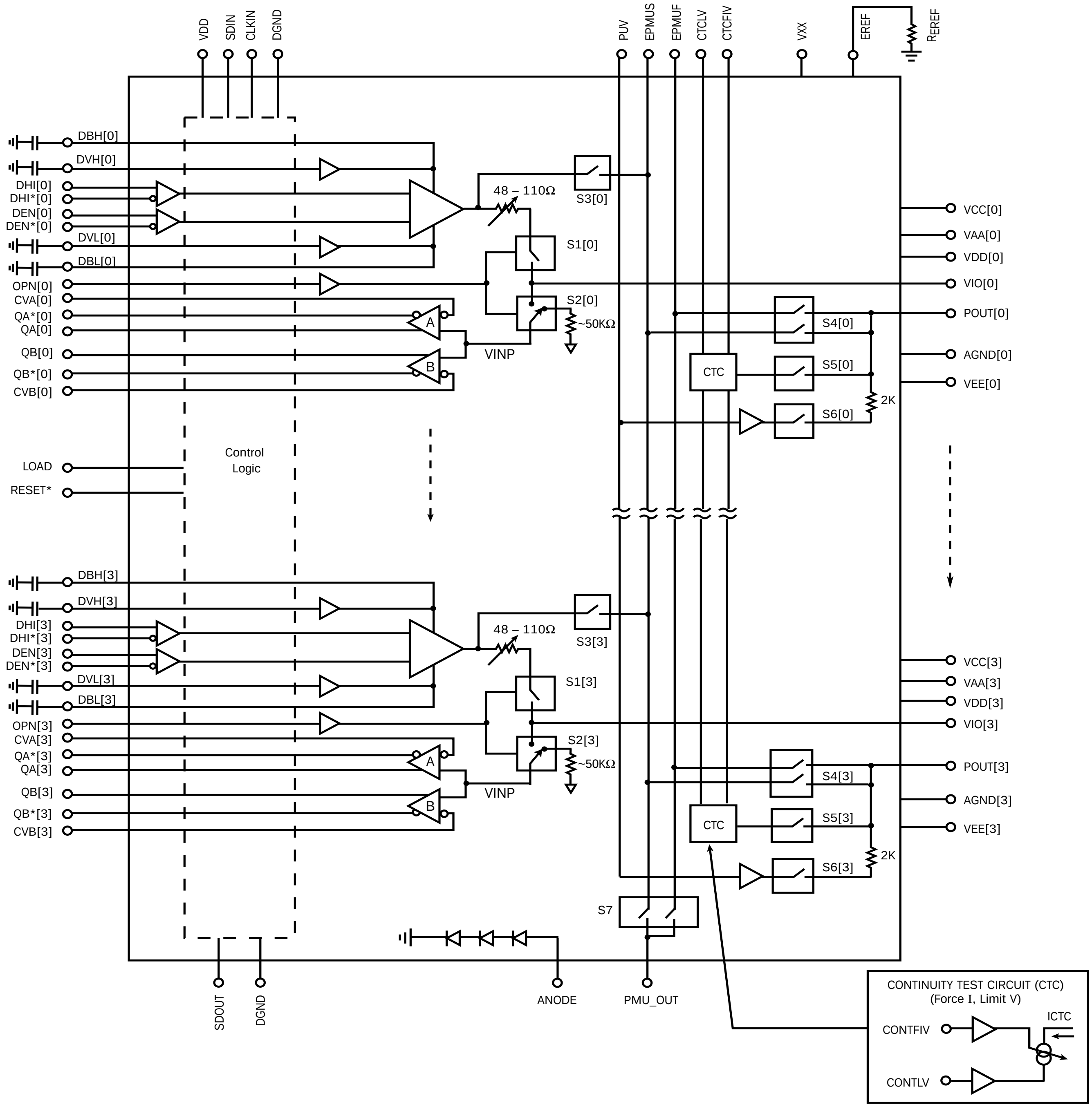


Figure 1. Detailed Block Diagram of Edge7804 Quad Driver and Window Comparator

Circuit Description *(continued)*

Introduction

The four driver and window comparator channels of the E7804 are shown in Figure 1.

Driver

Refer to Table 1 showing the modes of operation of the driver.

Each channel's driver states of HiZ, force DVH voltage, force DVL voltage and Open can be controlled either by external input pins or via internal registers and bits programmed through the serial interface.

The HiZ/DVH/DVL states are controlled by the differential, external inputs, DHI/DHI* and DEN/DEN*. Each channel also has internal register bits (see Table 2, *CH[0:3]_Relays_&_States* registers) SDHI and SDEN that accomplish the same functions as DHI and DEN. The serial register has another bit, SEN (Serial Enable) that allows the SDI and SDEN bits to override the external input pins DHI and DEN. If SEN is a logical "0", the SDHI and SDEN bits are ignored.

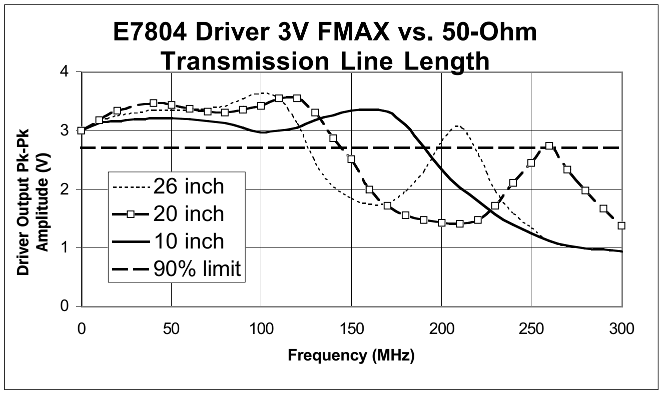
The DHI/DHI* and DEN/DEN* inputs are LV_TTL and differential LVDS, LV_PECL compatible.

Unused DHI/DHI* or DEN/DEN* must be tied to valid logic levels.

Optimizing Driver Waveforms

The driver output pin, VIO, will normally be connected to the parametric output pin, POUT, when designed into a system. See the recommended 7804 Hookup drawing farther on in this datasheet. The POUT pin has a lumped capacitance associated with it that will degrade the signal integrity of the driver output waveform if not properly compensated for. The recommendation is to insert ferrite devices between the connection of POUT to VIO to accomplish this. For more details on how and why this approach is used, please read Semtech Application Note *#ATE-A3 ATE-to-DUT Interface: Using Ferrites to Replace Relays for Lower Cost and Improved Performance.*

The driver output impedance has a reactive component to it and will not completely absorb reflections from an unterminated transmission line. This is common for all drivers, but more so in CMOS drivers than high speed bipolar stages. The figure here shows how transmission line length, here in the form of coaxial cable, will sum the reflections constructively and destructively to alter the peak-to-peak waveform excursions across frequency. More data on this performance and methods for optimizing signal integrity and extending Fmax will be available from Semtech staff. Check with Semtech for the latest information. From the graph below one can see that E7804 driver signals in excess of 150MHz are possible.



Driver Levels

Each channel's DVH and DVL are high input impedance voltage inputs which establish the channel driver's high and low levels. The driver's output range is –0.2V, +5.2V.

DVH to VIO and DVL to VIO offset errors are small, which allow the Edge7804 to be configured with common input levels to each channel (i.e. DVH[0:3] may be connected together externally, and the same for DVL[0:3]).

Driver Source Impedance

Drivers feature a self-calibrating source impedance calibrated to match an external resistor, R_{EREF}, connected between the EREF pin and analog ground. The source impedance can be chosen to calibrate in the range 48Ω to 110Ω using the calculation $R_{EREF}/100$.

A driver's source impedance is affected by its DVH and DVL levels, and therefore needs recalibrating whenever driver levels into the chip are changed. The calibration routine is initiated via the serial interface (see Table 2, *calibrate_output_z* register). When initiated, all channels are recalibrated in parallel.

Circuit Description *(continued)*

Driver Connect/Disconnect

The driver output connects to the VIO output pin through an internal, normally open switch (S1). Refer to the Functional Block diagram in Figure 1 for Switch S1. This switch can be closed by serially programming the internal register bit for the appropriate channel (see Table 2, *CH[0:3]_Relays_&_States* registers) denoted as S1 to a logical "1". Logical "0" will open the switch. An external pin, OPN[0:3] one input for each channel, is combined with the register bit and will override the internal register bit and Open the S1 switch for the channel. In its low state, the OPN input will *not* override and force the switch closed however. (It should be noted that OPN=1 will also open S2 to disconnect the channel's window comparators from the VIO pin.) OPN is a fast way of disconnecting the lower voltage driver and comparator circuitry from the VIO pin. When the driver (and comparator) are disconnected, the voltage at VIO may be in the range of the VEE to VXX power supplies.

The high voltage disconnect switches permit an external Parametric Measurement Unit (PMU) to be connected to the VIO pin having a maximum range from VEE to VXX volts and up to ± 40 mA.

This high voltage isolation also permits an external driver to apply up to VXX volts (when switches S1 and S2 are open) for high voltage applications.

Each driver may also be connected, internally, to EPMUS in order to measure its output for purposes of calibrating the DVH/L levels via switch S3.

		OPN=0		OPN=1
Digital Inputs		S1 Closed	S1 Open	X
DEN	DHI	VIO	VIO	VIO
1	0	DVL	Open	Open
1	1	DVH	Open	Open
0	0	HiZ	Open	Open
0	1	HiZ	Open	Open

OPN (Open Channel Input)
DVL (Driver Low)
DVH (Driver High)
HiZ (High Impedance)
Open (Driver, Comparator open/disconnected) (see Table 3)
X (Don't Care)
S1 (Driver Output Switch)

Table 1. Edge7804 Driver Modes of Operation

Comparator

Each channel's two comparators, A and B, are combined to form a window comparator to determine whether its input, VINP, is above, below, or in between the two comparator thresholds (CVA and CVB). VINP is tied to the positive input of both comparators.

The CVA/B inputs should be driven from low impedance sources. There is an input non-linear current shift of ~15µA when the VINP signal to the comparator crosses polarity with respect to the CVA/B input. If the source impedance is too great, this could affect the accuracy of the compare points. The voltage source's output impedance should be below 4KΩ to avoid this. DAC or op amp outputs will have no issue with this. (If resistor dividers are used to create the CVA/B voltages, the voltage should be buffered to prevent this shift.)

VINP has a range of –2V, +5.5V, but is restricted to the range of the drivers whenever a comparator is connected to its driver (S1 and S2 switches both closed), namely –0.2V, +5.2V.

The comparator outputs are differential LVDS compatible on the QA/QA* and QB/QB* device pins. The output states of the comparators for each channel can also be read back using the serial interface. See Table 3, *CH[0:3]_switches_&_states* read back instruction for the individual channels.

Comparator Levels

Each channel's CVA and CVB are the window comparator's two threshold levels. CVA and CVB are high impedance voltage inputs that determine the thresholds at which the window comparator changes state. CVA and CVB have a range of –2.0V, +5.5V.

Comparator Connect/Disconnect

The window comparator input (VINP) connects to the VIO pin through an internal switch (S2). This switch can be closed to VIO by serially programming the internal register bit for the appropriate channel (see Table 2, *CH[0:3]_switches_&_states* registers) denoted as S2 to a logical "1". Logical "0" will open the switch from VIO. The comparator input is connected to approximately zero volts when disconnected from VIO through ~50KΩ. To prevent the comparator outputs from switching due to noise when not in use, the CVA/B inputs should be parked >250mV from ground. An external pin, OPN[0:3] one input for each channel, is combined with the register bit, and will override the internal register bit and open the S2 switch for the channel. In its low state, the OPN input will *not* override and force the switch closed. (It should be noted that OPN=1 will also open S1 to disconnect the channel's driver output from the VIO pin.) OPN is a fast way of disconnecting the lower voltage driver and comparator circuitry from the VIO pin. When the comparator (and driver) are disconnected, the voltage at the VIO pin may be in the range of the VEE to VXX power supplies.

Parametric Measurements

The Edge7804 incorporates a switch matrix which permits an External Parametric Measurement Unit (EPMU) to be connected to one or more channel's POUT pin. The EPMU range is a function of the VEE and VXX power supplies with ± 40 mA capability. Typically, POUT is connected directly to the VIO pin or connected by an inductor so as to minimize the effect of the capacitance at the POUT pin on the driver's waveform and maximum frequency.

The EPMUF and EPMUS inputs are force and sense inputs respectively and connect to the POUT output pin through an internal, normally open, dual switch (S4). There is one dual switch for each channel [0:3]. This switch can be closed by serially programming the internal register bit for the appropriate channel (see Table 2, *CH[0:3]_switches_&_states* registers) denoted as S4 to a logical "1". Logical "0" will open the switch. The switch and metal lines for the EMPUF path are sized to accommodate the higher currents (up to 40mA). Do not use EPMUS for higher currents. The EPMUS line is the Kelvin sense path for the external PMU.

Continuity Test Circuit

Each channel has a programmable Continuity Test Circuit (CTC) which can be switched to its POUT pin. The CTC sinks current in the range –15 to –250 µA as determined by the voltage of the CTCFIV input pin which is common to all CTC's.

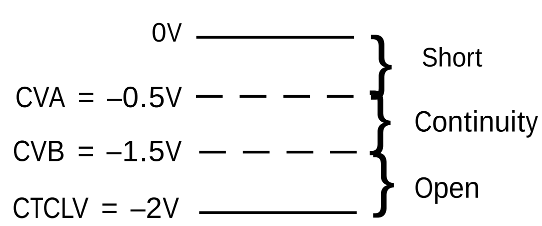
The relationship between the CTCFIV input voltage and the resulting current produced by the CTC uses the resistor R_{EREF}, as a reference. This gives a good degree of voltage to current accuracy. The relationship is:

$$I_{CTC} = -1.09 * [CTCFIV(V) / R_{EREF}(\Omega)].$$

CTCLV input determines the voltage limit to which CTC may sink current. CTCLV has a range of 0 to –2.0V and is common to all channels' CTCs. With POUT, connected externally to VIO, then with CTC connected and sinking current, the resultant voltage at VIO can be tested by the channel's comparators. As this voltage could be as low as –2V, when performing a continuity test, a channel's driver should be disconnected in order to protect the driver, which has a range of –0.2V to +5.2V. The driver output should be disconnected by opening switch S1 when connecting the CTC to the POUT pin. The CTC connects to the POUT pin through the normally open switch S5. Switch S5 can be closed by serially programming a logical "1" via the internal register for the appropriate channel. See Table 2,"*CH[0:3]_switches_&_states* write instruction for the individual channels.

Note that the CTC's use the external resistor on the EREF pin to calculate the I_{CTC} test currents. The driver output impedance calibration *also* uses this reference. If any CTC is switched in-circuit (S5 closed), then attempting to calibrate the driver output impedance will fail and not occur. No change to the calibration values will take place.

A typical continuity test will program the CTC's force current to –100 µA, its voltage limit at –2V, and CVA and CVB at –0.5V and –1.5V, respectively, so as to detect shorts, opens and continuity. Typically, in this test, the DUT power supplies are all set to zero volts. The continuity test will determine if each pin of the DUT is connected to the pin channel in the tester without shorts to supplies or ground.



Circuit Description *(continued)*

The tested pins will test good if the resulting voltage from a –100µA load on them results in ~–0.7V. This is the voltage that will be present if the pin substrate or ESD diodes are present. A short can be detected if the resulting voltage is close to zero volts. An Open will be detected if the voltage goes close to –2V. The figure above illustrates this test with the CVA =– 0.5V and CVB = –1.5V.

Pull-Up Resistor

Each channel has a 2KΩ (typ.) pull-up resistor that can be switched to its POUT. The effective pull-up, including resistor and switch, is in the range 1KΩ to 3KΩ.

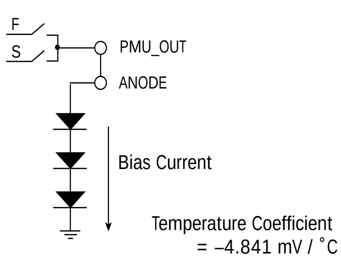
PUV is a single input and is buffered at each channel to the pull-up resistors. The buffer and resistor are capable of sourcing or sinking (pull-up or pull-down) currents for 0 to 5V external signals.

Thermal Monitor

An on-chip thermal diode string of three diodes in series allows accurate die temperature measurements (see diagram below).

A bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$T_j[^\circ C] = (0.813 - V_{ANODE}/3) / (0.00162)$$

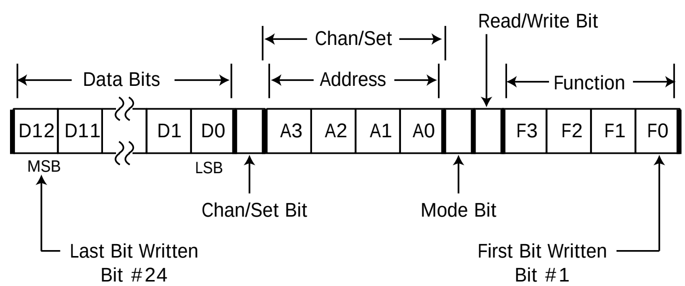


The ANODE of the diodes may be switched internally to the EPMU bus such that temperature measurements can be performed by the EPMU. The connection to the diode string's ANODE pin for the EPMU is performed externally by shorting the PMU_OUT pin to the ANODE pin. This external connection is available to make it possible to access the diode string when the device is not powered up. This is useful for calibration purposes of the diode string. The ANODE pin is internally ESD protected in the positive direction to VXX. To use the diode string, VXX needs to either be floating (unpowered operation) or ≥ 2V.

Programming Functional Description

The Edge7804 features a serial data input programming structure to program the channels functions and switches, assign or invoke Set functions, as well as control more global chip functions such as Reset and Calibration. The majority of the functions are both Read and Write. The serial streams are all 24-bits long and are referred to as "instructions" because the serial streams are built up with address, function, read and select bits as well as data into the 24-bit stream which is clocked serially into the device.

The following is a description of the 24-bit instruction stream.



Data: 13 bits
This field contains the data to be written into various registers which control the function of the part, or the selected channel(s).

Channel/Set Address Select: 1 bit
This bit determines whether a single channel or a set of channels is being addressed.

0 = channel direct functions
1 = set of channels

Channel/Set Address: 4 bits
This field contains the address of the channel or set being operated on.

Mode: 1 bit
This determines whether the instruction refers to a chip-level control (such as chip reset), or refers to a channel or set of channels.

0 = chip function
1 = channel or set function

Circuit Description *(continued)*

Read/Write: 1 bit
This determines whether a particular address/function is being written or read. (Note that some functions are read-only or write-only).

0 = write a control/data register
1 = read back the contents of a register

Function: 4 bits
This determines which function within a channel or set is being set or read.

Refer to Figure 2 for a block diagram of the Write and Read logic for the serial programming. The serial data is input into the device SDIN pin. The data at SDIN is clocked in on the high-going edge of the CLKIN input signal. The data at the SDOUT pin is clocked out on the low-going edge of the CLKIN input signal for ease of "daisy chaining" multiple devices.

RESET*

There is a single input pin to the entire Edge7804 chip that will clear all on-chip registers and open all on-chip switches. This input pin, RESET*, is active low and is asynchronous, not requiring any CLKIN transitions to operate. It is advised that, upon power-up in a system, this pin is either held low or cycled low for a brief time while the system and power supplies become stable in order to put the Edge7804 into a known starting state. After power-up, the RESET* may be exercised or a soft reset instruction may be programmed.

Write Serial Data

Data is shifted into the WRITE shift register using CLKIN. The data stored in the shift register will be stored into the Edge7804 by asserting the LOAD input signal during the 24^{th} CLKIN high-going edge. The LATCH will hold the instruction inside the Edge7804 for address decoding and data storage into the appropriate on-chip registers. **Seven (7) more CLKIN high-going edges should be given after a LOAD for full decode and all instruction executions.**

Refer to Figure 3 for a timing diagram of the writing operation. Notice that the SDOUT data that is clocked out on the low-going edge of CLKIN is a bit for bit representation of the data that had been shifted into the Edge7804 24 clock edges beforehand. This echoing of the data allows the user to "daisy chain" multiple Edge7804 devices to minimize the number of serial data streams that need to be implemented. The compromise is the length of time it takes to clock through all the 24-bit instructions for all the devices in the chain.

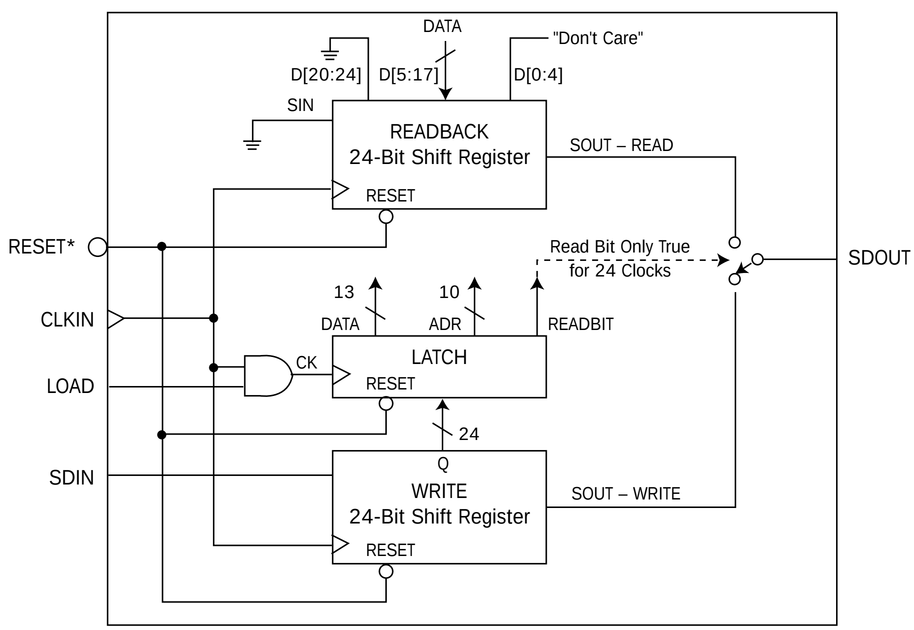


Figure 2. Block Diagram of Read and Write Shift Registers

Circuit Description *(continued)*

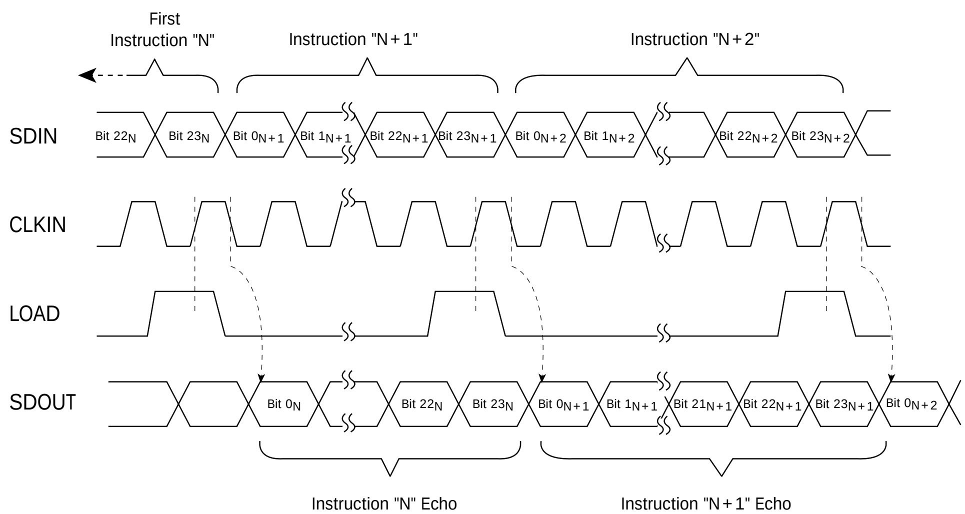


Figure 3. Serial Data Programming – Write Instruction

Figure 4 depicts two topologies to serially read and write multiple Edge7804 devices on a single assembly. Figure 4a daisy chains the serial I/O (SDOUT to SDIN) pins, and the CLKIN and LOAD functions are common for all the Edge7804s. This topology uses a minimum amount of I/O from the control logic. However, in order to read or write the Edge7804's an instruction string of 24 x N bits long needs to be created, clocked all the way through the devices, and a parallel LOAD signal asserted for all devices. NO_OP instructions may be used for the devices that are not being addressed.

Figure 4b shows a topology from the control logic that offers rapid programming time and complete independence. This topology relies on enough I/O signals being available from the control logic. Notice that the CLKIN pins are still all common because independence is allowed by the individual LOAD signals to each Edge7804.

If it is determined that readback from the Edge7804s are not necessary, the control logic can be further simplified. Readback is not necessary for the operation of the Edge7804. It is offered as a good diagnostic tool and possible programming aid.

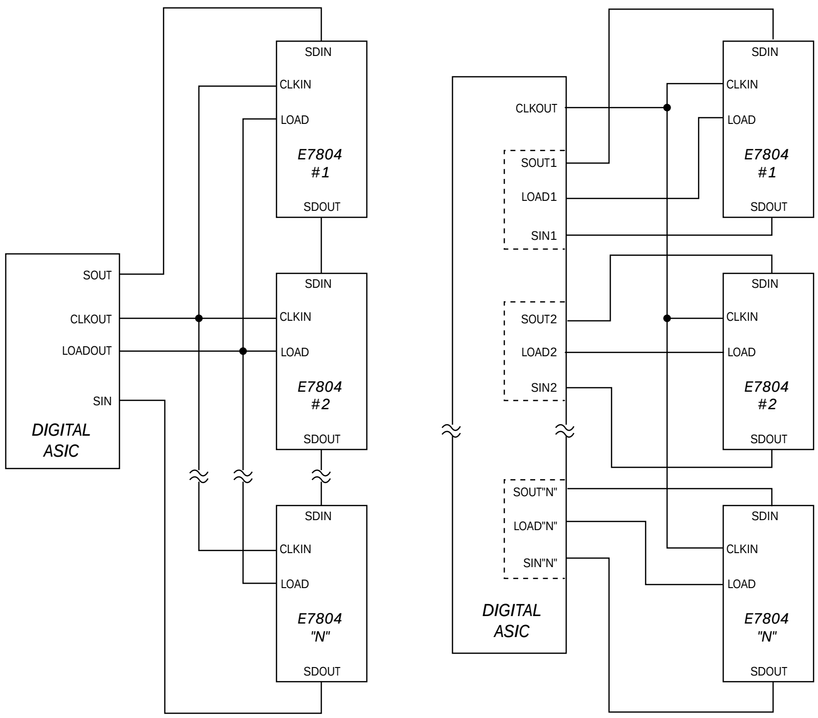
Read Serial Data

In order to readback data, an instruction is constructed with the *Read_Bit* set to a logical "1" in the instruction stream and written to the Edge7804. The instruction stream must be properly constructed for address and select bits to insure that the proper register will be accessed for readback. The data bits D0:D12 in this Read instruction are Don't_Care.

Refer to Figure 5 for a timing diagram of the readback process and Figure 2 for a block diagram of how the readback operation works. Once the LOAD signal is asserted on the 24^{th} high-going CLKIN edge to latch in the READ instruction for a particular address, the internal READ line will assert true and switch the SDOUT pin to output data from the internal readback shift register. The readback data will immediately start to output from the SDOUT pin on the low-going edge of CLKIN. The readback will continue for 24 bits.

The first 5 bits of data readback should be ignored. The next 13 bits will be the requested register's readback data. Finally, the last 6 bits are logical zeros.

While clocking out the readback data, a new instruction can be simultaneously clocked in at SDIN. At the conclusion of the 24-bit readback, the SDOUT data will revert back to echoing the SDIN data shifted by 24 clocks.



a. Minimum # of Control Lines from ASIC

b. Independent Control of Each E7804

Figure 4. Serial Control of Multiple Edge7804s

Figure 5 depicts the conclusion of a Read instruction being written to the Edge7804. The first LOAD pulse straddling the rising edge of CLKIN latches in the Read instruction, echoing at SDOUT stops, and the readback of the register begins. After 24 low-going clocks, the data at SDOUT resumes echoing the written data at SDIN. Even without the second LOAD pulse, the echoing will begin. Figure 5 depicts a Write instruction following the Read. This could be another Read instruction, in which case the echoing of SDIN would not begin as indicated. Instead, another sequence of 24 readback bits would begin.

The readback data format and address are defined in Table 3. The Read operation will continue for 24 low-going clock edges. The SDOUT will begin outputting data from the write shift register after the 24th low-going clock edge.

Address Map

Table 2 shows the Write Table and Address Map. Across the top of the table are the 24 bits of data denoted as Bit #0 through Bit #23. Hex notation is also provided as well as the binary positions.

The instruction is constructed of 13 Data bits, 8 address bits, 2 select bits and a read bit. Figure 3 shows the bit pattern in the write instructions. The instructions are separated into 3 main groups. The Chip Functions, the Channel Functions and the Set Functions. Each instruction has a Register Name associated with it. In the pages following Table 2 are descriptions of each of the register names and, where applicable, a bit-by-bit description of the data.

Circuit Description *(continued)*

Chip Functions

The Chip Functions group of instructions controls chip functions that are global in scope and not associated with a particular channel. Examples of these functions are the chip identification number and revision, the Reset function for chip wide reset, and initiation of calibration.

Function Address – Instructions in the group are denoted by this set of bits.
Read Bit— Set to “1” only if user intends to read back a register.
Chan Bit – Set to a “0” since this instruction group is not channel related.
Chan/Set Adr – These 4 bits are “don’t care”. Since these would select either a channel or set number, and these are Chip Functions, they don’t apply.
Set Select Bit – This bit is a “don’t care” for the Chip Functions group.

Channel Functions

The Channel Functions group of instructions address the functionality of individual registers and bits that are particular to specific channels of the Edge7804. Driver states, channel switches, calibration factors and set assignments are included in this group.

Function Address – These bits denote which function of the particular channels is being addressed.
Read Bit— Set to “1” only if user intends to read back a register.
Chan Bit – Set to a “1” because these instructions relate to specific channel registers.
Chan/Set Adr – These bits will denote which channel is being addressed for the particular function. Valid range is 0x0 through 0x3 for the E7804.
Set Select Bit – This bit is set to a “0” because this is the Channel Functions group.

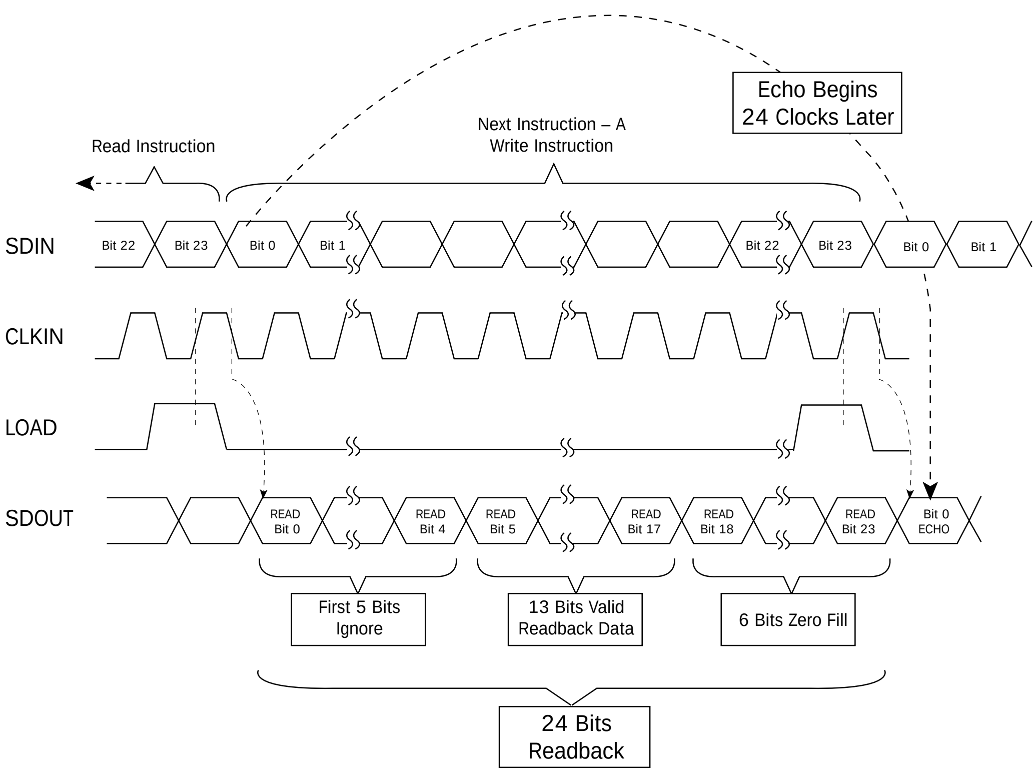


Figure 5. Serial Data Programming – Readback Sequence

Circuit Description *(continued)*

Set Functions

Set Functions are a group of 8 instructions corresponding to the 8 available *Sets* that will configure any channel that has been assigned to that *Set*. The Set Functions are write-only, but the effects of a Set instruction can be read back from the individual channel's registers. The Set is given control of any channel's driver states or switches. The *Set* concept is a way of programming all channels on any Edge7804 that have been assigned to that particular *SET* to a particular configuration with one instruction write cycle.

Function Address – These addresses should all be "0".
Read Bit— Set to "0" since there is no readback for set instructions.
Chan Bit – Set to a "1".
Chan/Set Adr – These bits will denote which set is being programmed. Valid set values are 0x0 through 0x7 corresponding to the eight valid *SETs.*
Set Select Bit – This bit is a "1" because this is the *SET* Functions group.

SET Programming

Referring to Table 2, a channel's *SETs* Register may be programmed via the *CH[0:3]_set_assign* instructions. This is an independent 8-bit register per channel which determines the *SETs* to which the channel belongs. A channel may belong to none, one, or any combination of up to 8 sets.

Programming the Driver's Source Impedance

Figure 1 shows that each driver's source impedance is programmable over a 48Ω to 110Ω range so as to match the impedance of the transmission line connecting VOP to the Device Under Test (DUT). The driver's source impedance is automatically programmed to match $R_{EREF}/100$, where R_{EREF} is the external reference resistor connected to the EREF pin.

Initiating the source match auto-calibration sequence is a "chip function" (Table 2). Auto-calibration is performed on all channels in parallel.

The Driver's source impedance is affected by its DVH and DVL levels and, therefore, auto-calibration should be initiated whenever driver levels are changed.

Following auto-calibration, a driver's source impedances match ($R_{EREF}/100$) Ω when its output is at (DVH + DVL) / 2. If the output voltages of the driver are reprogrammed, then it is advised to recalibrate to maintain the best accuracy.

Calibration will occur after writing the global function instruction *calibrate_output_z*. Calibration requires an additional 576 clock edges from CLKIN to complete the process. This is 24 instructions worth of clocks. Instructions for the device undergoing calibration may be any valid instruction except that which connects the CTC output to POUT, or simply applying the clocks without LOAD'ing instructions is also valid. At the end of the process, the new, calibrated output impedances will be applied to the driver output stage. The driver may be in the enabled or disabled state. If enabled, there could be a noticable perturbation on the output.

Circuit Description *(continued)*

Instruction Table

Group	Register Name		D12 (MSB)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	Set Sel	A3	A2	A1	A0	Chan Bit	Read Bit	F3	F2	F1	F0
	Bit #		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Hex Multiplier		010x0000				01x0000				0x1000				0x0100				0x0010				0x0001			
	Binary Position		8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
	Register Name (Write Only = WO, Read Only = RO, Read/Write = R/W)		Data Bits													Set Sel	Chan/Set Adr				Chan Bit	Read Bit	Function Adr			
CHIP FUNCTIONS	no_op	WO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	chip_id	RO	*(see Readback Table for data)*													x	x	x	x	x	0	1	0	0	0	1
	chip_revision	RO	*(see Readback Table for data)*													x	x	x	x	x	0	1	0	0	1	0
	calibrate_output_Z	R/W													CAL	x	x	x	x	x	0	0/1	0	0	1	1
	chip_switches	R/W													S7	x	x	x	x	x	0	0/1	0	1	0	0
	global_calib_factor	R/W						*0x00 to 0xFF*								x	x	x	x	x	0	0/1	0	1	0	1
	diagnostic (reserved)	R/W														x	x	x	x	x	0	0/1	0	1	1	0
	reserved															x	x	x	x	x	0	0/1	0111 - 1110			
	reset	WO												SETS	ALL	x	x	x	x	x	0	0	1	1	1	1
CHANNEL FUNCTIONS	CH0_relays_&_states	R/W					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	0	0	0	0	0	1	0/1	0	0	0	0
	CH1_relays_&_states	R/W					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	0	0	0	0	1	1	0/1	0	0	0	0
	CH2_relays_&_states	R/W					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	0	0	0	1	0	1	0/1	0	0	0	0
	CH3_relays_&_states	R/W					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	0	0	0	1	1	1	0/1	0	0	0	0
	reserved															0	0100 - 1111				1	0/1	0	0	0	0
	CH0_DVH_calib_Z	R/W						*impedance calibration code*								0	0	0	0	0	1	0/1	0	0	0	1
	CH1_DVH_calib_Z	R/W						*impedance calibration code*								0	0	0	0	1	1	0/1	0	0	0	1
	CH2_DVH_calib_Z	R/W						*impedance calibration code*								0	0	0	1	0	1	0/1	0	0	0	1
	CH3_DVH_calib_Z	R/W						*impedance calibration code*								0	0	0	1	1	1	0/1	0	0	0	1
	reserved															0	0100 - 1111				1	0/1	0	0	0	1
	CH0_DVL_calib_Z	R/W						*impedance calibration code*								0	0	0	0	0	1	0/1	0	0	1	0
	CH1_DVL_calib_Z	R/W						*impedance calibration code*								0	0	0	0	1	1	0/1	0	0	1	0
	CH2_DVL_calib_Z	R/W						*impedance calibration code*								0	0	0	1	0	1	0/1	0	0	1	0
	CH3_DVL_calib_Z	R/W						*impedance calibration code*								0	0	0	1	1	1	0/1	0	0	1	0
	reserved															0	0100 -1111				1	0/1	0	0	1	0
	reserved															0	0000-1111				1	0/1	0011-1110			
	CH0_set_assign	R/W						set7	set6	set5	set4	set3	set2	set1	set0	0	0	0	0	0	1	0/1	1	1	1	1
	CH1_set_assign	R/W						set7	set6	set5	set4	set3	set2	set1	set0	0	0	0	0	1	1	0/1	1	1	1	1
	CH2_set_assign	R/W						set7	set6	set5	set4	set3	set2	set1	set0	0	0	0	1	0	1	0/1	1	1	1	1
	CH3_set_assign	R/W						set7	set6	set5	set4	set3	set2	set1	set0	0	0	0	1	1	1	0/1	1	1	1	1
	reserved															0	0100 -1111				1	0/1	1	1	1	1
SET FUNCTIONS	Set0_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	0	0	0	1	0	0	0	0	0
	Set1_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	0	0	1	1	0	0	0	0	0
	Set2_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	0	1	0	1	0	0	0	0	0
	Set3_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	0	1	1	1	0	0	0	0	0
	Set4_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	1	0	0	1	0	0	0	0	0
	Set5_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	1	0	1	1	0	0	0	0	0
	Set6_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	1	1	0	1	0	0	0	0	0
	Set7_relays_&_states	W0					INT	SDEN	SDHI	S6	S5	S4	S3	S2	S1	1	0	1	1	1	1	0	0	0	0	0
	reserved															1	1000 - 1111				1	0	0	0	0	0

Table 2. Edge7804 Instruction Table/Address Map

Circuit Description *(continued)*

Readback Sequences

	Bit #		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Register Name		TRAILING 0's						VALID DATA READBACK													LEADING BITS					
									MSB												LSB						Notes
GLOBAL FUNCTIONS	chip_id	RO	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	0	X	X	X	X	X	1
	chip_revision	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	2
	calibrate_output_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CAL	X	X	X	X	X	
	chip_switches	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S7	X	X	X	X	X	
	global_calib_factor	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit global cal factor*								X	X	X	X	X	
	diagnostic (reserved)	R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	
CHANNEL FUNCTIONS	CH0_switches_&_states	R/W	0	0	0	0	0	0	0	0	QA	QB	SEN	SDEN	SDHI	S6	S5	S4	S3	S2	S1	X	X	X	X	X	
	CH1_switches_&_states	R/W	0	0	0	0	0	0	0	0	QA	QB	SEN	SDEN	SDHI	S6	S5	S4	S3	S2	S1	X	X	X	X	X	
	CH2_switches_&_states	R/W	0	0	0	0	0	0	0	0	QA	QB	SEN	SDEN	SDHI	S6	S5	S4	S3	S2	S1	X	X	X	X	X	
	CH3_switches_&_states	R/W	0	0	0	0	0	0	0	0	QA	QB	SEN	SDEN	SDHI	S6	S5	S4	S3	S2	S1	X	X	X	X	X	
	CH0_DVH_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH1_DVH_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH2_DVH_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH3_DVH_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH0_DVL_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH1_DVL_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH2_DVL_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH3_DVL_calib_Z	R/W	0	0	0	0	0	0	0	0	0	0	0	*8-bit impedance calibration code*								X	X	X	X	X	
	CH0_set_assign	R/W	0	0	0	0	0	0	0	0	0	0	0	set7	set6	set5	set4	set3	set2	set1	set0	X	X	X	X	X	
	CH1_set_assign	R/W	0	0	0	0	0	0	0	0	0	0	0	set7	set6	set5	set4	set3	set2	set1	set0	X	X	X	X	X	
	CH2_set_assign	R/W	0	0	0	0	0	0	0	0	0	0	0	set7	set6	set5	set4	set3	set2	set1	set0	X	X	X	X	X	
	CH3_set_assign	R/W	0	0	0	0	0	0	0	0	0	0	0	set7	set6	set5	set4	set3	set2	set1	set0	X	X	X	X	X	

Notes:

1 Device part number = 7804 decimal = 0x1E7C hex
2 Rev A = 0x000, B = 0x001, ...

Table 3. Registers' Readback Bit Sequences

Circuit Description *(continued)*

CHIP FUNCTIONS

Register Name	*no_op*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 don't care 0	**Set Select Bit** **Mode**	0 or 0 Write Only
Default Value	0 0000 0000 0000	0x00			
Description	This bit stream is used as a null stream. No operation will result if shifted in and a LOAD is executed. It is useful if multiple devices are connected in serial arrangement and a chip is not being addressed, but a parallel LOAD will occur for all devices on the serial bus.				
Register Name	*chip_id*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 don't care 0	**Set Select Bit** **Mode**	0 or 1 Read Only
Default Value	1 1110 0111 1100	0x1E7C			
Description	This identifies the device part number, decimal equivalent is 7804. It is a read only register.				
Register Name	*chip_revision*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x02 don't care 0	**Set Select Bit** **Mode**	0 or 1 Read Only
Default Value	0 0000 0000 0000	0x00			
Description	This identifies the device die revision number. The first revision is decimal 0, the second will be decimal 1, etc. It is a read only register.				
Register Name	*calibrate_output_z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x03 don't care 0	**Set Select Bit** **Mode**	0 or 1 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	Writing to the LSB of this address will initiate a chip-wide calibration of the output impedances of the drivers. The internal state machine that performs the calibrations will require 21 microseconds for complete calibration of all channels. This is 30 instructions (x24 clocks) clocked at 33 MHz CLKIN. Because the calibration and Continuity Test Circuits (CTC) both share the EREF pin, z_calibration cannot occur if any CTC is switched into operation using S5. D0 – writing a one to this bit will initiate the calibration process. Once calibration is completed, this bit will readback as a 0.				
Register Name	*chip_switches*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x04 don't care 0	**Set Select Bit** **Mode**	0 or 1 ReadWrite
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to switch non-channel specific switches. D0 – writing a one to this bit will close the S7 switch. The S7 switch is a dual pole switch that connects the EPMUS and the EPMUF signals to the PMU_OUT pin. The primary use is when PMU_OUT is externally shorted to the temperature diode ANODE pin. Closing this switch will allow the external PMU to connect to the temperature diode string on an individual E7804 to perform die temperature measurements.				
Register Name	*global_calib_factor*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x05 don't care 0	**Set Select Bit** **Mode**	0 or 1 ReadWrite
Default Value	0 0000 1111 1111	0xFF			
Description	This register holds the eight-bit calibration factor based upon the resistor value on the EREF pin. The value in this register is used in calculating the output impedances of the driver outputs during calibration. After RESET it will be 0xFF. D0-D7 – the eight-bit value of the calibration factor. D0=LSB.				
Register Name	*diagnostic*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x06 don't care 0	**Set Select Bit** **Mode**	0 or 1 ReadWrite
Default Value	0 0000 0000 0000	0x00			
Description	This register is used for test access. Do not write to this register.				
Register Name	*reset*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x0F don't care 0	**Set Select Bit** **Mode**	0 or 1 Write Only
Default Value	0 0000 0000 0000	0x00			
Description	This register is used for programmable (soft) reset of the device. D0 – **ALL** – writing a one to this bit will perform a soft reset of the entire chip. It is wire OR'd with the external RESET* pin. The ALL reset function requires 7 clock cycles after this bit is latched in by the LOAD signal. The RESET ALL instruction will clear the SDIN and SDOUT shift registers. It is advised to follow a RESET ALL instruction with a NO_OP instruction. D1 – **SETS** – writing a one to this bit will perform a soft reset of all the set assignments for all the channels of the device. This SET function function requires 5 clock cycles after this bit is latched in by the LOAD signal.				

Circuit Description *(continued)*

CHANNEL FUNCTIONS

Channel Relay and States Registers

Register Name	*CH0_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x00 1	**Set Select Bit** **Mode**	0 Read/Write		
Default Value	0 0000 0000 0000	0x00					
Description	This register is used for controlling the Channel_0 (CH0) switches. Bits are also present to control the CH0 driver state and read back the states of the CH0 comparator outputs. The comparator output states are indicated above as unknown unless the input voltage relationships are known. D0 – **S1** – writing a one to this bit will close the switch that connects the driver output to the channels VIO pin. D1 – **S2** – writing a one to this bit will close the switch that connects the window comparator input to the channel's VIO pin. D2 – **S3** – writing a one to this bit will close the switch that connects the driver output to the external PMU sense line (EPMUS) for purposes of system diagnostics. D3 – **S4** – writing a one to this bit will close the switches that connect both the external PMU bus sense (EPMUS) and force (EPMUF) lines to the channel's POUT pin. D4 – **S5** – writing a one to this bit will close the switch that connects the continuity test circuit (CTC) to the channel's POUT pin. If any channel has S5 closed, then output impedance calibration cannot occur. D5 – **S6** – writing a one to this bit will close the switch that connects the pull-up resistor and voltage to the channel's POUT pin. D6 – **SDHI (Serial Data Hi)** – writing a logical one to this bit will force the channel's driver to output the DVH voltage. Writing a zero to this bit will force the driver to output the DVL voltage. The SDHI bit will only have effect if the SEN bit (D8) in this register is set to a logical one, allowing the SDHI bit to override the state of the external DHI signal to this channel's driver. D7 – **SDEN (Serial Data Enable)** – writing a logical one to this bit will enable the channel's driver to output either DVH or DVL (based on the SDHI bit). Writing a zero to this bit disables the driver output to high impedance. The SDEN bit will only have effect if the SEN bit (D8) in this register is set to a logical 1, allowing the SDEN bit to override the state of the external DEN signal to this channel's driver. D8 – **SEN (Serial Enable)** – writing this bit to a logical one will allow the D6 and D7 bits in this register override the external driver control signals DHI and DEN. D9 – **QB** – this bit is a Read Only bit that is the state of the channel's comparator B output. Writing to this bit will have no effect. D10 – **QA** – this bit is a Read Only bit that is the state of the channel's comparator A output. Writing to this bit will have no effect.						
Register Name	*CH1_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x01 1	**Set Select Bit** **Mode**	0 Read/Write		
Default Value	0 0000 0000 0000	0x00					
Description	This register is used for controlling the Channel_1 (CH1) switches. Bits are also present to control the CH1 driver state and read back the states of the CH1 comparator outputs. See the bit definitions above for the CH0_relay_&_switches register.						
Register Name	*CH2_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x02 1	**Set Select Bit** **Mode**	0 Read/Write		
Default Value	0 0000 0000 0000	0x00					
Description	This register is used for controlling the Channel 2 (CH2) switches. Bits are also present to control the CH2 driver state and read back the states of the CH2 comparator outputs. See the bit definitions above for the CH0_relay_&_switches register.						
Register Name	*CH3_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x03 1	**Set Select Bit** **Mode**	0 Read/Write		
Default Value	0 0000 0000 0000	0x00					
Description	This register is used for controlling the Channel 3 (CH3) switches. Bits are also present to control the CH3 driver state and read back the states of the CH3 comparator outputs. See the bit definitions above for the CH0_relay_&_switches register.						

Circuit Description *(continued)*

CHANNEL FUNCTIONS *(continued)*

Channel Calibration Registers – DVH					
Register Name	*CH0_DVH_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x00 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH0's driver impedance to DVH. Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				
Register Name	*CH1_DVH_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x01 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH1's driver impedance to DVH. Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				
Register Name	*CH2_DVH_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x02 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH2s driver impedance to DVH. Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				
Register Name	*CH3_DVH_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x03 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH3s driver impedance to DVH. Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				

Channel Calibration Registers – DVL					
Register Name	*CH0_DVL_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x00 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH0's driver impedance to DVL Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				
Register Name	*CH1_DVL_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x01 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH1's driver impedance to DVL Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				
Register Name	*CH2_DVL_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x02 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH2's driver impedance to DVL Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				
Register Name	*CH3_DVL_calib_Z*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x01 0x03 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to store the calibration 8-bit code for CH3's driver impedance to DVL Data is written internally after a chipwide calibration of the output impedances has occurred. User can read back this data or write different data into the register.				

Circuit Description *(continued)*

CHANNEL FUNCTIONS *(continued)*

Channel Set Assignment Registers

Register Name	*CH0_set_assign*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x0F 0x00 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to assign CH0 to any or no "sets". A logical 1 in the bit position will assign CH0 to respond to global commands for the corresponding set.				

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
	set7	set6	set5	set4	set3	set2	set1	set0

Register Name	*CH1_set_assign*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x0F 0x01 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to assign CH1 to any or no "SETs". A logical 1 in the bit position will assign CH1 to respond to global commands for the corresponding set. See bit positions in CH0_set_assign register description above.				
Register Name	*CH2_set_assign*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x0F 0x02 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to assign CH2 to any or no "SETs". A logical 1 in the bit position will assign CH2 to respond to global commands for the corresponding set. See bit positions in CH0_set_assign register description above.				
Register Name	*CH3_set_assign*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x0F 0x03 1	**Set Select Bit** **Mode**	0 Read/Write
Default Value	0 0000 0000 0000	0x00			
Description	This register is used to assign CH3 to any or no "SETs". A logical 1 in the bit position will assign CH3 to respond to global commands for the corresponding set. See bit positions in CH0_set_assign register description above.				

SET FUNCTIONS

Register Name	*Set0_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x00 1	**Set Select Bit** **Mode**	1 Write Only
Default Value	0 0000 0000 0000	0x00			
Description	This register is used for controlling the SetI_0 (CH0) switches on any channel that has been assigned to Set_0. Bits are also present to control the channels' driver states. D0 – **S1** – writing a one to this bit will close the switch that connects the driver output to the channel's VIO pin. D1 – **S2** – writing a one to this bit will close the switch that connects the window comparator input to the channel's VIO pin. D2 – **S3** – writing a one to this bit will close the switch that connects the driver output to the external PMU sense line (EPMUS) for purposes of system diagnostics. D3 – **S4** – writing a one to this bit will close the switches that connect both the external PMU bus sense (EPMUS) and force (EPMUF) lines to the channel's POUT pin. D4 – **S5** – writing a one to this bit will close the switch that connects the continuity test circuit (CTC) to the channel's POUT pin. D5 – **S6** – writing a one to this bit will close the switch that connects the pull-up resistor and voltage to the channel's POUT pin. D6 – **SDHI (Serial Data Hi)** – writing a logical one to this bit will force the channel's driver to output the DVH voltage. Writing a zero to this bit will force the driver to output the DVL voltage. The SDHI bit will only have effect if the SEN bit (D8) in this register is set to a logical one, allowing the SDHI bit to override the state of the external DHI signal to this channel's driver. D7 – **SDEN (Serial Data Enable)** – writing a logical one to this bit will enable the channel's driver to output either DVH or DVL (based on the SDHI bit). Writing a zero to this bit disables the driver output to high impedance. The SDEN bit will only have effect if the SEN bit (D8) in this register is set to a logical 1, allowing the SDEN bit to override the state of the external DEN signal to this channel's driver. D8 – **SEN (Serial Enable)** – writing this bit to a logical one will allow the D6 and D7 bits in this register override the external driver control signals DHI and DEN.				
Register Name	*Set1_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x01 1	**Set Select Bit** **Mode**	1 Write Only
Default Value	0 0000 0000 0000	0x00			
Description	This register is used for controlling the Set_1 switches on any channel that has been assigned to Set_1. Bits are also present to control the channels' driver states. See the bit definitions to the *Set0_relays_&_states* for bit definitions.				
	Sets 2 through 6 . . .				
Register Name	*Set7_switches_&_states*	**Function Address** **Channel/Set Address** **Channel Select Bit**	0x00 0x07 1	**Set Select Bit** **Mode**	1 Write Only
Default Value	0 0000 0000 0000	0x00			
Description	This register is used for controlling the Set_7 switches on any channel that has been assigned to Set_7. Bits are also present to control the channels' driver states. See the bit definitions to the *Set0_relays_&_states* for bit definitions.				

Application Information

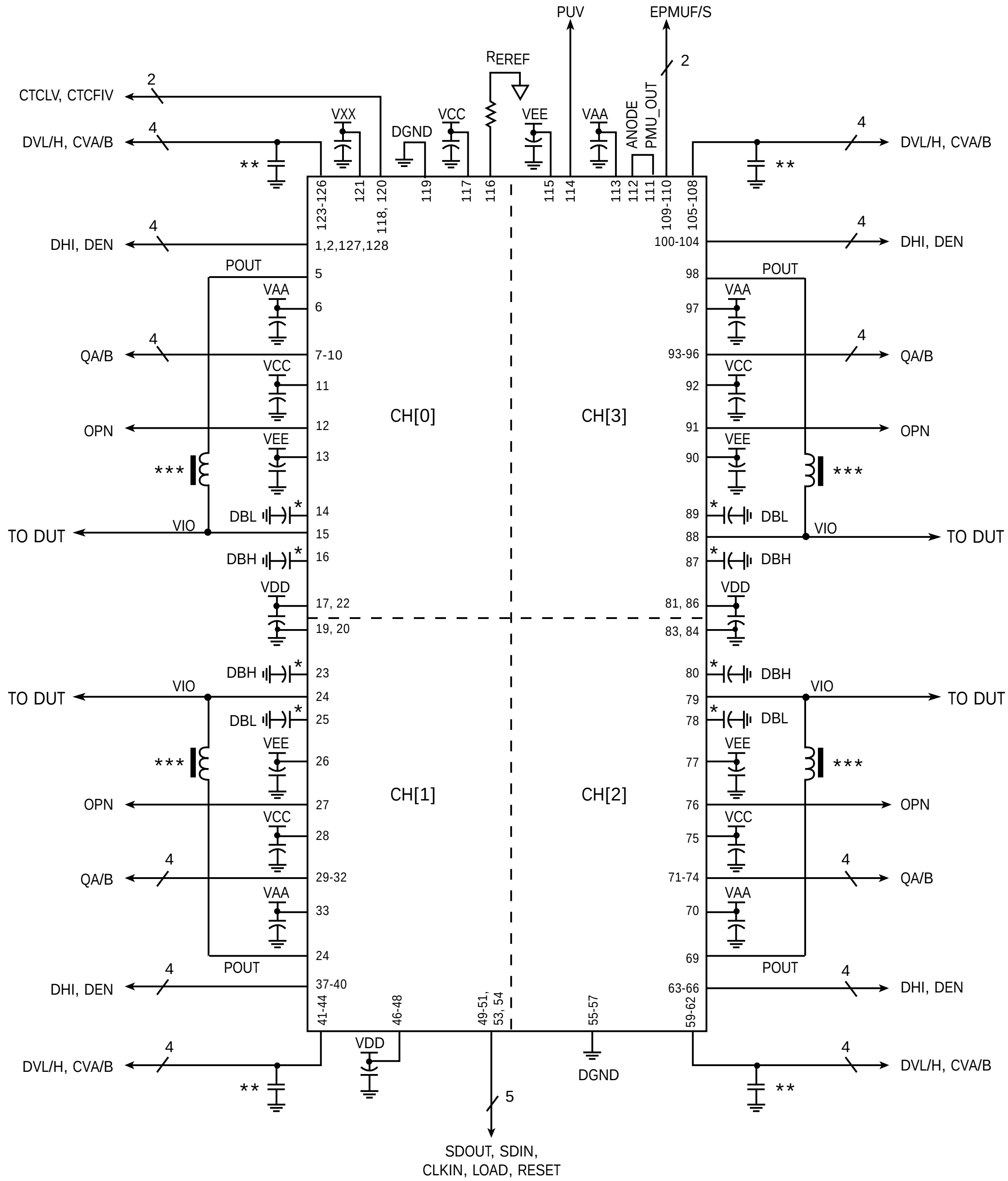


Figure 6. Edge7804 Hookup

VEEs of all Channels must be connected together; same for VCCs, VAAs, VDD and GNDs.

NOTE: All capacitors are 0.1µF unless otherwise noted.
* DBH/L capacitors are 0.47µF.
** DVH/L each have 0.22µF capacitors. Not necessary for CVA/B.
***Two ferrites in series. Each 600Ω; a 1206 and 0603 package sizes. Steward Part #MI0603J601R-00 and #MI1206K601R-00. See text for further explanation.

Application Information *(continued)*

Low Cost Pin Electronics with the Edge7804

Figure 7 shows 16 channels of 'Low Cost' Pin Electronics featuring the Edge7804, Edge6435 (Level DACs), and Edge4287 (PMU).

- 16 channels with levels per-pin and shared PMU per 16 pins
- 133 MHz clocks
- PMU, –3.25V, +9.75V with 4 current ranges to ± 40 mA
- Continuity test per pin
- Per-pin pull-up resistor
- Compatible Power (common) supply (VCC, VDD, VEE, etc.) requirements for each chip

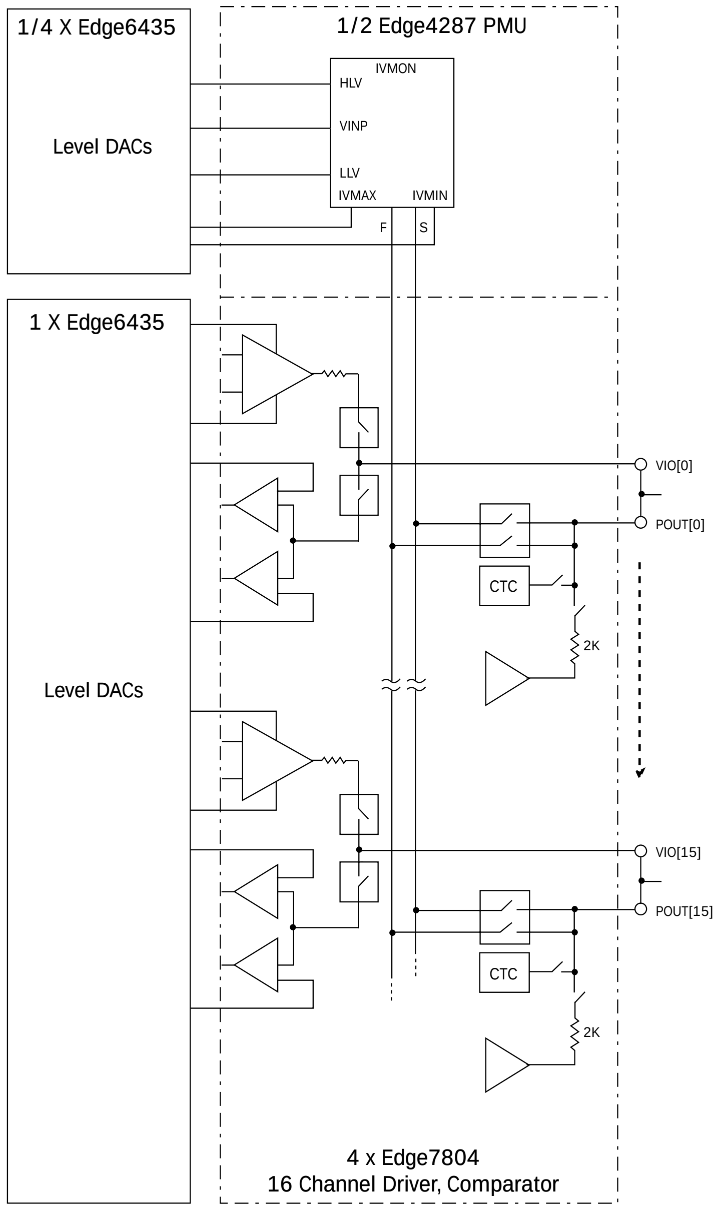
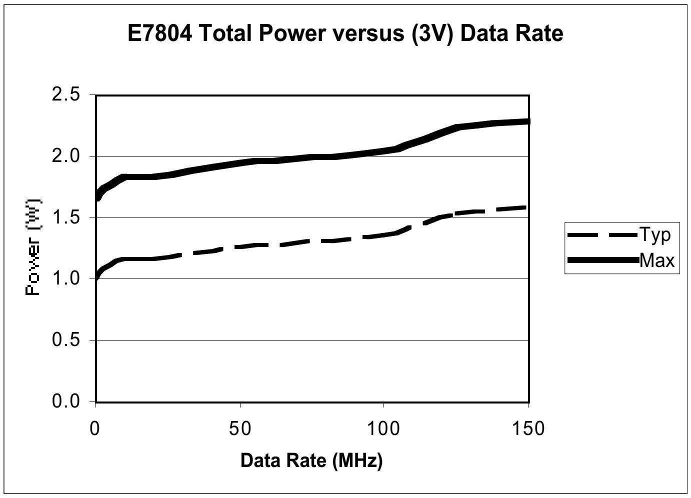


Figure 7. "Low Cost", 16 Channel Pin Electronics

Computing Maximum Power Consumption

The diagram below shows the power consumption of the Edge7804 as a function of clocking frequency of all channels.



The power consumption goes up with frequency and output voltage swing.

Cooling Considerations

Depending on the maximum operating frequencies and voltage swings the Edge7804 will need to drive, it may require the use of heatsinking to keep the maximum die junction termperature within a safe range and below the specified maximum of 100˚C.

The Edge7804 package has an internal heatspreader located at the top side of the package to efficiently conduct heat away from the die to the package top. The thermal resistance of the package to the top is the θ_{JC} (junction-to-case) and is specified at 4˚C/Watt.

In order to calculate what type of heatsinking should be applied to the Edge7804, the designer needs to determine the worst case power dissipation of the device in the application. The graph above gives a good visual relationship of the power dissipation to the maximum operating frequency (all channels simultaneously) and driver output voltage swings. Another variable that needs to be determined is the maximum ambient air temperature that will be surrounding or blowing on the device and/or the heatsink system in the application (assuming an air cooled system). A heatsinking solution should be chosen to be at or below a certain thermal impedance known as R_θ in units of ˚C/Watt. The heatsinking system is a combination of factors including the actual heatsink chosen and the selection of the intertface material between the Edge7804 and the heatsink itself. This could be thermal grease or thermal epoxy, and they also have their own thermal impedances. The heatsinking solution will also depend on the volume of air passing over the heatsink and at what angle the air is impacting the heatsink. There are many options available in selecting a heatsinking system. The formula below shows how to calculate the required maximum thermal impedance for the entire heatsink system. Once this is known, the designer can evaluate the options that best fit the system design and meet the required R_θ.

$R\theta(\text{heatsink\_system}) = (T_{Jmax} - T_{ambient} - P * \theta_{JC}) / P$

where, R_θ(heatsink_system) is the thermal resistance of the entire heatsink system

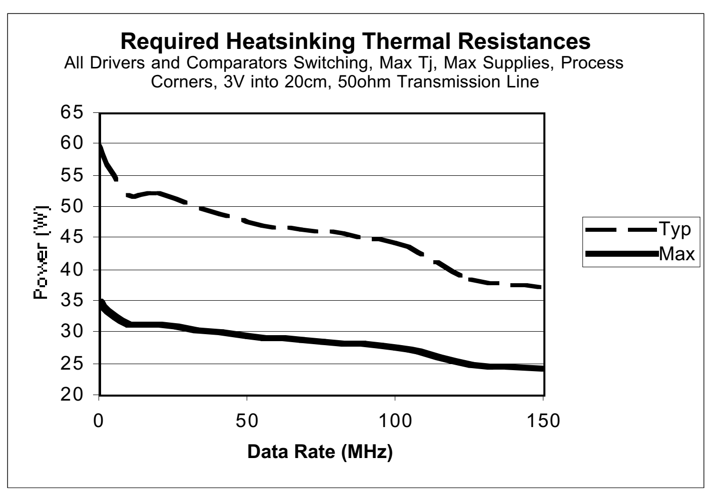
T_{Jmax} is the maximum die temperature (100˚C)

$T_{ambient}$ is the maximum ambient air temp expected at the heatsink (˚C)

P is the maximum expected power dissipation of the Edge7804 (Watts)

θ_{JC} is the thermal impedance of the Edge7804 junction to case (4˚C/W)

The graph below uses the power estimates from the previous graph and indicates the required maximum thermal impedances required for the heatsinking system using the above formula with $T_{ambient}$ at 35˚C.



Application Information *(continued)*

The value of the thermal resistance of the Edge7804 package junction to air with 400 linear feet per minute (LFPM) of airflow is specified at 22˚C/W. At operating points greater than or equal to this value, no additional heatsinking is needed to keep the die temperatures below the maximum 100˚C as long as the ambient temperature of the 400 LFPM air does not exceed 35˚C.

More information on heatsink system selections can be read on heatsink vendors' web sites and in the Semtech Application Note #ATE-A2 *Cooling High Power, High Density Pin Electronics*.

Protection Considerations

The Edge7804 has ESD protection on its input and outputs.

The Edge7804 has internal, high voltage, disconnect switches for VIO and POUT pins. When open, these provide protection against voltages input into VIO and POUT which might have damaged drivers, comparators, and other internal circuits.

Power Supply Sequencing/Latch-Up Protection

In order to avoid the possibility of latch-up when powering this part up (or down), be careful that the conditions listed in the Absolute Maximum Ratings are never violated. That is, the power supplies should never be reverse-polarity with respect to ground, and the input signals should never go beyond the power supply rails.

Furthermore, the lower-voltage analog supplies should never be greater than the higher-voltage supplies (VAA < VCC < VXX). This can easily be implemented by utilizing the diode circuit depicted in Figure 14 for each PCB that has Edge7804 devices on it. The following conditions must be met at all times during power-up and power-down.

1. VEE ≤ GND ≤ VAA ≤ VCC ≤ VXX
2. GND ≤ VDD ≤ VCC
3. VEE ≤ Analog Inputs ≤ VCC or VXX
4. GND ≤ Digital Inputs ≤ VDD

The following sequencing can be used as a guideline when powering up:

1. VEE
2. VXX
3. VCC
4. VAA
5. VDD
6. Digital Inputs
7. Analog Inputs

The recommended power-down sequence is the reverse order of the power-up sequence.

One approach to ensure that the power supply polarities do not become reversed is to use Schottky diodes, as shown in Figure 8. One set of these diodes should be used per board. The optimum type of Schottky will depend on how much current the power supplies can source.

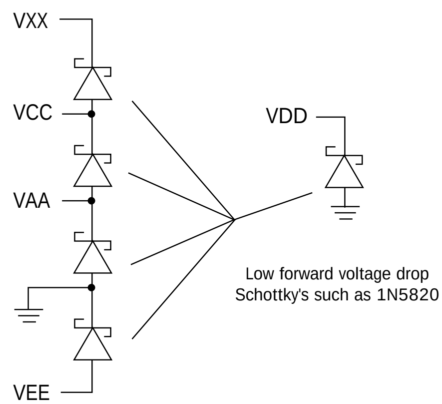
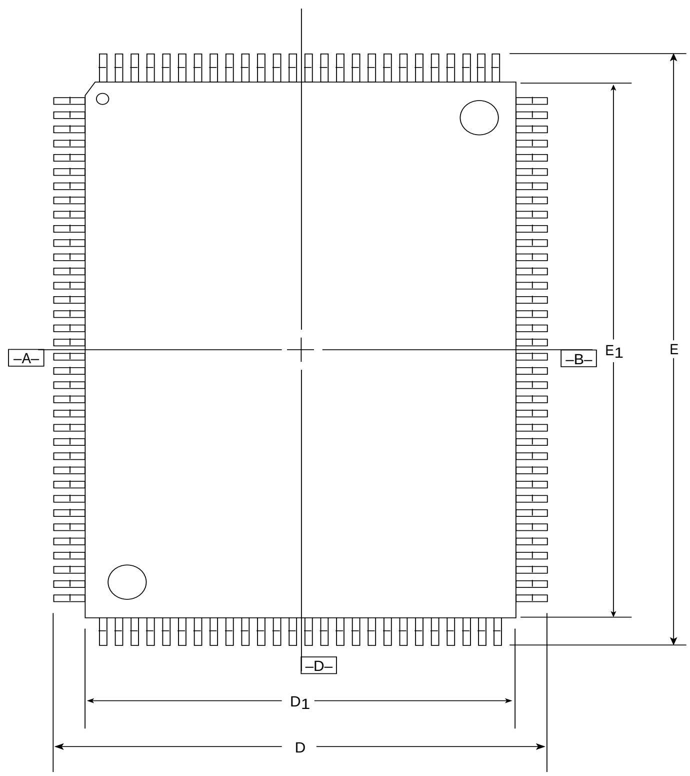
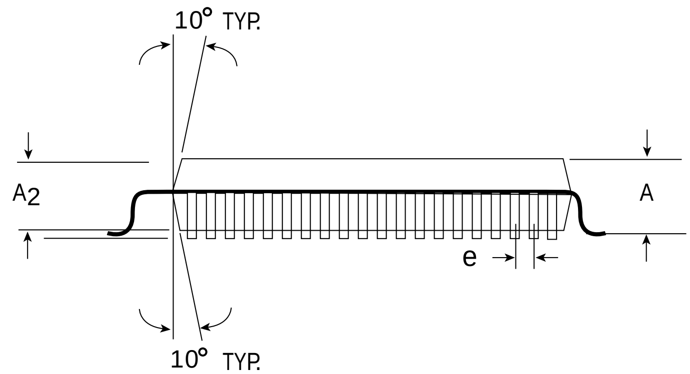


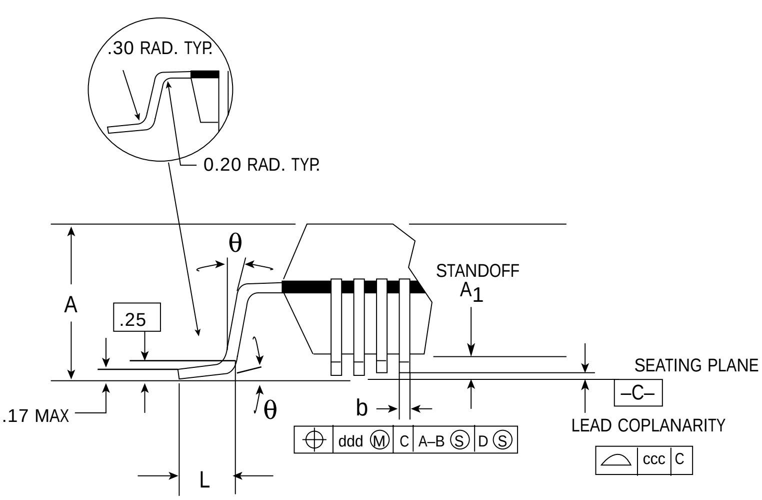
Figure 8. Board Level Supply Diodes

14 x 20 x 2 mm, 128-Pin MQFP Package (with Internal Heat Spreader)



Top View





DIMS.	TOL.	128 Leads
A	MAX	2.35
A_1	MAX.	.25
A_2	±.10	2.00
D	±.20	17.20
D_1	±.10	14.00
E	±.20	23.20
E_1	±10	20.00
L	±0.15	.88
e	BASIC	.50
b		0.19~0.27
θ		0° – 7°
θ_1	±4°	6°
ddd	MAX	.08
ccc	MAX	.08

NOTES:
1) All dimensions in mm.
2) Dimensions shown are nominal with tol. as indicated.
3) Foot length “L” is measured at gage plane at 0.25 above the seating plane.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Positive Analog Supply – VCC or VXX	VCC, VXX	–0.5	VEE + 16	V
Positive Analog Supply – VAA	VAA	–0.5	+6.0	V
Negative Analog Supply – VEE	VEE	–5.5	+0.5	V
Digital Power Supplies – VDD	VDD	–0.5	+6.0	V
Total Power Supply Ranges	VCC to VEE	–0.5	+16	V
	VCC to VAA	–0.5	+16.0	V
Digital Input Voltages	SDIN, CLKIN, LOAD, RESET*, OPN	DGND – 0.5	VDD + 0.5	V
Driver/Comparator Pin				
Comparator Only Connected	VIO	VEE	VCC	V
	VIO	CVL – 6	CVH + 6	V
Driver Connected	VIO	DVL – 0.7	DVH + 0.7	V
Parametric Pin				
CTC and PUV not Connected	POUT	VEE	VXX	V
CTC Connected	POUT	VEE	VAA	V
PUV Connected	POUT	0	VAA	V
Storage Temperature	TS	–65	+150	°C
Junction Temperature	TJ		+125	°C
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		+240	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those 'recommended', is not implied. Exposure to conditions above those recommended for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply to Switches	VXX to AGND	VCC	+9.5	VEE + 15.0	V
Positive Analog Power Supply – Channels	VCC to AGND	+8.0	+8.25	+8.5	V
Positive Analog Power Supply – Channels	VAA to AGND	+4.75	+5.0	+5.5	V
Negative Power Supply – Channels	VEE to AGND	–5.25	–5.0	–4.75	V
Total Analog Supply Range	VCC to VEE	+12.75		+13.75	V
Digital, Logic Power Supplies	VDD to DGND	+3.13	+3.3	+3.46	V
Thermal Resistance - Junction to Case (Top)	θ_{JC}		4		°C/W
Thermal Resistance - Junction to Ambient					
Still Air	θ_{JA}		28		°C/W
100 lfpm	θ_{JA}		25.2		°C/W
400 lfpm	θ_{JA}		22.1		°C/W
Junction Temperature	T_J	+25		+100	°C

Note: AGND and DGND must be connected together externally.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs (CLKIN, SDIN, LOAD, RESET*, OPN)					
Input Low Voltage	VIL			0.8	V
Input High Voltage	VIH	2.0			V
Input Current	IIN	–200		+200	nA
Digital Output (SDOUT)					
Output Low Voltage	VOL			0.4	V
Output High Voltage	VOH	2.4		VDD	V
Output Current Low	IOL			2.0	mA
Output Current High	IOH	–2.0			mA
Capacitive Load	C_{LOAD}			15	pF

Parameter	Symbol	Min	Typ	Max	Units
DRIVER Circuit					
Analog Inputs (DVH, DVL)					
High Level	DVH	DVL + 0.5		VAA + 0.1	V
Low Level	DVL	–0.25		DVH – 0.5	V
Input Current	IIN	–10		+20	µA
Driver Output (VIO)					
Range	DRNG	–0.2		VAA	V
Driver Swing	DSWG	0.5		5.4	V
DC Output Current	IOUT	–50		+50	mA
Output Impedance (Note 1)	ROUT	48		110	Ω
Output Impedance Accuracy (Note 2)	RACC		4		%
HiZ Leakage (DEN = 0) (Note 3)	IOZ	–1		+1	µA
Open Circuit Leakage (Driver, comparator disconnected) at VIO (VEE to VXX)	IOC	–10		+10	nA
DC Accuracy (Note 4)					
Offset Voltage (DVH – VIO, DVL – VIO)	VOS	–20		+20	mV
Gain		0.99		1.01	V/V
Linearity		–0.1		+0.1	% FSR
Digital Inputs to Driver					
Input Voltage Range	DHI(*), DEN(*)	0		VDD	V
Differential Input Swing	|Input – Input*|	±0.24		VDD	V
Input Current	IIN	–0.2		+0.2	µA
External Reference Resistor	R_{EREF}	4.5		11	KΩ

DC conditions (unless otherwise specified): Over the full "Recommended Operating Conditions", including the full range of the power supplies.

Note 1: At VIO = (DVH + DVL) / 2.
Note 2: Following calibration. Accuracy is measured as a percentage of R_{EREF}/100.
Note 3: Comparator disconnected. Driver leakage specified for 0 ≤ [V_{VIO} and DVH and DVL] ≤ VAA.
Note 4: Offset measured with input voltage (DVL or DVH) at the minimum value, and the gain error measured with the input voltage at the maximum allowed value. Measurements made with VIO unloaded.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
COMPARATOR Circuit					
Analog Inputs (CVA, CVB)					
Voltage Range	V_{CVA}, V_{CVB}	–2.0		+5.5	V
Input Current	IIN	–5		+30	µA
Input Differential Voltage Range [(VIO – CVA), (VIO – CVB)]	V_{DIFF}	–6.0		+6.0	V
Hysteresis	V_{HYS}	5		20	mV
Input Leakage (Driver disconnected) at VIO (–2.0 to +5.5V)	I_BIAS	–5		+25	µA
Input Leakage (Driver, Comparator disconnected) at VIO (VEE to VXX)	IOC	–10		+10	nA
Offset Voltage	VOS	–20		+20	mV
Digital Outputs (Figure 9)					
Differential Output Swing	VOD	250		450	mV
Common Mode Output Voltage Range	VCM	1.125		1.375	V
Change in VOD between Complimentary Output States	ΔVOD			±35	mV

Parameter	Symbol	Min	Typ	Max	Units
Continuity Test Circuit (CTC)					
CTCLV (Limit Voltage)					
Voltage Range		–2.0		0	V
Input Current	IIN	–1		+10	µA
Offset Error		–20		+20	mV
Gain Error		–5		+5	%
CTCFIV					
Input Current	IIN	–200		+200	nA
CTC Output Compliance Voltage		CTCLV + 0.25		VAA–1	V
CTC Output Current (Note 1)					
Programmable Range	I_{CTC}	–250		–15	µA
Offset		–15		+15	µA
Gain Error		–15		+15	%

DC test conditions (unless otherwise specified): Over the full "Recommended Operating Conditions", including the full range of the power supplies.

Note 1: Programmed by CTCFIV using the formula: $I_{CTC} = -1.09 * [CTCFIV(V) / R_{EREF}(\Omega)]$. Offset and gain are calculated from calibration points at 10% and 90% of the 250 µA full-scale range.

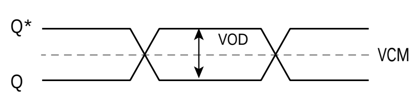


Figure 9. Comparator Outputs

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
External PMU Switches, VIO/POUT Capacitance					
On-Resistance (EPMU Force Switch S4 to POUT) (±40mA)			40	110	Ω
On-Resistance (EPMU Sense Switch S4 to POUT) (±4mA)				500	Ω
On-Resistance (EPMUF and EPMUS Switch S7 to PMU_OUT) (±100µA)		100		7000	Ω
On-Resistance (Driver Output to EPMUS Switch S3) (±100µA)		100		7000	Ω
Leakage Current @ EPMUS (all channel's switches onto EPMU bus are open)		–10		+10	nA
Leakage Current @ EPMUF (all channel's switches onto EPMU bus are open)		–15		+15	nA
Capacitance @ EPMUS (all channels' switches onto EPMUS bus are open)			15		pF
Capacitance @ EPMUF (all channel's switches onto EPMU bus, open) (0 to 50 MHz)			35		pF
Capacitance at POUT (Switches Open) (Note 1)			12		pF
Capacitance @ VIO (S1 = Open, S2 = Closed)			15		pF
Capacitance @ VIO (S1 = S2 = Closed)			38		pF
Leakage Current at POUT (Switches Open) (Note 1)		–10		+10	nA
Max Current for EPMU Force Paths		–40		+40	mA
Max Current for EPMU Sense Paths		–4		+4	mA
POUT Output Range with EPMUF ≤ +40 mA		VEE		VXX – 2.5	V
POUT Output Range with EPMUF ≥ –40 mA		VEE + 2.5		VXX	V
POUT Output Range with EPMUF ±40 µA		VEE		VXX	V
PMU_OUT Leakage		–1		+1	µA
Pull-Up Resistor					
Pull-Up Resistor (including its switch)		1		3	KΩ
PUV Voltage Range		0		VAA	V
PUV Gain Error		–2		+2	%
PUV Input Current		–3		+3	µA
POUT Voltage Range with S6 Closed	$V(POUT_{S6})$	0		VAA	V

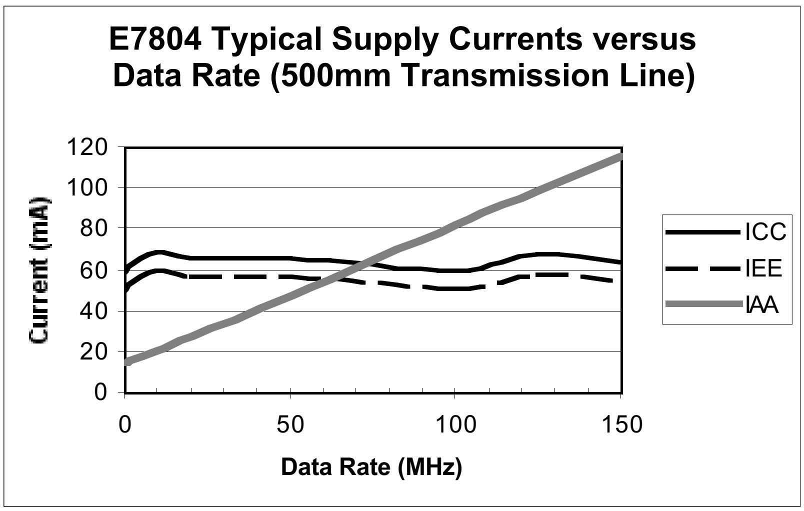
DC conditions (unless otherwise specified): Over the full "Recommended Operating Conditions".

Note 1: Includes the EPMU, Continuity Test and Pull-up Switches

DC Characteristics *(continued)*

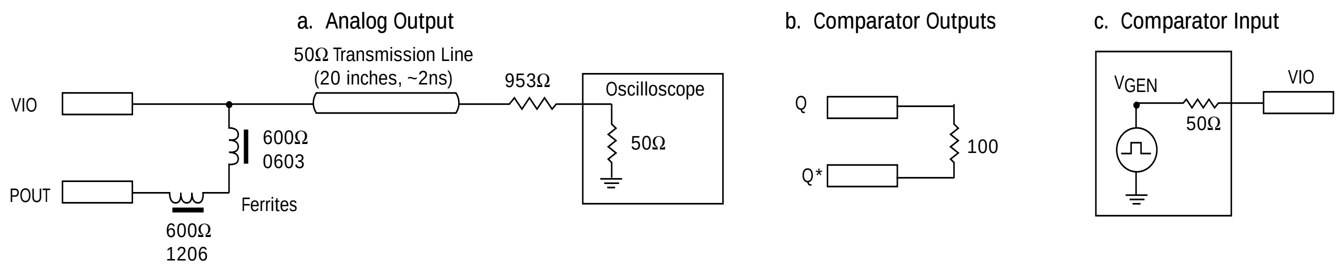
Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Max Quiescent Power Supply Consumption (Note 1)					
Positive Analog Supply 1	I_{CC}		60	90	mA
Positive Analog Supply 2	I_{AA}		18	30	mA
Digital Supply	I_{DD}		55	80	mA
Negative Power Supply	I_{EE}	–80	–45		mA
Switch Power Supply	I_{XX}		1	4	mA

Note 1: CLKIN Low, no VIO output currents, comparators with 100Ω floating terminations.



The above graph depicts supply current variation with respect to all the Drivers concurrently driving the same 3V output swings over frequency into a 50cm unterminated transmission line while also connected to the window comparators.

AC Characteristics



NOTE: Driver propagation delays specified with transmission line delay removed.

Figure 10. AC Test Circuits

Parameter	Symbol	Min	Typ	Max	Units
COMPARATOR Circuit (Driver S1 Open)					
Propagation Delay (0 to 3V Input) (Figure 16)					
Note 4	Tpd(+),(–)	3.0		7.0	ns
Note 5	Tpd(+),(–)	3.0		6.0	ns
Digital Output Rise and Fall Times (20% - 80%) (into 100Ω floating termination)	Tr, Tf		550		ps
Minimum Pulse Width (Note 1)				6	ns
Propagation Delay Matching (Note 5)	Tpd(+),(–)			1.0	ns
DRIVER Circuit					
Propagation Delay (0 to 3V Output) (Note 2, Figure 17)					
Data (DHI) to Output					
Note 4	TPLH, TPHL	3.3		6.1	ns
Note 5	TPLH, TPHL	3.4		5.7	ns
Enable to HiZ (Figure 12)	TPAZ	3.0		6.5	ns
Enable to Output Active (Figure 12)	TPZA	2.5		6.0	ns
Propagation Delay Match (Tpd(+) to Tpd(–)) (Note 5)	Tpd(+) to (–)			1.0	ns
Rise/Fall Times					
0 to 800 mV (20% - 80%)	Tr/Tf			2.0	ns
0 to 3V (10% - 90%)	Tr/Tf	2.4		2.5	ns
0 to 5V (10% - 90%)	Tr/Tf			3.0	ns
Fmax (Note 3, Figure 13)					
800 mV	Fmax	133			MHz
3V	Fmax	133			MHz
5V	Fmax	100			MHz
Minimum Pulse Width (Note 3, Figure 14)					
0 to 800 mV	T_{pw+}, T_{pw-}			3.0	ns
0 to 3V	T_{pw+}, T_{pw-}			3.0	ns
0 to 5V	T_{pw+}, T_{pw-}			4.5	ns

AC test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: For 3V input while maintaining less than 300 ps of propagation delay variation.
Note 2: Driver propagation delays are measured with LVDS differential logic inputs at DHI and DEN. Output delay is specified with transmission line delay removed.
Note 3: At less than 10% output amplitude attenuation, DVL = 0V.
Note 4: Over all recommended operating conditions and junction temperatures.
Note 5: VDD at 3.3V, VCC = 8.25V, VEE = –5V, Junction Temperature at 45°C.

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Driver Performance Specs					
Driver Temp. Coefficient (Δpd/ΔT) (Note 4)	ΔTpd/°C			10	ps/°C
Driver Tpd Dispersion vs. Amplitude (Note 1, Figure 11)	ΔTpd (Swing)		0.7	1	ns
Driver Tpd Dispersion vs. Common Mode (Note 2, Figure 11)	ΔTpd (cm)		0.8	1	ns
Driver Tpd Dispersion vs. Pulse Width (Note 3, Figure 15)	ΔTpw		0.3	0.4	ns
Comparator Performance Specs					
Comparator Temp. Coefficient (Δpd/ΔT)	ΔTpd/°C		6	10	ps/°C
Comparator Tpd Dispersion vs. Overdrive (Figure 17)			1.5	2	ns
Comparator Tpd Dispersion vs. Common Mode (Figure 18)			1.1	1.5	ns
Comparator Tpd Dispersion vs. Edge Rate (Figure 19)			0.8	1	ns
Comparator Waveform Tracking Dispersion (Figure 20)			3.0	3.5	ns
Comparator Tpd Dispersion vs. Pulse Width (Figure 21)			0.4	0.7	ns
Internal Switches					
OPN Input to S1 and S2, Time to:					
Disconnect				1	µs
Connect				1	µs
PMU to POUT, S4, Connect/Disconnect (measured from valid LOAD and CLKIN edges) (Note 5)				1	µs

Note 1: Variation in propagation delay when DVL = 0, vary DVH from 0.5V to 5.0V.
Note 2: Driver Output = 0.8V swing. Common mode = 1.0V to 3.0V.
Note 3: Propagation delay change when going from long to short pulse widths.
Note 4: DVL = 0V, DVH = 3V.
Note 5: Switches S1-S6 open on the fourth (4th) low-going CLKIN edge after a LOAD signal is applied.
S1-S6 will close on the fifth (5th) low-going CLKIN edge.
Switch S7 will open or close on the fourth (4th) low-going CLKIN edge after LOAD.

AC Characteristics *(continued)*

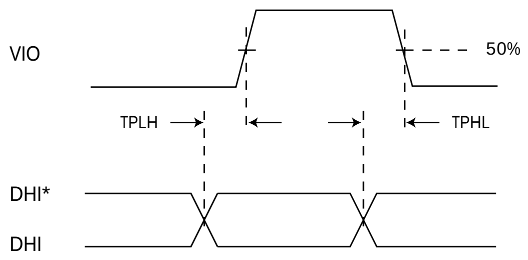


Figure 11. Driver Propagation Delay Measurements

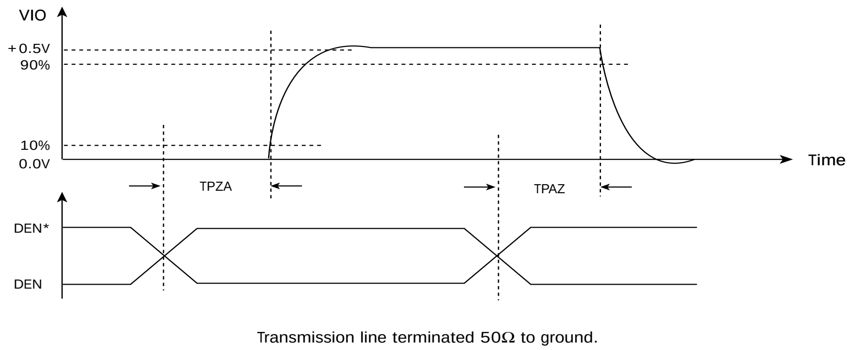


Figure 12. Driver HiZ Enable/Disable Delay Measurement Definition

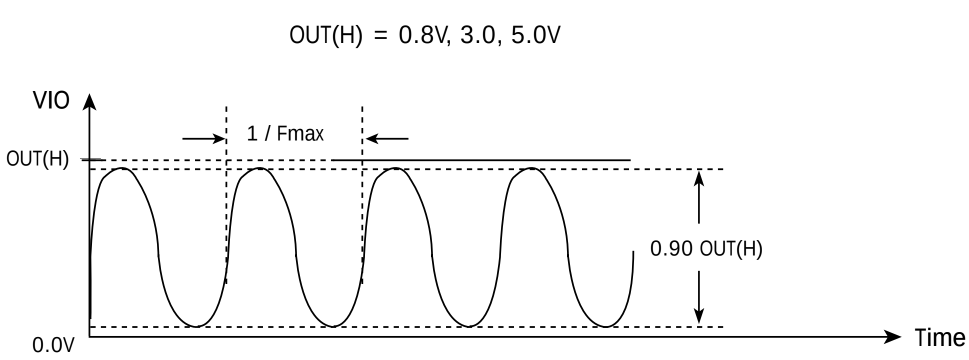


Figure 13. Driver Fmax Measurement Definition

AC Characteristics *(continued)*

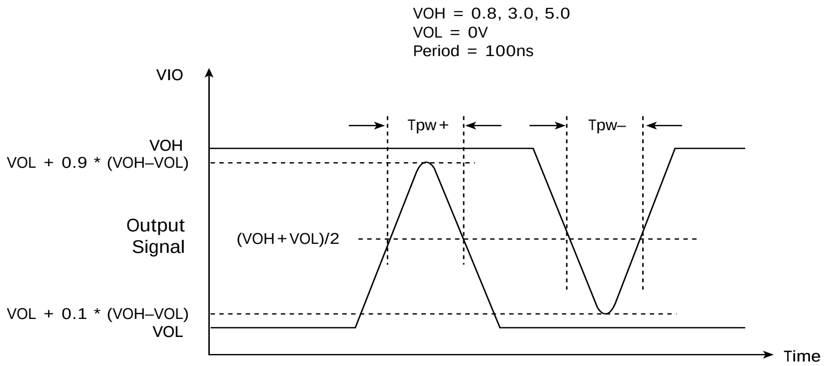
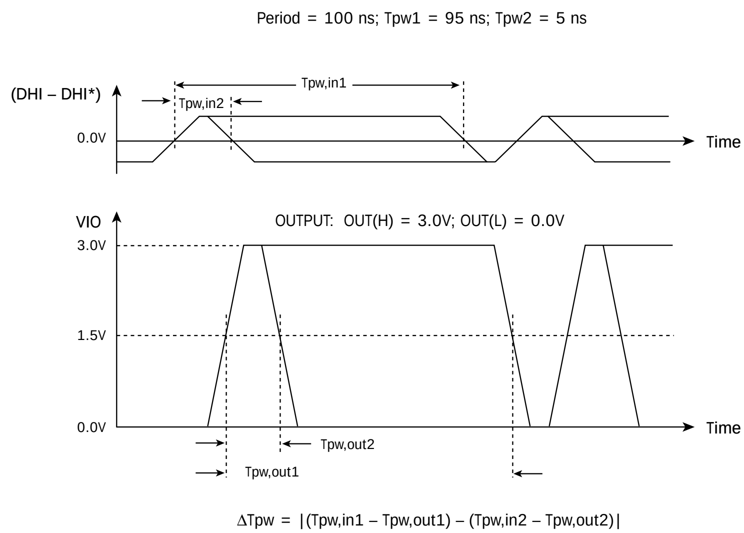


Figure 14. Driver Minimum Pulse Width Measurement Definition



The measured result is the absolute value of the change in [Tpw,in – Tpw,out] as P.W. changes from 50 ns to the endpoints of 5 ns and 95 ns.

Figure 15. Driver Dispersion: Pulse Width Measurement Definition

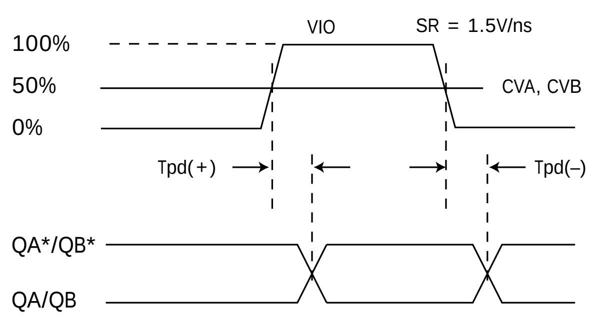
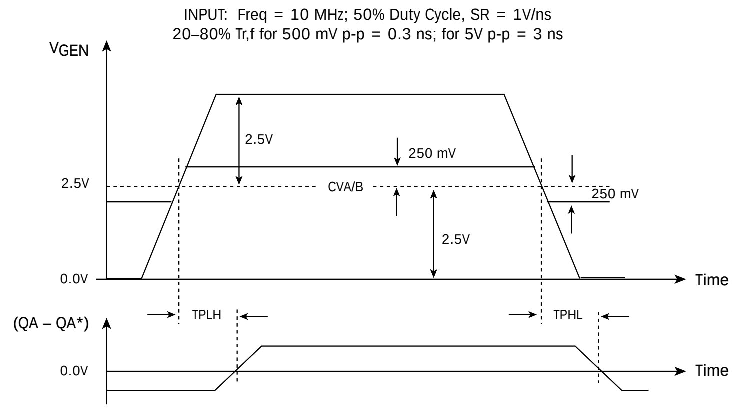


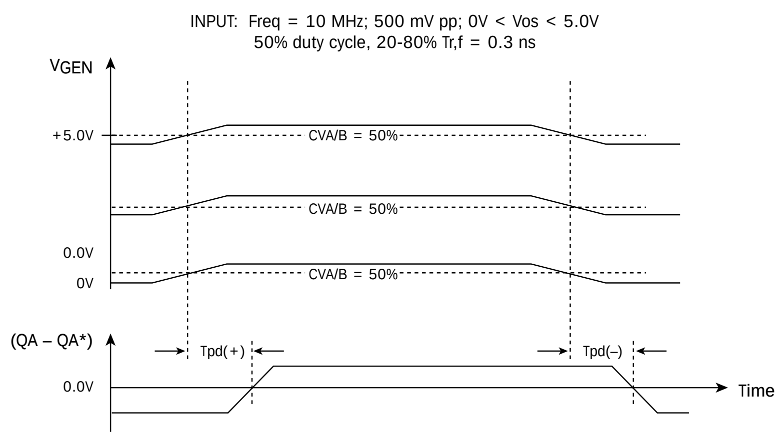
Figure 16. Comparator Propagation Delay Measurements

AC Characteristics *(continued)*



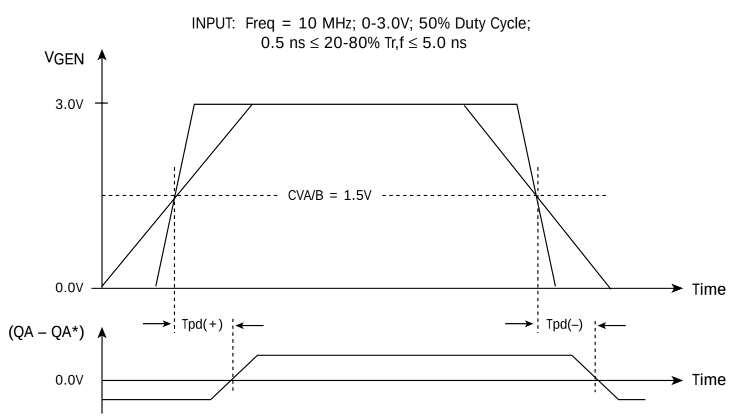
The measured result is the absolute value of the change in TPLH or the change in TPHL when the overdrive changes from 2.5V to 250 mV.

Figure 17. Comparator Dispersion: Overdrive Measurement Definition



The measured result is the maximum absolute value change in Tpd(+) or Tpd(–) over the different common mode levels.

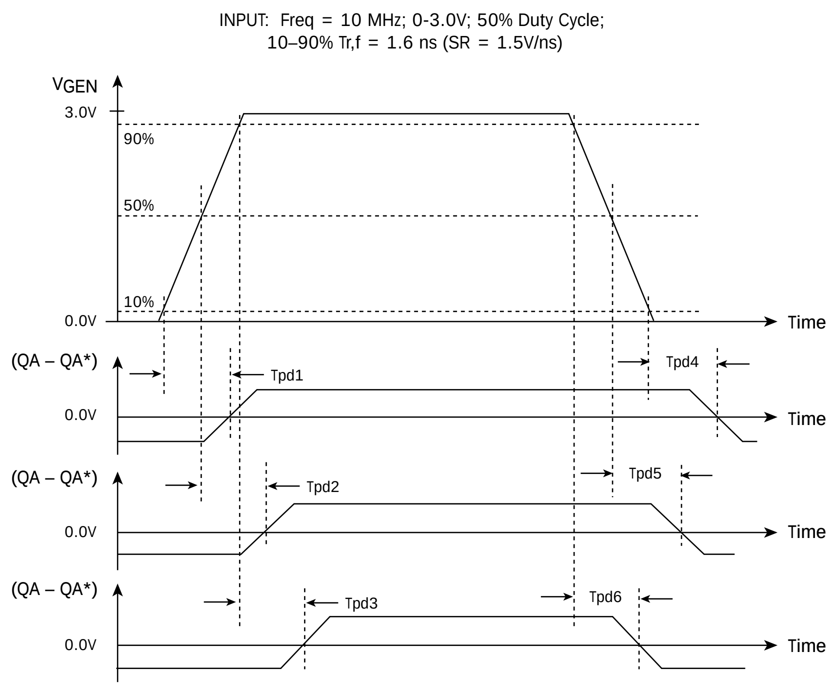
Figure 18. Comparator Dispersion: Common Mode Measurement Definition



The measured result is the absolute value of the change in Tpd(+) or Tpd(–) as the input slew rate changes from minimum to maximum as defined above.

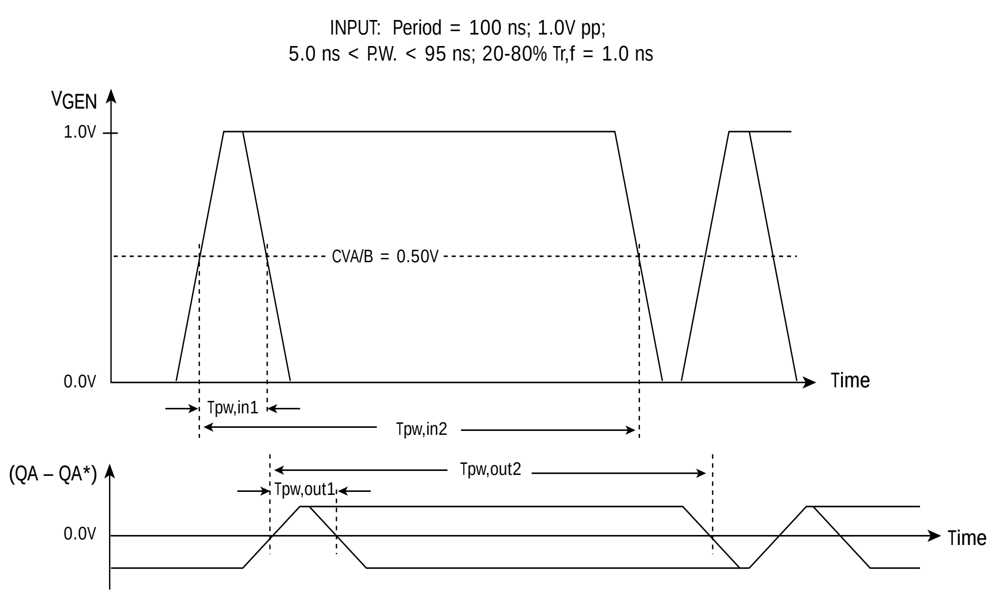
Figure 19. Comparator Input Slew Rate Measurement Definition

AC Characteristics *(continued)*



The measured result is the maximum absolute value change in Tpd(+) or Tpd(–) among the three measurement points on the waveform depicted above.

Figure 20. Comparator Dispersion: Waveform Tracking Measurement Definition



The measured result is the absolute value change in [Tpw,in – Tpw,out] as P.W. changes from 50 ns to the endpoints of 5 ns and 95 ns.

Figure 21. Comparator Dispersion: Pulse Width Measurement Definition

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Logic Specifications (see Figure 22)					
Set Up Times (to CLKIN rising edge)					
SDIN	T_{SU_SDIN}	3			ns
LOAD	T_{SU_LD}	5			ns
Hold Times (to CLKIN rising edge)					
SDIN	T_{HLD_SDIN}	5			ns
LOAD	T_{HLD_LD}	8			ns
Output Delay Times (to CLKIN falling edge)					
SDOUT	T_{SDOUT}	2.0		8.0	ns
CLKIN					
Fmax	Fmax			33	MHz
Clock High Time	T_{CLKH}	13			ns
Clock Low Time	T_{CLKL}	13			ns
RESET to Clock Hold-Off Time (Note 1)	T_{RST_IN}	10			ns
RESET Pulse Width	PW_{RESET}	20			ns

Note 1: After an external RESET* event, valid input signals (SDIN and CLKIN) should be held off to allow internal gates to exit RESET. SDIN and CLKIN edges may be present before T_{RST_IN}, but the clocked states cannot be guaranteed. The RESET signal is asynchronous on both assertion and de-assertion.

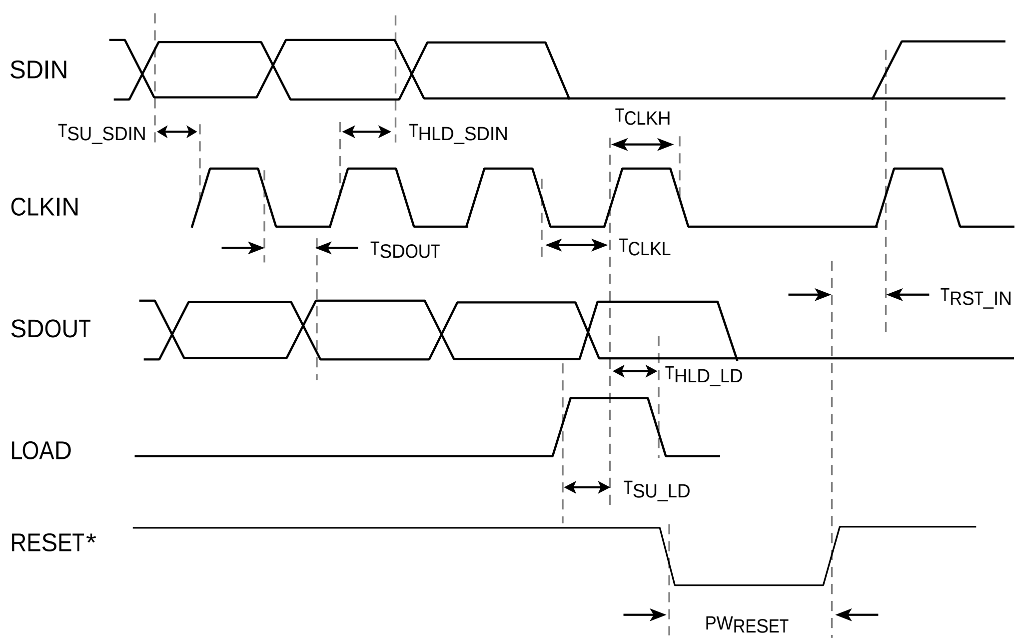


Figure 22. Logic Timing Diagram

Ordering Information

Model Number	Package
E7804BHF	128-Pin, 14 x 20 x 2mm MQFP 0.5 mm Lead Pitch (with Internal Heat Spreader)
EVM7804BHF	Edge7804 Evaluation Board

Contact Information

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