622 MHz 32:4 Multiplexer GD16334

Preliminary

General Description

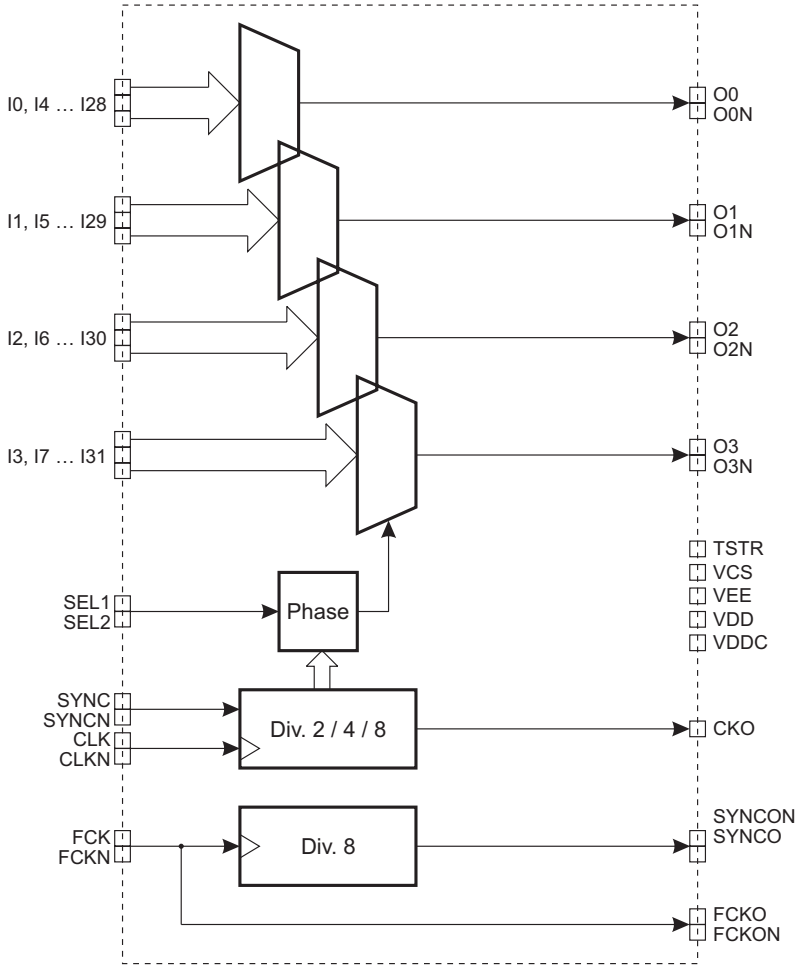
GD16334 is a 32:4 multiplexer, intended for use with the GD16255, an STM-64 16:1 mutliplexer with PLL or in DSP applications with fast DAC's.

The GD16334 consists of:
- four 8:1 multiplexers
- a clock generator circuit
- a synchronisation circuit

The synchronisation circuit, enables a parallel coupling of several devices. This is done with a master clock divider, which distributes a synchronisation signal to the parallel devices.

The GD16334 is provided in a 100 pin power enhanced plastic package.

The chip is designed for operation between -5 °C and +85 °C (case temperature).



Features

- Clock frequency to 622 MHz.
- 32:4 MUX, obtained by four 8:1 synchronised MUX'es.
- High speed differential inputs, CML/PECL level.
- High speed differential CML outputs.
- Low speed inputs are CMOS level.
- 100 pin QFP (14 x 20 mm) power enhanced plastic package.
- Power consumption: 2.0 W typical.
- Synchronisation of parallel devices, for wider bus widths.
- 5 V single supply operation.

Applications

- Tele Communication
  - STM-64
    STM-16
  - OC-192
    OC-48
- DSP
  - High speed DAC interface

Functional Details

Synchronisation

The GD16334 provides a synchronisation block that allows parallel operation of multiple devices for wider data width. When this is required only the synchronisation block in one GD16334 device is used as master controller, which drives the synchronisation input of all parallel connected (slave) MUX devices.

The synchronisation block provides a clock output (FCKO) and a SYNCO signal (which is a 1/8 clock signal) timed by the FCKO output. These signals are then daisy-chained to the CLK and SYNC inputs of all the MUX devices. This solution provides a fully synchronised parallel multiplexer structure, where all MUX data ports samples data in the same clock cycle.

The data inputs (FCK, CLK and SYNC) allow for either CML or PECL termination. Termination resistors must be provided externally (i.e. 50 Ω to V_{DD} if CML or 50 Ω to V_{DD} -2 V if PECL). The FCKO and SYNCO outputs are both open drain outputs accommodating the CLK and SYNC inputs in CML configuration.

There are two ways to connect the master clock, provided at the input to the GD16334's from the upstream device, with different timing constrains. Using the clock output (FCKO) from the synchronisation block, will give a good timing condition for the SYNC signal path, with respect to the clock. But it will put constrains on the timing at the data outputs, since the synchronisation block will add a delay to the master clock, with respect to the data coming from the upstream device (refer to Figure 1).

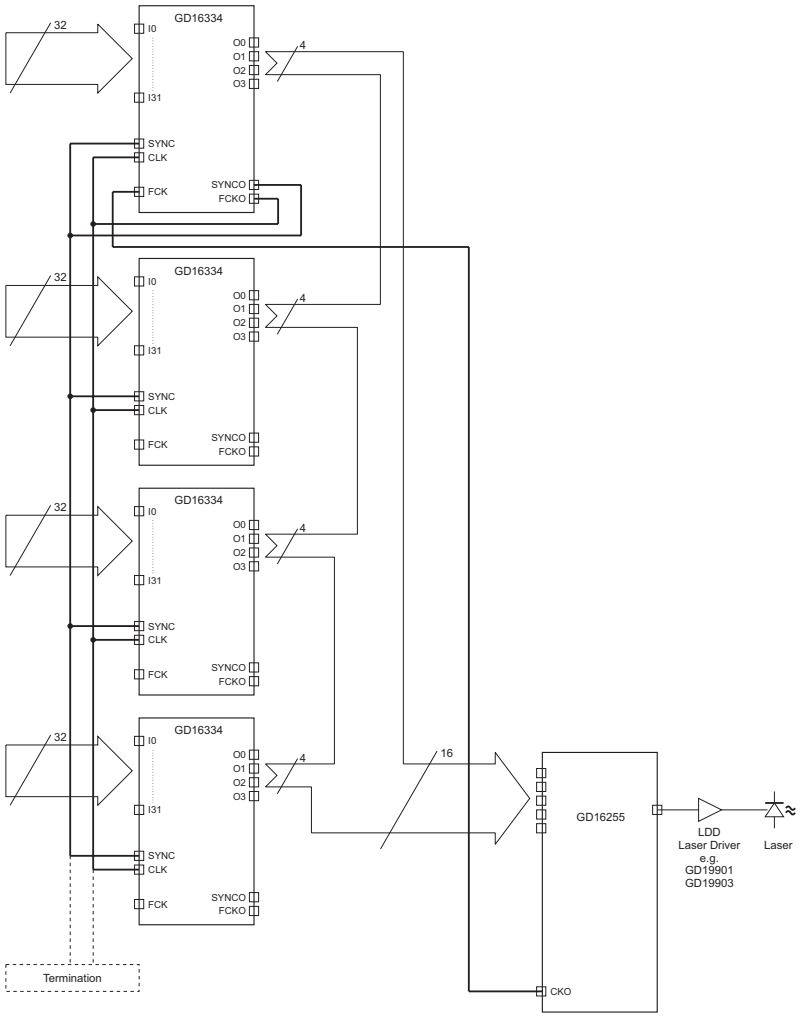


Figure 1. *GD16255: 10 Gbit/s, STM64 transmitter application.*

Another approach is to feed the input clock directly to the CLK input of the MUX'es, maintaining the data/clock relations as given by the upstream device. This will however put constrains on the timing of the SYNC signal path. Depending on actual timing of the upstream device and actual board layout, both approaches may prove applicable.

In either case, to compensate for board delays use the far-end device as clock master such that the clock propagating the slave devices compensates delay on data propagating to the GD16255.

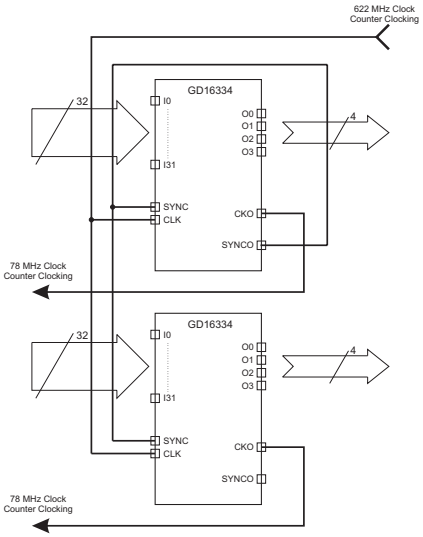


Figure 2. *Maintaining fast clock < - > data relations*

Practical Considerations

The SYNC and CLK control signals are differential high-speed control signals. Care should be taken to design the routing of these signals as transmission lines, i.e. as coplanar wave guides, or as strip lines. The signals should be routed without branches from the signal source with shortest possible distance to the first load, then onwards to the next load, and finally terminating in a resistor matching the transmission line impedance, normally 50 Ω. The transmission line should not have any branches in order to minimise stub effects (reflections).

Pin List

Mnemonic:	Pin No.	Pin Type:	Description:
O0, O0N O1, O1N O2, O2N O3, O3N	9, 8 72, 73 58, 57 23, 24	CML OUT	622 Mbit/s differential data output.
CLK, CLKN	63, 64	CML/PECL IN	622 MHz differential clock input.
SYNC, SYNCN	61, 62	CML/PECL IN	78 MHz synchronisation input.
I0, I4, I8, I12, I16, I20, I24, I28	7, 6, 5, 4, 99, 98, 97,96	CMOS IN	78 Mbit/s MUX input, for O0.
I1, I5, I9, I13, I17, I21, I25, I29	74, 75, 76, 77 82, 83, 84, 85	CMOS IN	78 Mbit/s MUX input, for O1.
I2, I6, I10, I14, I18, I22, I26, I30	56, 55, 54, 53 49, 48, 47, 46	CMOS IN	78 Mbit/s MUX input, for O2.
I3, I7, I11, I15, I19, I23, I27, I31	25, 26, 27, 28 32, 33, 34, 35	CMOS IN	78 Mbit/s MUX input, for O3.
CKO	67	CMOS OUT	78 MHz clock output, used to sample I0..I31, the sampling point can be adjusted in 4 phases defined by SEL1 and SEL2. 0° refers to sampling on clock going from high to low.
SEL1, SEL2	69, 13	CMOS IN	Select the sampling point of I0..I31 rel. to CKO. 0° : SEL1=0, SEL2=1 90° : SEL1=0, SEL2=0 180° : SEL1=1, SEL2=1 270° : SEL1=1, SEL2=0
FCK, FCKN	15, 16	PECL/CML IN	622 MHz differential input to clock divider.
FCKO, FCKON	17, 18	CML OUT	622 MHz differential clock output from clock divider.
SYNCO, SYNCON	19, 20	CML OUT	78 MHz synchronisation output, timing identical to FCKO for synchronisation.
TSTR	14	CMOS IN	Test reset. Only used in test, connect to V_{DD}.
VCS	68	Analog IN	Internal control voltage, leave open.
VEE	1, 2, 11, 21, 30, 31, 36, 39, 40, 41, 42, 45, 50, 51, 60, 66, 70, 79, 80, 81, 86, 89, 90, 91, 92, 95, 100	GND	0 V
VDDC	65	PWR	5 V, CMOS power
VDD	3, 10, 12, 22, 29, 37, 38, 43, 44, 52, 59, 71, 78, 87, 88, 93, 94	PWR	5 V, CML power
Heat sink			Connected to VEE

Package Pinout

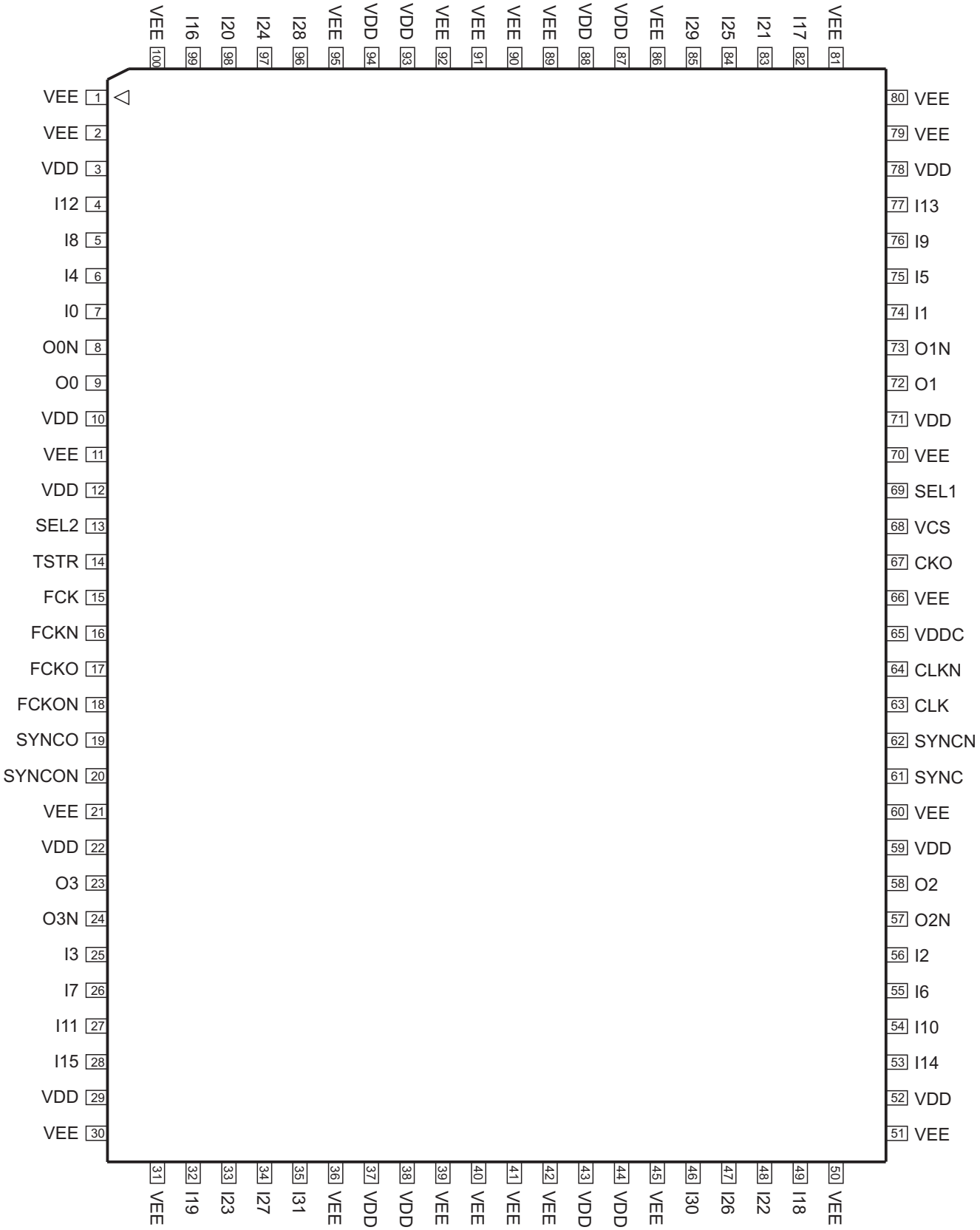


Figure 3. *Package 100 pin QFP, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VEE.
All currents are defined positive in to the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT
V_{DDC}	Supply Voltage CMOS	rel. to V_{EE}	0		6	V
V_{DD}	Supply Voltage	rel. to V_{EE}	0		6	V
V_O *max*	Output Voltage		-0.5		V_{DD}+0.5	V
I_O *max*	Output Current	CML	-15		0	mA
I_O *max-CMOS*	Output Current	CMOS	-30		30	mA
V_I *max*	Input Voltage		-0.5		V_{DD}+0.5	V
I_I *max*	Input Current		-1.0		1.0	mA
T_j	Operating Temperature	Junction	-55		125	°C
T_s	Storage Temperature		-65		150	°C

Thermal Characteristics

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$\theta_{j\text{-}c}$	Thermal resistance, junction to case			11.7		°C/W
$\theta_{j\text{-}a}$	Thermal resistance, junction to ambient	Still air, Horizontal mounting		42		°C/W
T_o	Operating Temperature	Case	-5		+85	°C

Thermal Considerations

A heat-conducting slug is placed at the bottom of the package allowing heat dissipation out of the bottom of the IC package to the PCB. The heat slug can be soldered to a conducting plane (VEE) on the PCB using solder paste, or a thermally conducting foil can be placed under the package. If the thermal foil method is preferred, a 0.25 mm thick foil may be used.

Via holes for heat transfer to the other side of the PCB should be made and a heat sink can be attached on the opposite side of the PCB if required.

DC Characteristics

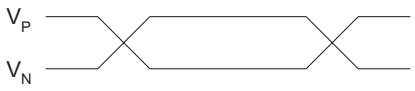
All voltages in table are referred to VEE.
All currents are defined positive in to the pin.
T_{CASE} = -5 °C to 85 °C.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply Voltage		4.75	5.00	5.40	V
I_{DD}	Supply Current	Note 1		210	250	mA
$V_{CM,CML/PECL}$	CML/PECL Input Common Mode Voltage	Note 2	V_{DD}-2.00		V_{DD}-0.2	V
$V_{Idiff,CML/PECL}$	CML/PECL Differential Input Voltage	Note 3	100	500	1400	mV
$I_{IH,\ CML}$	CML Input HI Current	$V_{IH}max$			0.4	mA
$I_{IL,\ CML}$	CML Input LO Current	$V_{IL}\ min$	-25			µA
$I_{O,CML\ LOW}$	CML Output Current	Logic “0”	6	8	10	mA
$I_{O,CML\ HIGH}$	CML Output Current	Logic “1”	0		1.5	mA
$V_{IH,CMOS}$	CMOS Input HI Voltage		$\frac{V_{DD}}{2}$ +0.5		V_{DD}	V
$V_{IL,CMOS}$	CMOS Input LO Voltage		0		$\frac{V_{DD}}{2}$ -0.5	V
$I_{IH,CMOS}$	CMOS Input HI Current	$V_{IH}max$			400	µA
$I_{IL,CMOS}$	CMOS Input LO Current	$V_{IL}min$	-300			µA
$V_{OH,CMOS}$	CMOS Output HI Voltage		0.8 x V_{DD}		V_{DD}	V
$V_{OL,CMOS}$	CMOS Output LO Voltage		0		0.3 x V_{DD}	V
$I_{OH,CMOS}$	CMOS Output HI Current	CKO			16	mA
$I_{OL,CMOS}$	CMOS Output LO Current	CKO	-16			mA

Note 1: Supply currents are estimates, based on post-layout simulations.

Note 2: $V_{CM} = \frac{V_P + V_N}{2}$

Note 3: $V_{Idiff} = |V_P - V_N|$



AC Characteristics

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$T_{pd,fcko}$	Delay from FCK to FCKO		0.6	0.9	1.3	ns
$T_{pd,synco}$	Delay from FCK to SYNCO		0.9	1.3	1.9	ns
$T_{setup,in}$	Ix set-up time before CKO			1.3		ns
$T_{hold,in}$	Ix hold time after CKO			-0.3		ns
$T_{setup,sync}$	Sync set-up time before CLK			0.1		ns
$T_{hold,sync}$	Sync hold time after CLK			0.3		ns
$T_{pd,cko}$	Delay from CLK to CKO		0.9	1.3	1.9	ns
$T_{pd,out}$	Delay from CLK to Ox		0.7	1.3	1.9	ns

Note: All timing data are estimates, based on post-layout simulations.

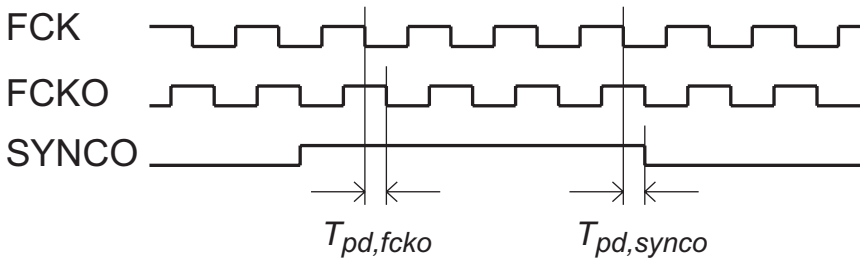


Figure 4. *Fast Clock Divider.*

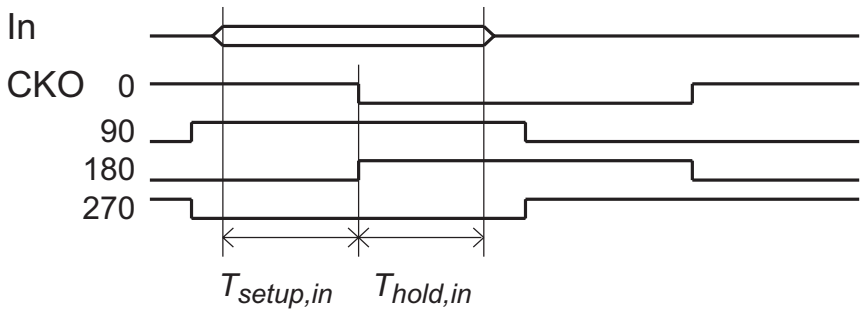


Figure 5. *Low Frequency.*

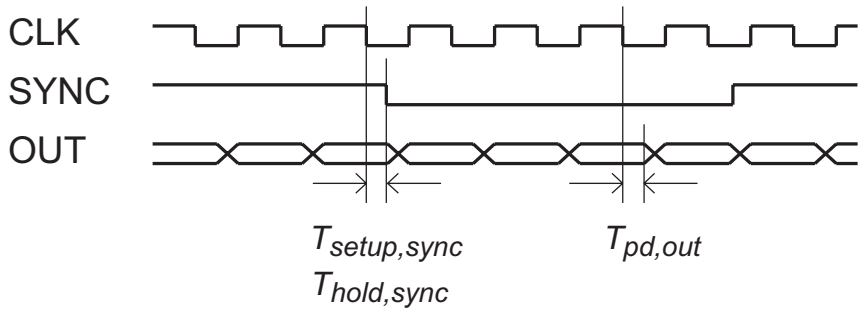


Figure 6. *High Frequency.*

Note: When SYNC is sampled high, after a low sample, the internal clock divider is reset, giving a low CKO and data output two CLK samples after SYNC is sampled low.

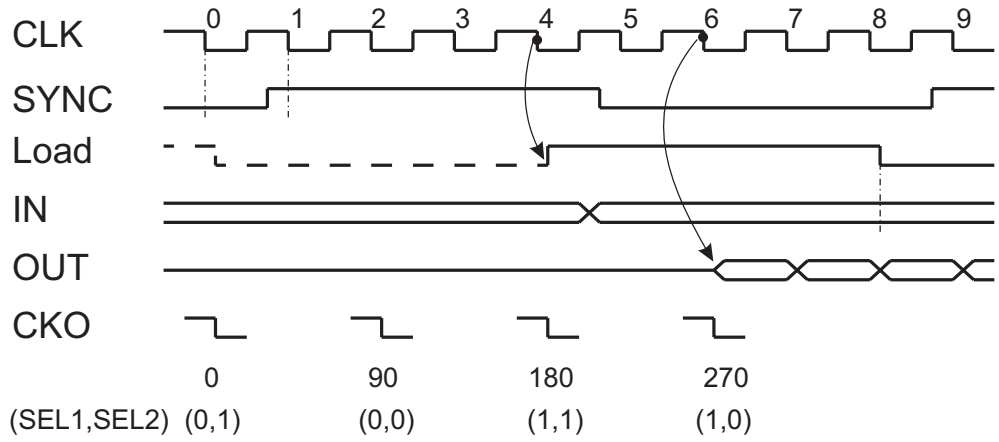


Figure 7. *Relation Between Data and Clock.*

The internal load signal is generated relative to the rising edge of SYNC. The synchronisation sequence is initiated by the sampling of SYNC low followed by high. A rising edge on the internal load signal (load) is generated four CLK cycles after SYNC is sampled high.

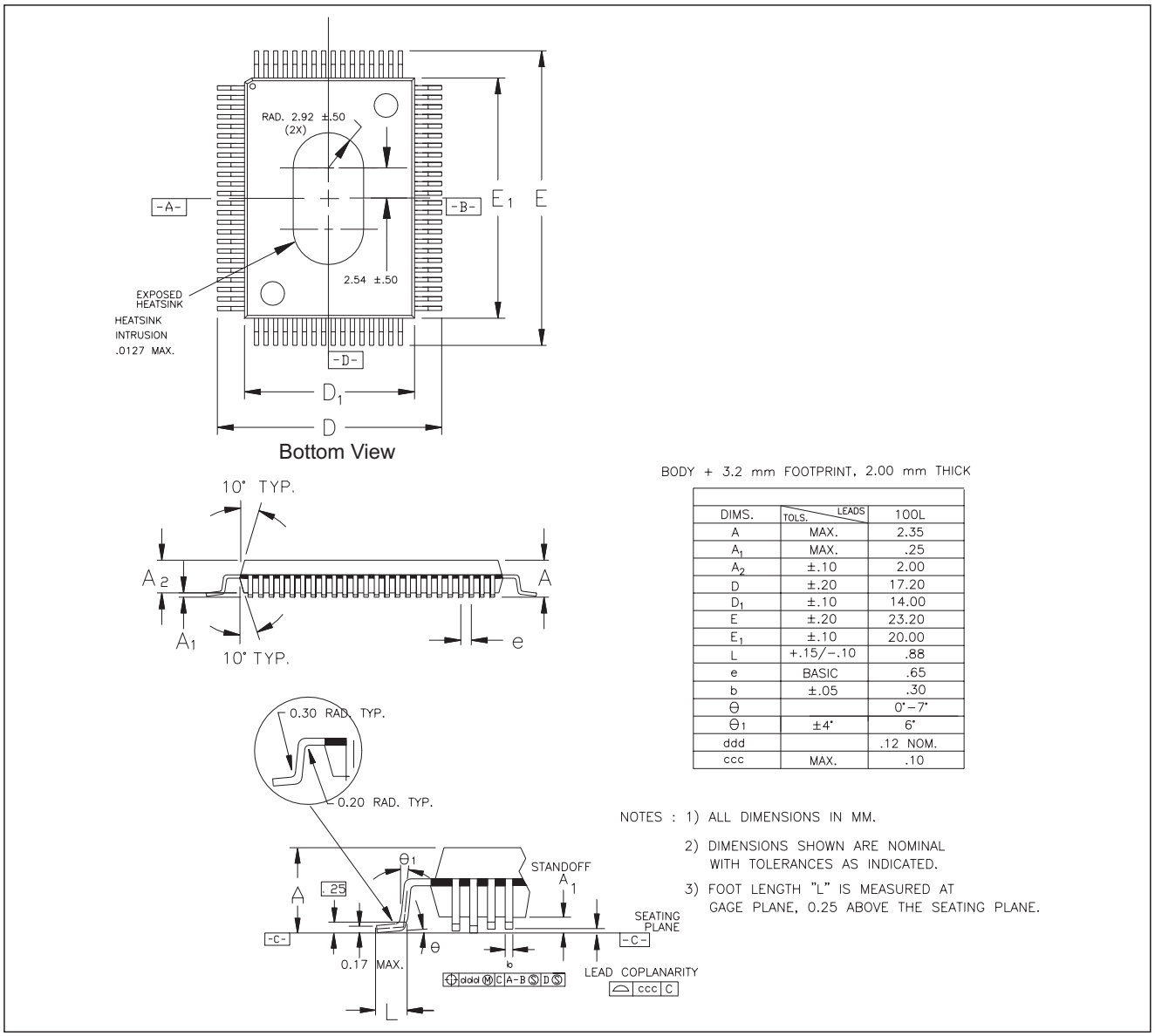
The external load clock CKO can be adjusted in four phases relative to the internal load signal, selected by SEL1 and SEL2, as shown in the figure.

The figure also shows the number of bits stored in the device. The GD16334 starts transmitting data on the 6th CLK cycle after SYNC is sampled high. The low frequency input data is sampled on the 8th CLK cycle. This will give a total of 15 bits just before sampling data, and a total of 22 bits just after sampling – for each of the four MUX'es in the GD16334.

Sequencing of Output Data

The GD16334 MUX contains four identical 8:1 MUX'es. The data bits of the first MUX are shifted out with the data of input I0 (pin 7) coming out first, then I4, I8…I28. The second MUX shifts out I1 (pin 74) first, followed by I5, I9….I29. The last two MUX blocks work in the same manner.

Package Outline



BODY + 3.2 mm FOOTPRINT, 2.00 mm THICK

DIMS.	TOLS. \ LEADS	100L
A	MAX.	2.35
A_1	MAX.	.25
A_2	±.10	2.00
D	±.20	17.20
D_1	±.10	14.00
E	±.20	23.20
E_1	±.10	20.00
L	+.15/−.10	.88
e	BASIC	.65
b	±.05	.30
θ		0°−7°
θ_1	±4°	6°
ddd		.12 NOM.
ccc	MAX.	.10

NOTES : 1) ALL DIMENSIONS IN MM.

2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.

3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE THE SEATING PLANE.

Figure 8. *Package 100 pin QFP*

Device Marking

Figure 9. *Device Marking - Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	**Package Type:**	**Case Temperature Range:**	**Option:**
GD16334 - 100BA	100 pin QFP	-5 °C +85 °C	

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