■Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Load supply voltage	V_{BB}	50	V
Logic supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	–0.3 to V_{CC}	V
Reference input voltage	V_{REF}	–0.3 to V_{CC}	V
Sense voltage	V_{sense}	1.5	V
Package power dissipation	P_D	1	W
Junction temperature	T_j	–20 to +85	°C
Operating temperature	T_{op}	+125	°C
Storage temperature	T_{stg}	–55 to +125	°C

■Recommended Operating Voltage Ranges

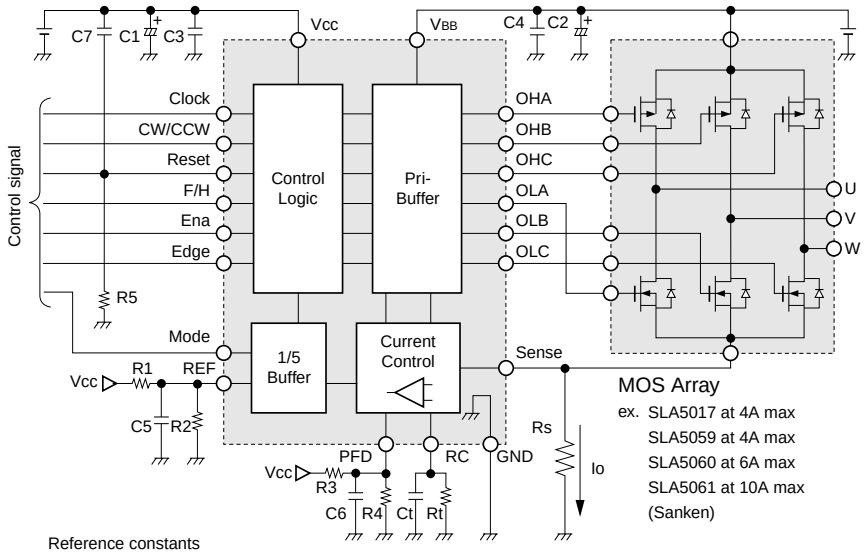
(Ta=25°C)

Parameter	Symbol	Ratings	Units
Load supply voltage	V_{BB}	15 to 45	V
Logic supply voltage	V_{CC}	3 to 5.5	V
Reference input voltage	V_{REF}	0.2 to Vcc–2	V

■Electrical Characteristics

Parameter	Symbol	Ratings			Units	Conditions
		min	typ	max		
Load supply voltage	V_{BB}	15		45	V	
Logic supply voltage	V_{CC}	3.0		5.5	V	
Output voltage	V_{OL1}	8		15	V	
	V_{OL2}	0		1	V	
	V_{OH1}	V_{BB}–15		V_{BB}–8	V	
	V_{OH2}	V_{BB}–1		V_{BB}	V	
Load supply current	I_{BB}			25	mA	V_{CC}=5.5V
Logic supply current	I_{CC}			10	mA	V_{CC}=5.5V
Logic input voltage	V_{IH}	3.75			V	
	V_{IL}			1.25	V	
Logic input current	I_{IH}			20	μA	V_{IN}=V_{CC}×0.75
	I_{IL}	–20			μA	V_{IN}=V_{CC}×0.25
Maximum clock frequency	F	200			kHz	Edge=0V
		100				Edge=V_{CC}
PFD input voltage	V_{Slow}	1.7		V_{CC}	V	
	V_{Mix}	0.7		1.3	V	
	V_{Fast}			0.3	V	
PFD input current	I_{PFD}		±50		μA	
Reference input voltage	V_{REF}	0		V_{CC}–2	V	
Reference input current	I_{REF}		±10		μA	V_{REF}=0~Vcc–2V
Sense voltage	V_{S1}		V_{REF}×0.2		V	Mode=V_{CC}, V_{REF}=0~V_{CC}–2V
	V_{S2}		V_{REF}×0.17		V	Mode=0V, AV$_{REF}$=0~V_{CC}–2V
RC source current	I_{RC}		220		μA	
Off time	T_{off}		1.1×R_t×C_t		Sec.	

■Internal Block Diagram/Diagram of Standard External Circuit



Reference constants

Rs:0.1 to 1Ω (1 to 5W)
Rt:15k to 75kΩ
Ct:420p to 1100pF

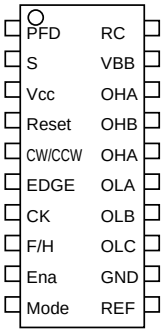
C1:10 μF/10V
C2:100 μF/63V
C3 to C6:0.01 to 1 μF
C7:1000pF

R1+R2≤10kΩ
(V_{REF}:0.2 to V_{CC}2-2V)
R3+R4≤10kΩ
(V_{PFD}:0 to V_{CC}2)

R5:10kΩ

■Terminal Connection

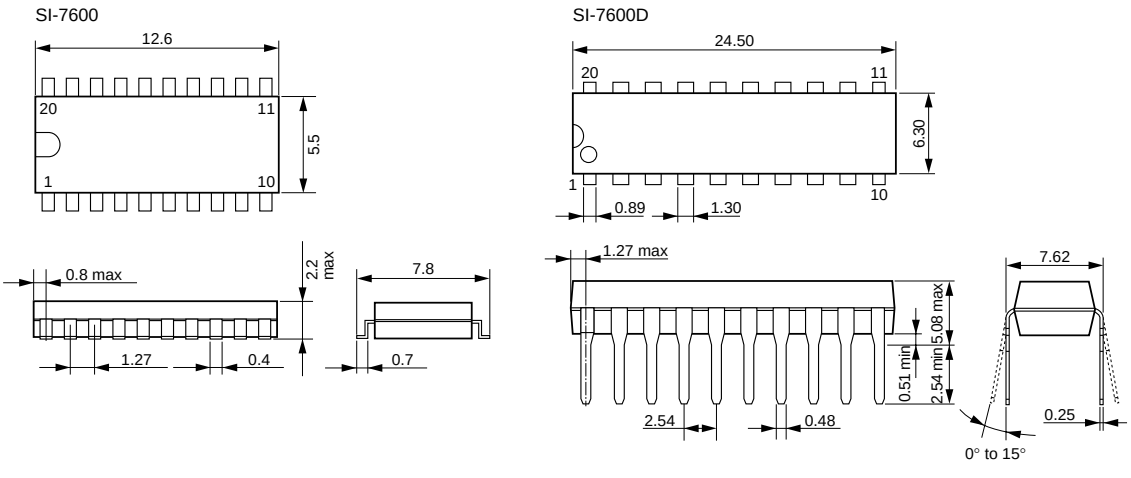
The package shapes of SI-7600 and SI-7600D are different, however the terminal connection is the same.



Pin No.	Name	Pin No.	Name	Pin No.	Name
Pin1	PFD	Pin8	Full/Half	Pin15	OLA
Pin2	Sense	Pin9	Enable	Pin16	OHC
Pin3	Vcc	Pin10	Mode	Pin17	OHB
Pin4	Reset	Pin11	REF	Pin18	OHA
Pin5	CW/CCW	Pin12	GND	Pin19	V_{BB}
Pin6	Edge	Pin13	OLC	Pin20	RC
Pin7	Clock	Pin14	OLB		

■External Dimensions (Unless specified otherwise, all values are typical)

(Units: mm)



Application Notes

1. Outline

The SI-7600/SI-7600D is a control IC used with a power MOS FET array to drive a 3-phase stepper motor. Select the output-stage MOS FET according to the rated current of the motor. The full step is 2-phase excitation when this IC is in a star connection but 3-phase excitation when it is in a delta connection.

2. Features

- Suitable for both star connection drive and delta connection drive
- Maximum load supply voltage V_{BB}=45V
- Control logic supply voltage Vcc=3 to 5.5V
- Supports star connection (2/2-3phase excitation) and delta connection (3/2-3phase excitation)
- Step switching timing by clock signal input
- Forward/reverse, hold, and motor-free control
- Step switching at the positive edge or positive/negative edge of the clock signal
- Control current automatic switching function for 2-3phase excitation (effective for star connection)
  (Current control: 86% for 2-phase excitation, 100% for 3-phase excitation)
- Self-excitation constant-current chopping by external C/R
- Slow Decay, Mixed Decay, or Fast Decay selectable
- Two package lineup: SOP (surface mounting) and DIP (lead insertion)
  SOP…SI-7600, DIP…SI-7600D
- Maximum output current depends on the ratings of the MOS FET array used

3. Input Logic Truth Table

Input terminal	Low level	High level
CW/CCW	CW	CCW
Full/Half	2-3phase excitation	2-phase excitation
Enable	Disable	Enable
Mode (Note 1)	Always 100%	2-phase excitation: 85% 3-phase excitation: 100%
Edge (Note 2)	Positive	Positive/negative
Reset (Note 3)	Enable	Internal logic reset output disable

Select CW/CCW, Full/Half, or Edge when the clock level is low.

Note 1: The control current is always 85% for the full step (2-phase excitation) when the Mode terminal level is high. The value of 100% control current is calculated at the V_{REF}/(5×Rs) terminal because a 1/5 buffer is built into the reference section.

Note 2: When the Edge terminal level is set high, the internal counter increments both at the rising and falling edges. Therefore, the duty ratio of the input clock should be set at 50%.

Note 3: When the Reset terminal level is set high, the internal counter is reset. Output remains disabled as long as the Reset terminal level is high.

4. Determining the control current

The control current Io can be calculated as follows:

When the Mode terminal level is low

$I_O \cong V_{REF}/(5 \times R_S)$

When the Mode terminal level is high

$I_O \cong V_{REF}/(5 \times R_S) \rightarrow$ 3-phase excitation

$I_O \cong V_{REF}/(5.88 \times R_S) \rightarrow$ 2-phase excitation

The reference voltage can be set within the range of 0.2V to Vcc –2V. (When the voltage is less than 0.2V, the accuracy of the reference voltage divider ratio deteriorates.)

5. About the Current Control System (Setting the Constant Ct/Rt)

The SI-7600 uses a current control system of the self-excitation type with a fixed chopping OFF time.

The chopping OFF time is determined by the constant Ct/Rt.

The constant Ct/Rt is calculated by the formula

$T_{OFF} \cong 1.1 \times Ct \times Rt$ …… (1)

The recommended range of constant Ct/Rt is as follows:

Ct: 420 to 1100pF

Rt: 15 to 75kΩ

(Slow Decay or Mixed Decay →560pF/47kΩ, Fast Decay → 470pF/20kΩ)

Usually, set T_{OFF} to a value where the chopping frequency becomes about 30 to 40kHz.

The mode can be set to Slow Decay, Fast Decay, or Mixed Decay depending on the PFD terminal input potential.

PFD applied voltage and decay mode

PFD applied voltage	Decay mode
0 to 0.3V	Fast Decay
0.7V to 1.3V	Mixed Decay
1.7V to Vcc	Slow Decay

In Mixed Decay mode, the Fast/Slow time ratio can be set using the voltage applied to the PFD terminal. The calculated values are summarized below.

In this mode, the point of switching from Fast Decay to Slow Decay is determined by the RC terminal voltage that determines the chopping OFF time and by the PFD input voltage V_{PFD}.

Formula (1) is used to determine the chopping OFF time.

The Fast Decay time is then determined by the RC discharge time from the RC voltage (about 1.5V) to the PFD input voltage (V_{PFD}) when chopping is turned from ON to OFF.

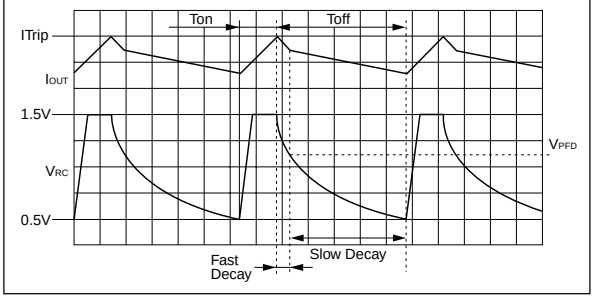
The Fast Decay time is

$$t_{OFFf} \cong -R_T \times C_T \times \ln\left(\frac{V_{PFD}}{1.5}\right) \quad \cdots\cdots(2)$$

The Slow Decay time (t_{OFFs}) is calculated by subtracting the value of (2) from that of (1).

$t_{OFFS} \cong T_{OFF} - t_{OFFf}$ ……(3)

Relationship between RC terminal voltage and output current



6. Method of Calculating Power Loss of Output MOS FET

The SI-7600 uses a MOS-FET array for output. The power loss of this MOS FET array can be calculated as summarized below. This is an approximate value that does not reflect parameter variations or other factors during use in the actual application. Therefore, heat from the MOS FET array should actually be measured.

● Parameters for calculating power loss

To calculate the power loss of the MOS FET array, the following parameters are needed:

(1) Control current Io (max)

(2) Excitation method

(3) Chopping ON-OFF time at current control: T_{ON}, T_{OFF}, t_{OFFf}

(T_{ON}: ON time, T_{OFF}: OFF time, t_{OFFf}: Fast Decay time at OFF)

(4) ON resistance of MOS FET: $R_{DS\ (ON)}$

(5) Forward voltage of MOS FET body diode: V_{SD}

For (4) and (5), use the maximum values of the MOS FET specifications.

(3) should be confirmed on the actual application.

● Power loss of Pch MOS FETs

The power loss of Pch MOS FETs is caused by the ON resistance and by the chopping-OFF regenerative current flowing through the body diodes in Fast Decay mode.

(In Slow Decay mode, the chopping-OFF regenerative current does not flow the body diodes.)

The losses are

ON resistance loss P1: $P1=I_M^2 \times R_{DS\ (ON)}$

Body diode loss P2: $P2=I_M \times V_{SD}$

With these parameters, the loss Pp per MOS FET is calculated depending on the actual excitation method as follows:

a) 2-phase excitation ($T=T_{ON}+T_{OFF}$)

$P_P=(P1 \times T_{ON}/T+P2 \times t_{OFFf}/T) \times (1/3)$

b) 2-3 phase excitation ($T=T_{ON}+T_{OFF}$)

$P_P=(P1 \times T_{ON}/T+P2 \times t_{OFFf}/T) \times (1/4)+(0.5 \times P1 \times T_{ON}/T+P2 \times t_{OFFf}/T) \times (1/12)$

● Power loss of Nch MOS FETs

The power loss of Nch MOS FETs is caused by the ON resistance or by the chopping-OFF regenerative current flowing through the body diodes.

(This loss is not related to the current control method, Slow, Mixed, or Fast Decay.)

The losses are

ON resistance loss N1: $N1=I_M^2 \times R_{DS(ON)}$

Body diode loss N2: $N2=I_M \times V_{SD}$

With these parameters, the loss P_N per MOS FET is calculated depending on the actual excitation method as follows:

a) 2-phase excitation ($T=T_{ON}+T_{OFF}$)

$P_N=(N1+N2 \times T_{OFF}/T) \times (1/3)$

b) 2-3 phase excitation ($T=T_{ON}+T_{OFF}$)

$P_N=(N1+N2 \times T_{OFF}/T) \times (1/4)+(0.5N1+N2 \times T_{OFF}/T) \times (1/12)$

● Determining power loss and heatsink when SLA5017 is used

If the SLA5017 is used in an output section, the power losses of a Pch MOS FET and an Nch MOS FET should be multiplied by three and added to determine the total loss P of SLA5017.

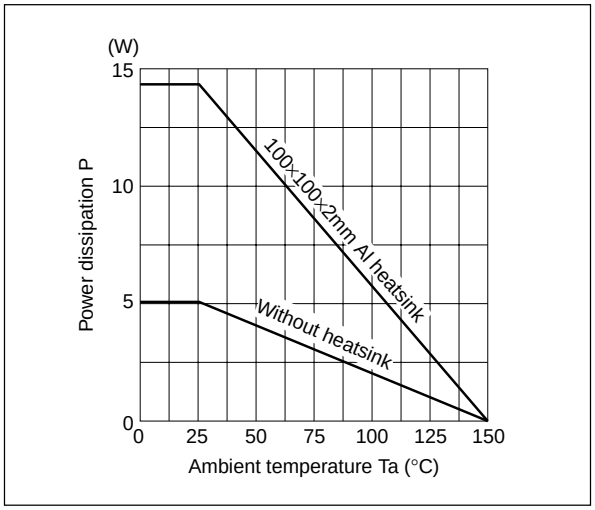
In other words, $P=3 \times P_P+3 \times P_N$

The allowable losses of SLA5017 are

Without heatsink: 5W θj-a=25°C/W

Infinite heatsink: 35W θj-c=3.57°C/W

Select a heatsink by considering the calculated losses, allowable losses, and following ratings:



When selecting a heatsink for SLA5017, be sure to check the product temperature when in use in an actual applicaiton.

The calculated loss is an approximate value and therefore contains a degree of error.

Select a heatsink so that the surface Al fin temperature of SLA5017 will not exceed 100°C under the worst conditions.

7. I/O Timing Chart