Extended Data Out (EDO) DRAM SMALL OUTLINE DIMM

3280AsEDM4G04TC 72 Pin 8Mx32 EDO SODIMM
Unbuffered, 4k Refresh, 3.3V

General Description

The 3280AsEDM4G04TC is a 8Mx32 bit, 4 chip, 3.3V, 72 Pin SODIMM module consisting of (4) 8Mx8 (TSOP2) DRAMs. The module is unbuffered and supports Extended Data Out (EDO) page mode access.

Features

- JEDEC-Standard 72-pin Small Outline Dual Inline Memory Module (SODIMM)
- Unbuffered
- Supports Extended Data Out (EDO) access cycles
- Based on 8Mx8 DRAM
- Power Supply: 3.3V ± 0.3V
- 64ms, 4096-cycle refresh
- Supports RAS-Only-Refresh (ROR), CAS-before-RAS (CBR) refresh and Hidden refresh cycles
- Seven Presence Detect (PD) lines
- LVTTL Compatible Inputs and Outputs
- One External Bank
- Gold PCB connector

Pin Assignment

Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
1	Vss	19	A10	37	DQ16	55	NC
2	DQ0	20	NC	38	DQ17	56	DQ24
3	DQ1	21	DQ8	39	Vss	57	DQ25
4	DQ2	22	DQ9	40	CAS0*	58	DQ26
5	DQ3	23	DQ10	41	CAS2*	59	DQ27
6	DQ4	24	DQ11	42	CAS3*	60	DQ28
7	DQ5	25	DQ12	43	CAS1*	61	Vcc
8	DQ6	26	DQ13	44	RAS0*	62	DQ29
9	DQ7	27	DQ14	45	NC	63	DQ30
10	Vcc	28	A7	46	NC	64	DQ31
11	PD1	29	A11	47	WE*	65	NC
12	A0	30	Vcc	48	NC	66	PD2
13	A1	31	A8	49	DQ18	67	PD3
14	A2	32	A9	50	DQ19	68	PD4
15	A3	33	NC	51	DQ20	69	PD5
16	A4	34	RAS2*	52	DQ21	70	PD6
17	A5	35	DQ15	53	DQ22	71	PD7
18	A6	36	NC	54	DQ23	72	Vss

* Active Low

Valid Part Numbers

Part Number	Access Time	Supply Voltage
3280A5EDM4G04TC	50ns	3.3V
3280A6EDM4G04TC	60ns	3.3V

Pin Descriptions

Pin	Name	Function
RAS#	Row Address Strobe	RAS# is used to strobe row addresses.
CAS#	Column Address Strobe	CAS# is used to strobe column addresses
WE#	Write Enable	WE# is used to control read/write cycles.
A#	Address Lines	Address lines are multiplexed to specify the row and column address.
DQ0-DQ31	Data Lines	Data input/output lines.
Vcc	Power Supply	Power Supply 3.3V±0.3V
Vss	Ground	Ground
PD#	Presence Detect Lines	Presence detect lines are used to specify module type. Lines are either grounded or NC in module (see Presence Detect Matrix).
NC	No Connection	Line is not connected in module.

Presence Detect Matrix

DIMM Type	PD1	PD2	PD3	PD4	PD5	PD6	PD7
3280A5EDM4G04TC	Vss	Vss	NC	NC	Vss	Vss	NC
3280A6EDM4G04TC	Vss	Vss	NC	NC	NC	NC	NC

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V_{in}	-0.5 to +4.6	V
Short circuit output current	I_{out}	80	mA
Power dissipation	Pt	4	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{st}	-55 to +125	°C

NOTE: Permanent damage may occur if absolute maximum ratings are exceeded.
Device should be operated within recommended operating conditions only.

DC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units	Note
Supply voltage	Vss	0	0	0	V	
Supply voltage	Vcc	3.0	3.3	3.6	V	16
Input high voltage	Vih	2.0	-	5.5	V	16
Input low voltage	Vil	-0.5	-	0.8	V	16
Output high voltage	Voh	2.4	-	Vcc	V	
Output low voltage	Vol	-	-	0.4	V	

DC Current Consumption (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	-50	-60	Unit	Note
Standby Current (TTL)	I_{CC1}	(RAS# = CAS# = V_{IH})	8	8	mA	17
Standby Current (CMOS)	I_{CC2}	All inputs = Vcc - 0.2V	4	4	mA	17
Operating Current Random Read/Write	I_{CC3}	RAS#, CAS#, address cycling. $t_{RC} = t_{RC[MIN]}$	672	552	mA	17, 18
Operating Current Fast Page Mode	I_{CC4}	RAS# = V_{IL}, CAS#, Address cycling. $t_{PC} = t_{PC[MIN]}$	N/A	N/A	mA	17, 18
Operating Current EDO Page Mode	I_{CC5}	RAS# = V_{IL}, CAS#, Address cycling. $t_{PC} = t_{PC[MIN]}$	480	384	mA	17, 18
Refresh Current: RAS#-Only	I_{CC6}	RAS# cycling, CAS#=V_{IH}; $t_{RC} = t_{RC[MIN]}$	624	528	mA	17
Refresh Current: CAS# before RAS#	I_{CC7}	RAS#, CAS#, address cycling $t_{RC} = t_{RC[MIN]}$	672	552	mA	17

Capacitance (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	Typ	Max	Units	Note
Input capacitance (Address)	C_{I1}	-	20	pF	
Input capacitance (WE#, OE#)	C_{I2}	-	28	pF	
Input/Output capacitance (Data)	$C_{I/O}$	-	7	pF	
Input capacitance (CAS#)	C_{I3}	-	7	pF	
Input capacitance (RAS#)	C_{I4}	-	14	pF	

AC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
Access time from column address	t_{AA}		25		30	ns	3, 5, 14
Column address setup to CAS# precharge	t_{ACH}	12		15		ns	
Column address hold time (from RAS#)	t_{AR}	40		50		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Access time from CAS#	t_{CAC}		15		17	ns	3, 4, 14
Column address hold time	t_{CAH}	8		10		ns	
CAS# pulse width	t_{CAS}	8	10 000	10	10 000	ns	
CAS# to output in Low-Z	t_{CLZ}	3		3		ns	
Data output hold after CAS# LOW	t_{COH}	3		3		ns	
CAS# precharge time	t_{CP}	8		10		ns	
Access time from CAS# precharge	t_{CPA}		28		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	40		50		ns	
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	
Data-in hold time	t_{DH}	8		10		ns	11
Data-in setup time	t_{DS}	0		0		ns	11
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	
EDO Page-mode read or write cycle time	t_{PC}	20		25		ns	
Access time from RAS#	t_{RAC}		50		60	ns	2, 3
RAS# to column address delay time	t_{RAD}	15	25	15	30	ns	9
Row-address hold time	t_{RAH}	10		10		ns	
RAS# pulse width	t_{RAS}, t_{RASP}	50	10 000	60	10 000	ns	
Random read/write cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	20	35	20	43	ns	8
Read command hold time	t_{RCH}	0		0		ns	
Read command setup time	t_{RCS}	0		0		ns	
Refresh Period 4,096 cycles)	t_{REF}		64		64	ms	15
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
READ command hold time	t_{RRH}	0		0		ns	
RAS# hold time	t_{RSH}	13		17		ns	
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition Time	t_{τ}	2	50	2	50	ns	7

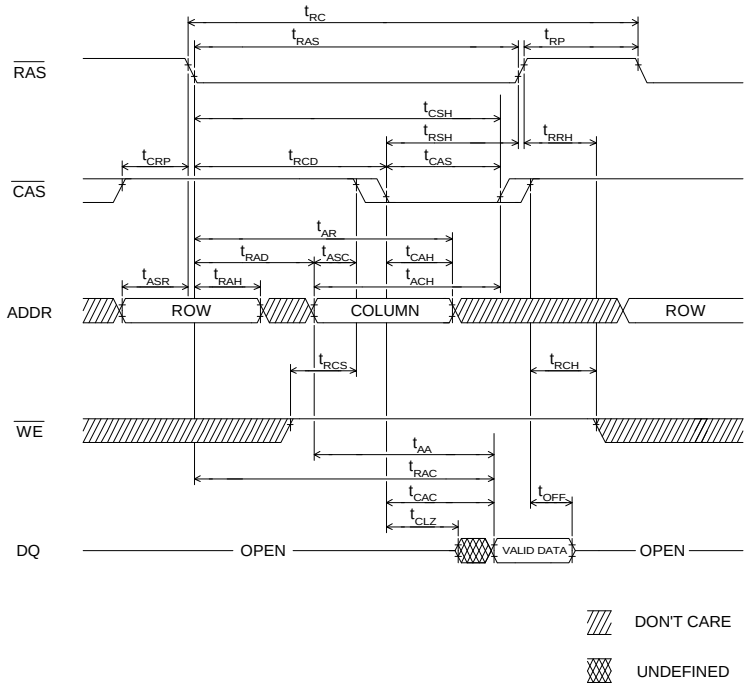
AC Characteristics (T_A = 0 to 70C, Vcc = 3.3V ± 0.3V, Vss = 0V)

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
WRITE command hold time	t_{WCH}	8	-	10	-	ns	
WRITE command hold time (RAS# referenced)	t_{WCR}	-	-	-	-	ns	
WE# command setup time	t_{WCS}	0	-	0	-	ns	10
Output disable delay from WE#	t_{WHZ}	0	12	0	15	ns	
Write command pulse width	t_{WP}	10	-	10	-	ns	

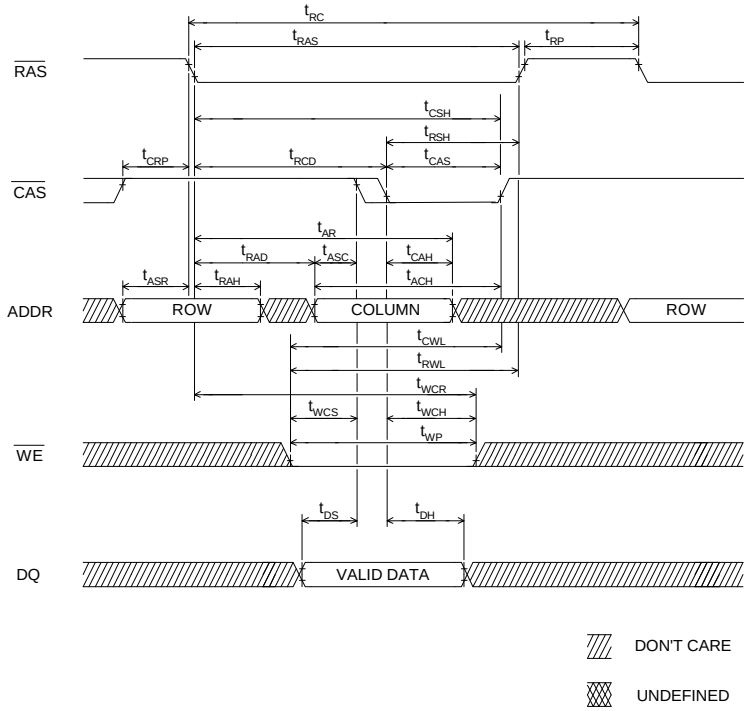
Notes

1. AC measurements assume t_T = 5ns
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater that the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivilaent to 1 TTL load and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Vih (min.) and Vil (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between Vih and Vil.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater that the specified t_{RCD} (max.) limit, then the access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater that the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min.))
11. These parameters are referenced to CAS* leading edge in an early write cycle.
12. An initial pause of 100us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS* clock such as RAS* only refresh)
13. t_{RASC} defines RAS* pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}
15. t_{REF} defined is 4,096 refresh cycle.
16. All voltages referenced to Vss
17. Typical maximum current consumption levels
18. Column address changed once per cycle

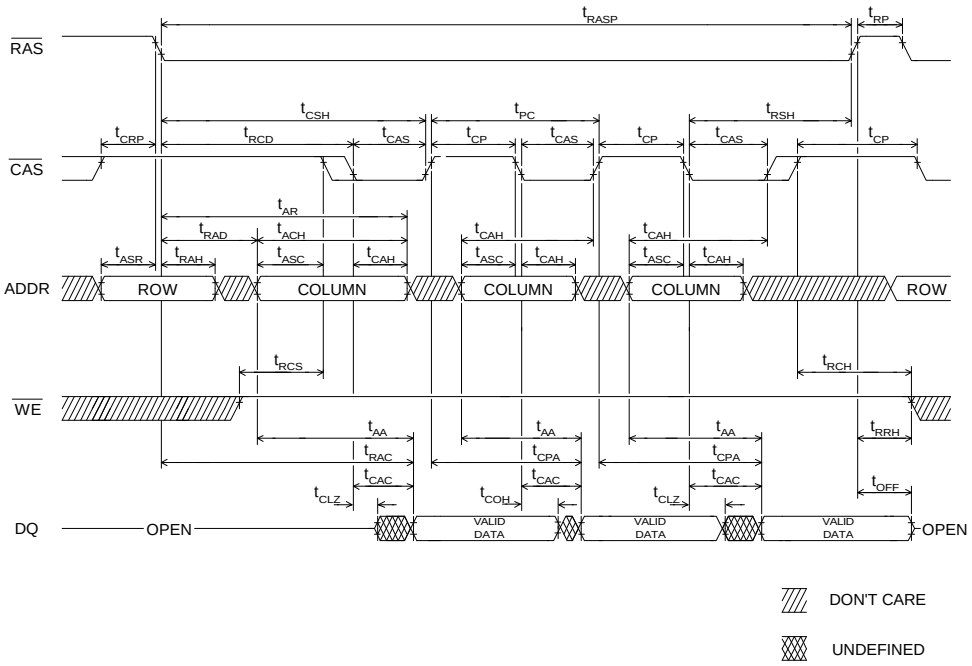
READ CYCLE



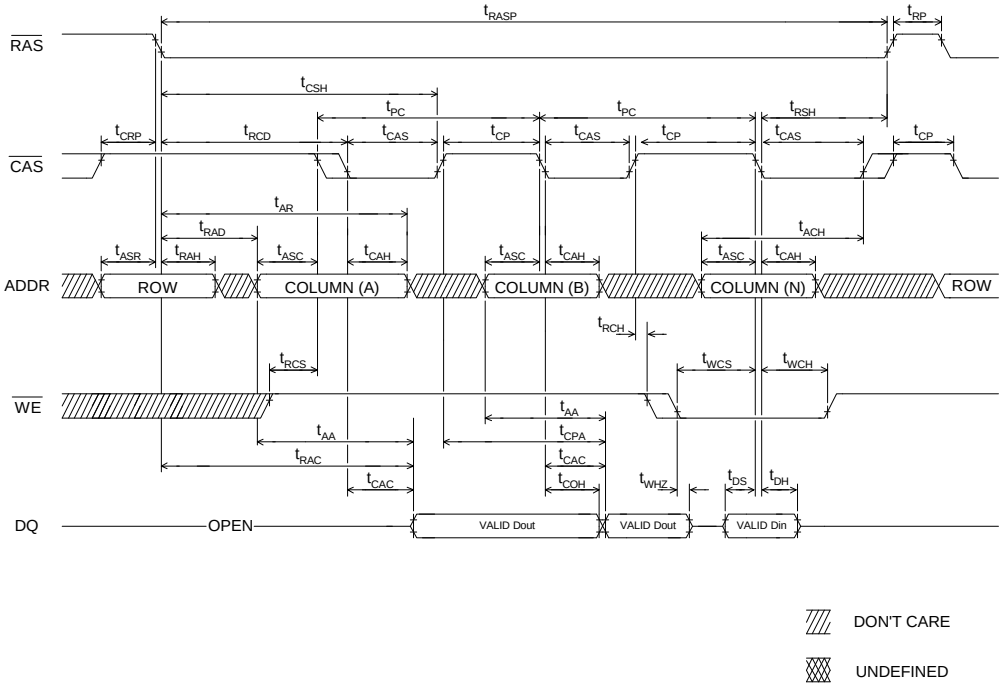
EARLY WRITE CYCLE



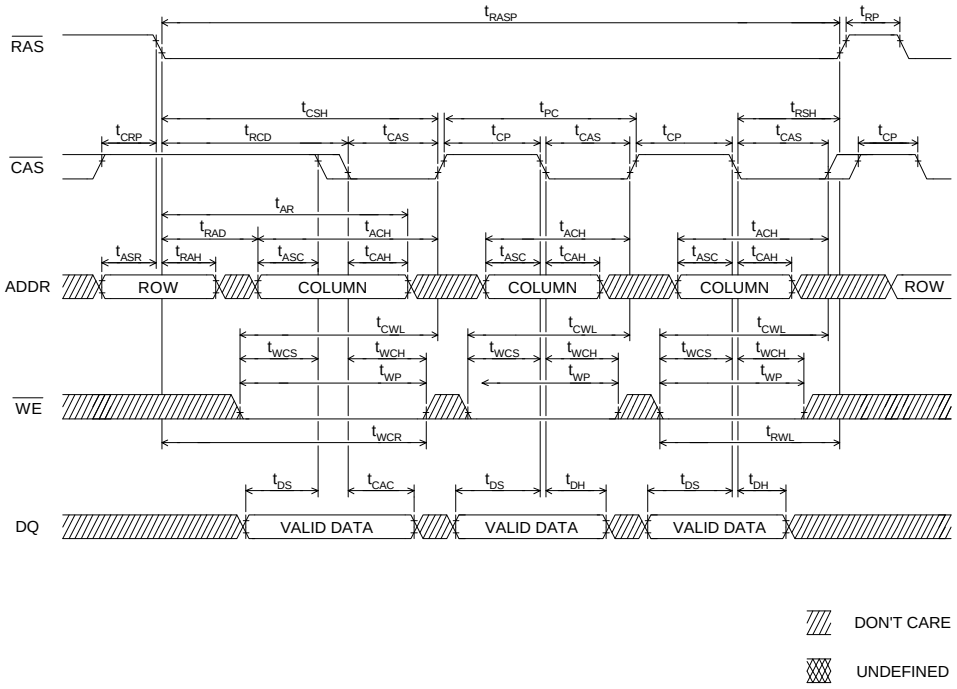
EDO-PAGE-MODE READ CYCLE



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE

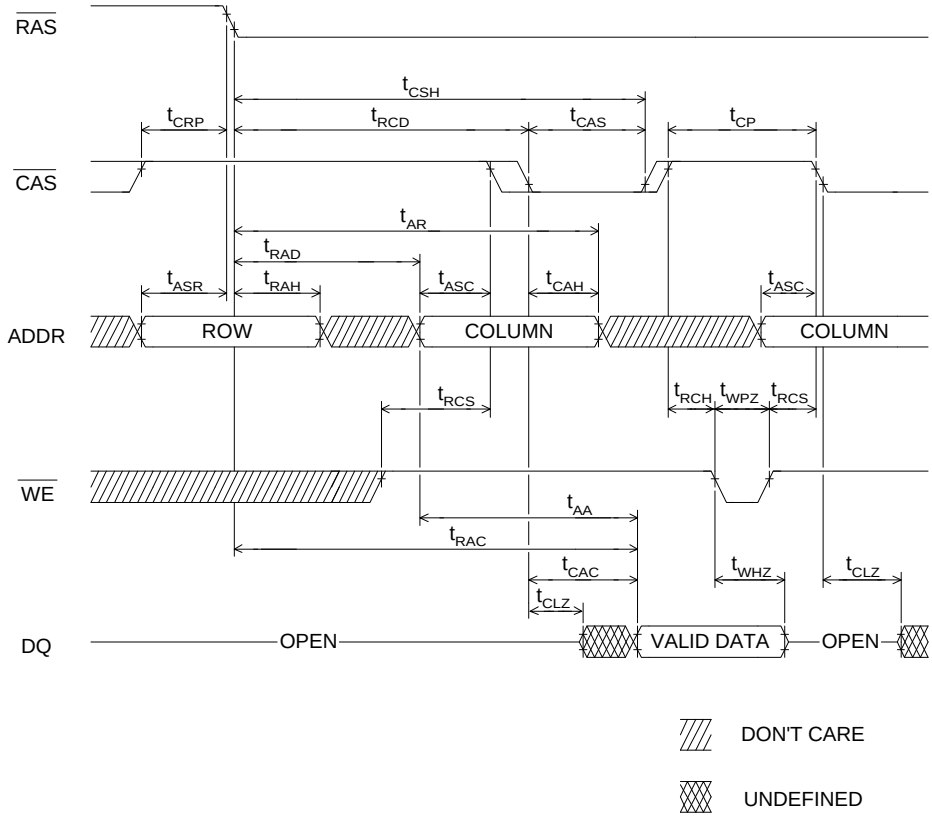


FAST/EDO-PAGE-MODE EARLY-WRITE CYCLE

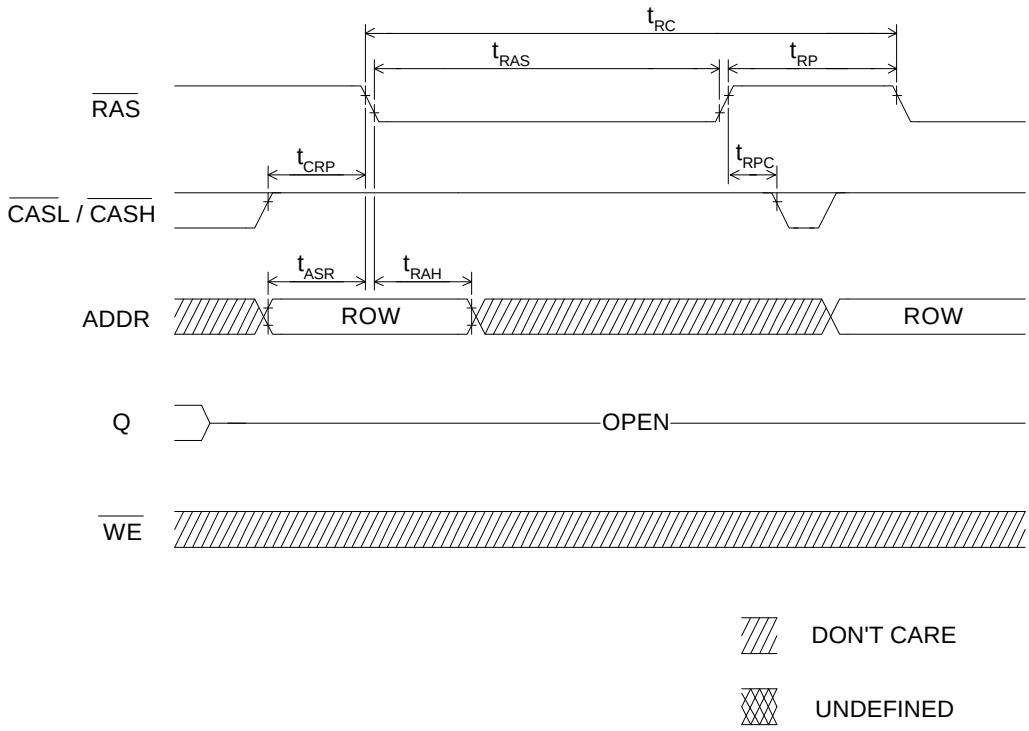


EDO READ CYCLE

(with /WE-controlled disable)

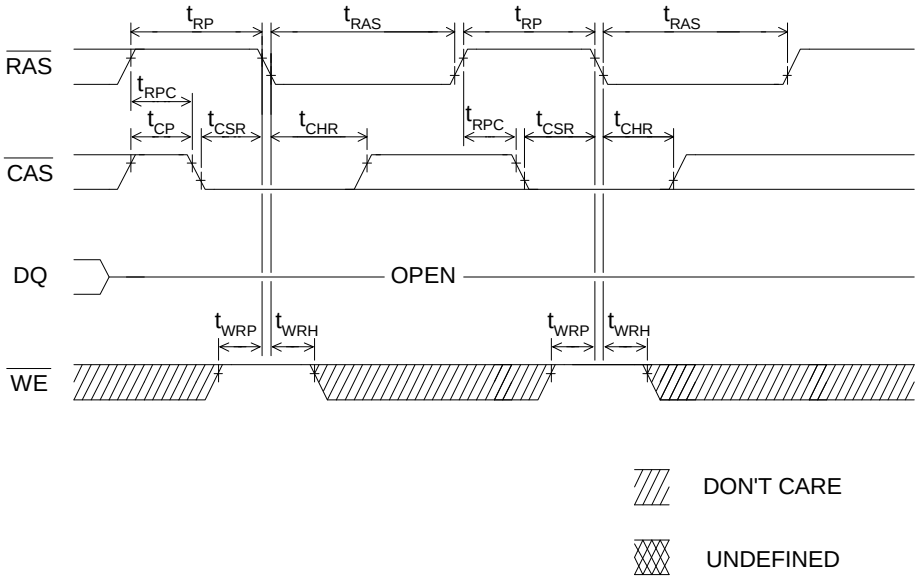


/RAS-ONLY REFRESH CYCLE

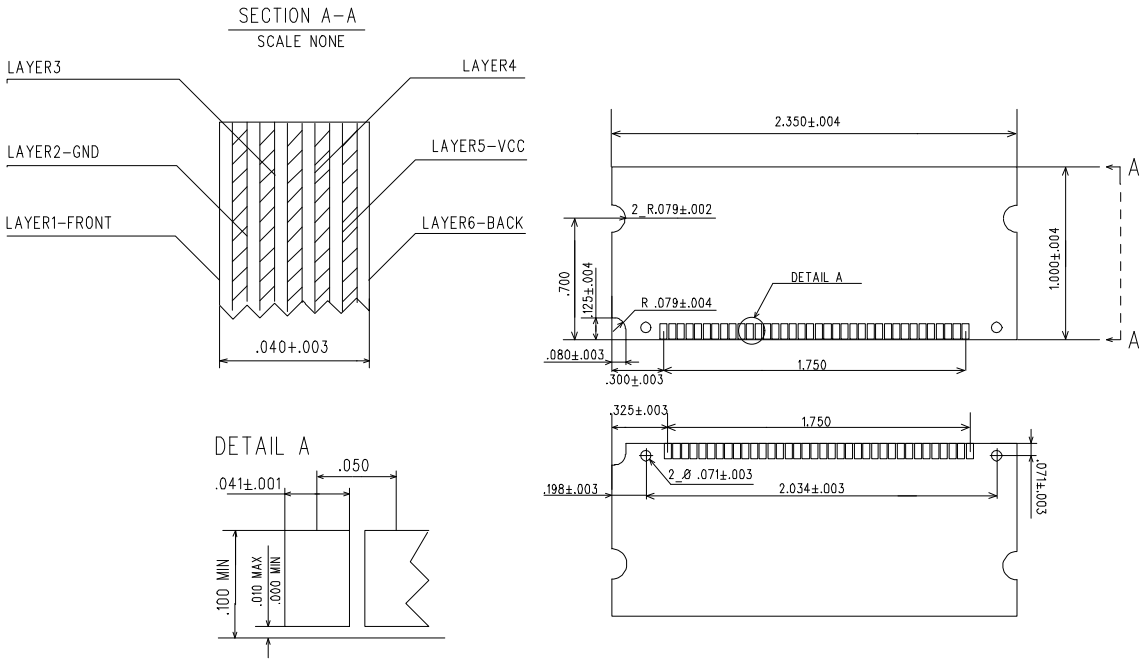


CBR REFRESH CYCLE

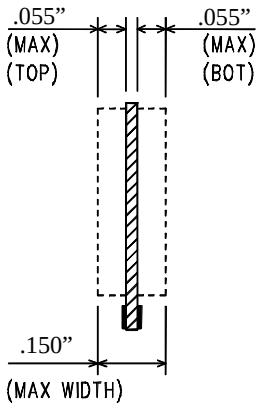
(Addresses = DON'T CARE)



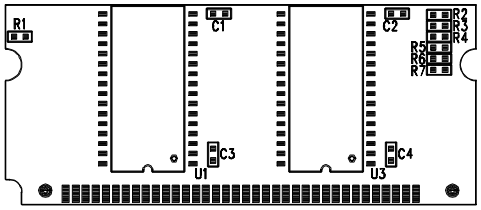
OUTLINE DRAWING



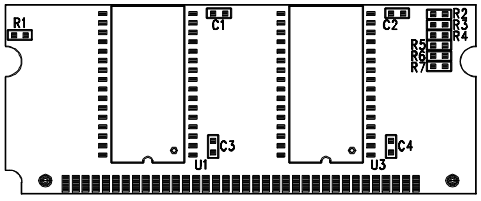
SIDEVIEW



FRONT SIDE



BACK SIDE



Note: Drawing is for component location only, assembly may not have all components installed.