DDR2 SDRAM Registered MiniDIMM

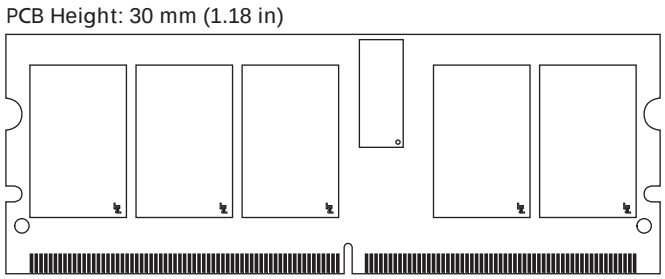
MT9HTF6472(P)K – 512MB
MT9HTF12872(P)K – 1GB

For component specifications, refer to Micron's Web site: www.micron.com/products/dram/ddr2

Features

- 244-pin, mini dual in-line memory module (MiniDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- 512MB (64 Meg x 72), 1GB (128 Meg x 72)
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18 compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 1: 244-Pin DIMM (MO-244 R/C "A")



Options	Marking
• Parity	P
• Package	
244-pin DIMM (lead-free)	Y
• Frequency/CAS latency[1]	
2.5ns @ CL = 5 (DDR2-800)	-80E
2.5ns @ CL = 6 (DDR2-800)	-800
3ns @ CL = 5 (DDR2-667)	-667
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)[2]	-40E
• PCB height	
30mm (1.18in)	

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
2. Not recommended for future designs.

Table 1: Address Table

	512MB	1GB
Refresh count	8K	8K
Row addressing	16K A[13:0]	16K A[13:0]
Device bank addressing	4 BA[1:0]	8 BA[2:0]
Device configuration	512Mb (64 Meg x 8)	1Gb (128Meg x 8)
Column addressing	1K A[9:0]	1K A[9:0]
Module rank addressing	1 (S0#)	1 (S0#)

Table 2: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 3: Part Numbers and Timing Parameters – 512MB

Base device: MT47H64M8[1], 512Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT9HTF6472(P)KY-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472(P)KY-800__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472(P)KY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472(P)KY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF6472(P)KY-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 1GB

Base device: MT47H128M8[1], 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT9HTF12872(P)KY-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872(P)KY-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872(P)KY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872(P)KY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF12872(P)KY-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. The data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF12872KY-667A2.

Pin Assignments and Descriptions

Table 5: Pin Assignments

244-Pin MiniDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	32	VSS	63	VDDQ	94	DQS5#
2	VSS	33	DQ24	64	A2	95	DQS5
3	DQ0	34	DQ25	65	VDD	96	VSS
4	DQ1	35	VSS	66	VSS	97	DQ42
5	VSS	36	DQS3#	67	VSS	98	DQ43
6	DQS0#	37	DQS3	68	PAR_IN	99	VSS
7	DQS0	38	VSS	69	VDD	100	DQ48
8	VSS	39	DQ26	70	A10/AP	101	DQ49
9	DQ2	40	DQ27	71	BA0	102	VSS
10	DQ3	41	VSS	72	VDD	103	SA2
11	VSS	42	CB0	73	WE#	104	NC
12	DQ8	43	CB1	74	VDDQ	105	VSS
13	DQ9	44	VSS	75	CAS#	106	DQS6#
14	VSS	45	DQS8#	76	VDDQ	107	DQS6
15	DQS1#	46	DQS8	77	NC	108	VSS
16	DQS1	47	VSS	78	NC	109	DQ50
17	VSS	48	CB2	79	VDDQ	110	DQ51
18	RESET#	49	CB3	80	NC	111	VSS
19	NC	50	VSS	81	VSS	112	DQ56
20	VSS	51	NC	82	DQ32	113	DQ57
21	DQ10	52	VDDQ	83	DQ33	114	VSS
22	DQ11	53	CKE0	84	VSS	115	DQS7#
23	VSS	54	VDD	85	DQS4#	116	DQS7
24	DQ16	55	NC/BA2	86	DQS4	117	VSS
25	DQ17	56	ERR_OUT	87	VSS	118	DQ58
26	VSS	57	VDDQ	88	DQ34	119	DQ59
27	DQS2#	58	A11	89	DQ35	120	VSS
28	DQS2	59	A7	90	VSS	121	SA0
29	VSS	60	VDD	91	DQ40	122	SA1
30	DQ18	61	A5	92	DQ41		
31	DQ19	62	A4	93	VSS		

244-Pin MiniDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
123	VSS	154	DQ28	185	A3	216	NC/ RDQS#5
124	DQ4	155	DQ29	186	A1	217	VSS
125	DQ5	156	VSS	187	VDD	218	DQ46
126	VSS	157	DM3/ RDQS3	188	CK0	219	DQ47
127	DM0/ RDQS0	158	NC/ RDQS#3	189	CK0#	220	VSS
128	NC/ RDQS#0	159	VSS	190	VDD	221	DQ52
129	VSS	160	DQ30	191	A0	222	DQ53
130	DQ6	161	DQ31	192	BA1	223	VSS
131	DQ7	162	VSS	193	VDD	224	RFU
132	VSS	163	CB4	194	RAS#	225	RFU
133	DQ12	164	CB5	195	VDDQ	226	VSS
134	DQ13	165	VSS	196	S0#	227	DM6/ RDQS6
135	VSS	166	DM8/ RDQS8	197	VDDQ	228	NC/ RDQS#6
136	DM1/ RDQS1	167	NC/ RDQS#8	198	ODT0	229	VSS
137	NC/ RDQS#1	168	VSS	199	A13	230	DQ54
138	VSS	169	CB6	200	VDD	231	DQ55
139	RFU	170	CB7	201	NC	232	VSS
140	RFU	171	VSS	202	VSS	233	DQ60
141	VSS	172	NC	203	DQ36	234	DQ61
142	DQ14	173	VDDQ	204	DQ37	235	VSS
143	DQ15	174	NC	205	VSS	236	DM7/ RDQS7
144	VSS	175	VDD	206	DM4/ RDQS4	237	NC/ RDQS#7
145	DQ20	176	NC	207	NC/ RDQS#4	238	VSS
146	DQ21	177	NC	208	VSS	239	DQ62
147	VSS	178	VDDQ	209	DQ38	240	DQ63
148	DM2/ RDQS2	179	A12	210	DQ39	241	VSS
149	NC/ RDQS#2	180	A9	211	VSS	242	SDA
150	VSS	181	VDD	212	DQ44	243	SCL
151	DQ22	182	A8	213	DQ45	244	VDDSPD
152	DQ23	183	A6	214	VSS		
153	VSS	184	VDDQ	215	DM5/ RDQS5		

Notes: 1. Pin 55 is NC for 512MB, or BA2 for 1GB.

Table 6: Pin Descriptions

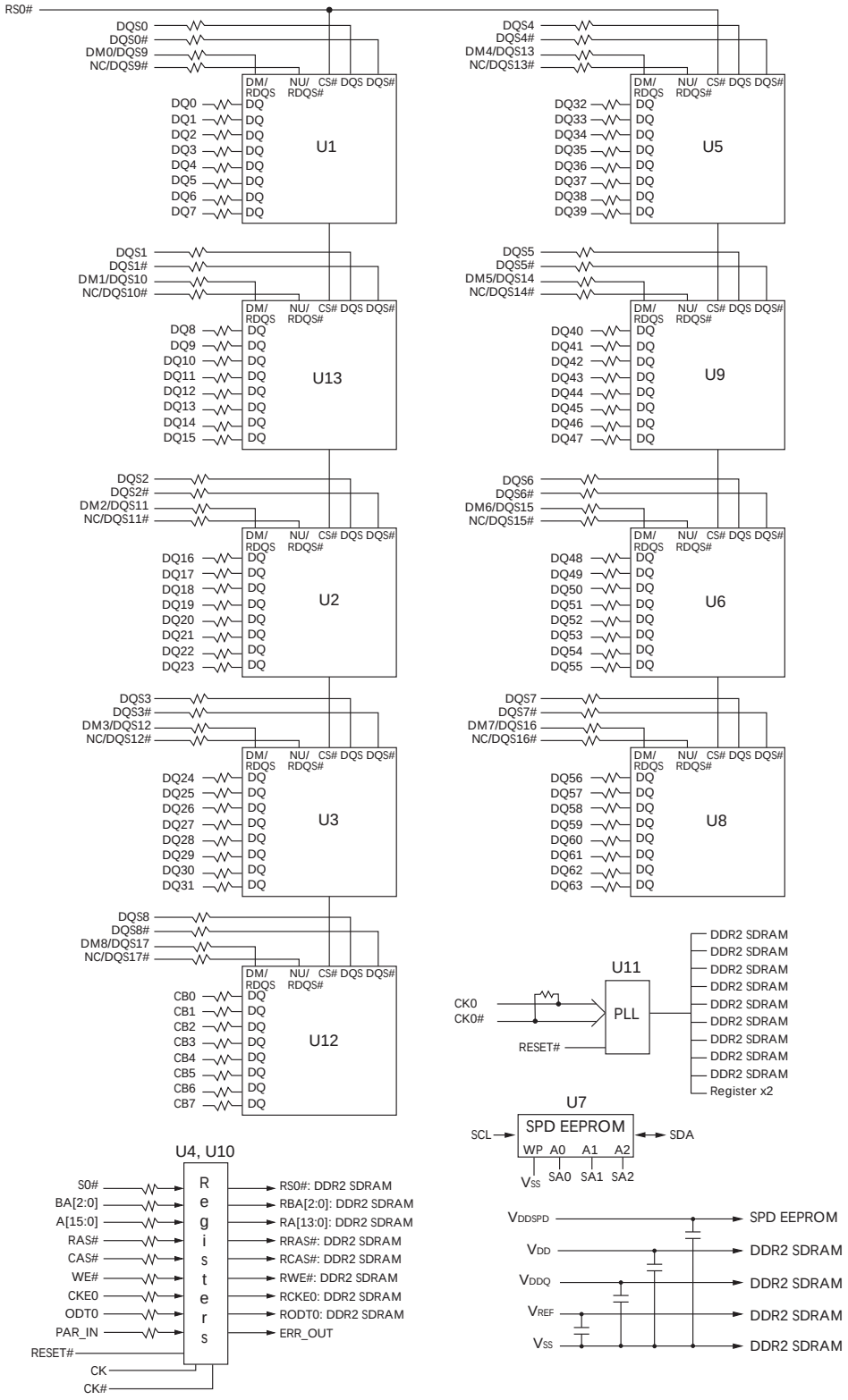
Symbol	Type	Description
A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2/1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A[13:0] (512MB, 1GB). A[15:14] are connected for parity.
BA[2:0]	Input	**Bank address inputs:** BA[2/1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2/1:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command. BA[1:0] (512MB) and BA[2:0] (1GB).
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ, DQS, and DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DM[8:0] RDQS[8:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. If RDQS is disabled, RDQS[8:0] become DM[8:0] and RDQS#[8:0] are not used.
ODT0	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
PAR_IN	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize communication to and from the SPD EEPROM.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I^2C bus.
ERR_OUT	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
VDD/VDDQ	Supply	**Power supply:** 1.8V ±0.1V. The component VDD and VDDQ are connected to the module VDD.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
V_{DDSPD}	Supply	**SPD EEPROM power supply:** +1.7V to +3.6V.
V_{REF}	Supply	**Reference voltage:** $V_{DD}/2$.
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.
RFU	–	Reserved for future use.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT9HTF6472(P)K and MT9HTF12872(P)K DDR2 SDRAM modules are high-speed, CMOS dynamic random access 512MB and 1GB memory modules organized in x72 configurations. These modules use 512Mb DDR2 SDRAM devices with four internal banks, or 1Gb DDR2 SDRAM device with eight internal banks.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL EEPROM Operation

These DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7, may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}/V_{DDQ}	V_{DD}/V_{DDQ} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
I_I	Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; V_{REF} input $0V \le V_{IN} \le 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA	–5	+5	µA
		CK, CK#	–250	+250	
		DM	–5	+5	
I_{OZ}	Output leakage current; $0V \le V_{OUT} \le V_{DD}$; DQ and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–18	+18	µA
T_A	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. The refresh rate is required to double when $85°C < T_C \le 95°C$.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades
DDR2 components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

Table 9: IDD Specifications and Conditions – 512MB

Values are for the MT47H64M8 DDR2 SDRAM components only, and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	900	810	720	720	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	1,035	945	855	810	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	405	360	315	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	495	450	405	360	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	360	315	270	225	mA
	Slow PDN Exit MR[12] = 1		108	108	108	108	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	630	585	495	405	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,755	1,530	1,260	1,035	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,845	1,620	1,305	1,035	mA
Burst refresh current; tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,070	1,620	1,530	1,485	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions for detail		IDD7	2,700	2,160	2,025	1,980	mA

Table 10: IDD Specifications and Conditions – 1GB

Values are for the MT47H128M8 DDR2 SDRAM components only, and are computed from values specified in the 1Gb (128Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	810	765	630	630	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	990	900	855	810	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	360	360	315	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	450	360	360	315	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	360	270	270	270	mA
	Slow PDN Exit MR[12] = 1		90	90	90	90	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	540	495	405	360	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,440	1,215	1,125	945	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,440	1,215	1,125	945	mA
Burst refresh current; tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,115	1,935	1,890	1,845	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions for detail		IDD7	3,015	2,520	2,430	2,340	mA

Register and PLL Specifications

Table 11: Register Specifications
SSTU32866 devices or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	SSTL_18	$V_{REF(DC)}$ + 125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	V
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	V
Input current	I_I	All pins	V_I = V_{DDQ} or V_{SSQ}	–5	+5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I_O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	–	40	mA
Dynamic operating (clock tree)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data input switching at ^{t}CK/2, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	V_I = V_{REF} ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Table 12: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	RESET#, CK, CK#	–	–0.3	$V_{DD}Q$ + 0.3	V
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	($V_{DD}Q$/2) - 0.15	($V_{DD}Q$/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	$V_{DD}Q$ + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	$V_{DD}Q$ + 0.4	V
Input current	I_I	RESET#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–10	+10	µA
		CK, CK#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–250	+250	µA
Output disabled current	I_{ODL}		RESET# = $V_{SS}Q$; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = $V_{DD}Q$ or $V_{SS}Q$	2	3	pF

Table 13: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^tL	–	15	µs
Input clock slew rate	slr(i)	1.0	4.0	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Serial Presence-Detect

Table 14: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CC_R}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CC_W}	2.0	3.0	mA

Table 15: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA fall time	^tF	–	300	ns	2
SDA rise time	^tR	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tH:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

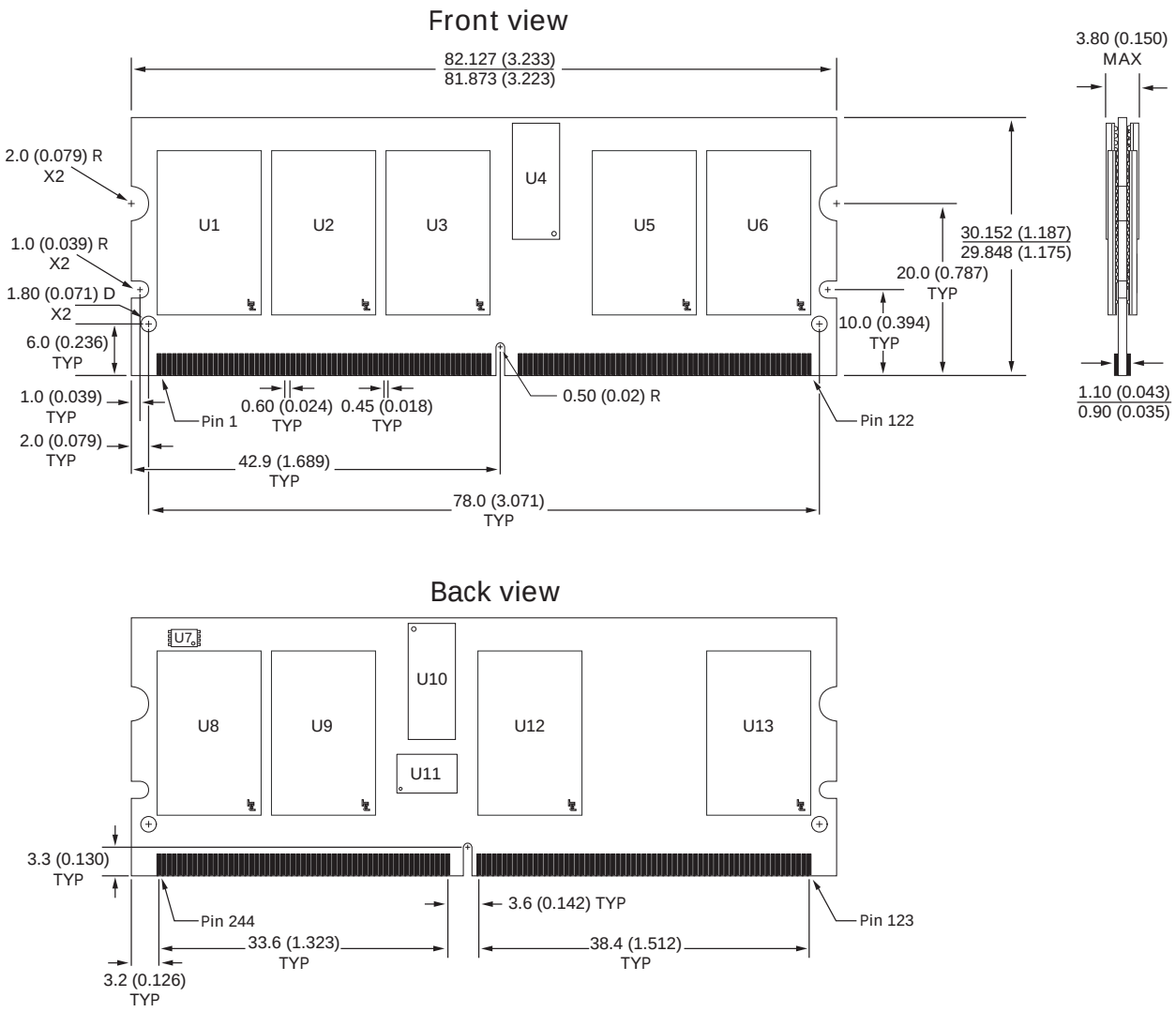
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 244-pin DIMM DDR2 Module Dimensions



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992