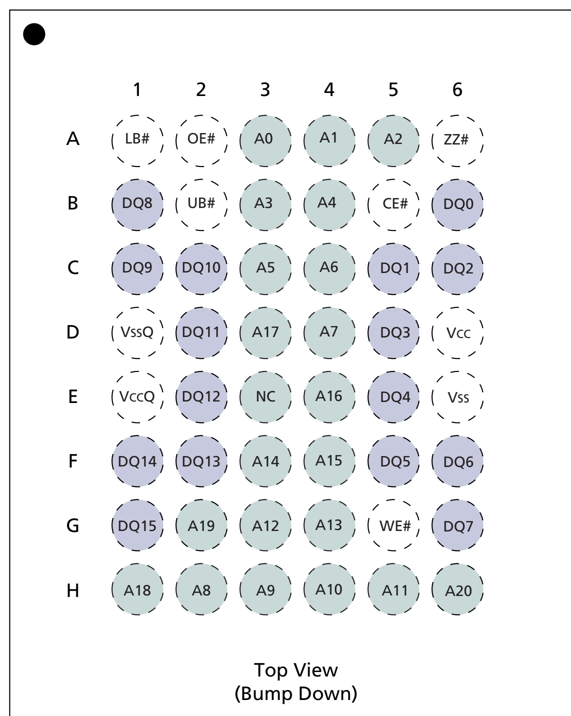
ASYNCHRONOUS CellularRAM™

MT45W2MW16PAFA **MT45W1MW16PAFA**
MT45W2ML16PAFA **MT45W1ML16PAFA**

Features

- Asynchronous and Page Mode interface
- Random Access Time: 70ns, 85ns
- Page Mode Read Access
  Sixteen-word page size
  Interpage read access: 70ns, 85ns
  Intrapage read access: 20ns, 25ns
- VCC, VCCQ Voltages
  1.70V–1.95V VCC
  1.70V–2.25V VCCQ (Option W)
  2.30V–2.70V VCCQ (Option V—contact factory)
  2.70V–3.30V VCCQ (Option L)
- Low Power Consumption
  Asynchronous READ < 25mA
  Intrapage READ < 15mA
  Standby: 110µA (32Mb—standard), 70µA (16Mb)
  90µA (32Mb—low-power option)
  Deep Power-Down < 10µA
- Low-Power Features
  Temperature Compensated Refresh (TCR)
  On-Chip Sensor Control
  Partial Array Refresh (PAR)
  Deep Power-Down (DPD) Mode

Figure 1: 48-Ball FBGA



NOTE:
See Table 1 on page 3 for Ball Descriptions. See Figure 21 on page 24 for the 48-ball mechanical drawing.

Options	Designator
• Configuration	
2 Meg x 16	MT45W2Mx16PA
1 Meg x 16	MT45W1Mx16PA
• Vcc Core Voltage Supply	
1.8V – MT45WxMx16PA	W
• VccQ I/O Voltage	
3.0V – MT45WxML16PA	L
2.5V – MT45WxMV16PA	V[1]
1.8V – MT45WxMW16PA	W
• Package	
48-ball FBGA	FA
48-ball FBGA—Lead-free	BA[1]
• Access Time	
60ns	-60[1]
70ns	-70
85ns	-85

Options (continued)	Designator
• Standby Power	
Standard	None
Low-Power (32Mb)	L
• Operating Temperature Range	
Wireless (-25°C to +85°C)	WT
Industrial (-40°C to +85°C)	IT[1]

Note 1: Contact factory.

Part Number Example:
MT45W2ML16PAFA-70LWT

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General Description

Micron® CellularRAM™ products are high-speed, CMOS dynamic random access memories that have been developed for low-power portable applications. The MT45W2Mx16PA is a 32Mb device organized as 2 Meg x 16 bits, and the MT45W1Mx16PA is a 16Mb device organized as 1 Meg x 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings.

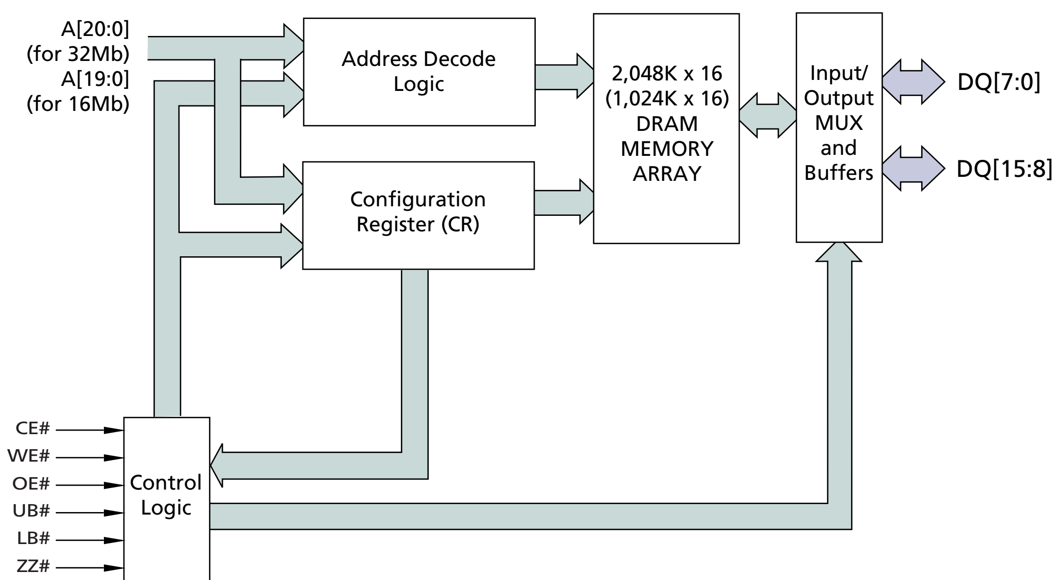
Operating voltages have been reduced in an effort to minimize power consumption. The core voltage has been reduced to a 1.80V operating level. To maintain compatibility with different memory bus interfaces, CellularRAM devices are available with I/O voltages of 3.00V, 2.50V or 1.80V.

A user-accessible configuration register (CR) defines how the CellularRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.

To operate seamlessly on an asynchronous memory bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Special attention has been focused on current consumption during self refresh. CellularRAM products include three system-accessible mechanisms to minimize refresh current. Temperature compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. TCR can also be set by the system for maximum device temperatures of +85°C, +45°C, and +15°C. Setting the sleep enable pin ZZ# to LOW enables one of two low-power modes: partial array refresh (PAR); or deep power-down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the CR.

**Figure 2: Functional Block Diagram
2 Meg x 16 and 1 Meg x 16**



NOTE:

Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information.

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Table 1: FBGA Ball Descriptions

FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, G2, H6	A[20:0]	Input	Address Inputs: Inputs for the address accessed during READ or WRITE operations. The address lines are also used to define the value to be loaded into the CR. On the 16Mb device, A20 (ball H6) is not internally connected.
A6	ZZ#	Input	Sleep Enable: When ZZ# is LOW, the CR can be loaded or the device can enter one of two low-power modes (DPD or PAR).
B5	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
A2	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write Enable: Enables WRITE operations when LOW.
A1	LB#	Input	Lower Byte Enable. DQ[7:0]
B2	UB#	Input	Upper Byte Enable. DQ[15:8]
B6, C5, C6, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	DQ[15:0]	Input/ Output	Data Inputs/Outputs.
E3	NC	—	Not internally connected.
D6	VCC	Supply	Device Power Supply: (1.7V–1.95V) Power supply for device core operation.
E1	VCCQ	Supply	I/O Power Supply: (1.8V, 2.5V, 3.0V) Power supply for input/output buffers.
E6	VSS	Supply	VSS must be connected to ground.
D1	VSSQ	Supply	VSSQ must be connected to ground.

Table 2: Bus Operations

MODE	POWER	CE#	WE#	OE#	LB#/UB#	ZZ#	DQ[15:0][1]	NOTES
Standby	Standby	H	X	X	X	H	High-Z	2, 5
Read	Active	L	H	L	L	H	Data-Out	1, 4
Write	Active	L	L	X	L	H	Data-In	1, 3, 4
No Operation	Idle	L	X	X	X	H	X	4, 5
PAR	Partial Array Refresh	H	X	X	X	L	High-Z	6
DPD	Deep Power-Down	H	X	X	X	L	High-Z	6
Load Configuration Register	Active	L	L	X	X	L	High-Z	

NOTE:

1. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When LB# only is in select mode, only DQ[7:0] are affected. When UB# only is in the select mode, DQ[15:8] are affected.
2. When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.
3. When WE# is invoked, the OE# input is internally disabled and has no effect on the I/Os.
4. The device will consume active power in this mode whenever addresses are changed.
5. VIN = VCCQ or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.
6. DPD is enabled when configuration register bit CR[4] is “0”; otherwise, PAR is enabled.

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Table 3: Abbreviated Component Marks—CellularRAM FBGA-Packaged Components

PART NUMBER	ENGINEERING SAMPLE	QUALIFIED PRODUCT
MT45W2MW16PAFA-85 WT	PX400	PW400
MT45W2MW16PAFA-70 WT	PX401	PW401
MT45W2ML16PAFA-85 WT	PX403	PW403
MT45W2ML16PAFA-70 WT	PX404	PW404
MT45W1MW16PAFA-85 WT	PX104	PW104
MT45W1MW16PAFA-70 WT	PX105	PW105
MT45W1ML16PAFA-85 WT	PX107	PW107
MT45W1ML16PAFA-70 WT	PX108	PW108

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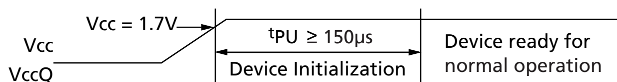
Functional Description

In general, the MT45W2Mx16PA device and the MT45W1Mx16PA device are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The MT45W2Mx16PA contains 33,554,432 bits organized as 2,097,152 addresses by 16 bits.The MT45W1Mx16PA contains 16,777,216 bits organized as 1,048,576 addresses by 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default setting. VCC and VCCQ must be applied simultaneously, and when they reach a stable level above 1.70V, the device will require 150µs to complete its self-initialization process (see Figure 3 below). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 3: Power-Up Initialization Timing



Bus Operating Modes

The MT45W2Mx16PA and the MT45W1Mx16PA CellularRAM products incorporate the industry-standard, asynchronous interface found on other low-power SRAM or Pseudo SRAM offerings. This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 4) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 5) occur when CE#, WE#, and LB#/UB# are driven LOW. During WRITE operations, the level of OE# is a “Don't Care”; WE# will override OE#. The data to be written will be latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first).

Figure 4: READ Operation

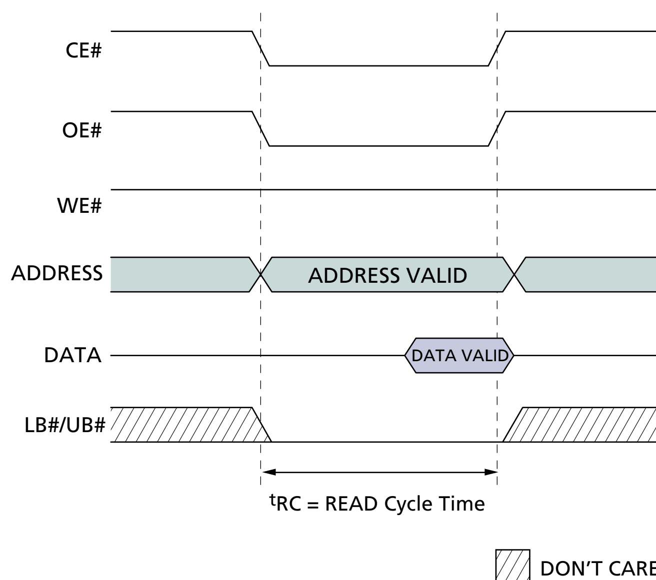
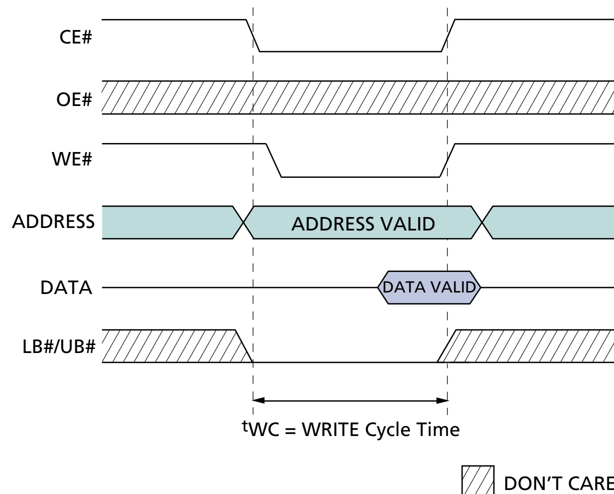


Figure 5: WRITE Operation



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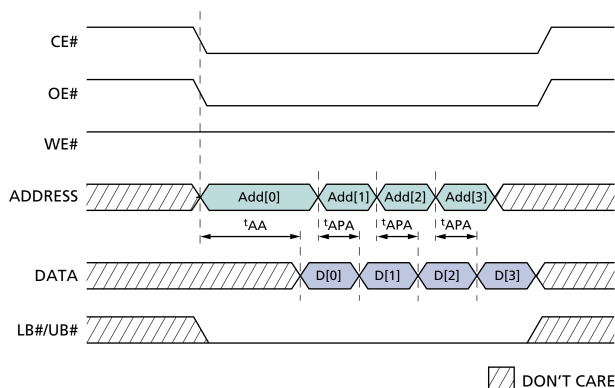
Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 6 shows the timing diagram for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

Figure 6: Page READ Operation



LB#/UB# Operation

The lower byte (LB#) enable and upper byte (UB#) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the memory array and the internal value will remain unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, the device remains in an active mode as long as CE# remains LOW.

Low Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation on the full array. Standby operation occurs when CE# and ZZ# are HIGH.

The device will enter a reduced power state during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh

Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor. When the sensor is enabled, it continually adjusts the refresh rate according to the operating temperature. The on-chip sensor is enabled by default.

Three fixed refresh rates are also available, corresponding to temperature thresholds of +15°C, +45°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35°C, the system can minimize self-refresh current consumption by selecting the +45°C setting. The +15°C setting would result in inadequate refreshing and cause data corruption.

Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the system to reduce refresh current by only refreshing that part of the memory array that is absolutely necessary. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. Data stored in addresses not receiving refresh will become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (Tables 5 and 6 on page 11). READ and WRITE operations are ignored during PAR operation.

The device only enters PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by bring the ZZ# pin to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause an exit from PAR and the entire array will be immediately available for READ and WRITE operations.

Alternatively, PAR can be initiated using the CR software access sequence (see Software Access to the Configuration Register on page 8). PAR is enabled

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immediately upon setting CR[4] to “1” using this method. However, using software access to write to the CR alters the function of the ZZ# pin so that ZZ# LOW no longer initiates PAR, although ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up. (See Figure 7.)

Driving the ZZ# pin LOW will place the device in the PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).

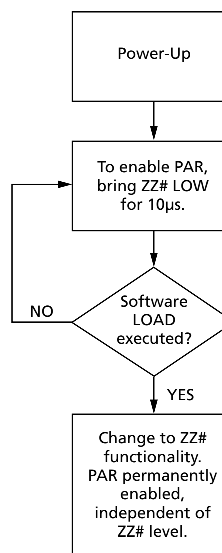
The device should not be put into DPD using CR software access.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing the ZZ# pin to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause the device to exit DPD and begin a 150µs initialization process. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

Figure 7: Software Access PAR Functionality



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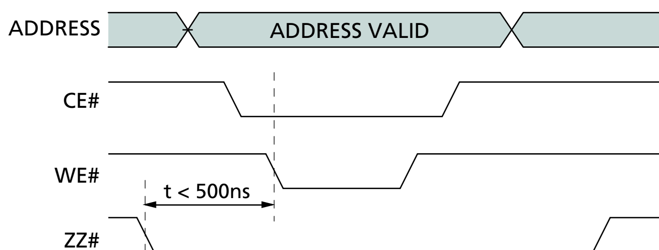
Configuration Register Operation

The configuration register (CR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the CR. This register can be updated anytime while the device is operating in a standby state. Table 4 on page 11 describes the control bits used in the CR. At power up, the CR is set to 0010h.

Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (Figure 8). The values placed on addresses A[20:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are "Don't Care." Access using ZZ# is WRITE only.

Figure 8: Load Configuration Register Operation



Software Access to the Configuration Register

The contents of the CR can either be read or modified using a software sequence. The nature of this access mechanism may eliminate the need for the ZZ# pin.

If the software mechanism is used, the ZZ# pin can simply be tied to VCCQ. The port line typically used for ZZ# control purposes will no longer be required. However, ZZ# should not be tied to VCCQ if the system will use DPD; DPD cannot be enabled or disabled using the software access sequence.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 8). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 9 on page 9).

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFh for 32Mb and FFFFFh for 16Mb); the contents of this address are not changed by using this sequence. The data bus is used to transfer data into or out of the CR.

Writing to the CR using the software sequence modifies the function of the ZZ# pin. Once the software sequence loads the CR, the level of the ZZ# pin no longer enables PAR operation. PAR operation will be updated whenever the software sequence loads a new value into the CR. This ZZ# functionality will continue until the next time the device is powered-up. The operation of the ZZ# pin is not affected if the software sequence is only used to read the contents of the CR. The use of the software sequence does not affect the ability to perform the standard (ZZ# controlled) method of loading the CR.

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Figure 9: Software Access Load Configuration Register

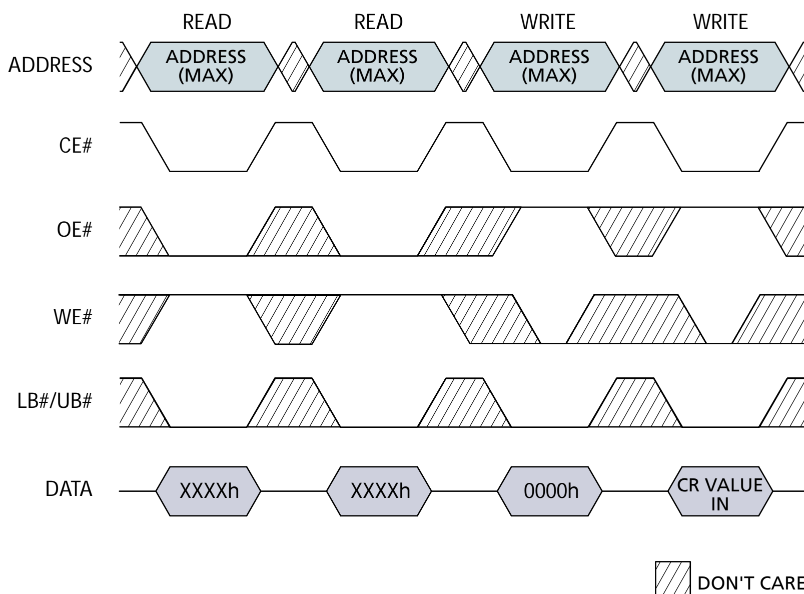
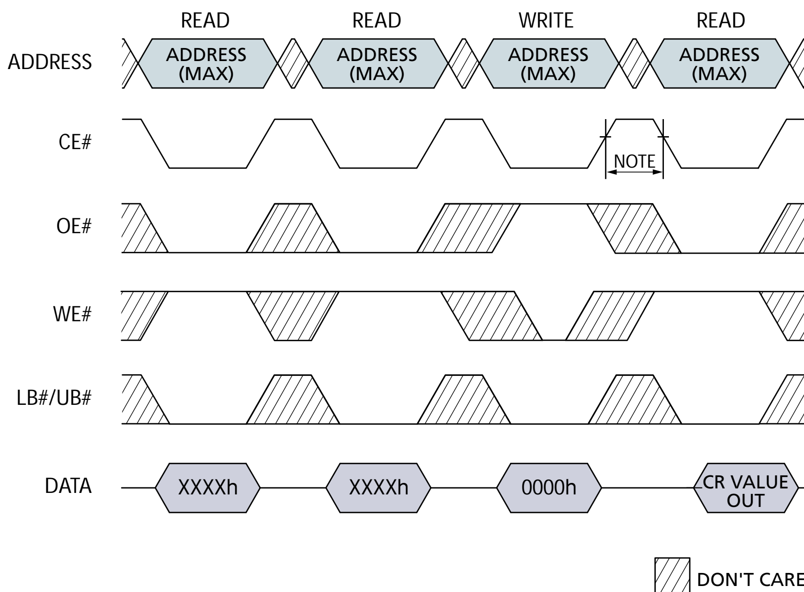


Figure 10: Software Access Read Configuration Register



NOTE:

CE# must be HIGH for 150ns before performing the cycle that reads the configuration register.

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Partial Array Refresh (CR[2:0])
Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the system to reduce current by only refreshing that part of the memory array required by the host system. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Tables 5 and 6 on page 11).

Sleep Mode (CR[4])
Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables ZZ# initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; this should only be done using ZZ# to access the CR.

DPD operation disables all refresh-related activity. This mode will be used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

Temperature Compensated Refresh (CR[6:5])
Default = On-Chip Temperature Sensor

This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The on-chip TCR is enabled by clearing both of the TCR bits in the refresh configuration register (CR[6:5] = 00b). Any other TCR setting enables a fixed refresh rate. When the on-chip temperature sensor is enabled, the device continually adjusts the refresh rate according to the operating temperature.

The TCR bits also allow for adequate fixed-rate refresh at three different temperature thresholds (+15°C, +45°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35°C, the system can minimize self refresh current consumption by selecting the +45°C setting. The +15°C setting would result in inadequate refreshing and cause data corruption.

Page Mode READ Operation (CR[7])
Default = Disabled

The page mode operation bit determines whether page mode READ operations are enabled. In the power-up default state, page mode is disabled.

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Table 4: Configuration Register Bit Mapping

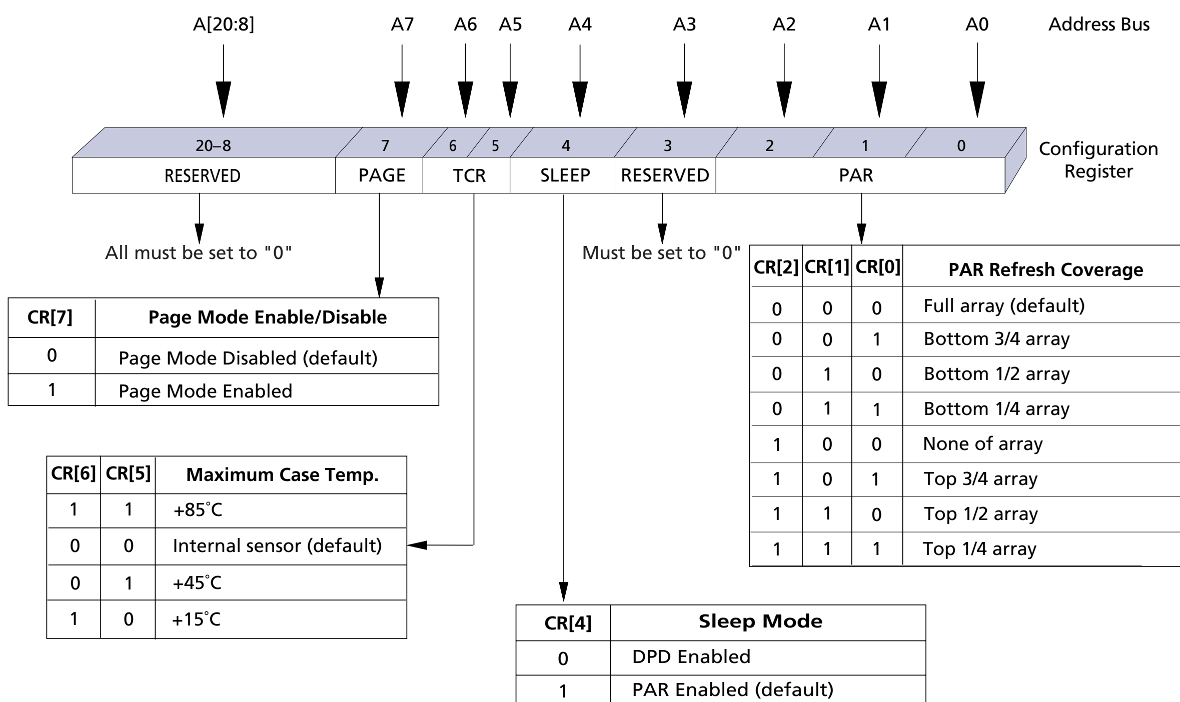

Table 5: 32Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	Three-quarters of die	000000h–2FFFFFh	1.5 Meg x 16	24Mb
0	1	0	One-half of die	000000h–1FFFFFh	1 Meg x 16	16Mb
0	1	1	One-quarter of die	000000h–0FFFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	100000h–3FFFFFh	1.5 Meg x 16	24Mb
1	1	0	One-half of die	200000h–3FFFFFh	1 Meg x 16	16Mb
1	1	1	One-quarter of die	300000h–3FFFFFh	512K x 16	8Mb

Table 6: 16Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	00000h–FFFFFh	1 Meg x 16	16Mb
0	0	1	Three-quarters of die	00000h–BFFFFh	768K x 16	12Mb
0	1	0	One-half of die	00000h–7FFFFh	512K x 16	8Mb
0	1	1	One-quarter of die	00000h–3FFFFh	256K x 16	4Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	40000h–FFFFFh	768K x 16	12Mb
1	1	0	One-half of die	80000h–FFFFFh	512K x 16	8Mb
1	1	1	One-quarter of die	C0000h–FFFFFh	256K x 16	4Mb

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Absolute Maximum Ratings*

Voltage to Any Ball Except VCC, VCCQ
Relative to VSS . . . .
-0.50V to (4.0V or VccQ + 0.3V, whichever is less)
Voltage on VCC Supply Relative to VSS. . -0.20V to 2.45V
Voltage on VCCQ Supply Relative to VSS . -0.20V to 4.0V
Storage Temperature . . . . -55°C to 150°C
Operating Temperature (Case)
Wireless. . . . . -25°C to 85°C
Industrial . . . . -40°C to 85°C
Soldering Temperature and Time
10s (lead only) . . . . .260°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Electrical Characteristics and Operating Conditions

Wireless Temperature (-25°C ≤ T_C ≤ +85 °C)
Industrial Temperature (-40°C < T_C < +85°C)

DESCRIPTION	CONDITIONS	SYMBOL		MIN	MAX	UNITS	NOTES
Supply Voltage		VCC		1.70	1.95	V	
I/O Supply Voltage		VCCQ	L: 3.00V	2.70	3.30	V	
			V: 2.50V	2.30	2.70	V	
			W:1.80V	1.70	2.25	V	
Input High Voltage		VIH		1.4	VCCQ + 0.2	V	1
Input Low Voltage		VIL		-0.2	+0.4	V	2
Output High Voltage	IOH = -0.2mA	VOH		0.80 VCCQ		V	
Output Low Voltage	IOL = 0.2mA	VOL			0.20 VCCQ	V	
Input Leakage Current	VIN = 0 to VCCQ	ILI			1	µA	
Output Leakage Current	OE# = VIH or Chip Disabled	ILO			1	µA	
Operating Current							
Asynchronous Random READ	VIN = VCCQ or 0V Chip Enabled, IOUT = 0	ICC1	-70		25	mA	3
			-85		20		
Asynchronous Page READ	VIN = VCCQ or 0V Chip Enabled, IOUT = 0		-70		15		
			-85		12		
Write Operating Current	VIN = VCCQ or 0V Chip Enabled	ICC2	-70		25	mA	
			-85		20		
Standby Current	VIN = VCCQ or 0V CE# = VCCQ	ISB	32Mb—Std		110	µA	4
			32MB—L		90		
			16Mb		70		

NOTE:
1. Input signals may overshoot to VccQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to Vss - 1.0V for periods less than 2ns during transitions
3. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
4. ISB (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. In order to achieve low standby current, all inputs must be driven to VCCQ or VSS.

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Table 8: Temperature Compensated Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	POWER	MAX CASE TEMPERATURE SETTING (CR[6:5])	MAX	UNITS
Temperature Compensated Refresh Standby Current	V_{IN} = $V_{CC}Q$ or 0V, CE# = $V_{CC}Q$	I_{TCR}	32Mb Standard (no desig.)	+85°C	110	µA
				+45°C	TBD	µA
				+15°C	TBD	µA
			32Mb Low-power option (L)	+85°C	90	µA
				+45°C	TBD	µA
				+15°C	TBD	µA
			16Mb	+85°C	70	µA
				+45°C	TBD	µA
				+15°C	TBD	µA

NOTE:

I_{TCR} (MAX) values measured with FULL ARRAY refresh.

Table 9: Partial Array Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	POWER	ARRAY PARTITION	MAX	UNITS
Partial Array Refresh Current	V_{IN} = $V_{CC}Q$ or 0V ZZ# = 0V CR[4] = 1	I_{PAR}	32Mb Standard (no desig.)	Full	110	µA
				3/4	TBD	µA
				1/2	TBD	µA
				1/4	TBD	µA
				0	TBD	µA
			32Mb Low-power option (L)	Full	90	µA
				3/4	TBD	µA
				1/2	TBD	µA
				1/4	TBD	µA
				0	TBD	µA
			16Mb	Full	70	µA
				3/4	TBD	µA
				1/2	TBD	µA
				1/4	TBD	µA
				0	TBD	µA

NOTE:

I_{PAR} (MAX) values measured with TCR set to 85°C.

Table 10: Deep Power-Down Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Deep Power-Down	V_{IN} = $V_{CC}Q$ or 0V; +25°C ZZ# = 0V CR[4] = 0	I_{ZZ}	10	µA

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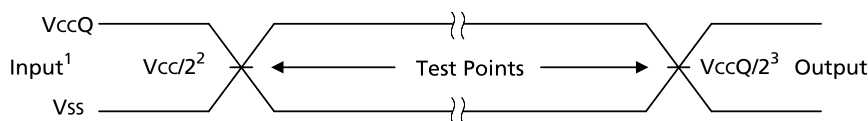
Table 11: Capacitance Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_C = +25°C; f = 1 MHz; VIN = 0V	CIN	–	6	pF	1
Input/Output Capacitance (DQ)		CIO	–	6	pF	1

NOTE:
1. These parameters are verified in device characterization and are not 100% tested.

Figure 11: AC Input/Output Reference Waveform



NOTE:
1. AC test inputs are driven at VccQ for a logic 1 and Vss for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at Vcc/2. Due to the possibility of a difference between Vcc and VccQ, the input test point may not be shown to scale.
3. Output timing ends at VccQ/2.

Figure 12: Output Load Circuit

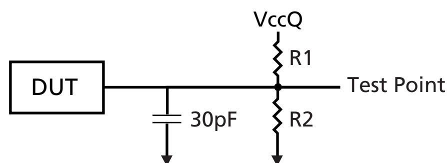


Table 12: Output Load Circuit

VccQ	R1/R2
1.8V	2.7KΩ
2.5V	3.7KΩ
3.0V	4.5KΩ

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Table 13: READ Cycle Timing Requirements

PARAMETER	SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS	NOTES
Address Access Time	^tAA		70		85	ns	
Page Access Time	^tAPA		20		25	ns	
LB#/UB# Access Time	^tBA		70		85	ns	
LB#/UB# Disable to High-Z Output	^tBHZ		8		8	ns	2
LB#/UB# Enable to Low-Z Output	^tBLZ	10		10		ns	1
Chip Select Access Time	^tCO		70		85	ns	
Chip Disable to High-Z Output	^tHZ		8		8	ns	2
Chip Enable to Low-Z Output	^tLZ	10		10		ns	1
Output Enable to Valid Output	^tOE		20		20	ns	
Output Hold from Address Change	^tOH	5		5		ns	
Output Disable to High-Z Output	^tOHZ		8		8	ns	2
Output Enable to Low-Z Output	^tOLZ	5		5		ns	1
Page Cycle Time	^tPC	20		25		ns	
Read Cycle Time	^tRC	70		85		ns	

Table 14: WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS	NOTES
Address Setup Time	^tAS	0		0		ns	
Address Valid to End of Write	^tAW	70		85		ns	
Byte Select to End of Write	^tBW	70		85		ns	
CE# HIGH Time During Write	^tCEH	5		5		ns	
Maximum CE# Pulse Width	^tCEM		10		10	µs	
Chip Enable to End of Write	^tCW	70		85		ns	
Data Hold from Write Time	^tDH	0		0		ns	
Data Write Setup Time	^tDW	23		25		ns	
Chip Enable to Low-Z Output	^tLZ	10		10		ns	1
End Write to Low-Z Output	^tOW	5		5		ns	
Write Cycle Time	^tWC	70		85		ns	
Write to High-Z Output	^tWHZ		8		8	ns	2
Write Pulse Width	^tWP	46		50		ns	
Write Pulse Width HIGH	^tWPH	10		10		ns	
Write Recovery Time	^tWR	0		0		ns	

NOTE:

1. High-Z to Low-Z timings are tested with the circuit shown in Figure 12 on page 14. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 12 on page 14. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.

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Table 15: Load Configuration Register Timing Requirements

DESCRIPTION	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	^tAS	0		0		ns	
Address Valid to End of Write	^tAW	70		85		ns	
Chip Deselect to ZZ# LOW	^tCDZZ	5		5		ns	
Chip Enable to End of Write	^tCW	70		85		ns	
Write Cycle Time	^tWC	70		85		ns	
Write Pulse Width	^tWP	40		40		ns	
Write Recovery Time	^tWR	0		0		ns	
ZZ# LOW to WE# LOW	^tZZWE	10	500	10	500	ns	

Table 16: Deep Power-Down Timing Requirements

DESCRIPTION	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Chip Deselect to ZZ# LOW	^tCDZZ	5		5		ns	
Deep Power-Down Recovery	^tR	150		150		µs	
Minimum ZZ# Pulse Width	^tZZMIN	10		10		µs	

TIMING DIAGRAMS

Figure 13: Power-Up Initialization Period

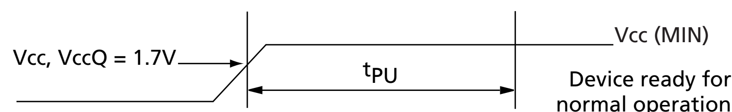

Table 17: Power-Up Initialization Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Power-Up Initialization Period	^tPU	150		150		µs	

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Figure 14: Load Configuration Register

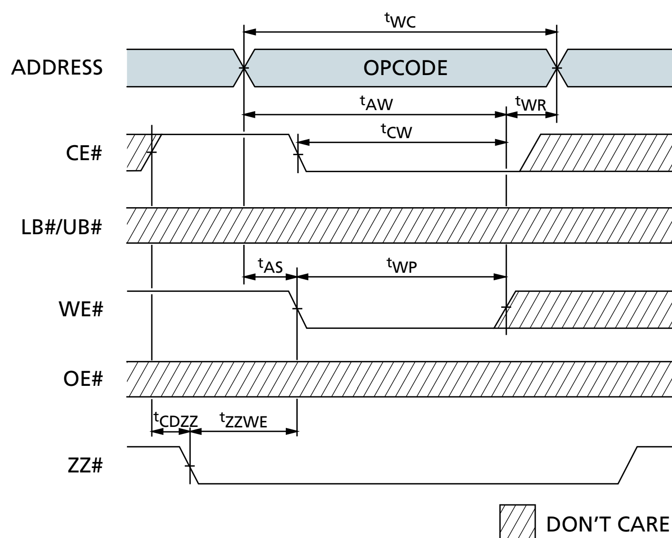

Table 18: Load Configuration Register Timing Requirements

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tAS	0		0		ns
^tAW	70		85		ns
^tCDZZ	5		5		ns
^tCW	70		85		ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tWC	70		85		ns
^tWP	40		40		ns
^tWR	0		0		ns
^tZZWE	10	500	10	500	ns

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Figure 15: Deep Power-Down—Entry/Exit

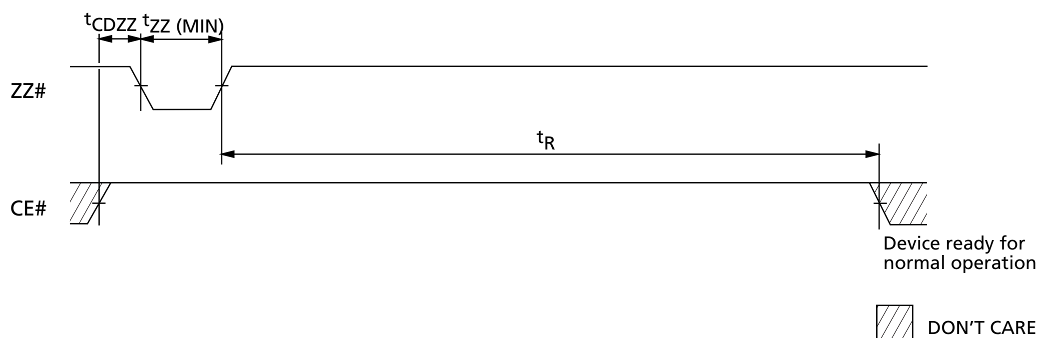

Table 19: Deep Power-Down Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}CDZZ	5		5		ns
^{t}R	150		150		µs
^{t}ZZ (MIN)	10		10		µs

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Figure 16: Single READ Operation (WE# = VIH)

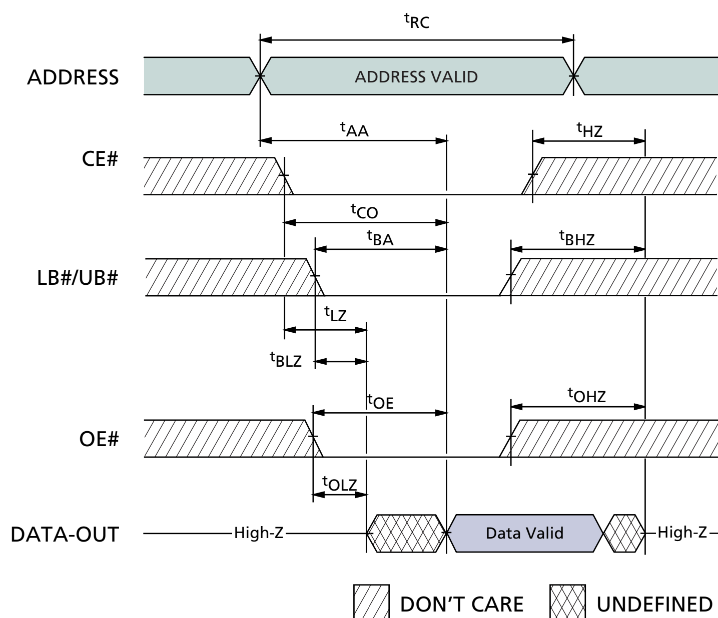

Table 20: READ Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tAA		70		85	ns
^tBA		70		85	ns
^tBHZ		8		8	ns
^tBLZ	10		10		ns
^tCO		70		85	ns
^tHZ		8		8	ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tLZ	10		10		ns
^tOE		20		20	ns
^tOHZ		8		8	ns
^tOLZ	5		5		ns
^tRC	70		85		ns

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Figure 17: Page Mode READ Operation (WE# = VIH)

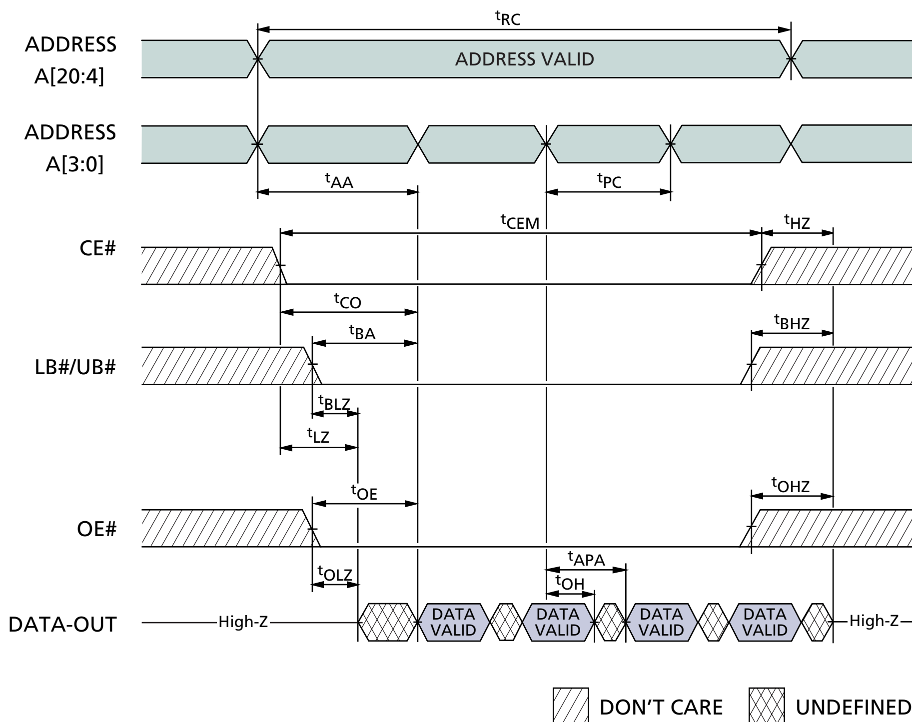

Table 21: Page Mode READ Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^{t}AA		70		85	ns
^{t}APA		20		25	ns
^{t}BA		70		85	ns
^{t}BHZ		8		8	ns
^{t}BLZ	10		10		ns
^{t}CEM		10		10	µs
^{t}CO		70		85	ns
^{t}HZ		8		8	ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^{t}LZ	10		10		ns
^{t}OE		20		20	ns
^{t}OH	5		5		ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}PC	20		25		ns
^{t}RC	70		85		ns

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Figure 18: WRITE Cycle (WE# Control)

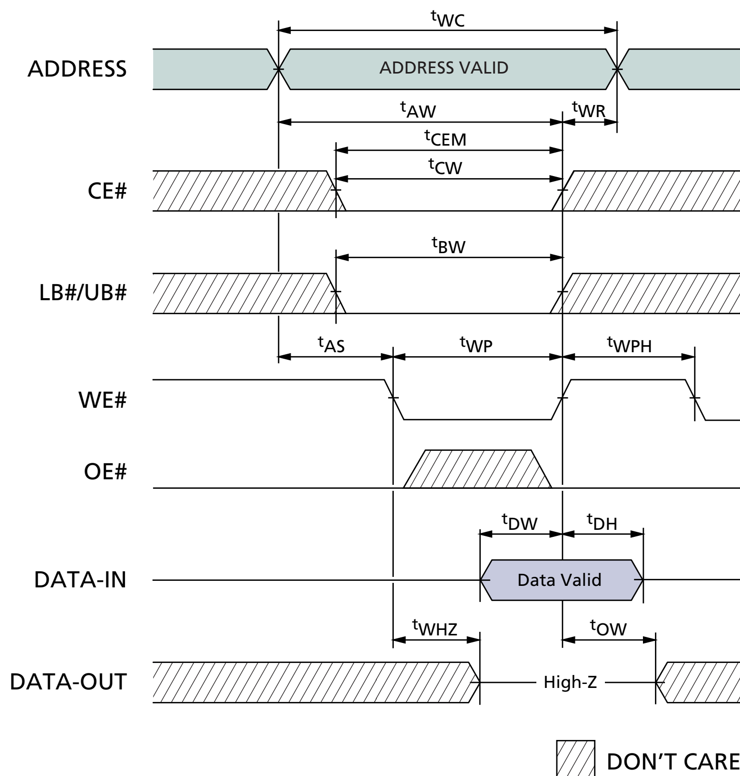

Table 22: WRITE Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tAS	0		0		ns
^tAW	70		85		ns
^tBW	70		85		ns
^tCEM		10		10	µs
^tCW	70		85		ns
^tDH	0		0		ns
^tDW	23		25		ns
^tOW	5		5		ns
^tWC	70		85		ns
^tWHZ		8		8	ns
^tWP	46		50		ns
^tWPH	10		10		ns
^tWR	0		0		ns

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Figure 19: WRITE Cycle (CE# Control)

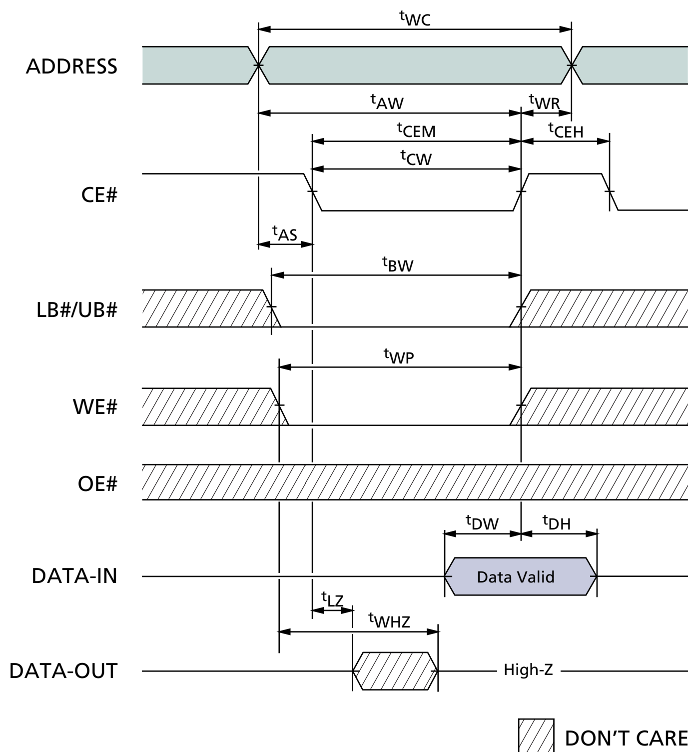

Table 23: WRITE Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tAS	0		0		ns
^tAW	70		85		ns
^tBW	70		85		ns
^tCEH	5		5		ns
^tCEM		10		10	µs
^tCW	70		85		ns
^tDH	0		0		ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tDW	23		25		ns
^tLZ	10		10		ns
^tWC	70		85		ns
^tWHZ		8		8	ns
^tWP	46		50		ns
^tWR	0		0		ns

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Figure 20: WRITE Cycle (LB#/UB# Control)

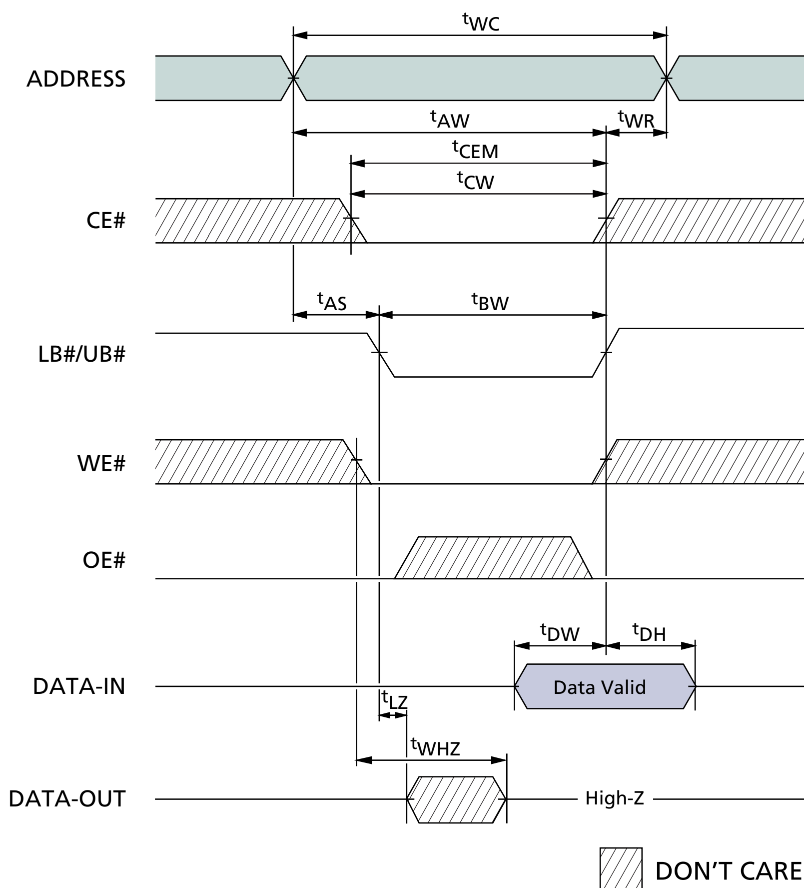

Table 24: WRITE Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tAS	0		0		ns
^tAW	70		85		ns
^tBW	70		85		ns
^tCEM		10		10	µs
^tCW	70		85		ns
^tDH	0		0		ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
^tDW	23		25		ns
^tLZ	10		10		ns
^tWC	70		85		ns
^tWHZ		8		8	ns
^tWR	0		0		ns

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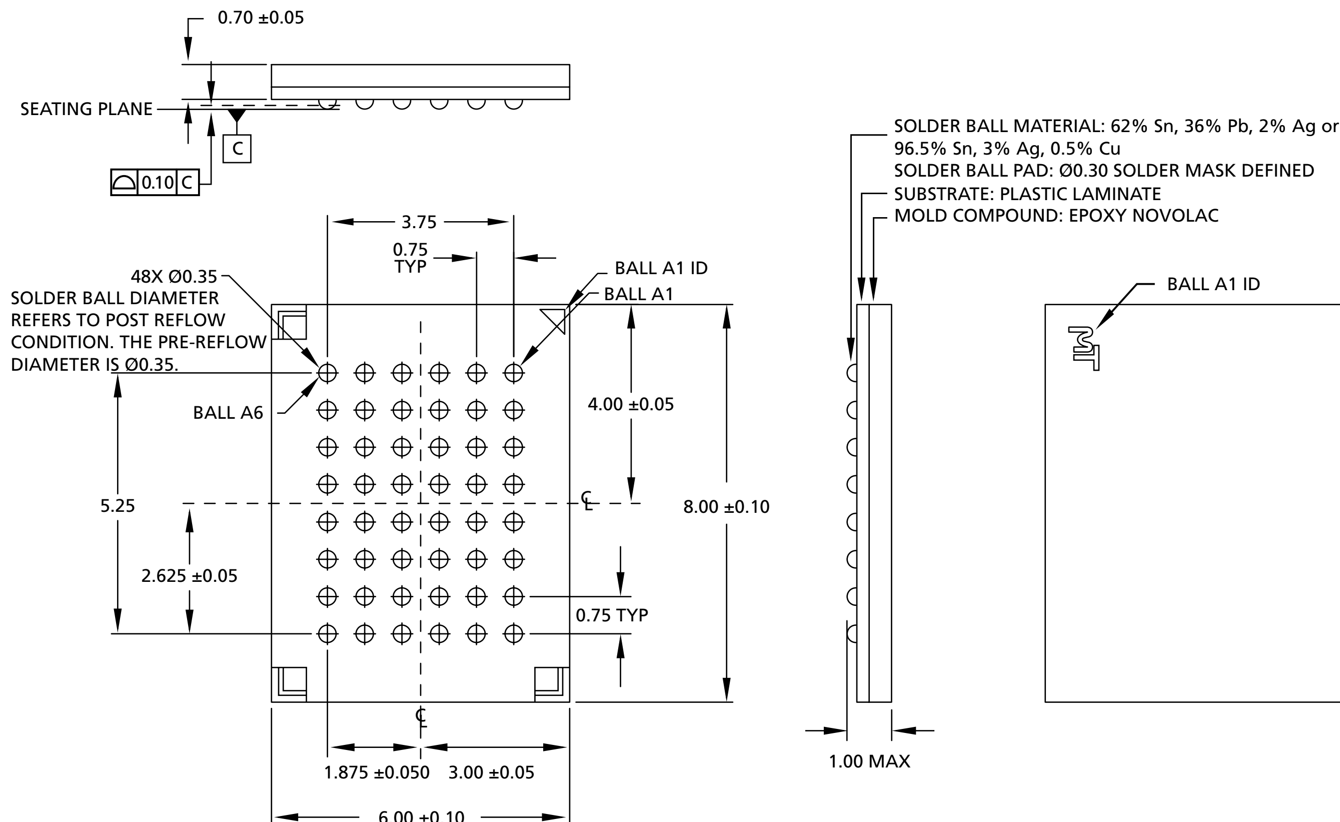
Figure 21: 48-Ball FBGA



NOTE:

1. All dimensions in millimeters, MAX/MIN or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Data Sheet Designation: ADVANCE

This data sheet contains initial descriptions of products still in development.

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APPENDIX A

How Extended Timings Impact CellularRAM™ Operation

Introduction

CellularRAM™ products use a DRAM technology that periodically requires refresh to ensure against data corruption. CellularRAM devices include on-chip circuitry that performs the required refresh in a manner that is completely transparent in systems with normal bus timings. The refresh circuitry does impose constraints on timings in systems that take longer than 10µs to complete operations. This appendix describes CellularRAM timing requirements in systems that perform extended operations. Table 25 below summarizes this information.

WRITE Operation

The timing parameters provided in Table 14 on page 15 require that all WRITE operations must be completed within 10µs. After completing a WRITE operation, the device must either enter standby (by transitioning CE# HIGH), or else perform a second operation (READ or WRITE) using a new address. Figures 22 and 23 demonstrate these constraints as they apply during an asynchronous (page-mode-disabled) operation. Either the CE# active period (^{t}CEM in Figure 22) or the address valid period (^{t}TM in Figure 23) must be less than 10µs during any WRITE operation, otherwise, the extended WRITE timings must be used.

Figure 22: Extended Timing for ^{t}CEM

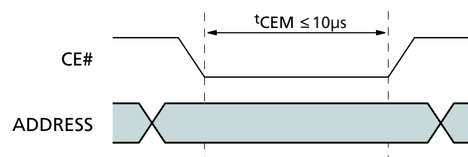

Figure 23: Extended Timing for ^{t}TM

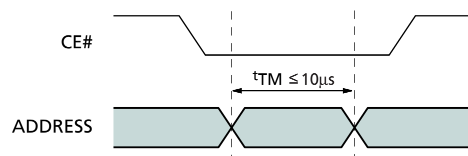

Table 25: Extended Cycle Impact on READ and WRITE Cycles

PAGE MODE	TIMING CONSTRAINT	READ CYCLE	WRITE CYCLE
Disabled	^{t}CEM and ^{t}TM > 10µs (See Figures 22 and 23 above.)	No impact.	Must use extended WRITE timing. (See Figure 24 on page 26.)
Enabled	^{t}CEM > 10µs (See Figure 22 above.)	Not allowed.	

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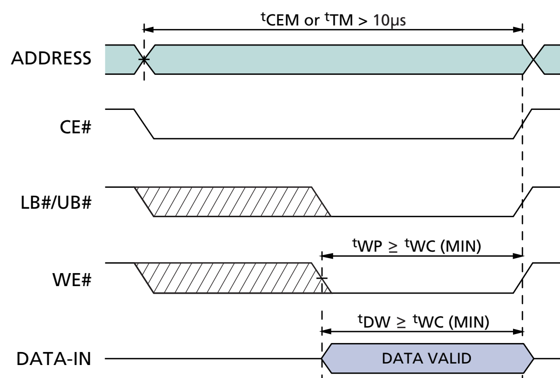
Page Mode READ Operation

When a CellularRAM device is configured for page mode operation, the address inputs are used to accelerate read accesses and cannot be used by the on-chip circuitry to schedule refresh. If CE# is LOW longer than the ^{t}CEM maximum time of 10µs, or no refresh will occur and data may be lost. Page mode should only be used in systems that can limit CE#-LOW times to less than 10µs.

Extended WRITE Timing

Modified timings are required during extended WRITE operations (see Figure 24 below). An extended WRITE operation requires that both the write pulse width (^{t}WP) and the data valid period (^{t}DW) be lengthened to at least the minimum WRITE cycle time (^{t}WC [MIN]). These increased timings ensure that time is available for both a refresh operation and a successful completion of the WRITE operation.

Figure 24: Extended WRITE Operation



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Revision History

Rev. A, Advance 2/04

- Corrected typographic error in software access description.

Rev. A, Advance 1/04

- Last address not changed by software access sequence.
- Added on-chip sensor to TCR.
- Clarified software access description.

Rev. A, Advance 12/03

- Initial Release

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