128MB to 2GB
Industrial Grade SD Cards

STEC
www.stec-inc.com

SLSDxxxBS(I)U

Compliant to Specifications

- SD Memory Card Specification Part 1, Physical Layer Specification V1.1
- SD Memory Card Specification Part 2, File System Specification V1.01
- SD Memory Card Specification Part 3 Security Specification V1.01 (CPRM)

Supports SD and SPI Modes

Variable Clock Rate:

- Low speed mode: 0 to 25MHz
- High speed mode: 26 to 50MHz

Voltage Range

- Basic communication : 2.0V to 3.6V (CMD0, CMD15, CMD55, ACMD41)
- Normal operating status: 2.7 to 3.6V

Low Power Consumption

Extended Data Write/Erase Endurance

- Optimized wear leveling algorithm
- Hardware ECC to automatically detect and correct errors
- 2,000,000 Program/Erase cycles per block for 128MB, 256MB and 512MB
- 300,000 Program/Erase cycles per block for 1GB and 2GB

Data Retention: 10 years

Power-on damage free card insertion and removal

Two Operating Temperature Ranges available:

- Commercial: 0 to 70°C
- Industrial: -40 to 85°C

RoHS compliant lead-free

General Description

The Secure Digital Industrial Grades provide a high reliable storage media in a very small space. The simplicity of the SD and SPI protocols allows easy host design and integration.

The SD Memory Card support high security level of copyright protection and an easy to implement interface.

STEC's Industrial Grade SD cards are specifically designed, manufactured and tested to withstand extreme environmental conditions and to improve system reliability and endurance.

At the heart of each card there is an advanced microcontroller that performs elaborate Flash management including 5 Bytes on-the-fly Error Detection and 4-Bytes Error Correction (EDC/ECC), bad block management (BBM) and extensive wear leveling. STEC selects the highest reliability Single Level Cell (SLC) Flash for its superior endurance.

This combination allows achieving 2,000,000 logical program/erase cycles for 128MB, 256MB, and 512MB capacities, and 300,000 logical program/erase cycles for 1GB and 2GB capacities.

STEC manufacturing process and test methodology makes the card more robust and capable to perform at the extreme temperature conditions.

To assure that each card shipped meets the rigorous threshold set by the OEM customers, each card is extensively tested at STEC's manufacturing facility to guarantee perfect functionality in extreme conditions. STEC provides rigorous bill of material control as an additional guarantee for the customer, ensuring long term product stability and support.

Ordering Information: SD Card

Part Number	Capacity
SLSD128BS(I)U	128 Mbytes
SLSD256BS(I)U	256 Mbytes
SLSD512BS(I)U	512 Mbytes
SLSD1GBBS(I)U	1 GBytes
SLSD2GBBS(I)U	2 GBytes

Legend:

- **(I) =** Industrial temperature range (-40ºC to +85 ºC).
- **Part numbers without (I) =** Commercial temperature range (0ºC to 70ºC).

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1.0 Product Specifications

1.1 Package Dimensions

Refer to the Table 1, Figure 1, and Figure 2 for package dimensions of the card. Units are in millimeters, and tolerances are ±0.15mm unless otherwise specified.

Table 1: Mechanical Dimensions SD Card

Parameter	Value
Length	32.00 ± 0.10 mm
Width	24.00 ± 0.10 mm
Height	2.10 ± 0.15 mm

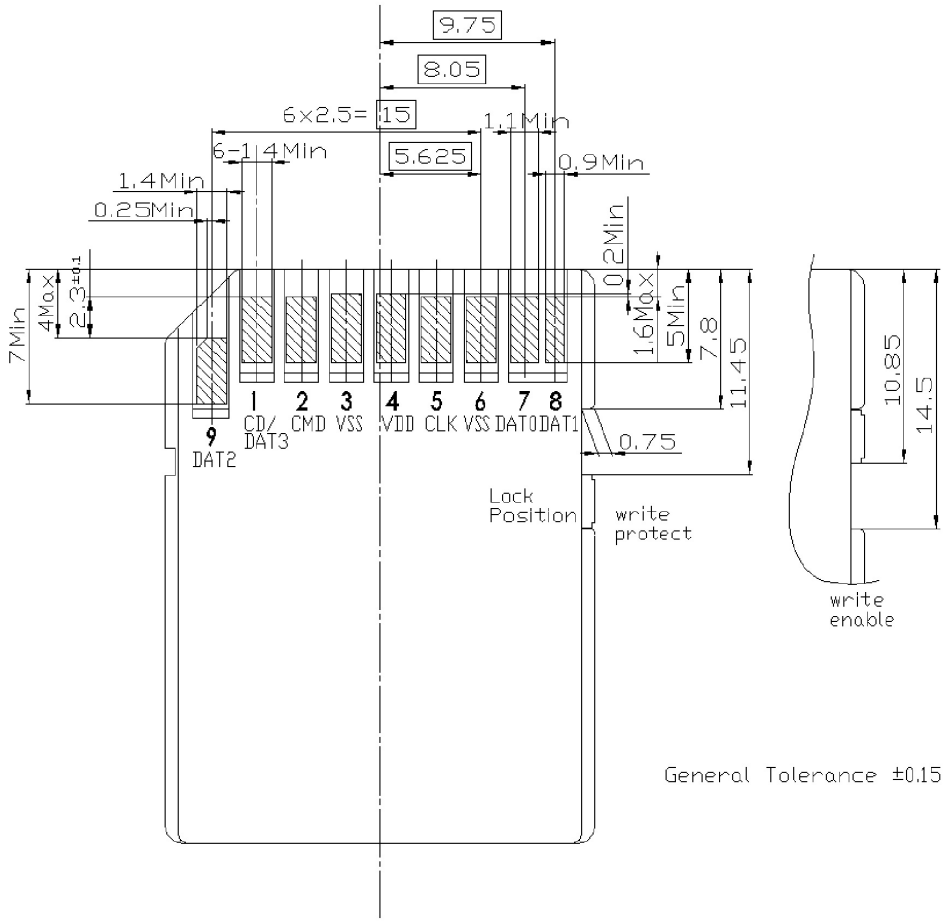

Figure 1: Mechanical Dimensions SD Card

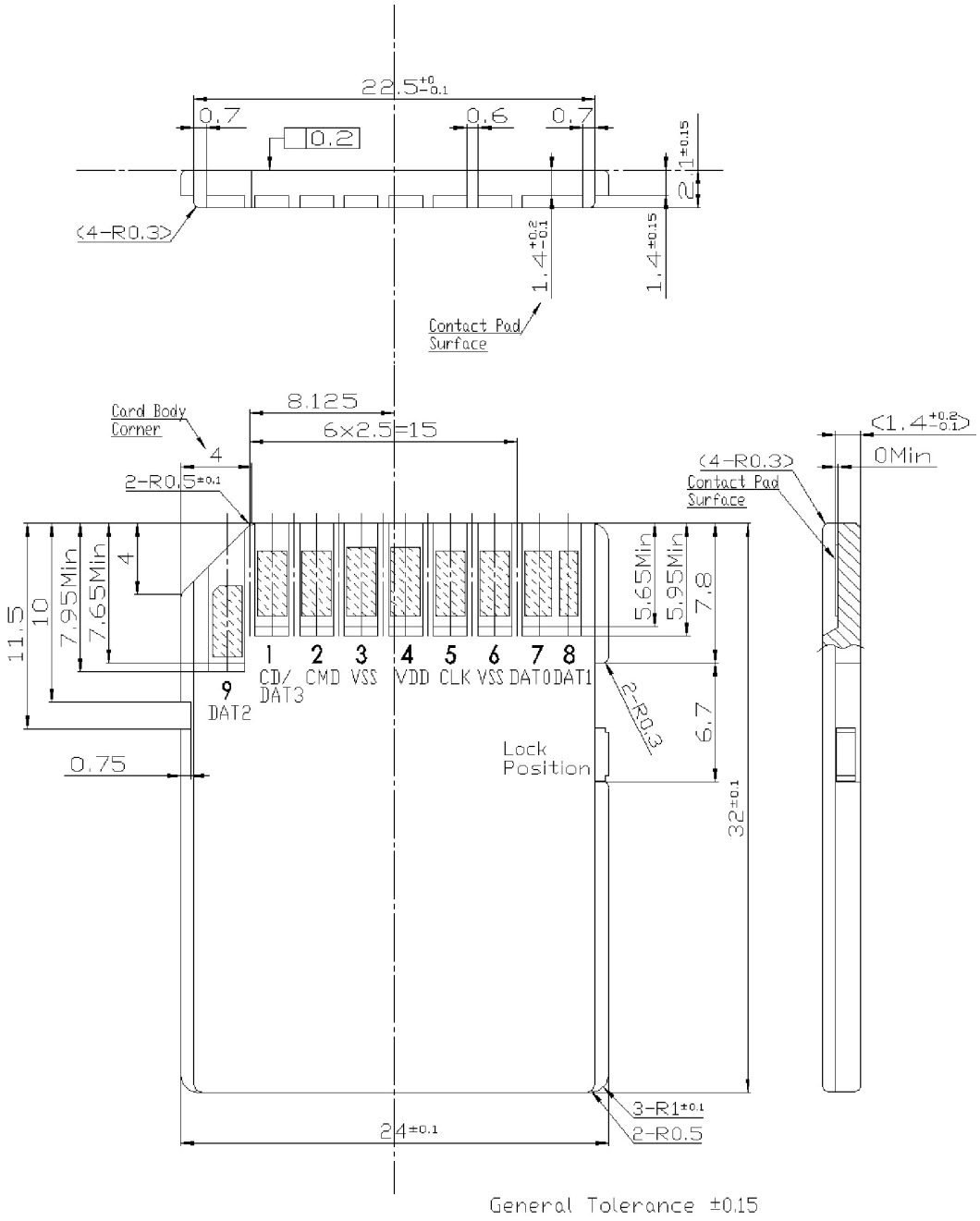

Figure 2: Mechanical Dimensions SD Card (continued)

1.2 Pin Assignment and Signal Description

Table 2: SD Mode Pin Assignment and Signal Description

Pin	Signal Name	Pin Type	Description
1	CD, DAT3	I/O, Push-Pull Drivers	Card Detect, Data line bit 3. See Notes 1 and 2.
2	CMD	Push-Pull Drivers	Command/Response
3	VSS1	Supply	Supply voltage ground
4	VDD	Supply	Supply voltage
5	CLK	Input	Clock
6	VSS2	Supply	Supply voltage ground
7	DAT0	I/O, Push-Pull Drivers	Data line bit 0. For read only cards, DAT0 is output only.
8	DAT1	I/O, Push-Pull Drivers	Data line bit 1. For read only cards, DAT1 is output only.
9	DAT2	I/O, Push-Pull Drivers	Data line bit 2. For read only cards, DAT2 is output only.

Table 3: SPI Mode Pin Assignment and Signal Description

Pin	Signal Name	Pin Type	Description
1	/CS	Input	Chip select (“/” indicates low active)
2	DI	Input	Data in
3	VSS1	Supply	Supply voltage ground
4	VDD	Supply	Supply voltage
5	SCLK	Input	Clock
6	VSS2	Supply	Supply voltage ground
7	DO	Output; Push Pull Drivers	Data out
8	—	—	Reserved for future use. Host should pull up with 10 to 100K ohm resistance.
9	—	—	Reserved for future use. Host should pull up with 10 to 100K ohm resistance.

Notes:

1. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.

2. After power up the CD line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

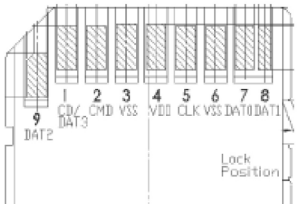

Figure 3: SD Card Contact Area

1.3 Performance

Measurements are in SD bus mode using HB Bench test.

Table 4: SD Card Read/Write Performance

Parameter	128MB	256MB	512MB	1GB	2GB	Unit
Sequential Read	Up to 12.1	Up to 12.1	Up to 11.9	Up to 11.5	Up to 13.0	Mbytes/s
Sequential Write	Up to 5.8	Up to 5.9	Up to 8.1	Up to 7.5	Up to 11.3	Mbytes/s
Random Read	Up to 11.9	Up to 11.6	Up to 11.6	Up to 11.1	Up to 12.5	Mbytes/s
Random Write	Up to 2.1	Up to 2.0	Up to 2.7	Up to 2.6	Up to 1.7	Mbytes/s

2.0 Environmental Specifications

2.1 Recommended Operating Conditions

Table 5: SD Card Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta1	Commercial Operating Temperature	0	25	70	°C
Ta2	Industrial Operating Temperature	-40	-	85	°C
VDD1	Supply Voltage: Normal Operating Status	2.7	-	3.6	V
VDD2	Supply Voltage: Basic Communication (CMD0, CMD15, CMD55, ACMD41)	2.0	3.3	3.6	V
VSS1 VSS2	Supply Voltage Differentials	-0.5	-	0.5	V
-	Power Up Time (from 0V to VDD min)	-	-	250	ms

2.2 Reliability

Table 6: SD Card Endurance & Data Retention

Parameter	Value
Endurance (128MB, 256MB, 512MB)	2,000,000 Write/Erase Cycles
Endurance (1GB, 2GB)	300,000 Write/Erase Cycles
Data retention	10 years

2.3 Durability

Table 7: Durability

Parameter	Value
Durability	10,000 insertion
Drop Test	1.5m free fall
Bending	20N middle of the card and 20N border of the card
Torque	0.15N or +/-2.5 deg
Bump	25G; 6ms; +/- 3 x 4000 shocks
Shock	1000 G max.
Minimum moving force of WP switch	40gf
WP switch cycles	1000 cycles at slide force 0.4N to 5N
Vibration: Operating	15G peak-to-peak
Vibration: Strorage	15G peak-to-peak

2.4 Humidity, & ESD

Table 8: SD Card Humidity & ESD

Parameter	Value
Humidity: Operating	25 °C/95% RH
Humidity: Storage	40°C/93% RH 500 hours
ESD: Contact Pad, Human Body Model IEC61000-4-2: Charge C=100pF; Discharge R=1.5 K ohm IEC61000-4-2: Charge C=150pF; Discharge R=0 ohm	 >±10KV >±10KV
ESD Contact Pad, Machine Model IEC61000-4-2: Charge C=200pF; Discharge R=0 ohm	±0.25KV

2.5 Absolute Maximum Ratings

Table 9: SD Card Absolute Maximum Ratings

Parameter	Value
Storage temperature range	-40 to +85^{o}C
Salt water spray	3% NaCl/35^{o}C; 24h acc. MIL STD Method 1009
Solar Exposure	1000W/m^{2} @ 40^{o}C
Impermeability	IP67
UV Light Exposure	UV: 254nm, 15Ws/cm^{2}

3.0 Electrical Specifications

3.1 DC Characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 10: SD Card DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Peak Voltage on all Lines	-0.6		3.6	V	
VIL	Input LOW Voltage			+0.8	V	VCC=3.3V
VIH	Input HIGH Voltage	2.0			V	VCC=3.3V
VOL	Output LOW Voltage			0.4	V	VCC=3.3V
VOH	Output HIGH Voltage	2.4			V	VCC=3.3V
IDD	Operating Current		25	50	mA	VCC=3.3V
IDDSB1	Pre-initialization Standby Current			3	mA	VCC=3.3V
IDDSB2	Post-initialization Standby Current		80	150	µA	VCC=3.3V
ILI	Input Leakage Current	-1		1	µA	without pull up R
ILO	Output Leakage Current	1		1	µA	without pull up R

3.2 Signal Loading

The total capacitance C_L is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS}, and the capacitance C_{CARD} of the card connected to the line:

$C_L = C_{HOST} + C_{BUS} + C_{CARD}$

To allow the sum of the host and bus capacitances to be up to 20pF for the card, the following conditions in Table 11 are met by the card.

Table 11: SD Card Signal Loading

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance	RCMD	4.7	100	K ohms	To prevent bus floating
Pull up resistance	RDAT	50	100	K ohms	To prevent bus floating
Bus signal line capacitance	CL		30	pF	Single card
Signal card capacitance	C card		7	pF	Single card
Signal line inductance			16	nH	

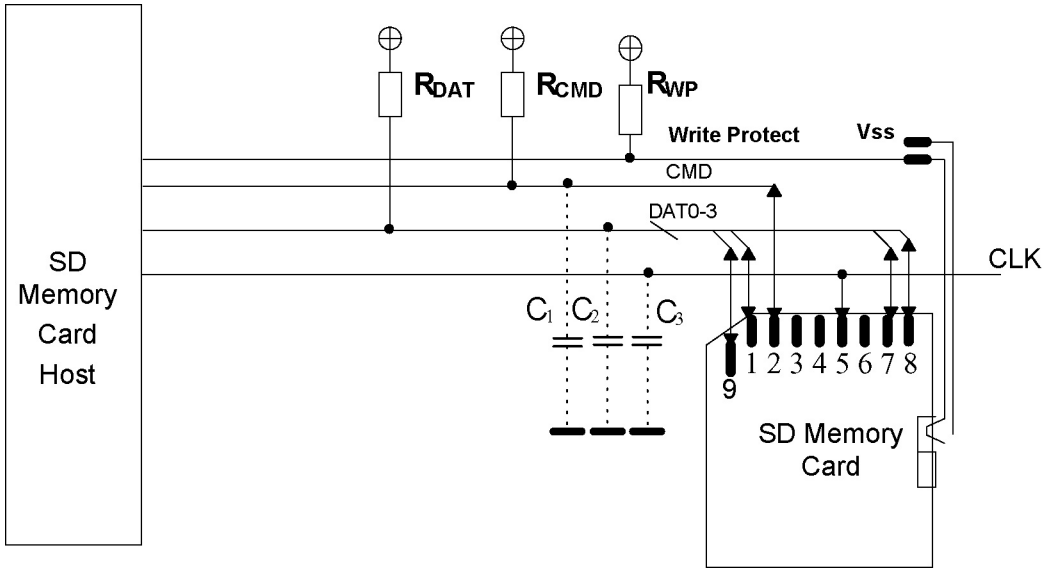

Figure 4: SD Card Signal Loading

3.3 AC Characteristics

Table 12: Characteristics Low Speed Mode

Parameter	Symbol	Min	Max	Unit
Clock frequency in data transfer mode	fPP	0	25	MHz
Clock frequency in card id mode	fOD	0	400	KHz
Clock low time	tWL	10		ns
Clock high time	tWH	10		ns
Clock rise time	tTLH		10	ns
Clock fall time	tTHL		10	ns
CMD, DAT input setup time	tISU	5		ns
CMD, DAT input hold time	tIH	5		ns
CMD, DAT output delay time	tODLY	0	14	ns

Notes:

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.
5. Specified for one card. $C_L \leq 30pF$

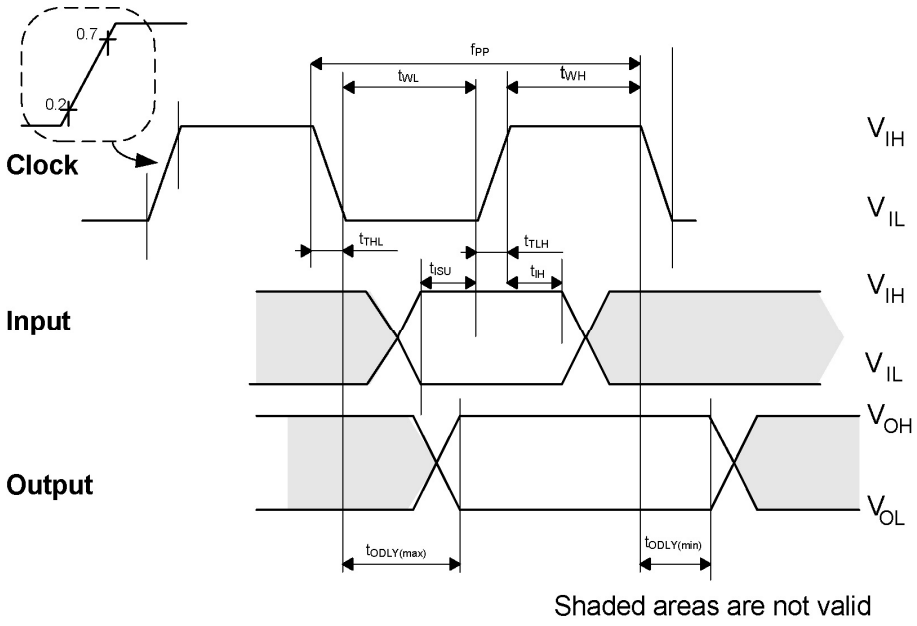

Figure 5: AC Characteristics Low Speed Mode

Table 13: AC Characteristics High Speed Mode

Parameter	Symbol	Min	Max	Unit
Clock frequency in data transfer mode	fPP	26	50	MHz
Clock low time	tWL	7.0		ns
Clock high time	tWH	7.0		ns
Clock rise time	tTLH		3	ns
Clock fall time	tTHL		3	ns
CMD, DAT input setup time	tISU	6		ns
CMD, DAT input hold time	tIH	2		ns
CMD, DAT output delay time during data transfer mode	tODLY		14	ns
CMD, DAT output hold time	tOHU	2.5		ns

Notes:

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.
5. In order to satisfy severe timing, the host shall drive only one card. $C_L \leq 30pF$

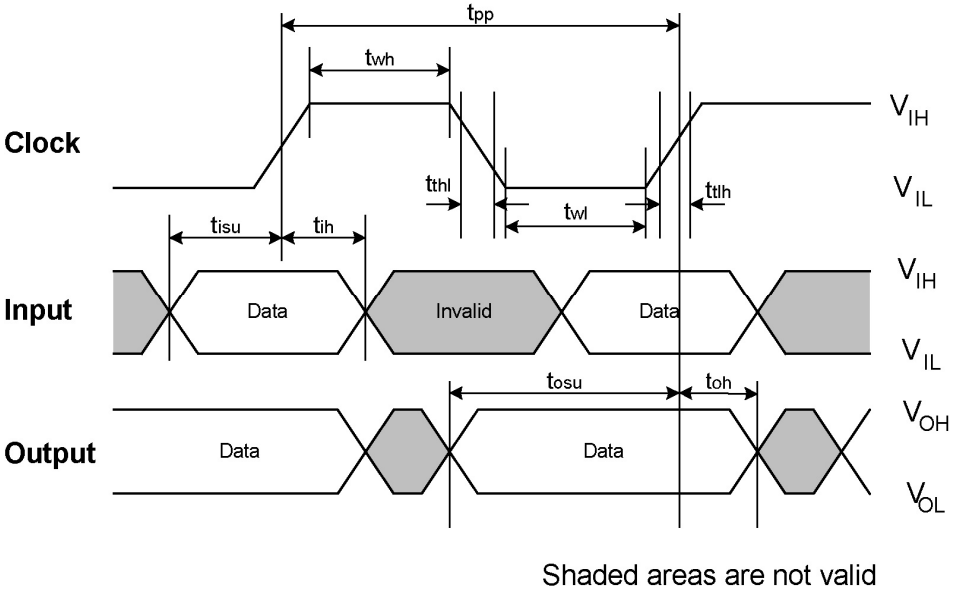

Figure 6: AC Characteristics High Speed Mode

4.0 Host Access Specifications

The following chapters summarize how the host accesses the card:

- The block diagram in *Chapter 4.1* shows how the SD and SPI buses interact with the registers via the controller.
- *Chapter 4.2* summarizes the SD and SPI buses.
- *Chapter 4.3* summarizes the registers.

4.1 Functional Block Diagram

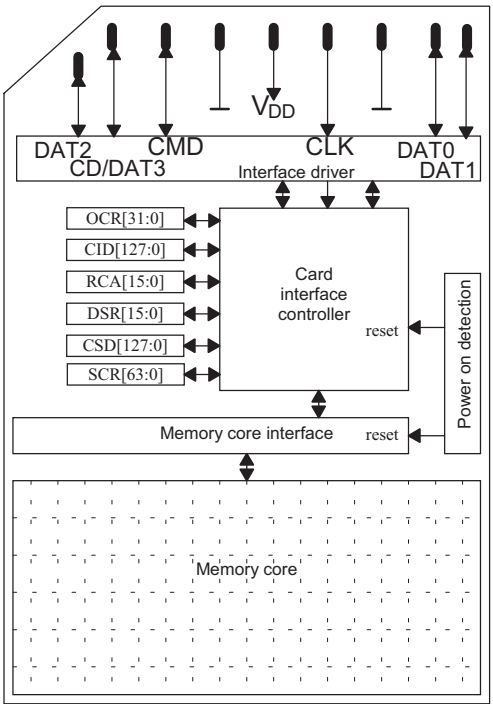

Figure 7: SD Card Function Block Diagram

4.2 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

4.2.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- *Command*: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- *Response*: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- *Data*: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

The SD bus signals are listed in Table 14 and the SD bus topology is illustrated in Figure 8.

Table 14: SD Bus Signals

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT0-DAT3	4 Bidirectional data signals
Vdd, Vss	Power and Ground

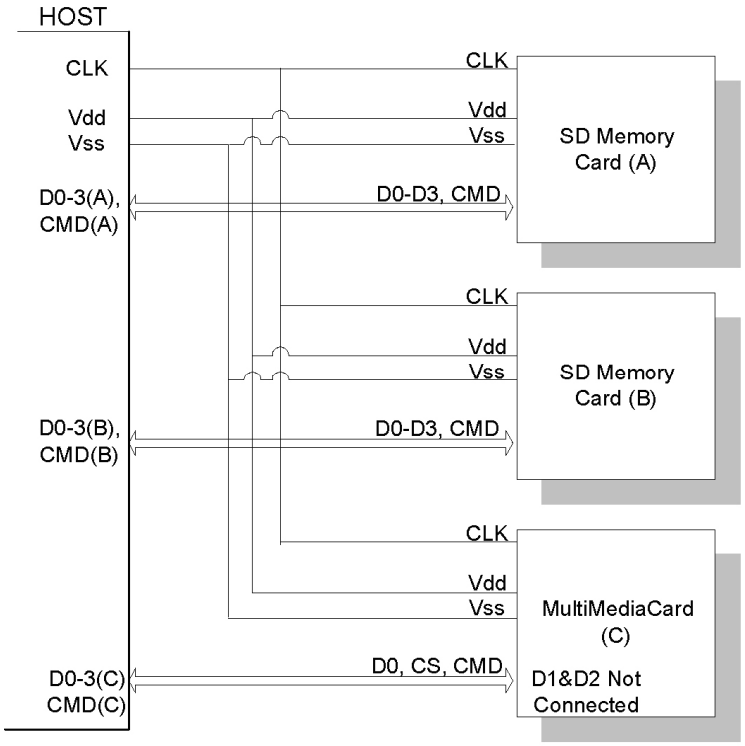

Figure 8: SD Bus Topology

4.2.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.

While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed in Table 15 and the SPI bus topology is illustrated in Figure 9.

Table 15: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

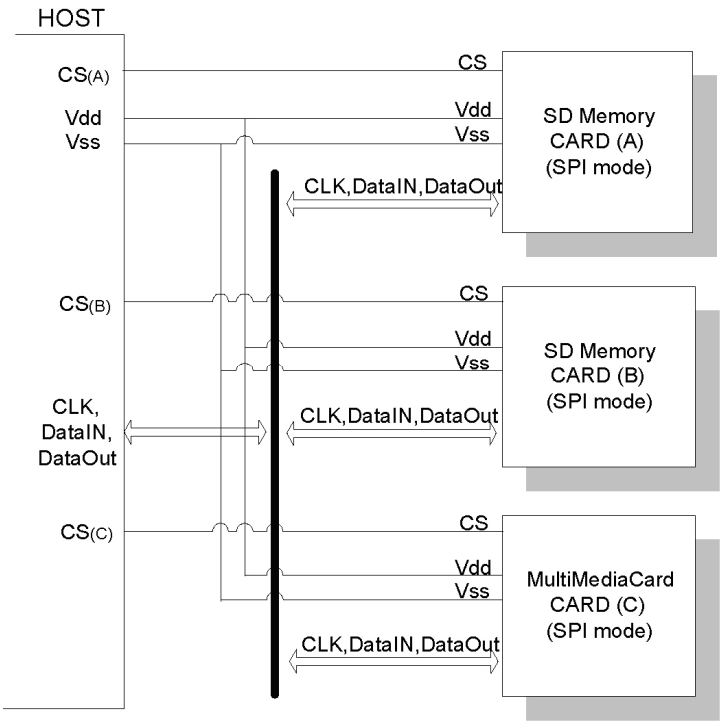

Figure 9: SPI Bus Topology

4.2.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.

The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.

During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is MultiMediaCard. In that case it should re-start the card as MultiMediaCard using CMD0 and CMD1.

4.3 Card Registers

The SD Card has six registers. Refer to the tables that follow for details.

Table 16: SD Card Registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD(CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address is SD Card mode.
DSR	16	Driver Stage Register	This register provides an optional function for the output driver condition.

Table 17: CID Register

Register Name	Bit Width	Description	Value
MID	8	Manufacture ID	0x51
OID	16	OEM/Application ID	0x53 60
PNM	40	Product Name	STEC (0X5354454320)
PRV	8	Product Version	1.0 (10)
PSN	32	Product Serial Number	---
—	4	Reserved	00
MDT	12	Manufacture Date	---
CRC	7	Check sum of CID contents	---
—	1	Not used; always=1	

Table 18: OCR Register

OCR bit position	VDD voltage window	OCR bit position	VDD voltage window
0-3	Reserved	15	2.7-2.8
4	1.6-1.7	16	2.8-2.9
5	1.7-1.8	17	2.9-3.0
6	1.8-1.9	18	3.0-3.1
7	1.9-2.0	19	3.1-3.2
8	2.0-2.1	20	3.2-3.3
9	2.1-2.2	21	3.3-3.4
10	2.2-2.3	22	3.4-3.5
11	2.3-2.4	23	3.5-3.6
12	2.4-2.5	24-30	Reserved
13	2.5-2.6	31	0=busy; 1=ready
14	2.6-2.7		

Table 19: CSD Register

Register Name	Bit Width	Description
CSD_STRUCTURE	2	CSD structure
—	6	Reserved
TAAC	8	Data read access time 1
NSAC	8	Data read access time 2 (CLK cycle)
TRAN_SPEED	8	Data transfer rate
CCC	12	Card command classes
READ_BL_LEN	4	Read data block length
READ_BL_PARTIAL	1	Partial blocks for read allowed
WRITE_BLK_MISALIGN	1	Write block misalignment
READ_BLK_MISALIGN	1	Read block misalignment
DSR_IMP	1	DSR implemented
—	2	Reserved
C_SIZE	12	Device size
VDD_R_CURR_MIN	3	VDD min read current
VDD_R_CURR_MAX	3	VDD max read current
VDD_W_CURR_MIN	3	VDD min write current
VDD_W_CURR_MAX	3	VDD max write current
C_SIZE_MULT	3	Device size multiplier
ERASE_BLK_EN	1	Erase single block enable
SECTOR_SIZE	7	Erase sector size
WP_GRP_SIZE	7	Write protect group size
WP_GRP_ENABLE	1	Write protect group enable
—	2	Reserved
R2W_FACTOR	3	Write speed factor
WRITE_BL_LEN	4	Write data block length
—	5	Reserved
FILE_FORMAT_GRP	1	File format group
COPY	1	Copy flag
PERM_WRITE_PROTECT	1	Permanent write protection
TMP_WRITE_PROTECT	1	Temporary write protection
FILE_FORMAT	2	File format
—	2	Reserved
CRC	7	Checksum of CSD contents
—	1	Always=1

Table 20: CSD Register values

Capacity	Register value
128MB	00 5E 00 32 5F 59 83 C9 ED B6 7F 83 96 40 00 65
256MB	00 5E 00 32 5F 59 83 CF ED B6 FF 87 96 40 00 3F
512MB	00 5E 00 32 5F 59 83 D2 ED B7 7F 8F 96 40 00 F7
1GB	00 5E 00 32 5F 59 83 D0 6D B7 FF 9F 96 40 00 8F
2GB	00 5E 00 32 5F 5A 83 D5 2D B7 FF BF 96 80 00 85

Table 21: SCR Register

Field	Bit Width
SCR_STRUCTURE	4
SD_SPEC	4
DATA_STAT_AFTER_ERASE	1
SD_SECURITY	3
SD_BUS_WIDTHS	4
Reserved	16
Reserved	32

5.0 Revision History

Revision	*Date*	*Description*
-101	10/12/07	Initial release
-102	10/19/07	Corrected AC parameters
-103	11/09/07	Added CID and CSD register values
-104	11/27/07	Styles applied for cleaner layout and easier editing.
-105	01/03/07	Reduced Program/Erase cycles to 300,000 for 1GB and 2GB.
-106	03/07/08	Contact information on last page updated.

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