128MB to 4GB
IDE Single Chip Drive

STEC

www.stec-inc.com

SLISCDxxx(M/G)M1U(I)-y

Capacity: 128MB - 4GB

ATA-5 Compatible

ATA Transfer modes:

- PIO 0-6, MWDMA 0-4

Supports TrueIDE and PC Card Memory and I/O Modes

Form Factors:

- 50-Ball Single Flash iSCD
- 50-Ball Stacked Flash iSCD

Endurance Guarantee of 2,000,000 Write/Erase Cycles

5V or 3.3V Power Supply

Commercial and Industrial Operating Temperature Range

5-Byte Detection, 4-Byte Correction ECC Engine

10 Year Data Retention

RoHS-6 Compliant

General Description and Key Features

STEC's flash storage adheres to the latest industry compliance and regulatory standards including UL, FCC, RoHS, and various compliance associations. Each device incorporates a proprietary state-of-the-art flash memory controller that provides the greatest flexibility to customer-specific applications while supporting key flash management features resulting in the industry's highest reliability and endurance. Key features include:

- Built-in ECC engine detects up to 5-byte and corrects up to 4-byte errors
- Sophisticated block management and wear leveling algorithms guarantees 2,000,000 write/erase cycles
- Power-down data protection ensures data integrity and errors in case of power loss
- Lifecycle management feature allows users to monitor the device's block management

STEC's IDE Single Chip Drive™ (iSCD) is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, ESD, and temperature. The rugged industrial design combined with industrial temperature (-40°C to 85°C) testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments.

In addition to custom hardware and firmware designs, STEC also offers value-added services including:

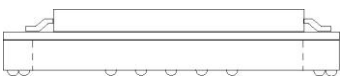
- Custom labeling and packaging
- Custom software imaging and ID strings
- Full BOM control and product change notification
- Total supply-chain management to ensure continuity of supply
- In-field application engineering to help customers through product design-ins

Ordering Information: IDE Single Chip Drive

Part Number	iSCD Factor	Capacity
SLISCD128MM1U(I)-y	y=A	128 Mbytes
SLISCD256MM1U(I)-y	y=A	256 Mbytes
SLISCD512MM1U(I)-y	y=A	512 Mbytes
SLISCD1GM1U(I)-y	y=A	1 GByte
SLISCD2GM1U(I)-y	y=A, B	2 GBytes
SLISCD4GM1U(I)-y	y=B	4 GBytes

Legend:

- **SLISCD =** STEC standard iSCD part number prefix.
- **(M/G) =** proceeding capacity (xxx) is in Megabytes (M) or Gigabytes (**G).**
- **M1 =** STEC Mach 1 controller.
- **U =** RoHS-6 compliant lead-free.
- **Part numbers without (I) =** Commercial temperature range (0ºC to 70ºC).
- **(I) =** Industrial temperature range (-40ºC to +85 ºC).
- y = A for Single Flash iSCD
- y= B for STEC patented IC Tower Stacked Flash iSCD



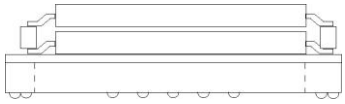


Table of Contents

1.0 Introduction

This datasheet includes the following sections:

- Product Specifications covers the most referenced specifications, such as mechanical dimensions, ball assignment, signal description, and performance.
- Flash Management explains the flash management algorithm and features, and Life Cycle Management feature.
- Environmental Specifications characterizes the recommended operating conditions, reliability, shock, vibration and humidity parameters and MTBF calculations.
- Electrical Specifications describes the absolute maximum ratings and AC/DC characteristics.
- Host Access Specifications describes the host access interface modes, Card Information Structure (CIS) and Identify Drive parameter information.
- Registers explains the ATA registers that are part of the Mach1 controller.
- Supported ATA commands reviews the commands that are supported by the Mach1 controller.
- Evaluating IDE Single Chip Drive describes how designers can evaluate the IDE Single Chip Drive before the hardware design is finalized.

Figure 1: IDE Single Chip Drive

2.0 Product Specifications

2.1 Mechanical Dimensions

2.1.1 IDE Single Chip Drive - Single Flash

Table 1 and Figure *2* show the mechanical dimensions of the IDE Single Chip Drive - Single Flash.

Table 1: Mechanical dimensions iSCD - Single Flash

Parameter	Value
Length	21.72 ± 0.15 mm (0.855 ±. 0.006 in)
Width	19.81 ± 0.15 mm (0.780 ± 0.096 in)
Height	3.60 ± 0.15 mm (0.142 ± 0.006 in)

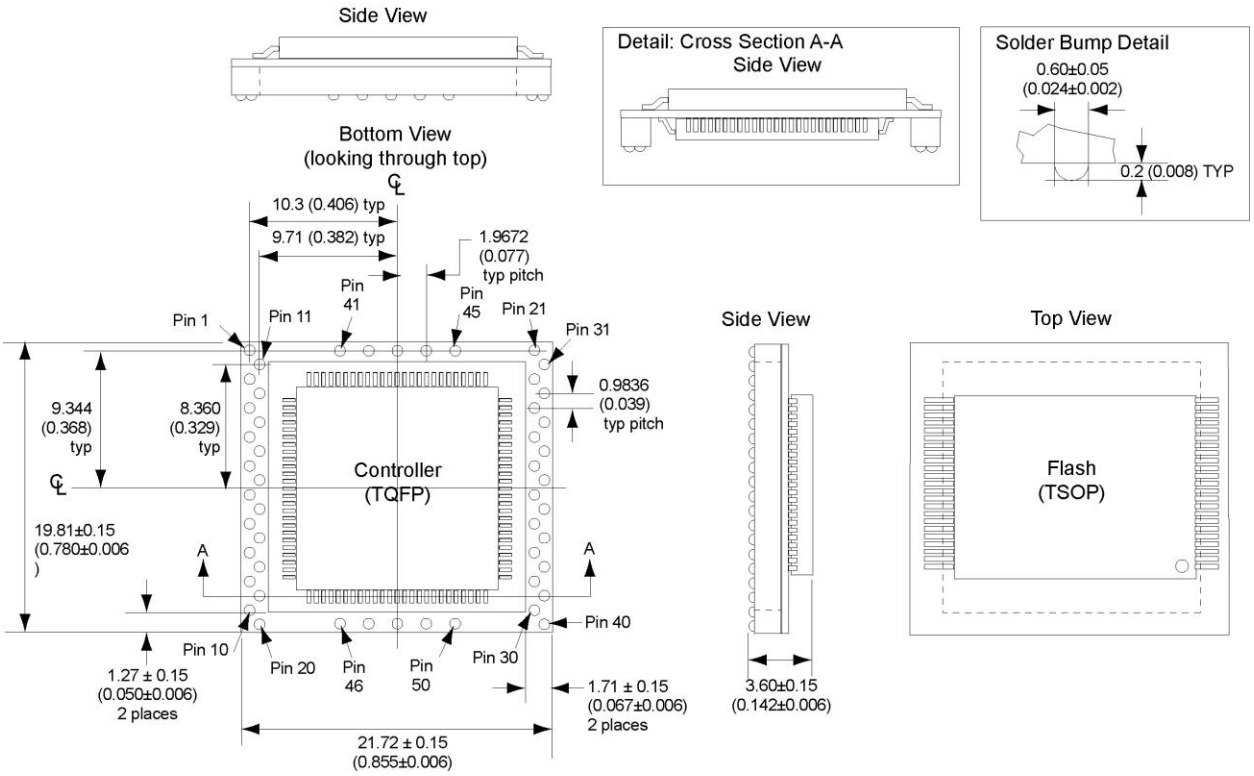


Figure 2: Mechanical dimensions iSCD - Single Flash

2.1.2 IDE Single Chip Drive - Stacked Flash

Table 2 and Figure 3 show the mechanical dimensions of the IDE Single Chip Drive – Stacked Flash.

Table 2: Mechanical dimensions iSCD – Stacked Flash

Parameter	Value
Length	21.72 ± 0.15 mm (0.855 ±. 0.006 in)
Width	19.81 ± 0.15 mm (0.780 ± 0.006 in)
Height	4.80 ± 0.15 mm (0.189 ± 0.006 in)

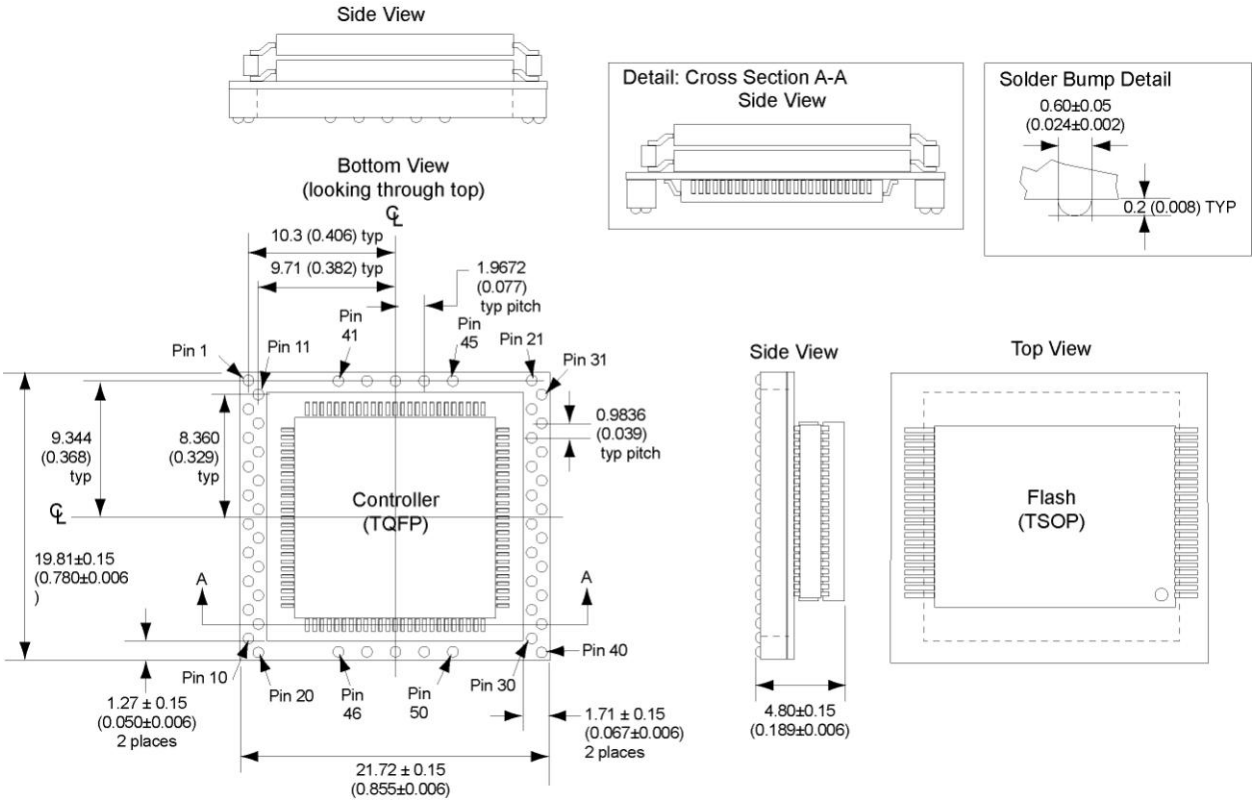


Figure 3: Mechanical dimensions iSCD – Stacked Flash

2.2 Pin Assignment

Note: It is recommended to add termination resistors on the board design, as per the recommendations in the ATA-5 specifications.

Table 3: iSCD Pin Assignment

Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type
1	NC	No Connect	26	A0	I
2	IORDY (-WAIT)	O	27	GND	Ground
3	-CSEL*	I	28	GND	Ground
4	-DMACK (-REG)	I	29	DMARQ (-INPACK)	O
5	-IORD*	I	30	D11	I/O
6	-CE1 (-CS0)	I	31	D10	I/O
7	D07	I/O	32	D9	I/O
8	D06	I/O	33	D8	I/O
9	D05	I/O	34	-PDIAG (-STSCHG) (BVD1)	I/O
10	D04	I/O	35	-DASP (-SPKR) (BVD2)	I/O
11	A2	I	36	A1	I
12	-RESET (RESET)	I	37	VCC	Power
13	INTRQ (-IREQ) (RDY/-BSY)	O	38	VCC	Power
14	-IOWR	I	39	D3	I/O
15	-CE2 (-CS1)	I	40	NC	No Connect
16	D15	I/O	41	A03	I
17	D14	I/O	42	A04	I
18	D13	I/O	43	A05	I
19	D12	I/O	44	A06	I
20	NC	No Connect	45	A07	I
21	NC	No Connect	46	A10	I
22	-IOIS16 (WP)	O	47	-OE (-ATASEL)	I
23	D2	I/O	48	A09	I
24	D1	I/O	49	A08	I
25	D0	I/O	50	-WE	I

Legend: "-" = Low active

2.3 Signal Descriptions

Table 4: iSCD Signal Descriptions

Signal Name	Type	Pin Number	Description
BVD2 (PC Card Memory Mode)	I/O	35	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product produces no audio.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15-D00 (PC Card Memory Mode)	I/O	16, 17, 18, 19, 30, 31, 32, 33, 7, 8, 9, 10, 39, 23, 24, 25	These lines carry the data, commands, and host and the controller. D00 is the LSB of the LSB of the Odd Byte of the Word.
D15-D00 PC Card I/O Mode			This signal is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode)	I	14	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data onto the data bus and into the controller registers. The clocking occurs on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IORD (PC Card Memory Mode)	I	5	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the iSCD.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-WE (PC Card Memory Mode)	I	50	This is a signal driven by the host and used for strobing memory write data into the registers. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC.
-OE (PC Card Memory Mode)	I	47	This is an Output Enable strobe generated by the host interface. It is used to read data from the iSCD in PC Card Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATASEL (True IDE Mode)			To enable True IDE Mode, this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	13	In Memory Mode, this signal is set high when the iSCD is ready to accept a new data transfer operation and held low when the iSCD is busy. The host must provide a pull-up

Signal Name	Type	Pin Number	Description
			resistor. At power up and at reset, the RDY/-BSY signal is held low (busy) until the iSCD completes its power up or reset function. No access of any type should be made to the iSCD during this time. The RDY/-BSY signal is held high (disabled from being busy) when the iSCD is powered up with RESET continuously disconnected or asserted high.
-IREQ (PC Card I/O Mode)			After the iSCD has been configured for I/O operation, this signal is used as the active low interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high interrupt request to the host.
A10-A0 (PC Card Memory Mode)	I	46, 48, 49, 45, 44, 43, 42, 41, 11, 36, 26	These address lines along with the -REG signal are used to select the following: the I/O port address registers within the iSCD, the memory mapped port address registers within the iSCD, a byte in the CIS and the Configuration Control and Status Registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2-A0 (True IDE Mode)		11, 36, 26	In True IDE Mode only, A2:A0 are used to select the one of eight registers in the Task File. The remaining address lines should be grounded.
-CE1, -CE2 (PC Card Memory Mode Card Enable	I	6, 15	These input signals are used both to select the iSCD and to indicate to the iSCD whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8-bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the iSCD Control Register.
-CSEL (PC Card Memory Mode)	I	3	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			To configure the iSCD as a Master, pull down this signal to GND via a 10kΩ resistor. To configure the iSCD as a Slave, pull up this signal to VCC through 10kΩ resistor
-REG (PC Card Memory Mode) Attribute Memory Select	I	4	This signal distinguishes between accesses to Common Memory (high) and Register Attribute Memory (low).
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the bus.
-DMACK (not used for part numbers with P) (True IDE Mode)			In True IDE Mode this input signal is used by host in response to DMARQ to initiate DMA transfers.
WP (PC Card Memory Mode) Write Protect	O	22	The iSCD does not have a write protect switch; therefore, this signal is held low after the completion of the reset initialization sequence.

Signal Name	Type	Pin Number	Description
-IOIS16 (PC Card I/O Mode)			A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			Not defined in IDE Mode.
-INPACK (PC Card Memory Mode)	O	29	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the iSCD when it is selected and responding to an I/O read cycle at the address that is on the bus. The host uses this signal to control the enable of any input data buffers between the iSCD and the host's CPU.
DMARQ (Not used for part numbers with P) (True IDE Mode)			In True IDE Mode this signal is asserted by the iSCD when it is ready to transfer data to/from the host. Data direction is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK.
BVD1 (PC Card Memory Mode)	I/O	34	This signal is asserted high as since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states. Its use is controlled by the Configuration and Status Register.
-PDIAG (True IDE Mode)			In True IDE Mode, this input/output signal is the Pass Diagnostic signal in the Master/Slave handshake protocol.
-WAIT (PC Card Memory Mode)	O	2	This signal is not used by the iSCD, and is pulled up to VCC through a 4.7K ohm resistor.
-WAIT (PC Card I/O Mode)			This signal is not used by the iSCD, and is pulled up to VCC through a 4.7K ohm resistor.
IORDY (True IDE Mode)			This signal is not used by the iSCD, and is pulled up to VCC through a 4.7K ohm resistor.
GND (PC Card Memory Mode)	GND	27, 28	Ground
GND (PC Card I/O Mode)			Ground
GND (True IDE Mode)			Ground
VCC (PC Card Memory Mode)	VCC	37, 38	+5 V or 3.3V power
VCC (PC Card I/O Mode)			+5 V or 3.3V power
VCC (True IDE Mode)			+5 V or 3.3V power
RESET (PC Card Memory Mode)	I	12	When RESET is high, this signal resets the iSCD. The iSCD is reset only at power up if this signal is left high or open from power-up. The iSCD can also be reset when the soft reset bit in the Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
-VS1 -VS2 (True IDE Mode)			This signal is not used in IDE Mode.

2.4 Performance

Table 5: iSCD Read/Write Performance

Parameter	Value
Data transfer rate to/from host	25 MBytes/s (burst)
Sustained read	up to 10 MBytes/s
Sustained write	up to 7 MBytes/s

2.5 CHS Parameters

Table 6: CHS Parameters per capacity

Capacity	Cylinder (C) (standard)	Head (H)	Sectors/Track (S)
128MB	980	8	32
256MB	980	16	32
512MB	993	16	63
1GB	1,986	16	63
2GB	3,970	16	63
4GB	7,964	16	63

2.6 TrueIDE/PC Card Mode

The iSCD is shipped with default configuration for PC Card Mode. The -ATASEL signal can be used to set the IDE Single Chip Drive into TrueIDE mode, as described in Table 7 below.

Table 7: TrueIDE/PC Card Memory Mode

Configuration	-ATASEL signal (Ball 47)
TrueIDE mode	Pulled down to GND through 0Ω resistor
PC Card Mode (default)	Open

2.7 Master/Slave Cable Select

If the iSCD is set into TrueIDE mode via a pull-down resistor, as described in *2.6 TrueIDE/PC Card Mode*, the Master/Slave setting needs to be set too. The Cable Select signal (-CSEL) is used to configure the iSCD as a Master or Slave IDE device, as described in Table 8 below.

Table 8: Master/Slave configuration

Configuration	-CSEL signal (Ball 3)
Master	Pulled down to GND through 10kΩ resistor
Slave	Pulled up to VCC through 10kΩ resistor

2.8 Standards Compliance

STEC products specified in this document are certified for compliance with the following industry standards:

- PCMCIA v7.0
- UL 950
- CE, and FCC Class B & D
- RoHS

2.8.1 CE and FCC Class B & D

The STEC products specified in this document meet the following requirements and limits of the European Standards:

- **Class B** requirements of the following European Standard:

  EN 55022: 1998 – “Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement”

- **Class D** limits of the following European Standards:

  EN 61000-3-2 “Electromagnetic compatibility (EMC) Part 3-2: Limits – Limits for harmonic current emissions (equipment input current up to and including 16 A per phase)”

  EN 61000-3-3: 1995 – “Part 3: Limits – Section 3: Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with rated current <= 16A”

  EN 55024 – “Information technology equipment – Immunity characteristics – Limits and methods of measurement”

2.8.2 RoHS

STEC certifies that its products do not contain any of the restricted substances as stated below and are in compliance with RoHS EU directive 2002/95/EC, specifically:

- Mercury (Hg)
- Cadmium Cd)
- Chromium VI (Cr +6)
- Polybrominated biphenyl (PBB)
- Polybrominated biphenyl ether (PBDE)
- Lead (Pb)

Materials used in the STEC's products are limited to the following:

- Steel, Nylon 6/6, PCB laminate
- Copper, Gold, Nickel
- Silicon on ICs and Components
- Polyester on Labels

3.0 Flash Management

3.1 Overview

Since the IDE Single Chip Drive provides a standard IDE interface to the host, no software integration is required, providing the shortest time-to-market for design engineers.

The firmware of the embedded Mach1 controller contains STEC's advanced flash memory management algorithms to ensure the most optimum device performance, reliability and endurance. It was designed to maximize the benefits of flash memory, while at the same time overcoming inherent NAND flash limitations. Implemented in firmware are the below features:

- Flash file system management
- Bad-block management
- Dynamic Wear-leveling
- Power failure management
- Performance optimization

3.2 Bad Block Management

Inherent to NAND flash technology are areas (blocks) on the media that cannot be used for storage because of their high error rate. These so-called "bad blocks" are already identified by the flash vendor during manufacturing, but can also be accumulated over time during device operation.

The Mach1 controller contains a table that lists all the bad blocks on the device (Bad Block Table), and automatically maps out these blocks upon system initialization. During device operation it ensures that newly accumulated bad blocks are also mapped out and added to the Bad Block Table.

Bad block management is 100% transparent to the host application, which will not be aware of the location or existence of bad blocks on the media.

3.3 Wear Leveling

The SLC NAND flash devices that are being used in the IDE Single Chip Drive are guaranteed for 100,000 Write/Erase cycles per block. This means that after approximately 100,000 erase cycles, the erase block has a higher probability for errors than the error rate that is typical to the flash. While 100,000 write/erase cycles may be good for consumer data storage, such as digital cameras, MP3 players, etc., it is not sufficient for industrial and embedded applications where data is constantly written to the device and long product life is required.

For example, operating systems that use a file system, will update the File Allocation Table (FAT) every time a write is done to the device. Without any wear leveling in place, the area on the flash where the FAT table is located would wear out faster than other areas, reducing the lifetime of the entire flash device.

To overcome this limitation, the flash management algorithm needs to make sure that each block in the device ages, i.e. is “worn out”, at the same rate. The built-in wear leveling scheme makes sure that with every write to the flash, the youngest block is used. This ensures that the full flash media is used uniformly, so that one area of the flash will not reach the endurance limits prematurely before other areas. The implemented wear leveling algorithm ensures a minimum of 2 million write/erase cycles for the entire flash media.

3.4 Error Correction/Detection

The Mach1 controller implements an advanced Error Correction/Detection scheme, based on the Reed-Solomon algorithm. The ECC engine can detect up to 5 bytes and correct up to 4 bytes per 512 bytes (symbol based). To ensure the fastest performance, both detection and correction are done on-the-fly, in hardware only.

Each time the host application writes a sector of 512 bytes to the iSCD, a unique ECC signature is created by the ECC engine and written together with the data to the flash. When the data is read back by the host, the ECC engine creates again a unique ECC signature. It will then compare the original written signature with the newly created signature, and sets an error flag if the two signatures are not the same. Correction of the data is done on-the-fly when the error flag is set, and the data presented to the host will be the same as the original written data. This powerful Error Correction/Detection scheme results in an overall error rate of less than 1 in 10^{14} bits, read.

3.5 Power Failure Management

The embedded flash management software uses algorithms that ensure data integrity, even during power failures. After each write, a *verify write flag* is set in the extra area of the flash page, while a *dismount flag* is set for the whole device during regular power-down. When a power failure occurs, both the *verify write* and the *dismount flag* will not be set, indicating a power failure during a write or erase operation. Upon the next power-up, the mapping tables will be reconstructed from the information stored in the flash memory, and the last version of the sector with a correct *verify write flag* will be used.

This mechanism ensures complete data integrity. When writing, copying, or erasing the flash device, the data format remains valid at all intermediate stages. Old data is never erased until the *verify write flag* of the new sector has been set. Therefore, a data sector cannot exist in a partially written state. The operation is either successfully completed (*verify write flag* is set) and the new data is valid, or the operation has not yet been completed or has failed, in which case the old sector contents remain valid.

3.6 Life Cycle Management

The flash management algorithm monitors the program/erase operations of the flash device so that bad blocks resulting from wear, etc. can be marked, mapped, and retired and then replaced with a reserved ‘good block’. The number of spare good blocks is approximately 2% of the usable capacity of the flash media at the time of manufacturing. For reference; a 1GB IDE Single Chip Drive contains about 8000

usable blocks and about 160 spare blocks at the time of manufacturing. Block size is 128KB for current SLC NAND flash technology. The flash media will last as long as there are spare blocks available for replacing the bad blocks that are generated due to wear-out of the flash. Once all of the spare blocks are exhausted, data can no longer be written to the device, and the IDE Single Chip Drive turns into a read-only storage device. This typically happens after many years of operation and is primarily affected by the usage pattern and the application in which the device is used.

Monitoring the spare block count is a particularly effective way to determine the approximate amount of useful life remaining on the IDE Single Chip Drive. The Life Cycle Management feature does just that. The LCM feature is implemented as a vendor unique ATA command. Please refer to Application Note *AN-7003 Life Cycle Management Features for Mach1 Flash products* for full details on implementing this ATA command.

4.0 Environmental Specifications

4.1 Recommended Operating Conditions

Table 9: iSCD Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Commercial Operating Temperature	Ta	0	25	70	°C
Industrial Operating Temperature	Ta	-40	-	85	°C
VCC voltage 5.0	VCC5	4.75	5.0	5.25	V
VCC voltage 3.3	VCC3.3	3.18	3.3	3.465	V

4.2 Reliability

Table 10: iSCD Endurance & Data Reliability

Parameter	Value
Endurance	2,000,000 Write/Erase Cycles
Data reliability	1 in 10^{14} bits, read
Data retention	10 years

4.3 Shock, Vibration, and Humidity

Table 11: iSCD Shock, Vibration & Humidity

Parameter	Value
Shock	1.5K G peak, 0.5ms pulse duration, five (5) pulses per each of six (6) directions (per JEDEC JESD22 standard, method B110)
Vibration	20 G peak, 20Hz-2000Hz, 4 cycles per direction (per JEDEC JESD22 standard, method B103)
Humidity	85°C 85% RH, 500 hrs

4.4 Electrostatic Discharge (ESD)

The IDE Single Chip Drive has been tested and approved for immunity from ESD under the conditions described in Table 12 below.

Table 12: ESD Rating for IDE Single Chip Drive

ESD Type	Value (KV)
Air	2, 4, 8
Contact	2, 4

4.5 Mean Time Between Failure (MTBF)

STEC estimates Mean Time Between Failure (MTBF), using a prediction methodology based on reliability data for the individual components in the IDE Single Chip Drive. Table 13 below summarizes the prediction results for the IDE Single Chip Drive, based on the following two methodologies:

- Telcordia Special Report SR-332, Reliability Prediction Procedure for Electronic Equipment.
- MIL-HNBK-217

The analysis was performed using Relex Software.

Table 13: IDE Single Chip Drive MTBF

Product	Condition	MTBF (hours)
SLISCD128MM1U-A	Telcordia SR-332, GB, 25°C, MIL-HNBK-217	> 8,000,000
SLISCD2GM1U-A	Telcordia SR-332, GB, 25°C, MIL-HNBK-217	> 8,000,000
SLISCD4GM1U-B	Telcordia SR-332, GB, 25°C, MIL-HNBK-217	>7,000,000

5.0 Electrical Specifications

Absolute Maximum Ratings

Table 14: iSCD Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage	Vin, Vout	-0.5 to VCC +0.5	V
Storage temperature range	Tstg	-65 to +150	°C

5.1 DC Characteristics

Measurements at Recommended Operating Conditions unless otherwise specified.

Table 15: iSCD DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
VIL	Input LOW Voltage	-0.3	+0.8	V	VCC=3.3V or 5.0V
VIH	Input HIGH Voltage	2.0	VCC +0.3	V	VCC=3.3V or 5.0V
VOL3.3	Output LOW Voltage 3.3		0.45	V	VCC=3.3V
VOL5	Output LOW Voltage 5		0.8		VCC=5.0V
VOH	Output HIGH Voltage	2.4		V	VCC=3.3V or 5.0V
ICCSB	Standby Mode		2	mA	ICC at VCC=3.3V or 5.0V
ICC	Operating Current		75	mA	ICC at VCC=3.3V or 5.0V; Operating current measured with 2-way interleaving.
ILI	Input Leakage Current		10	µA	VCC=3.3V or 5.0V
ILO3.3	Output Leakage Current 3.3		1	µA	VCC=3.3V
ILO5	Output Leakage Current 5		2	µA	VCC= 5.0V
CI/O	Input/output Capacitance		25	pF	VCC=3.3V or 5.0V

5.2 AC Characteristics

Measurements at Recommended Operating Conditions, unless otherwise specified.

5.2.1 PC Card Memory Mode Attribute Memory Read

Table 16: PC Card Memory Mode Attribute Memory Read AC Characteristics

Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read Cycle Time	tc(R)	tAVAV	250	
Address Access Time	ta(A)	tAVQV		250
Card Enable Access Time	ta(CE)	tELQV		250
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from -CE	tdis(CE)	tEHQZ		100
Output Disable Time from -OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from -CE	ten(CE)	tELQNZ	5	
Output Enable Time from -OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	
Address Hold Time	th(A)	—	20	
-CE Setup Time	tsu(CE)	—	0	
-CE Hold Time	th(CE)	—	20	

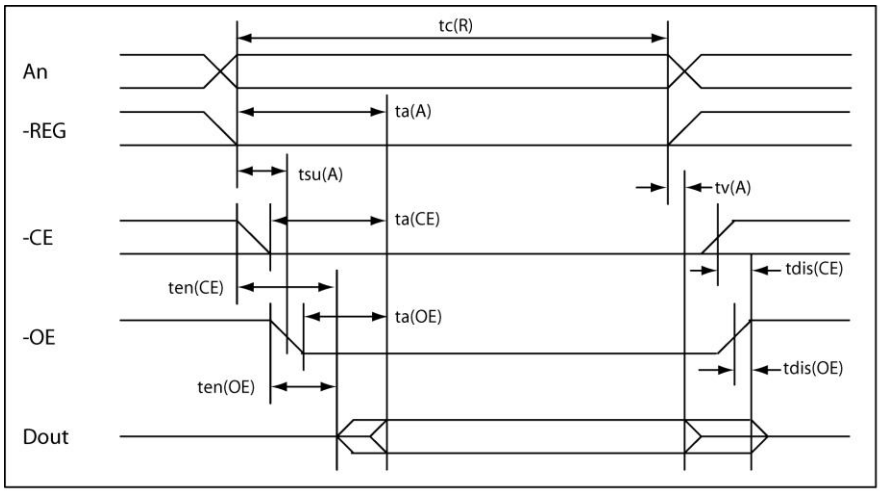


Figure 4: PC Card Memory Mode Attribute Memory Read Timing Diagram

5.2.2 PC Card Memory Mode Attribute Memory Write

Table 17: PC Card Memory Mode Attribute Memory Write AC Characteristics

Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Address Setup Time (-WE)	tsu(A-WEH)	—	180	
-CE Setup Time (-WE)	tsu(CE-WEH)	—	180	
Data Setup Time (-WE)	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Output Disable Time (-WE)	tdis(WE)	—		100
Output Disable Time (-OE)	tdis(OE)	—		100
Output Enable Time (-WE)	ten(WE)	—	5	
Output Enable Time (-OE)	ten(OE)	—	5	
Output Enable Setup Time (-WE)	tsu(OE-WE)	—	10	
Output Enable Hold Time (-WE)	th(OE-WE)	—	10	
-CE Setup Time	tsu(CE)	—	0	
-CE Hold Time	th(CE)	—	20	

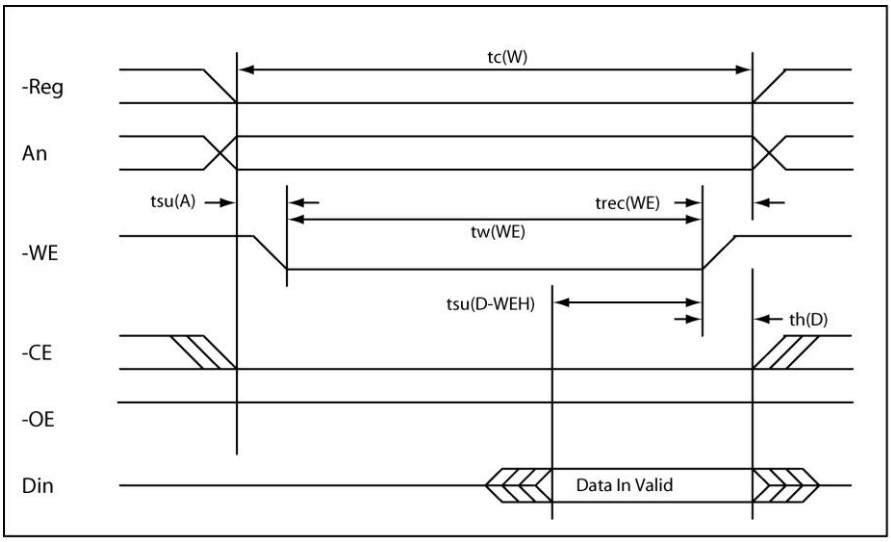


Figure 5: PC Card Memory Mode Attribute Memory Write Timing Diagram

5.2.3 PC Card Memory Mode Common Memory Read

Table 18: PC Card Memory Mode Common Memory Read AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Output Enable Access Time (max)	ta(OE)	tGLQV	125	60	50	45
Output Disable Time from OE (max)	tdis(OE)	tGHQZ	100	60	50	45
Address Setup Time (min)	tsu(A)	tAVGL	30	15	10	10
Address Hold Time (min)	th(A)	tGHAX	20	15	15	10
CE Setup before OE (min)	tsu(CE)	tELGL	0	0	0	0
CE Hold following OE (min)	th(CE)	tGHEH	20	15	15	10
Wait Delay Falling from OE (max)	tv(WT-OE)	tGLWTV	35	35	35	N/A
Data Setup for Wait Release (max)	tv(WT)	tQVWTH	0	0	0	N/A
Wait Width Time (max)	tw(WT)	tWTLWTH	350	350	350	N/A

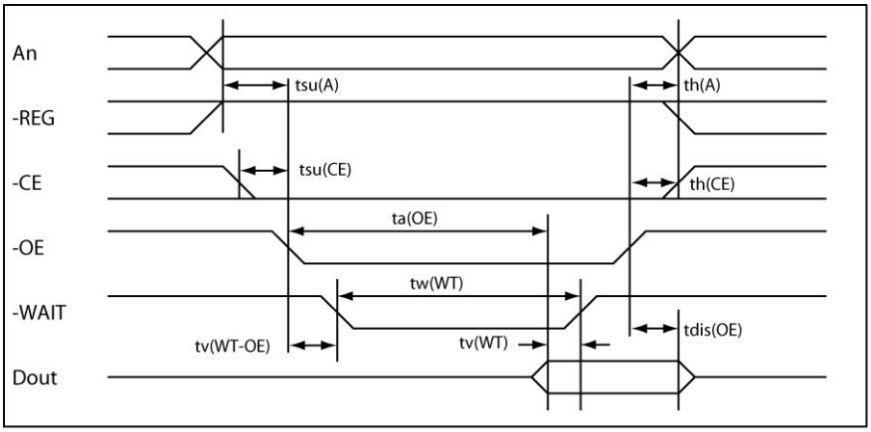


Figure 6: PC Card Memory Mode Common Memory Read Timing Diagram

5.2.4 PC Card Memory Mode Common Memory Write

Table 19: PC Card Memory Mode Common Memory Write AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80ns Cycle Time Mode
Data Setup before WE (min)	tsu (D-WEH)	tDVWH	80	50	40	30
Data Hold following WE (min)	th(D)	tWMDX	30	15	10	10
WE Pulse Width (min)	tw(WE)	tWLWH	150	70	60	55
Address Setup Time (min)	tsu(A)	tAVWL	30	15	10	10
CE Setup before WE (min)	tsu(CE)	tELWL	0	0	0	0
Write Recovery Time (min)	trec(WE)	tWMAX	30	15	15	15
Address Hold Time (min)	th(A)	tGHAX	20	15	15	15
CE Hold following WE (min)	th(CE)	tGHEH	20	15	15	10
Wait Delay Falling from WE (max)	tv(WT-WE)	tWLWTV	35	35	35	N/A
WE High from Wait Release (min)	tv(WT)	tWTHWH	0	0	0	N/A
Wait Width Time (max)	tw(WT)	wWTLWTH	350	350	350	N/A

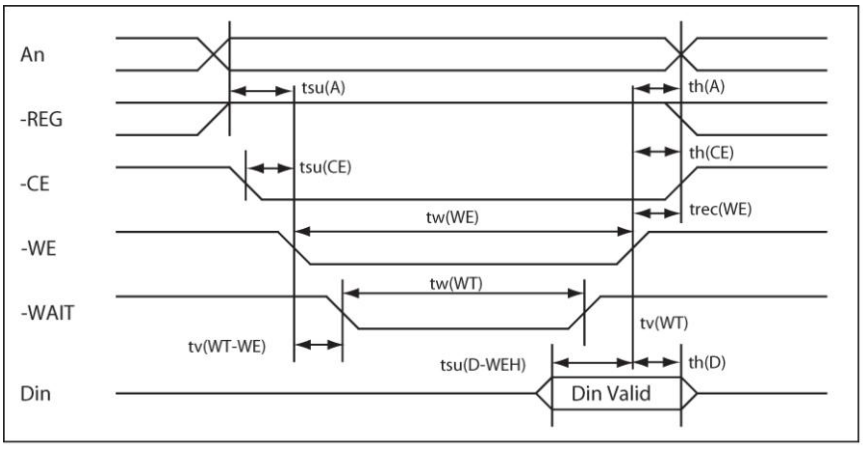


Figure 7: PC Card Memory Mode Common Memory Write Timing Diagram

5.2.5 PC Card I/O Mode Read AC Characteristics

Table 20: PC Card I/O Mode Read AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Data Delay after -IORD (max)	td(IORD)	tIGLQV	100	50	50	45
Data Hold following -IORD (min)	th(IORD)	tIGHQX	0	5	5	5
-IORD Width Time (min)	tw(IORD)	tIGLIGH	165	70	65	55
Address Setup before -IORD (min)	tsuA(IORD)	tAVIGL	70	25	25	15
Address Hold following -IORD (min)	thA(IORD)	tIGHAX	20	10	10	10
-CE Setup before -IORD (min)	tsuCE(IORD)	tELIGL	5	5	5	5
-CE Hold following -IORD	thCE(IORD)	tIGHEH	20	10	10	10
-REG Setup before -IORD (min)	tsuREG(IORD)	tRGLIGL	5	5	5	5
-REG Hold following –IORD (min)	thREG(IORD)	tIGHRGH	0	0	0	0

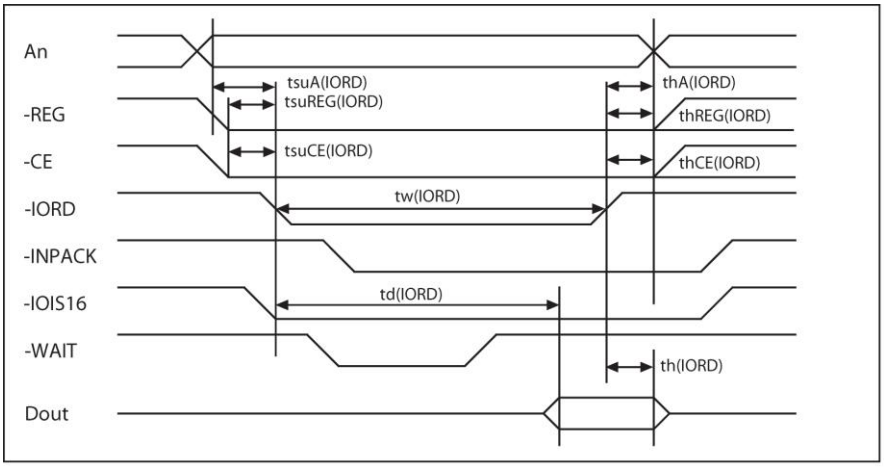


Figure 8: PC Card I/O Mode Read Timing Diagram

5.2.6 PC Card I/O Mode Write AC Characteristics

Table 21: PC Card I/O Mode Write AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Data Setup before -IOWR (min)	tsu(IOWR)	tDVIWH	60	20	20	15
Data Hold following -IOWR (min)	th(IOWR)	tIWHDX	30	10	5	5
-IOWR Width Time (min)	tw(IOWR)	tIWLIWH	165	70	65	55
Address Setup before -IOWR (min)	tsuA(IOWR)	tAVIWL	70	25	25	15
Address Hold following –IOWR (min)	thA(IOWR)	tIWHAX	20	20	10	10
-CE Setup before -IOWR (min)	tsuCE(IOWR)	tELIWL	5	5	5	5
-CE Hold following -IOWR (min)	thCE(IOWR)	tIWHEH	20	20	10	10
-REG Setup before -IOWR (min)	tsuREG(IOWR)	tRGLIWL	5	5	5	5
-REG Hold following -IOWR (min)	thREG(IOWR)	tIWHRGH	0	0	0	0

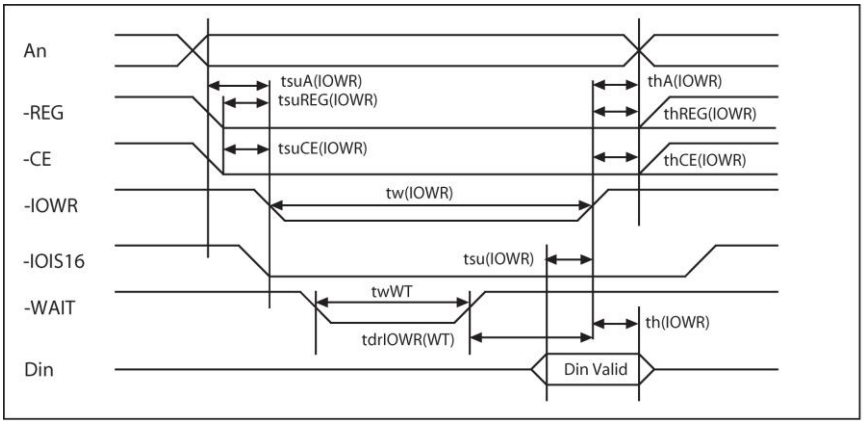


Figure 9: PC Card I/O Mode Read Timing Diagram

5.2.7 True IDE Mode Register Access

Table 22: True IDE Mode Register Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Cycle time (min)	t0	600	383	330	180	120	100	80	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	15	10	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	65	55	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	25	20	ns
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	ns
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	ns
-IORD data setup (min)	t5	50	35	20	20	20	15	10	ns
-IORD data hold (min)	t6	5	5	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	20	20	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	N/A	N/A	ns
Address valid to -IOCS16 release (max)	t8	60	45	30	N/A	N/A	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	ns

5.2.8 True IDE Mode PIO Access

Table 23: True IDE Mode PIO Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Cycle time (min)	t0	600	383	330	180	120	100	80	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	15	10	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	65	55	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	25	20	ns
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	ns
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	ns
-IORD data setup (min)	t5	50	35	20	20	20	15	10	ns
-IORD data hold (min)	t6	5	5	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	20	20	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	N/A	N/A	ns
Address valid to -IOCS16 release	t8	60	45	30	N/A	N/A	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	ns

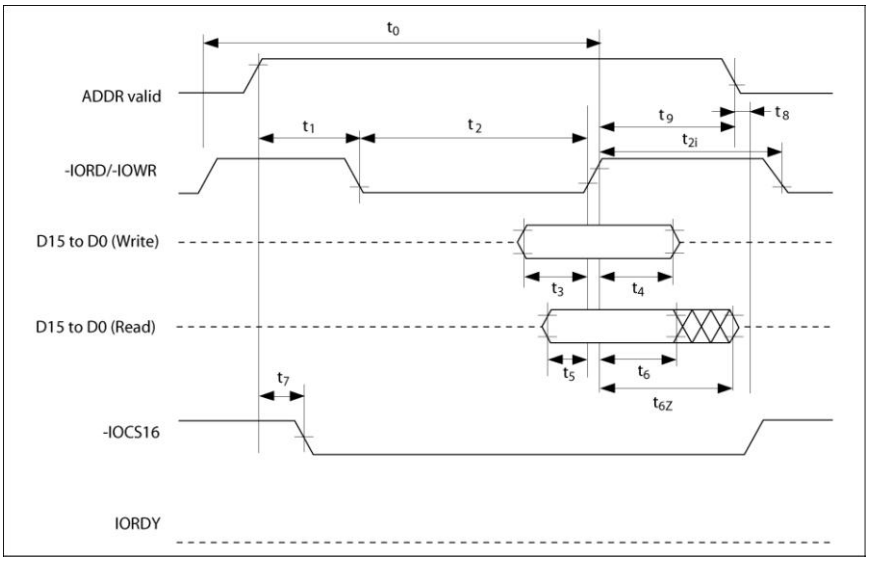


Figure 10: True IDE Mode PIO Access Timing Diagram

5.2.9 True IDE Mode Multiword DMA

Table 24: True IDE Mode Multiword DMA AC Characteristics

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Cycle time (min)	t_0	480	150	120	100	80	ns
-IORD/-IOWR Asserted Pulse (min)	t_D	215	80	70	65	55	ns
-IORD data access (max)	t_E	150	60	50	50	45	ns
-IORD data hold (min)	t_F	5	5	5	5	5	ns
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10	ns
-IOWR data hold (min)	t_H	20	15	10	5	5	ns
DMACK to -IORD/-IOWR setup (min)	t_I	0	0	0	0	0	ns
-IORD/-IOWR to DMACK hold (min)	t_J	20	5	5	5	5	ns
-IORD negated pulse width (max)	t_{KR}	50	50	25	25	20	ns
-IOWR negated pulse width (min)	t_{KW}	215	50	25	25	20	ns
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35	ns
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35	ns

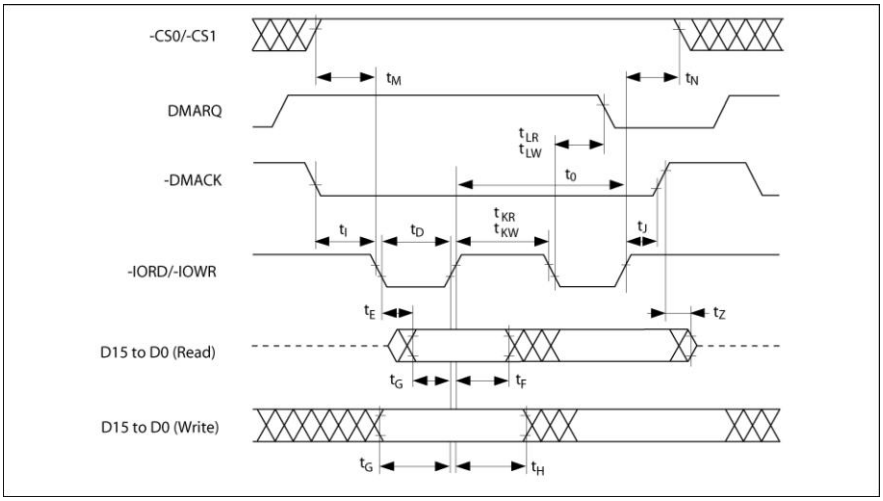


Figure 11: True IDE Mode Multiword DMA Timing Diagram

6.0 Host Access Specification

6.1 Task File Register and Byte/Word/Odd-Byte Mode Mappings

Please refer to the iSCD standards for complete details on:

- Task File Register mapping for the interface modes
- Byte/Word/Odd-byte mode mapping within each of the interface modes

6.2 Host Access Interface Modes

The host can access the iSCD by using the following interface modes with the Task Registers:

1. *PC Card Memory Mode, Attribute Memory*
   The Card Information Structure (CIS) in Attribute Memory can be accessed by Byte/Word/Odd-byte modes in PC Card Memory Mode. The -REG signal must be asserted when accessing Attribute Memory. The iSCD is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register. An example of a CIS is listed in *6.3 Card Information Structure (CIS).*

2. *PC Card Memory Mode, Common Memory*
   Common Memory can be accessed in the Byte/Word/Odd Byte modes in PC Card Memory Mode. The -REG signal must be de-asserted when accessing the Common Memory. The iSCD is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register

3. *PC Card I/O Mode*
   The iSCD can be accessed by Byte/Word/Odd Byte modes in PC Card I/O Mode. The iSCD is mapped to PC Card I/O Mode by the Index bits in the Configuration Option Register. The Index bits also select Contiguous I/O, Primary I/O, or Secondary I/O mapping when using the PC Card I/O Mode.

4. *True-IDE mode*
   The iSCD is configured in a True IDE Mode of operation when the -ATASEL input signal is asserted GND by the host at power up. In the True IDE Mode, Attribute Registers are not accessible from the host. The Data Register is accessed in word (16-bit) mode at power up. The iSCD permits 8-bit accesses if the host issues a Set Feature Command to put the iSCD in 8-bit mode. Parameter information that the iSCD uses in True IDE mode is returned when the Identify Drive command (ECh) is invoked. Refer *to 6.4 Identify Drive Parameter Information* for an example.

6.3 Card Information Structure (CIS)

The iSCD uses a Card Information Structure (CIS) as summarized below:

1. 0000: Code 01, link 03
   D9 01 FF
   Tuple CISTPL_DEVICE (01), length 3 (03) at offset 0
   - Device type is FUNCSPEC
   - Device speed is 250ns
   - Write protect switch is not in control
   - Device size is 2K bytes
2. 0005: Code 1C, link 04
   03 D9 01 FF
   Tuple CISTPL_DEVICE_OC (1C), length 4 (04) at offset 5
   - Device conditions: minimum cycle with WAIT at Vcc = 3.3V
   - Device type is FUNCSPEC
   - Device speed is 250ns
   - Write protect switch is not in control
   - Device size is 2K bytes
3. 000B: Code 18, link 02
   DF 01
   Tuple CISTPL_JEDEC_C (18), length 2 (02) at offset B
   - Device 0 JEDEC id: Manufacturer DF, ID 01
4. 000F: Code 20, link 04
   4D 01 00 01
   Tuple CISTPL_MANFID (20), length 4 (04) at offset F
   - Manufacturer # 0x014D hardware rev 1.00
5. 0015: Code 15, link 13
   04 01 53 54 49 00 46 6C 61 73 68 20 37 2E 30 2E 30 00 FF
   Tuple CISTPL_VERS_1 (15), length 19 (13) at offset 15
   - Major version 4, minor version 1
   - Product Information: "STI" (Manufacuturer) "Flash X.Y.Z" (Product Name)
6. 002A: Code 21, link 02
   04 01
   Tuple CISTPL_FUNCID (21), length 2 (02) at offset 2A
   - Function code 04 (Fixed), system init 01
7. 002E: Code 22, link 02
   01 01
   Tuple CISTPL_FUNCE (22), length 2 (02) at offset 2E
   - This is an PC Card ATA Disk

8. 0032: Code 22, link 03
   02 0C 0F
   Tuple CISTPL_FUNCE (22), length 3 (03) at offset 32
   - Vpp is not required
   - This is a silicon device
   - Identify Drive Model/Serial Number is guaranteed unique
   - Low-Power Modes supported: Sleep Standby Idle
   - Drive automatically minimizes power
   - All modes include 3F7 or 377
   - Index bit is not supported
   - -IOIS16 is unspecified in Twin configurations
9. 0037: Code 1A, link 05
   01 03 00 02 0F
   Tuple CISTPL_CONFIG (1A), length 5 (05) at offset 37
   - Last valid configuration index is 3
   - Configuration Register Base Address is 200
   - Configuration Registers Present:
     - Configuration Option Register at 200
     - Card Configuration and Status Register at 202
     - Pin Replacement Register at 204
     - Socket and Copy Register at 206
10. 003E: Code 1B, link 08
    C0 C0 A1 01 55 08 00 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 8 (08) at offset 3E
    - Configuration Table Index is 00 (default)
    - Interface type is Memory
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support required
    - Vcc Power Description: Nom V = 5.0 V
    - Map 2048 bytes of memory to iSCD address 0
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
11. 0048: Code 1B, link 06
    00 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 48
    - Configuration Table Index is 00
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

12. 0050: Code 1B, link 0A
    C1 41 99 01 55 64 F0 FF FF 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length10 (0A) at offset 50 10 (0A) at offset 50
    - Configuration Table Index is 01 (default)
    - Interface type is I/O
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support not required
    - Vcc Power Description: Nom V = 5.0 V
    - Decode 4 I/O lines, bus size 8 or 16
    - IRQ may be shared, pulse and level mode interrupts are supported
    - Interrupts in mask FFFF are supported
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
13. 005C: Code 1B, link 06
    01 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 5C
    - Configuration Table Index is 01
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA
14. 0064: Code 1B, link 0F
    C2 41 99 01 55 EA 61 F0 01 07 F6 03 01 EE 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 64
    - Configuration Table Index is 02 (default)
    - Interface type is I/O
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support not required
    - Vcc Power Description: Nom V = 5.0 V
    - Decode 10 I/O lines, bus size 8 or 16
    - I/O block at 01F0, length 8
    - I/O block at 03F6, length 2
    - IRQ may be shared, pulse and level mode interrupts are supported
    - Only IRQ14 is supported
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
15. 0075: Code 1B, link 06
    02 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 75
    - Configuration Table Index is 02
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

16. 007D: Code 1B, link 0F
    C3 41 99 01 55 EA 61 70 01 07 76 03 01 EE 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 7D
    - Configuration Table Index is 03 (default)
    - Interface type is I/O
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support not required
    - Vcc Power Description: Nom V = 5.0 V
    - Decode 10 I/O lines, bus size 8 or 16
    - I/O block at 0170, length 8
    - I/O block at 0376, length 2
    - IRQ may be shared, pulse and level mode interrupts are supported
    - Only IRQ14 is supported
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
17. 008E: Code 1B, link 06
    03 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 8E
    - Configuration Table Index is 03
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA
18. 0096: Code 14, link 00
    Tuple CISTPL_NO_LINK (14), length 0 (00) at offset 96
19. 0098: Code FF
    Tuple CISTPL_END (FF) at offset 98

6.4 Identify Drive Parameter Information

An example of the parameter information received from the iSCD when invoking the Identify Drive command (ECh) is listed in Table 25.

Table 25: Identify Drive Parameter Information

Word Address	Data	Total Bytes	Description
0	044AH	2	Value fixed by CFA
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per track
5	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7 - 8	XXXXH	4	Number of sectors per iSCD (word 7 = MSW, word 8 = LSW)
9	0000H	2	Reserved
10 - 19	Unique per card	20	Serial Number in ASCII (20 characters): STEC proprietary
20	XXXXH	2	Do not use this word. Before retirement, was buffer type
21	XXXXH	2	Do not use this word. Before retirement, was buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long commands
23 - 26	See description	8	Firmware revision in ASCII (8 characters): Rev8.0.0 52 65 76 38 2E 30 2E 30 hex
27 - 46	See description	40	Model Number in ASCII (40 characters): STI Flash 8.0.0 <left justified> 53 54 49 20 46 6C 61 73 68 20 38 2E 30 2E 30 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 hex
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0300H	2	DMA supported, LBA supported
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Single word DMA data transfer cycle timing mode (not supported)
53	0003h	2	Words 54 - 58 and 64 - 70 are valid
54	XXXXH	2	Number of Current Cylinders
55	XXXXH	2	Number of Current Heads
56	XXXXH	2	Number of Current Sectors Per Track
57	XXXXH	2	LSW of the Current Capacity in Sectors
58	XXXXH	2	MSW of the Current Capacity in Sectors
59	010XH	2	Current Setting for Block Count=1 for R/W Multiple commands
60 - 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single word DMA transfer not supported
63	0407H	2	Multiword DMA modes supported
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum multiword DMA transfer cycle time per word (ns)
66	0078H	2	Recommended multiword DMA transfer cycle time per word (ns)
67	0078H	2	Minimum PIO transfer without flow control
68	0078H	2	Minimum PIO transfer with IORDY flow control
69 - 255	0000H	374	Reserved
XXXXH = These values depend on the specific iSCD.			

7.0 Registers

This chapter lists the registers of the iSCD. Refer to PC Card standards for further details.

7.1 Configuration Registers

In PC Card Mode, four configuration registers, as listed in Table 26, are used.

Note: In True IDE Mode, these registers cannot be used.

Table 26: Configuration Registers

Configuration Register	Description
Configuration Option Register	This register is used to configure and observe the status of the iSCD, and to issue soft resets to it. Also, the Index bits of this register are used to select the PC Card mapping mode that the iSCD uses: 1) PC Card Memory, 2) PC Card Contiguous I/O, 3).PC Card Primary I/O, and 4) PC Card Secondary I/O
Configuration and Status Register	This register is used for observing the iSCD state.
Pin Replacement Register	This register is used for providing the signal state of -IREQ when the iSCD is configured in the PC Card I/O Mode.
Socket and Copy Register.	This read/write register is used to identify the iSCD from other devices. This register should be set by the host before this Configuration Option register is set.

7.2 Task File Registers

Table 27: iSCD Task File Registers

Task File Register	Description
Data Register	The Data Register is a 16-bit read/write register used for transferring data between the iSCD and the host. This register can be accessed in word mode and byte mode.
Error Register	The Error Register is a read-only register that is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to “0” (Ready). Diagnostic Codes are returned in the Error Register after a Execute Drive Diagnostic command (code 90h). Extended Error Codes returned in the Error Register after an Request Sense command (code 03h).
Sector Count Register	This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the iSCD. If the value in the register is 0, a count of 256 sectors is indicated.
Sector Number Register	When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.
Cylinder Low Register	In CHS mode (LBA=0), this register contains the low-order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.
Cylinder High Register	In CHS mode (LBA=0), this register contains the high-order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.
Drive/Head Register	This register selects the iSCD address translation (CHS or LBA) and provides head address (CHS) or high-order address bits 27:24 for LBA.
Status Register	This read-only register indicates status of a command execution. When the BSY bit is “0”, the other bits are valid; when the BSY bit is “1”, the other bits are not valid. When the register is read, the interrupt pin, is cleared.
Alternate Status Register	This register is the same as the Status register, except that is not negated when the register is read.
Device Control Register	This write-only register is used for controlling the interrupt request and issuing an ATA soft reset to the iSCD.
Drive Address Register	This read-only register is used for confirming the iSCD’s status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host’s I/O space because of potential conflicts on bit 7.
Command Register	This write-only register is used for writing the command that executes the iSCD’s operation. The command code is written in the command register after its parameters are written in the Task File during the iSCD ready state.

8.0 Supported ATA Commands

The ATA commands used by the iSCD are listed in Table 28. Refer to PC Card standards for details.

Table 28: iSCD Supported ATA Commands

Command Set	Code	Description
Check Power Mode	E5h or 98h	This command checks the power mode.
Execute Drive Diagnostic	90h	This command performs the internal diagnostic tests implemented by the iSCD. The Diagnostic Code is returned in the Error Register.
Erase Sector(s)	C0h	Command is used to pre-erase/condition data sectors in advance.
Format Track	50h	Command writes the desired head/cylinder of the selected drive with a vender unique data pattern (typically 00h or FFh). iSCD accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.
Identify Drive	ECh	This command lets the host receive parameter information from the iSCD in the same protocol as Read Sector(s) command.
Idle	E3h or 97h	Command causes the iSCD to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.
Idle Immediate	E1h or 95h	This command causes the iSCD to set BSY, enter the Idle mode, clear BSY, and generate an interrupt.
Initialize Drive Parameters	91h	This command enables the host to set the number of sectors per track and the number of heads per cylinder.
NOP	00h	No Operation.
Read Buffer	E4h	This command enables the host to read the current contents of the iSCD's sector buffer.
Read DMA	C8h	Command is sector read command used for MWDMA transfer.
Read Multiple	C4h	This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Read Long Sector	22h or 23h	Command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
Read Sector(s)	20h (w/ retry) 21h (w/o retry)	Command reads from 1 to 256 sectors as specified in the Sector Count register. Sector count of 0 requests 256 sectors. Transfer begins at the sector specified in the Sector Number register.
Read Verify Sector(s)	40h (w/ retry) 41h (w/o retry	This command verifies one or more sectors on the iSCD by transferring data from the flash media to the data buffer in the iSCD and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
Recalibrate	1Xh	The iSCD performs only the interface timing and register operations. When this command is issued, the iSCD sets BSY and waits for an appropriate length of time, after which it clears BSY and issues an interrupt. When this command ends normally, the iSCD is initialized.
Request Sense (Extended Error)	03h	This command requests an extended error code after a command ends with an error. The extended error code is returned in the Error Register
Seek	7Xh	This command is effectively a NOP command to the iSCD although it does perform a range check.

Command Set	Code	Description
Set Features	EFh	This command is used by the host to establish or select certain features.
Set Multiple Mode	C6h	This command enables the iSCD to perform multiple read and write operations and establishes the block count for these commands.
Set Sleep Mode	E6h or 99h	This is the only command that allows the host to set the iSCD into Sleep mode. When the iSCD is set to sleep mode, the iSCD clears the BSY line and issues an interrupt. The iSCD enters sleep mode and the only method to make the iSCD active again (back to normal operation) is by performing a hardware reset or a software reset.
Stand By	E2h or 96h	This command sets the iSCD in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the iSCD returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.
Stand By Immediate	E0h or 94h	This command causes the iSCD to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
Translate Sector	87h	This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.
Wear Level	F5h	This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.
Write Buffer	E8h	This command enables the host to overwrite the contents of the iSCD's sector buffer with any data pattern desired.
Write DMA	CAh	This command is the sector write command used for Multiword DMA transfer.
Write Long Sector	32h or 33h	This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
Write Multiple	C5h	This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
Write Multiple w/o Erase	CDh	This command is similar to the Write Multiple command, except that an implied erase before the write operation is not performed. ***Note:*** *Before using this command, it is required to erase the respective sectors using the Erase Sectors command*
Write Sector(s)	30h (w/ retry) 31h (w/o retry)	This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
Write Sector(s) w/o Erase	38h	This command is similar to the Write Sector(s) command, except that an implied erase before the write operation is not performed. ***Note***: *Before using this command, it is required to erase the respective sectors using the Erase Sectors command*.
Write Verify	3Ch	This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

9.0 Evaluating IDE Single Chip Drive

An Evaluation Board is available for customers that do not yet have the hardware layout ready for the IDE Single Chip Drive 50-ball footprint.

The Evaluation Board has an IDE Single Chip Drive soldered onto it, and comes with a standard 44-pin IDE connector, as shown in Figure 12. This will allow customers to start their software testing and evaluation, before the hardware design is finalized.

Figure 12: IDE Single Chip Drive Evaluation Board

The Evaluation Board can be ordered with the following ordering information:

- SLISCDxxx(M/G)M1U-EVB

where (M/G) indicates if proceeding capacity (xxx) is in MBytes (M) or GBytes (G).

10.0 Revision History

Revision	***Date***	***Description***
-101	9/29/06	Initial release.
-102	10/2/06	T/P options removed from P/Ns. Section for IDE Mode Only iSCD removed from Host Access Specification. 10/16/06. Dimension tables corrected; warranty bullet made visible.
-103	1/10/07	Corrected Serial Number, Firmware Revision, and Model Number entries in Identify Drive Parameter Information. Added MTBF Calculations, TrueIDE/PC Card mode configuration, Flash Management, Evaluating IDE Single Chip Drive, and updated Environmental Parameters.
-104	1/24/07	Updated TrueIDE/PC Card mode configuration and Master/Slave configuration.
-105	1/30/07	Updated all references from SimpleTech to STEC.
-106	3/08/07	Updated burst transfer rate MTBF Calculations. Added ESD Rating and Standards Compliance.
-107	5/11/07	Added additional MTBF Calculations, corrected DMARQ signal in Table 10. Product Released, preliminary mark removed from datasheet.
-108	8/06/07	Warranty bullet removed from features column on page 1
-109	11/2/07	Pasting error corrected in CIS (paper error only).
-110	11/7/07	Layout updated for consistency and easier editing. Disclaimer notice reformatted with headings.
-111	3/7/08	Contact information on last page updated.
-112	4/2/08	STEC China address on last page updated.
-113	4/8/08	Pinout 4 and 8 transposed in Pin Assignments table.

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