REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add six new device types for vendor CAGE number 65786. Add vendor CAGE number 1FN41 as a source of supply for devices 01KX, 02KX, 03KX, and 04KX. Change to vendor similar part number for vendor CAGE number 1FN41. Change to margin test method A for vendor CAGE number 66579. Remove 4.5.1, 4.5.2, 4.5.3, figures 5 and 6, and table III from drawing. Change to parameters t_{CS} and t_{DF} in table I. Change to figures 2 and 3. Editorial changes throughout.	93-01-21	M. A. Frye
B	5 year review and update. Changed input capacitance from 6 pF to 10 pF. ksr	06-06-06	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-06-21

REVISION LEVEL
B

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 8K X 8 UV EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87515**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87515	01	J	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		8K x 8 UV EPROM	45 ns
02		8K x 8 UV EPROM	55 ns
03		8K x 8 UV EPROM	70 ns
04		8K x 8 UV EPROM	90 ns
05		8K x 8 UV EPROM	45 ns
06		8K x 8 UV EPROM	55 ns
07		8K x 8 UV EPROM	35 ns
08		8K x 8 UV EPROM	35 ns
09		8K x 8 UV EPROM	45 ns
10		8K x 8 UV EPROM	55 ns
11		8K x 8 UV EPROM	25 ns
12		8K x 8 UV EPROM	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 OR CDIP2-T24	24	Dual-in-line 2/
K	GDFP2-F24 OR CDFP3-F24	24	Flat pack 2/
L	GDIP3-T24 OR CDIP4-T24	24	Dual-in-line 2/
3	CQCC1-N28	28	Square leadless chip carrier 2/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Storage temperature ..... -65°C to +150°C
Voltages on any pin with respect to ground ..... -0.5 V dc to +7.0 V dc
V_{PP} with respect to ground ..... -0.5 V dc to +14.0 V dc
Maximum power dissipation (P_D) 3/ ..... 1 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}) MIL-STD-1835
Junction temperature (T_J) 4/ ..... +150°C

1.4 Recommended operating conditions. 1/

Case operating temperature (T_C) ..... -55°C to +125°C
Supply voltage (V_{CC}) ..... +4.5 V dc to +5.5 V dc

1/ Generic numbers are listed on the Standardized Microcircuit Drawing Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

2/ Lid shall be transparent to permit ultraviolet light erasure.

3/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total numbers of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{IN} = 5.5 V and GND	1,2,3	All		±10	µA
Output leakage current	I_{LO}	V_{OUT} = 5.5 V and GND	1,2,3	All		±10	µA
Operating supply current (active) 1/	I_{CC1}	$\overline{CS} = V_{IL}$, V_{CC} = 5.5 V D0 to D7 = 0 mA f = max	1,2,3	01-10		120	mA
				11-12		140	
Standby current, TTL inputs	I_{CC2}	$\overline{CS}$ = 2.0 V, V_{CC} = 5.5 V	1,2,3	01-07		40	mA
				12		50	
Standby current, CMOS inputs	I_{CC3}	V_{CC} = 5.5 V, $\overline{CS} = V_{CC}$ -0.3 V	1,2,3	01-07		40	mA
				12		50	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All		0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	2.0		V
Output voltage low	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V; I_{OL} = 16 mA	1,2,3	01-10		0.45	V
		I_{OL} = 6 mA		11,12		0.4	
Output voltage high	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V; I_{OH} = -4 mA	1,2,3	01-10	2.4		V
		I_{OH} = -2 mA		11,12			
Output short circuit current 2/ 3/	I_{OS}	V_O = GND	1,2,3	All		-100	mA
Input capacitance 3/	C_{IN}	f = 1.0 MHz; T_C = +25°C; V_{IN} = 0 V	4	All		10	pF
Output capacitance 3/	C_{OUT}	See 4.3.1e; V_{CC} = 5.5 V; V_{OUT} = 0 V				12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address to output delay	t_{ACC}	V_{CC} = 4.5 V See figures 3 and 4	9,10,11	11,12		25	ns
				07,08		35	
				01,05			
				09		45	
				02,06			
				10		55	
				03		70	
				04		90	
$\overline{CS}$ to output delay	t_{CS}		9,10,11	11		15	ns
				08		20	
				12		25	
				09		30	
				01,02			
				10		35	
				07		40	
				05		45	
				03,04, 06		55	
$\overline{CS}$ high to output float 3/ 4/	t_{DF}		9,10,11	11		15	ns
				08,12		25	
				09		30	
				01,02			
				07,10		35	
				05		45	
				03,04, 06		55	
Address to output hold 3/	t_{OH}		9,10,11	All	0		ns

1/ TTL inputs: $V_{IL} \le 0.8$ V, $V_{IH} \ge 2.0$ V.

2/ Not more than one output should be shorted at a time, and short circuit test (I_{OS}) should not exceed 30 seconds.

3/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

4/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the output load in figure 3, circuit B.

Device types	All	
Case outlines	J, K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	A_{12}	O_5
19	A_{11}	O_6
20	$\overline{CS}$	O_7
21	A_{10}	NC
22	A_9	A_{12}
23	A_8	A_{11}
24	V_{CC}	$\overline{CS}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Mode	V_{CC}	$\overline{CS}$ / V_{PP}	$O_0 - O_7$
Read	5 V ±10%	V_{IL}	FF H
Output disable	5 V ±10%	V_{IH}	High Z
Program 1/	V_{CC}	V_{PP}	Data in
Verify 1/	V_{CC}	V_{IL}	Programmed byte

1/ See 4.5 herein.

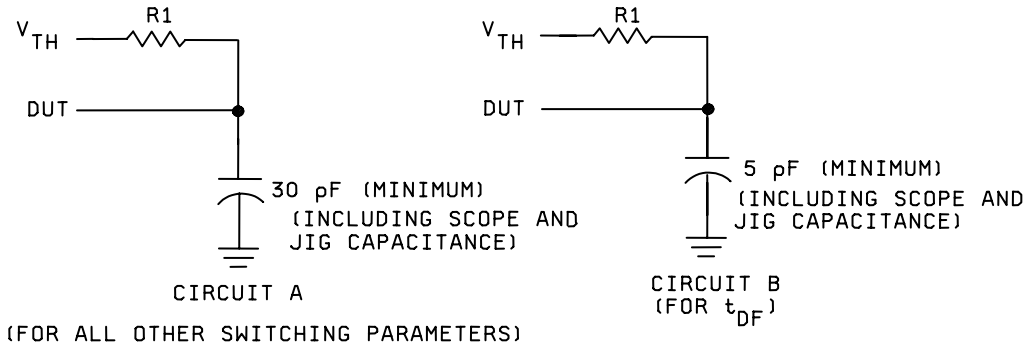
Device types 01 - 04

Type	Mode	Outputs	A_{12}	A_{11}	$\overline{CS}$	A_{10}	A_9	A_8	V_{CC}	Power
All	Read	D_{OUT}	A_{12}	A_{11}	V_{IL}	A_{10}	A_9	A_8	V_{CC}	I_{CC1}
05-07, 12	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{CC2}, I_{CC3}
08-11	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{CC1}
All	Program 1/	D_{IN}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{ILP}	V_{IHP}	V_{CC}	I_{CC1}
All	Program inhibit 1/	High-Z	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{IHP}	V_{CC}	I_{CC1}
All	Program verify 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC1}
All	Blank check 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC1}

1/ See 4.5 herein.

Device types 05- 12

FIGURE 2. Truth tables.



	Device types	
	01 – 10	11,12
R_1	98 Ω	250 Ω
V_{TH}	2.01 V	1.9 V

FIGURE 3. Output load circuits or equivalent circuit.

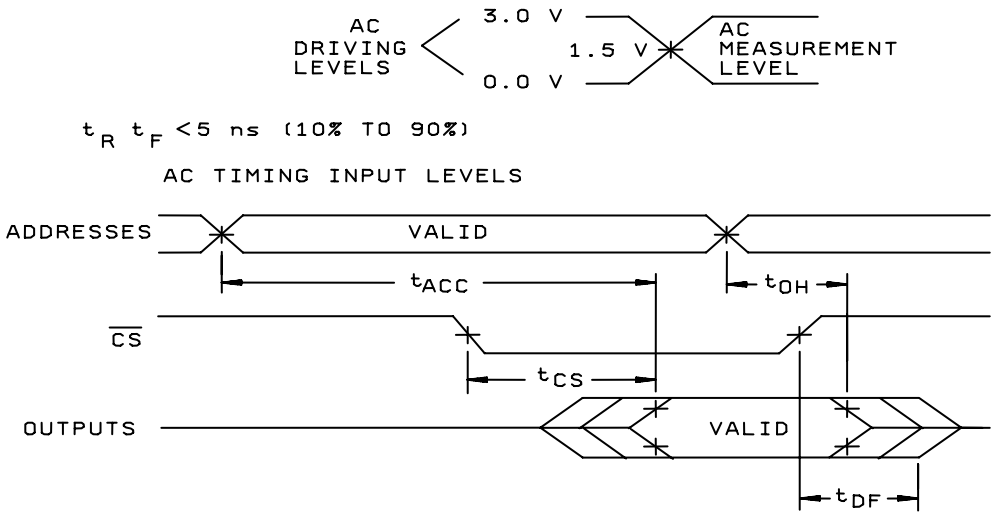


FIGURE 4. AC read timing diagram.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.6.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed (see 4.5 herein) to specified program or erased (see 4.4 herein). As a minimum, verification shall consist of performing a funtional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. * Steps 1 through 3 may be performed at wafer level.

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worse case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or 48 hours at 225°C (unassembled devices only).

(3) At +25°C, perform a margin test using V_m = +5.8 V to loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in in accordance with 4.2a.

(5) At +25°C, perform a margin test using V_m = +5.8 V.

(6) Perform electrical test in accordance with 4.2b.

(7) Erase in accordance with 3.6.1. Devices may be submitted to quality conformance inspection.

(8) Verify erasure in accordance with 3.6.3.

Margin test method B.

(1) Program at +25°C greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.

(3) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.6.1).

(4a) Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(5) Program at +25°C with a 50 percent pattern (checkerboard or equivalent).

(6) Perform margin test using V_m = +5.75 V and V_m = +4.40 V at +25°C with loose timing.

(7) Perform dynamic burn-in in accordance with 4.2a.

(8) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing.

(9) Perform electrical tests (see 4.2b).

(10) Erase (see 3.6.1), except devices submitted for groups A, B, C, and D testing.

(11) Verify erasure (see 3.6.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

d. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum intergrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.5 Progamming procedure. The progamming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE II. Electrical test requirements. *

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, (8A, 8B)***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* Indicates PDA applies to subgroup 1 and 7.
** See 4.3.1e.
*** See 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-06

Approved sources of supply for SMD 5962-87515 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-8751501JA	0C7V7	WS57C49C-45DMB
	0C7V7	QP7C264-45WMB
	3/	AT27HC641R-45DM/883
5962-8751501LA	0C7V7	WS57C49C-45TMB
	0C7V7	QP7C263-45WMB
	3/	AT27HC642R-45DM/883
5962-87515013A	0C7V7	WS57C49C-45CMB
	0C7V7	QP7C263-45QMB
	3/	AT27HC641R-45LM/883
5962-87515013C	0C7V7	WS57C49C-45CMB
	0C7V7	QP7C263-45QMB
5962-8751501KA	0C7V7	WS57C49C-45FMB
	0C7V7	QP7C263-45TMB
	3/	AT27HC641R-45FM/883
5962-8751502JA	0C7V7	WS57C49C-55DMB
	0C7V7	QP7C264-55WMB
	3/	AT27HC641R-55DM/883
5962-8751502LA	0C7V7	WS57C49C-55TMB
	0C7V7	QP7C263-55WMB
	3/	AT27HC642R-55DM/883
5962-87515023A	0C7V7	WS57C49C-55CMB
	0C7V7	QP7C263-55QMB
	3/	AT27HC642R-55LM/883
5962-87515023C	0C7V7	WS57C49C-55CMB
	0C7V7	QP7C263-55QMB
5962-8751502KA	0C7V7	WS57C49C-55FMB
	0C7V7	QP7C263-55TMB
	3/	AT27HC642R-55FM/883
5962-8751503JA	0C7V7	WS57C49C-70DMB
	0C7V7	QP7C264-70WMB
	3/	AT27HC641R-70DM/883
5962-8751503LA	0C7V7	WS57C49C-70TMB
	0C7V7	QP7C263-70WMB
	3/	AT27HC642R-70DM/883
5962-87515033A	0C7V7	WS57C49C-70CMB
	0C7V7	QP7C263-70QMB
	3/	AT27HC641R-70LM/883
5962-87515033C	0C7V7	WS57C49C-70CMB
	0C7V7	QP7C263-70QMB
5962-8751503KA	0C7V7	WS57C49C-70FMB
	0C7V7	QP7C263-70TMB
	3/	AT27HC641R-70FM/883

See notes at end of table.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-8751504JA	0C7V7 0C7V7 3/	WS57C49C-90DMB QP7C264-90WMB AT27HC641R-90DM/883
5962-8751504LA	0C7V7 0C7V7 3/	WS57C49C-90TMB QP7C263-90WMB AT27HC642R-90DM/883
5962-87515043A	0C7V7 0C7V7 3/	WS57C49C-90CMB QP7C263-90QMB AT27HC641R-90LM/883
5962-87515043C	0C7V7 0C7V7	WS57C49C-90CMB QP7C263-90QMB
5962-8751504KA	0C7V7 0C7V7 3/	WS57C49C-90FMB QP7C263-90TMB AT27HC641R-90FM/883
5962-8751505JA	0C7V7	WS57C49C-45DMB
5962-8751505LA	0C7V7 0C7V7 65786	WS57C49C-45TMB QP7C261-45WMB CY7C261-45WMB
5962-87515053A	0C7V7 0C7V7 3/	WS57C49C-45CMB QP7C261-45QMB CY7C261-45QMB
5962-87515053C	0C7V7	WS57C49C-45CMB
5962-8751505KA	0C7V7 0C7V7 3/	WS57C49C-45FMB QP7C261-45TMB CY7C261-45TMB
5962-8751506JA	0C7V7	WS57C49C-55DMB
5962-8751506LA	0C7V7 0C7V7 65786	WS57C49C-55TMB QP7C261-55WMB CY7C261-55WMB
5962-87515063A	0C7V7 0C7V7 3/	WS57C49C-55CMB QP7C261-55QMB CY7C261-55QMB
5962-87515063C	0C7V7	WS57C49C-55CMB
5962-8751506KA	0C7V7 0C7V7 3/	WS57C49C-55FMB QP7C261-55TMB CY7C261-55TMB
5962-8751507JA	0C7V7	WS57C49C-35DMB
5962-8751507LA	0C7V7 0C7V7 3/	WS57C49C-35TMB QP7C261-35WMB CY7C261-35WMB
5962-87515073A	0C7V7 0C7V7 65786	WS57C49C-35CMB QP7C261-35QMB CY7C261-35QMB

See notes at end of table.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-87515073C	0C7V7	WS57C49C-35CMB
5962-8751507KA	0C7V7	WS57C49C-35FMB
	0C7V7	QP7C261-35TMB
	3/	CY7C261-35TMB
5962-87515083A	0C7V7	WS57C49C-35CMB
	0C7V7	QP7C263-35QMB
	3/	CY7C263-35QMB
5962-87515083C	0C7V7	WS57C49C-35CMB
5962-8751508JA	0C7V7	WS57C49C-35DMB
	0C7V	QP7C264-35WMB
	3/	CY7C264-35WMB
5962-8751508KA	0C7V7	WS57C49C-35FMB
	0C7V7	QP7C263-35TMB
	3/	CY7C263-35TMB
5962-8751508LA	0C7V7	WS57C49C-35TMB
	0C7V7	QP7C263-35WMB
	3/	CY7C263-35WMB
5962-87515093A	0C7V7	WS57C49C-45CMB
	0C7V7	QP7C263-45QMB
	3/	CY7C263-45QMB
5962-87515093C	0C7V7	WS57C49C-45CMB
5962-8751509JA	0C7V7	WS57C49C-45DMB
	0C7V	QP7C264-45WMB
	3/	CY7C264-45WMB
5962-8751509KA	0C7V7	WS57C49C-45FMB
	0C7V7	QP7C263-45TMB
	3/	CY7C263-45TMB
5962-8751509LA	0C7V7	WS57C49C-45TMB
	0C7V7	QP7C263-45WMB
	3/	CY7C263-45WMB
5962-87515103A	0C7V7	WS57C49C-55CMB
	0C7V7	QP7C263-55QMB
	3/	CY7C263-55QMB
5962-87515103C	0C7V7	WS57C49C-55CMB
5962-8751510JA	0C7V7	WS57C49C-55DMB
	0C7V	QP7C264-55WMB
	3/	CY7C264-55WMB
5962-8751510KA	0C7V7	WS57C49C-55FMB
	0C7V7	QP7C263-55TMB
	3/	CY7C263-55TMB
5962-8751510LA	0C7V7	WS57C49C-55TMB
	0C7V7	QP7C263-55WMB
	3/	CY7C263-55WMB

See notes at end of table.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-87515113A	0C7V7 3/	QP7C263-25QMB CY7C263-25QMB
5962-8751511JA	0C7V7 3/	QP7C264-25WMB CY7C264-25WMB
5962-8751511KA	0C7V7 3/	QP7C263-25TMB CY7C263-25TMB
5962-8751511LA	0C7V7 3/	QP7C263-25WMB CY7C263-25WMB
5962-87515123A	0C7V7 3/	QP7C261-25QMB CY7C261-25QMB
5962-8751512KA	0C7V7 3/	QP7C261-25TMB CY7C261-25TMB
5962-8751512LA	0C7V7 3/	QP7C261-25WMB CY7C261-25WMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134-1506
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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