



# STF24NM60N STP24NM60N

N-channel 600 V, 0.168  $\Omega$ , 17 A MDmesh™ II Power MOSFET  
TO-220 and TO-220FP

## Features

Order codes	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STF24NM60N	650 V	< 0.19 $\Omega$	17 A
STP24NM60N	650 V	< 0.19 $\Omega$	17 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

Switching applications

## Description

These N-channel 600 V Power MOSFET devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converter.

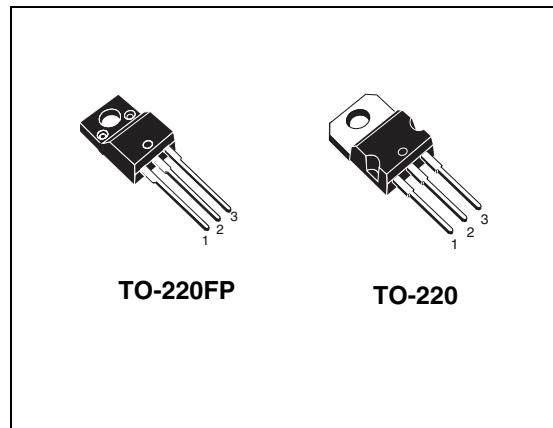


Figure 1. Internal schematic diagram

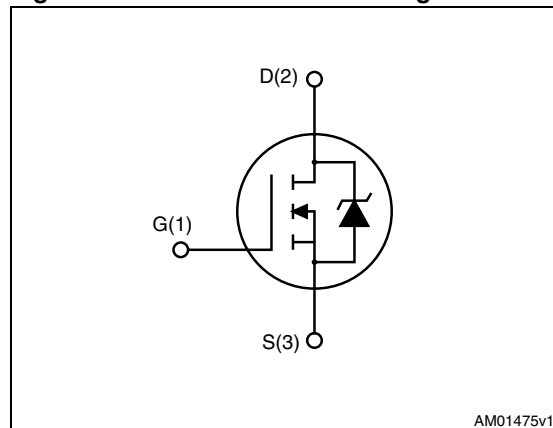


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF24NM60N	24NM60N	TO-220FP	Tube
STP24NM60N		TO-220	Tube

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# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$V_{GS}$	Gate- source voltage	± 30		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	17	17 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	11	11 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	68	68 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	125	30	W
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ °C}$ )		2500	V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150		°C

- Limited only by maximum temperature allowed.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 17\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ , peak  $V_{DS} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max.	1	4	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.	0.63		°C/W
$T_J$	Maximum lead temperature for soldering purpose	300		°C

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	300	mJ

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> =125 °C			1 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 25 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		0.168	0.19	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	1400	-	pF
C <sub>oss</sub>	Output capacitance			44		pF
C <sub>rss</sub>	Reverse transfer capacitance			7.4		pF
C <sub>oss eq.</sub> (1)	Equivalent output capacitance	V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0	-	190	-	pF
R <sub>g</sub>	Gate input resistance	f=1 MHz open drain	-	5	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 17 A, V <sub>GS</sub> = 10 V (see Figure 16)	-	46	-	nC
Q <sub>gs</sub>	Gate-source charge			7		nC
Q <sub>gd</sub>	Gate-drain charge			23		nC

1. C<sub>o(eff)</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>.

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 8.5 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see Figure 15)	-	11.5	-	ns
t <sub>r(v)</sub>	Voltage rise time			16.5		ns
t <sub>d(off)</sub>	Turn-off-delay time			73		ns
t <sub>f(i)</sub>	Fall time			37		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		340		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	4.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 17)		27		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		404		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V } T_J = 150\text{ }^\circ\text{C}$	-	5.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 17)		28		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

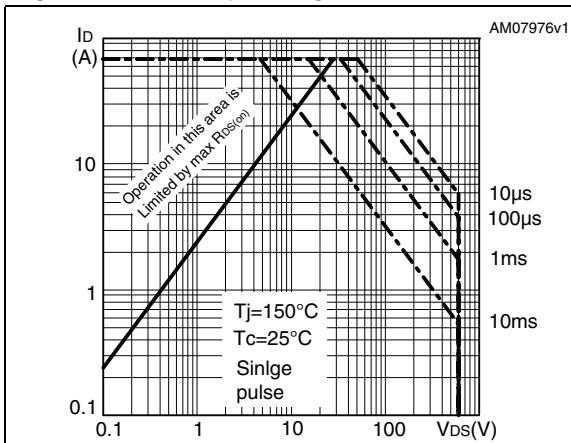


Figure 3. Thermal impedance for TO-220

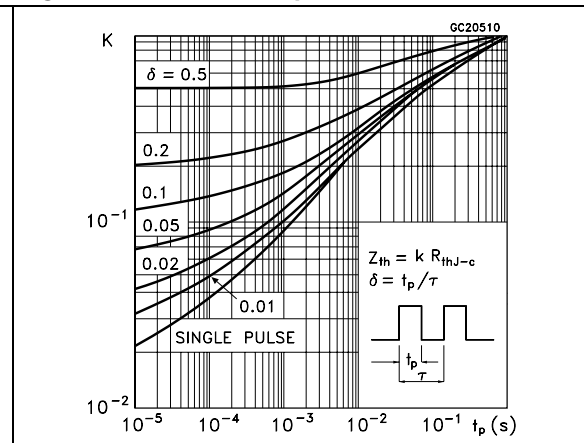


Figure 4. Safe operating area for TO-220FP

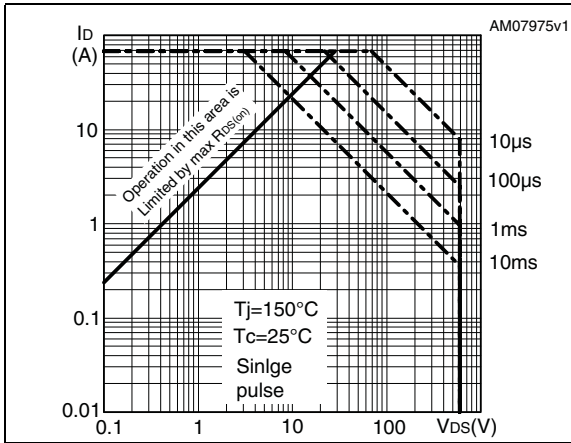


Figure 5. Thermal impedance for TO-220FP

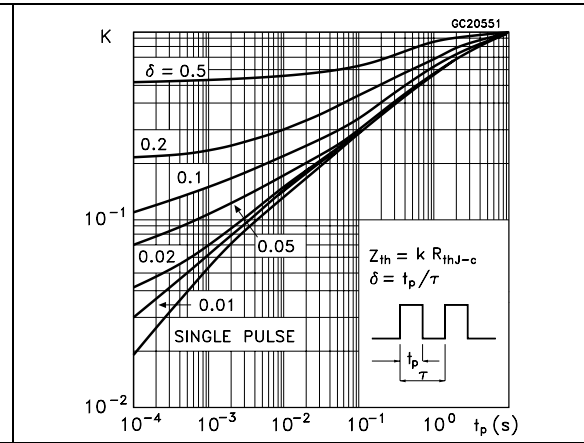


Figure 6. Output characteristics

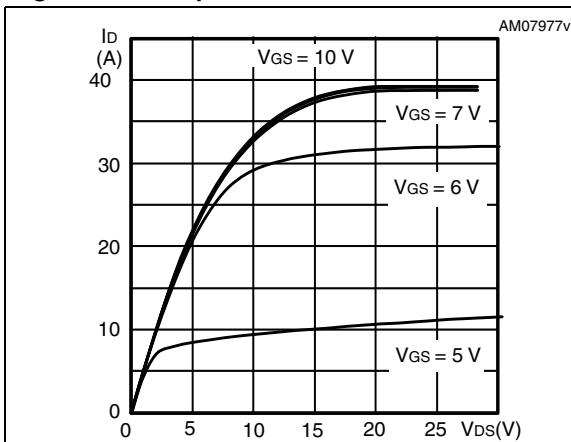


Figure 7. Transfer characteristics

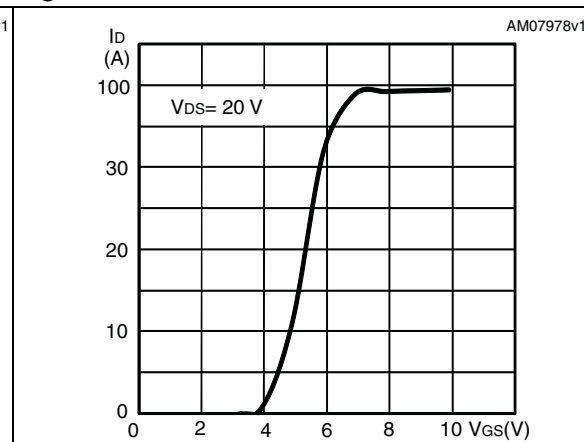


Figure 8. Gate charge vs gate-source voltage Figure 9. Static drain-source on resistance

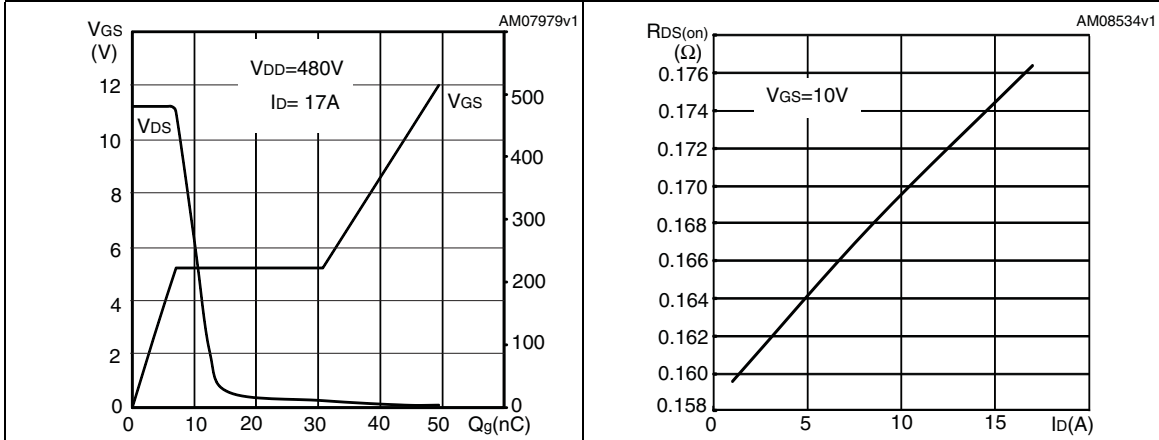


Figure 10. Capacitance variations Figure 11. Output capacitance stored energy

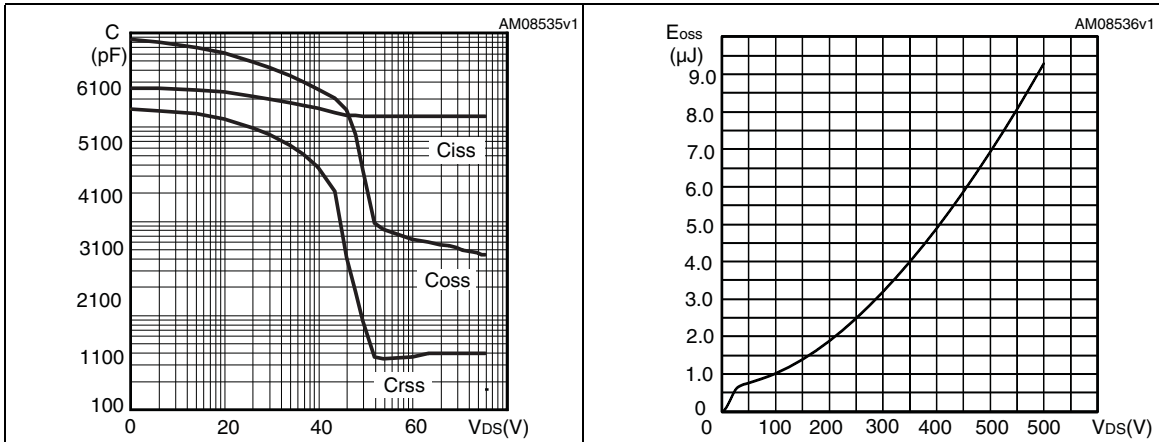


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on resistance vs temperature

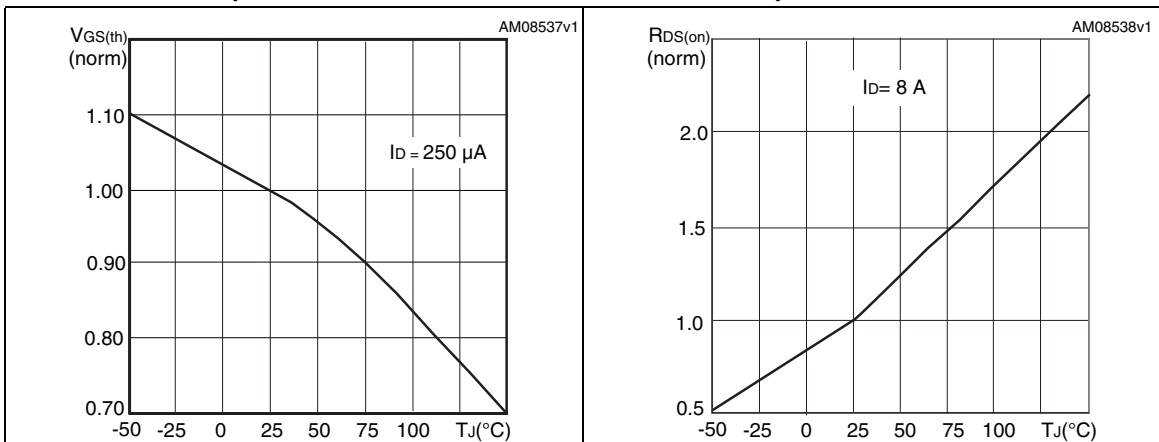
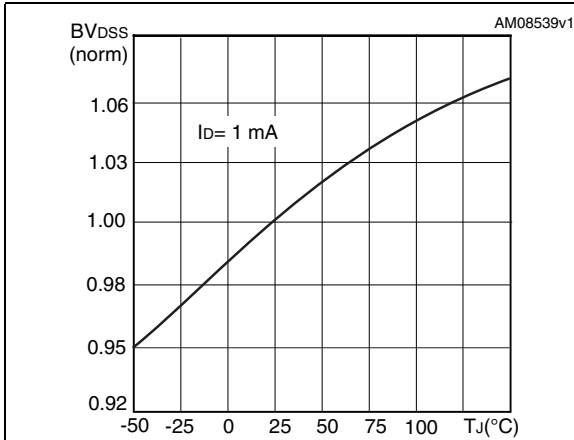


Figure 14. Normalized  $B_{VDSS}$  vs temperature



### 3 Test circuits

Figure 15. Switching times test circuit for resistive load

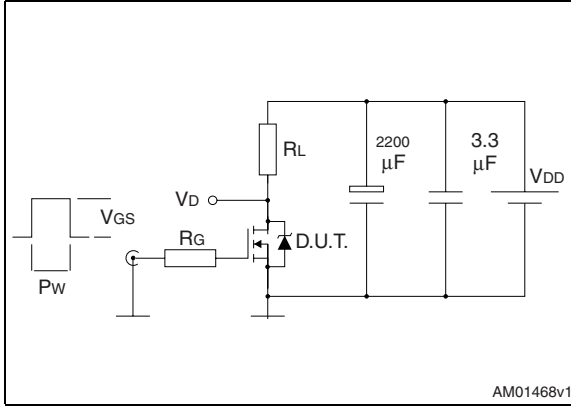


Figure 16. Gate charge test circuit

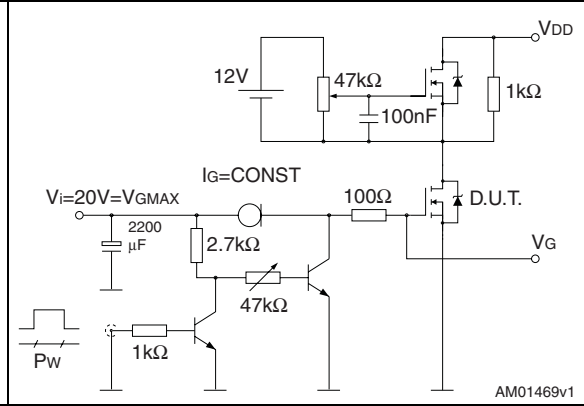


Figure 17. Test circuit for inductive load switching and diode recovery times

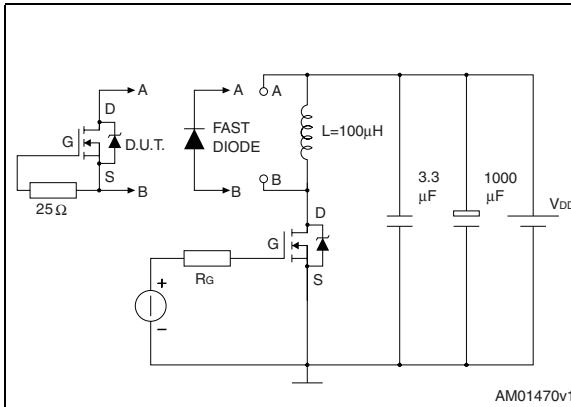


Figure 18. Unclamped inductive load test circuit

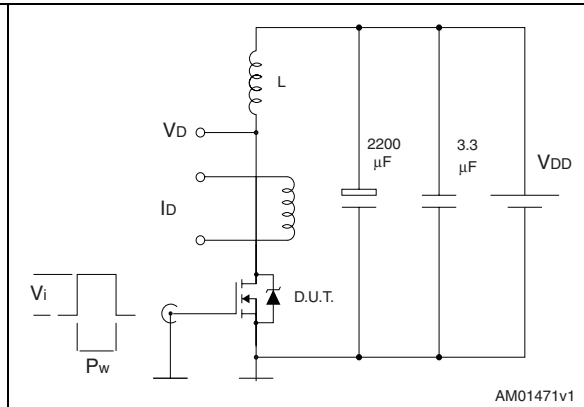


Figure 19. Unclamped inductive waveform

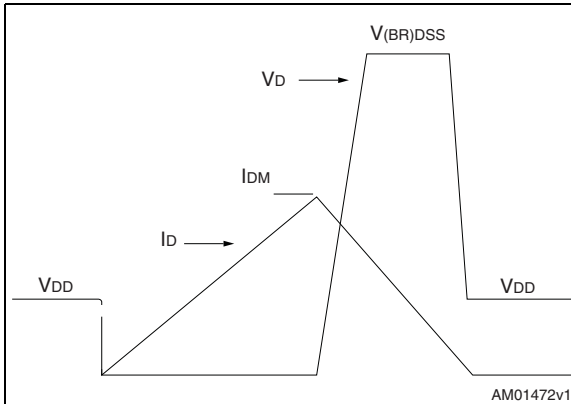
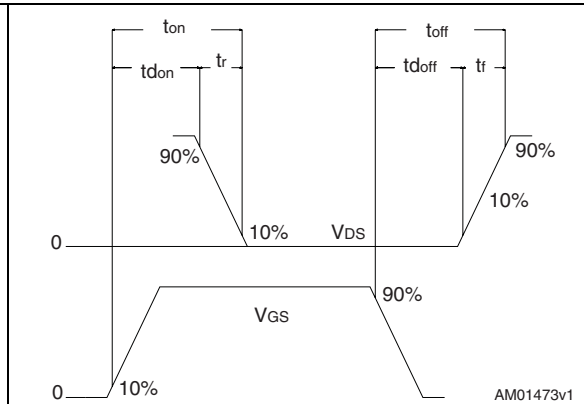


Figure 20. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 21. TO-220FP drawing

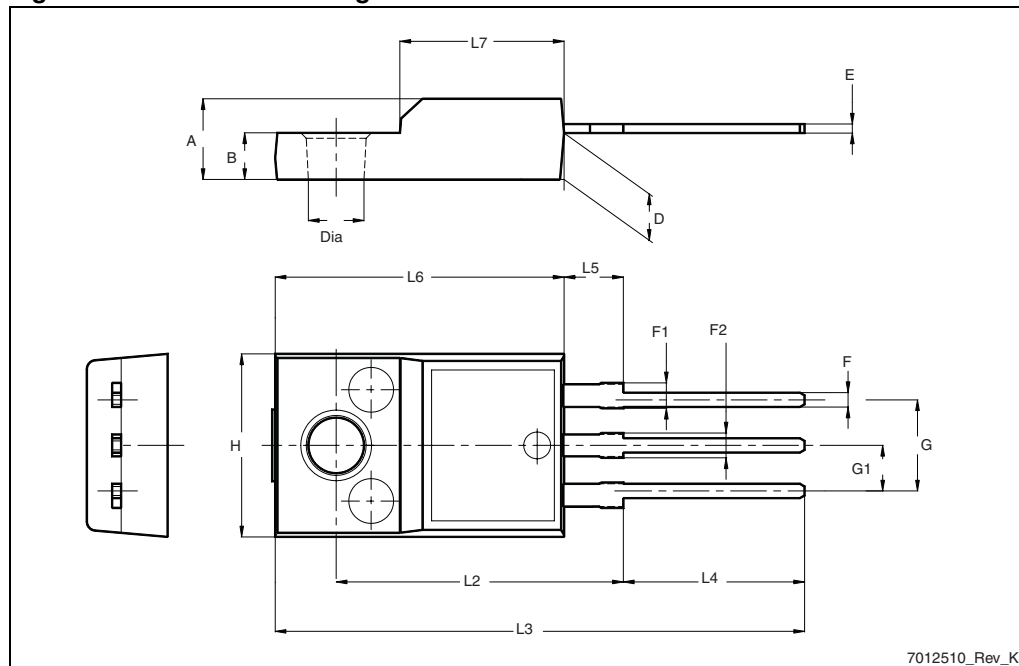
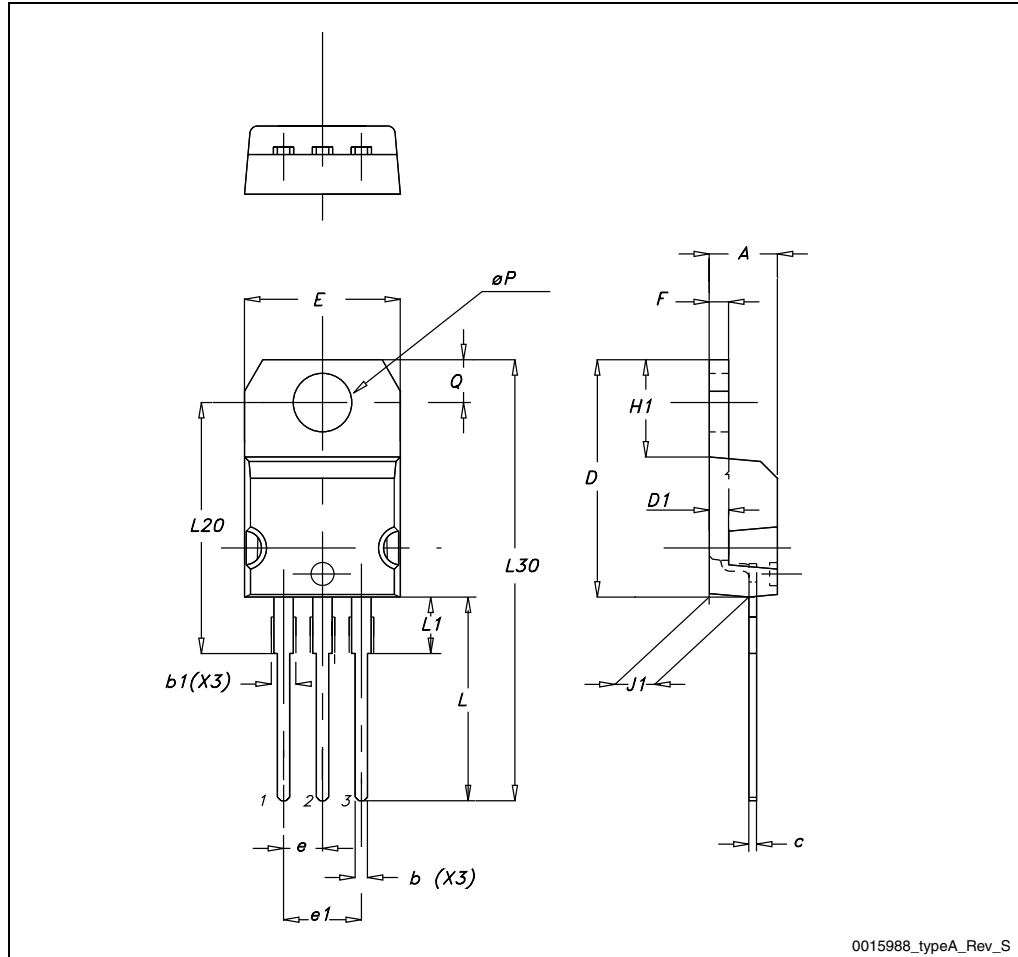


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 22. TO-220 type A drawing



## 5 Revision history

Table 11. Document revision history

Date	Revision	Changes
05-Jan-2011	1	First release.

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