



# STL24NM60N

N-channel 600 V, 0.200  $\Omega$ , 16 A PowerFLAT™ (8x8) HV  
MDmesh™ II Power MOSFET

Preliminary data

## Features

| Type       | V <sub>DSS</sub> @<br>T <sub>Jmax</sub> | R <sub>DS(on)</sub><br>max | I <sub>D</sub>      |
|------------|---|----------------------------|---------------------|
| STL24NM60N | 650 V                                   | < 0.215 $\Omega$           | 16 A <sup>(1)</sup> |

1. The value is rated according to R<sub>thj-case</sub>

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

Switching applications

## Description

This device is made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

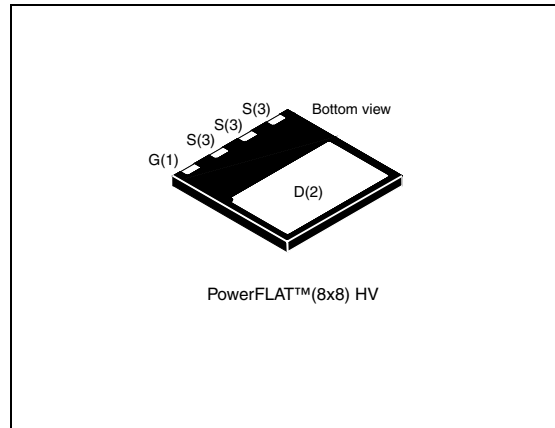


Figure 1. Internal schematic diagram

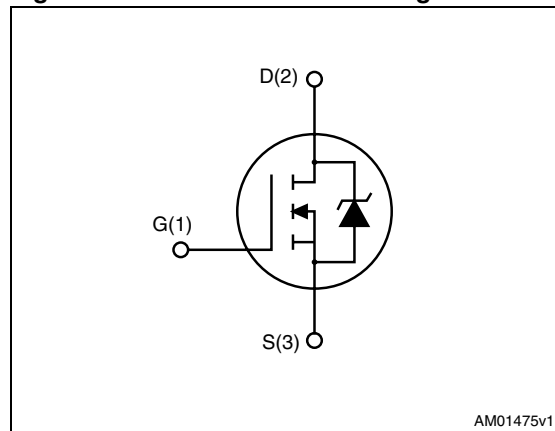


Table 1. Device summary

| Order code | Marking | Package             | Packaging     |
|------------|---------|---------------------|---------------|
| STL24NM60N | 24NM60N | PowerFLAT™ (8x8) HV | Tape and reel |

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter  | Value       | Unit             |
|--------------------|--|-------------|------------------|
| $V_{DS}$           | Drain-source voltage ( $V_{GS} = 0$ )  | 600         | V                |
| $V_{GS}$           | Gate-source voltage  | $\pm 25$    | V                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$   | 16          | A                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$  | 10          | A                |
| $I_D^{(2)}$        | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$   | 3.3         | A                |
| $I_D^{(2)}$        | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$  | 1.5         | A                |
| $I_{DM}^{(2),(3)}$ | Drain current (pulsed)   | 13.2        | A                |
| $P_{TOT}^{(3)}$    | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)   | 3           | W                |
| $P_{TOT}^{(1)}$    | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)   | 125         | W                |
| $I_{AR}$           | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)                                   | 4           | A                |
| $E_{AS}$           | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 300         | mJ               |
| $dv/dt^{(4)}$      | Peak diode recovery voltage slope  | 15          | V/ns             |
| $T_{stg}$          | Storage temperature  | - 55 to 150 | $^\circ\text{C}$ |
| $T_j$              | Max. operating junction temperature  | 150         | $^\circ\text{C}$ |

1. The value is rated according to  $R_{thj-case}$
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu
4.  $I_{SD} \leq 16\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DSpeak} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

| Symbol              | Parameter                            | Value | Unit                      |
|---------------------|--------------------------------------|-------|---------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case max | 1     | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}^{(1)}$ | Thermal resistance junction-amb max  | 45    | $^\circ\text{C}/\text{W}$ |

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

| Symbol        | Parameter  | Test conditions  | Min. | Typ. | Max.     | Unit                           |
|---------------|--|--|------|------|----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 1\text{ mA}$ , $V_{GS} = 0$   | 600  |      |          | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{Max rating}$<br>$V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$ |      |      | 1<br>100 | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 25\text{ V}$   |      |      | 100      | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                   | 3    | 4    | 5        | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$  |      | 0.2  | 0.215    | $\Omega$                       |

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|--|------|------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$  | -    | 1400 | -    | pF       |
| $C_{oss}$                  | Output capacitance            |  |      | 44   |      | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |  |      | 7.4  |      | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Output equivalent capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0$   | -    | 190  | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ open drain  | -    | 5    | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 16\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 3</a> ) | -    | 46   | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |  |      | 7    |      | nC       |
| $Q_{gd}$                   | Gate-drain charge             |  |      | 23   |      | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max | Unit |
|--------------|---------------------|---|------|------|-----|------|
| $t_{d(off)}$ | Turn-off delay time | $V_{DD} = 300\text{ V}$ , $I_D = 8\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 4</a> ) | -    | 11.5 | -   | ns   |
| $t_r$        | Rise time           |   |      | 16.5 |     | ns   |
| $t_c$        | Cross time          |   |      | 73   |     | ns   |
| $t_f$        | Fall time           |   |      | 37   |     | ns   |

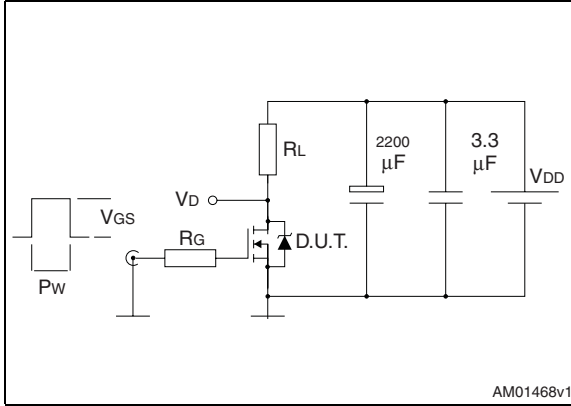
Table 7. Source drain diode

| Symbol          | Parameter                     | Test conditions   | Min. | Typ. | Max. | Unit |     |    |
|-----------------|-------------------------------|---|------|------|------|------|-----|----|
| $I_{SD}$        | Source-drain current          |   | -    |      | 16   | A    |     |    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |   | -    |      | 64   | A    |     |    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 16 \text{ A}$ , $V_{GS} = 0$  | -    |      | 1.5  | V    |     |    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 16 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 100 \text{ V}$ (see <a href="#">Figure 4</a> )                             | -    | 340  |      | ns   |     |    |
| $Q_{rr}$        | Reverse recovery charge       |   |      |      |      |      | 4.6 | μC |
| $I_{RRM}$       | Reverse recovery current      |   |      |      |      |      | 27  |    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 16 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 100 \text{ V}$ , $T_j = 150 \text{ °C}$<br>(see <a href="#">Figure 4</a> ) | -    | 4.4  |      | ns   |     |    |
| $Q_{rr}$        | Reverse recovery charge       |   |      |      |      |      | 5.7 | μC |
| $I_{RRM}$       | Reverse recovery current      |   |      |      |      |      | 28  |    |

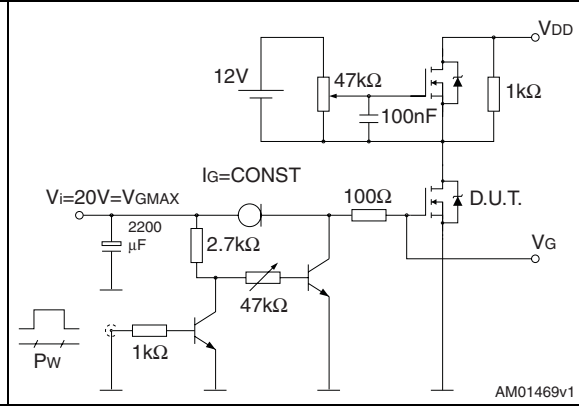
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

### 3 Test circuits

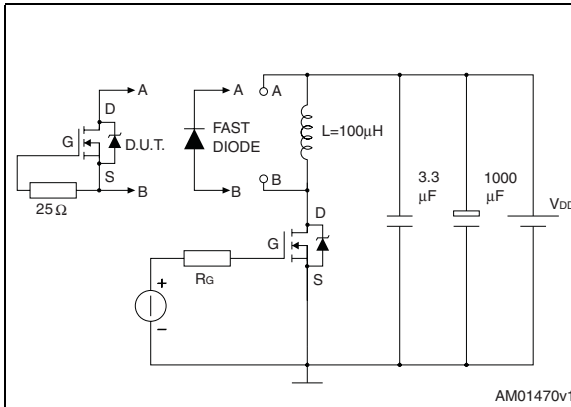
**Figure 2. Switching times test circuit for resistive load**



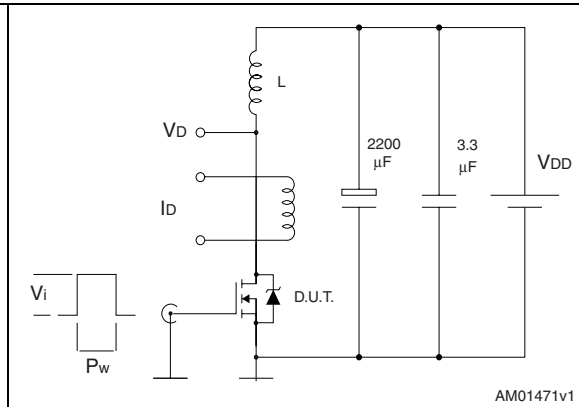
**Figure 3. Gate charge test circuit**



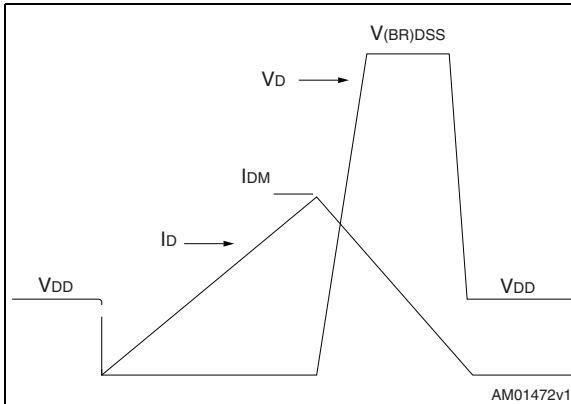
**Figure 4. Test circuit for inductive load switching and diode recovery times**



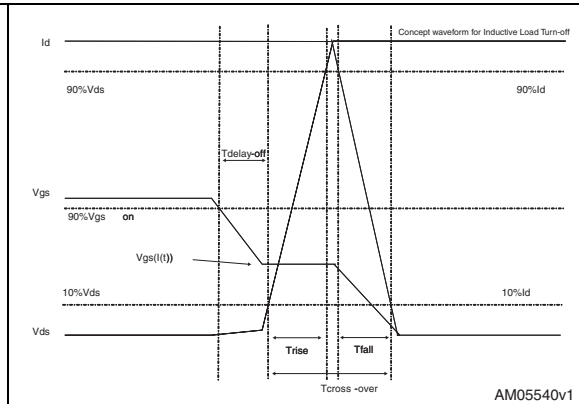
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 8. PowerFLAT™ 8x8 HV mechanical data**

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.80 | 0.90 | 1.00 |
| A1   |      | 0.02 | 0.05 |
| b    | 0.95 | 1.00 | 1.05 |
| c    |      | 0.10 |      |
| D    |      | 8.00 |      |
| E    |      | 8.00 |      |
| D2   | 7.05 | 7.20 | 7.30 |
| E2   | 4.15 | 4.30 | 4.40 |
| e    |      | 2.00 |      |
| L    | 0.40 | 0.50 | 0.60 |

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

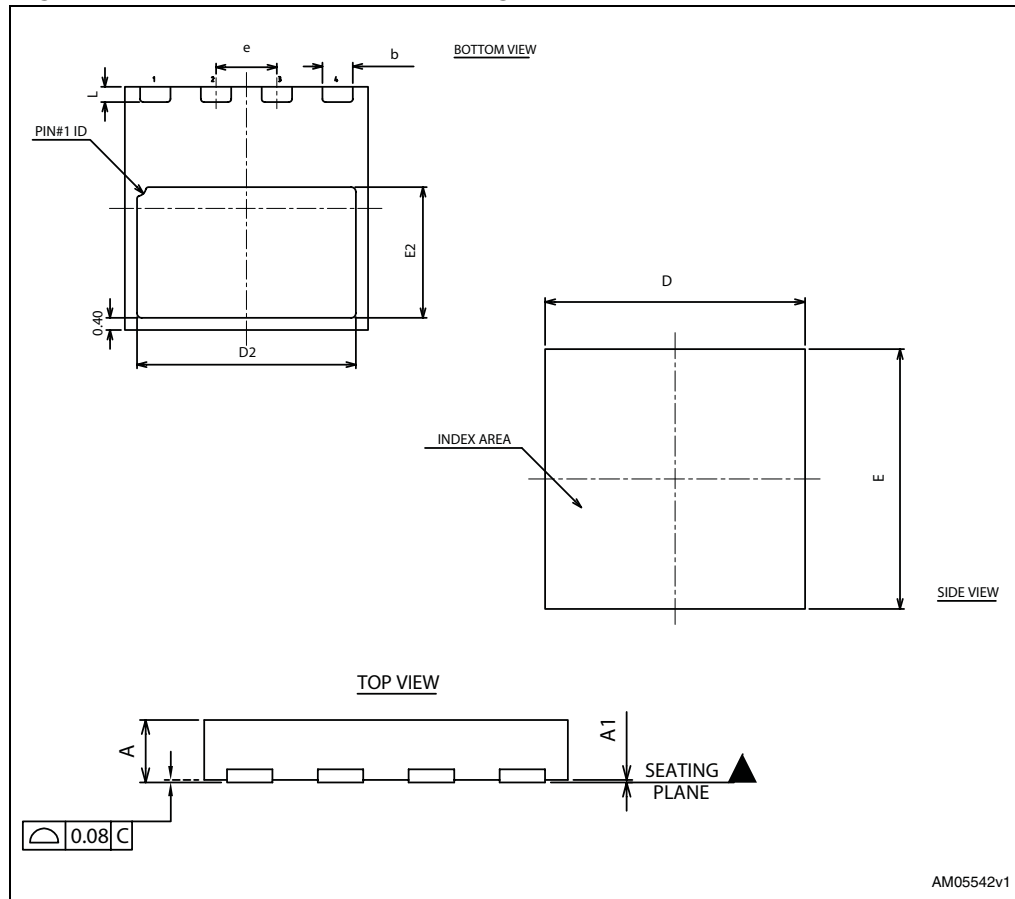
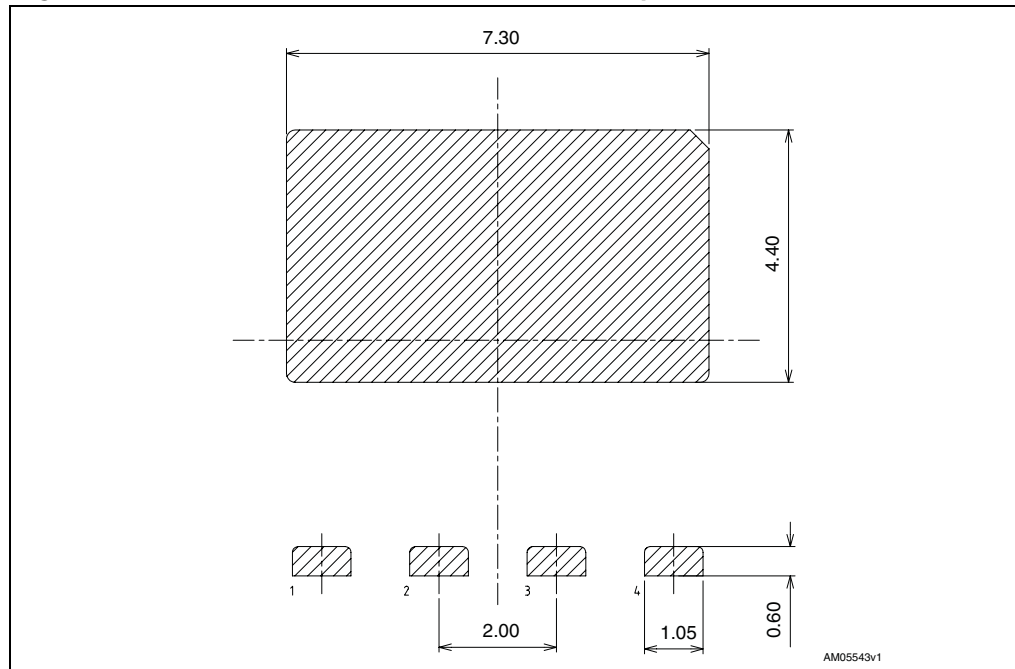




Figure 9. PowerFLAT™ 8x8 HV recommended footprint



## 5 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes        |
|-------------|----------|----------------|
| 05-Jan-2011 | 1        | First release. |

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