



# STH180N10F3-2 STP180N10F3

N-channel 100 V, 3.9 mΩ, 180 A STripFET™ Power MOSFET  
H<sup>2</sup>PAK, TO-220

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH180N10F3-2	100 V	4.5 mΩ	180 A
STP180N10F3	100 V	5.1 mΩ	120 A

- Ultra low on-resistance
- 100% avalanche tested

## Application

High current switching applications

## Description

These devices are the latest refinement of STMicroelectronics unique “single feature size” strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

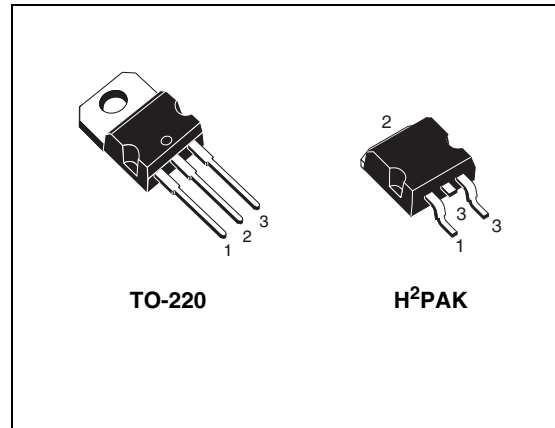


Figure 1. Internal schematic diagram

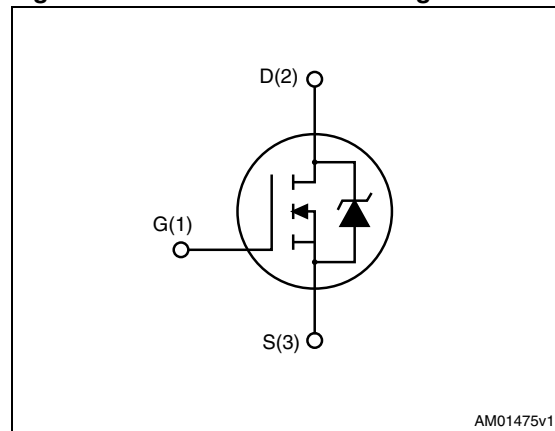


Table 1. Device summary

Order codes	Marking	Package	Packaging
STH180N10F3-2	180N10F3	H <sup>2</sup> PAK	Tape and reel
STP180N10F3	180N10F3	TO-220	Tube

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## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	H <sup>2</sup> PAK	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> =0)	100		V
V <sub>GS</sub>	Gate-source voltage	± 20		V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25°C	120	180	A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> =100°C	110	120	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	480	720	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	315		W
	Derating factor	2.1		W/°C
dv/dt	Peak diode recovery voltage slope	20		V/ns
E <sub>AS</sub> <sup>(3)</sup>	Single pulse avalanche energy	350		mJ
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature storage temperature	- 55 to 175		°C

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 80 A, V<sub>DD</sub> = 50 V.

**Table 3. Thermal data**

Symbol	Parameter	TO-220	H <sup>2</sup> PAK	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	0.48		°C/W
R <sub>thj-a</sub>	Thermal resistance junction-ambient max	62.5		°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-ambient max		35	°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on FR-4 board, on 1inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ , $V_{DS} = \text{max rating}$ , @ $125\text{ °C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 200$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 60\text{ A}$ H <sup>2</sup> PAK TO-220		3.9 4.5	4.5 5.1	m $\Omega$ m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	6665	-	pF
$C_{oss}$	Output capacitance			786		pF
$C_{rss}$	Reverse transfer capacitance			49		pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}$ , $I_D = 120\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	114.6	-	nC
$Q_{gs}$	Gate-source charge			38.8		nC
$Q_{gd}$	Gate-drain charge			31.9		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$ , $I_D = 60\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> , <a href="#">Figure 21</a> )	-	25.6	-	ns
$t_r$	Rise time			97.1		ns
$t_{d(off)}$	Turn-off delay time			99.9		ns
$t_f$	Fall time			6.9		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120\text{ A}$ , $V_{GS}=0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=120\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=80\text{ V}$ , $T_j=150^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	83.4		ns
$Q_{rr}$	Reverse recovery charge			295.7		nC
$I_{RRM}$	Reverse recovery current			7.1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

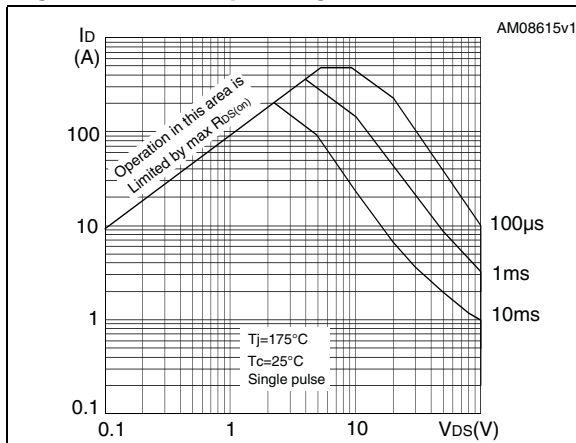


Figure 3. Thermal impedance for TO-220

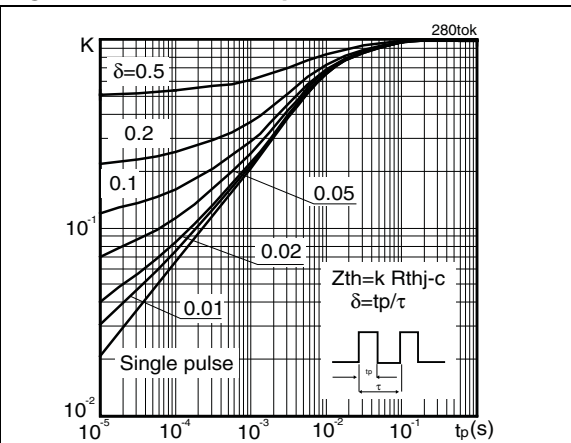


Figure 4. Safe operating area for H<sup>2</sup>PAK

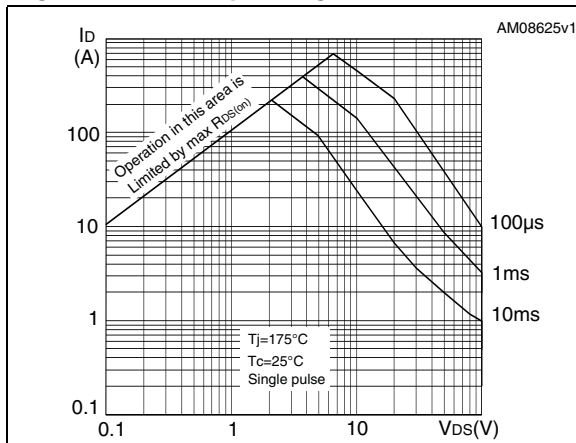


Figure 5. Thermal impedance for H<sup>2</sup>PAK

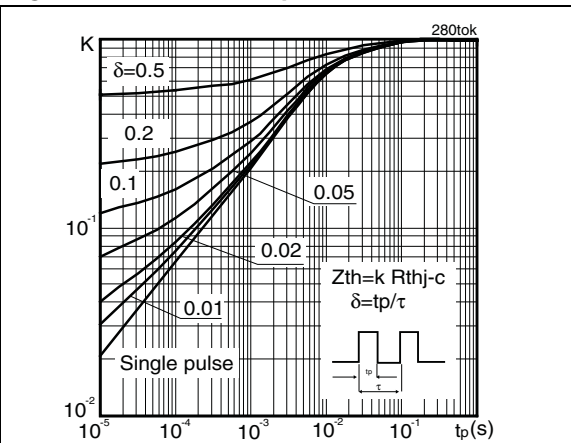


Figure 6. Output characteristics

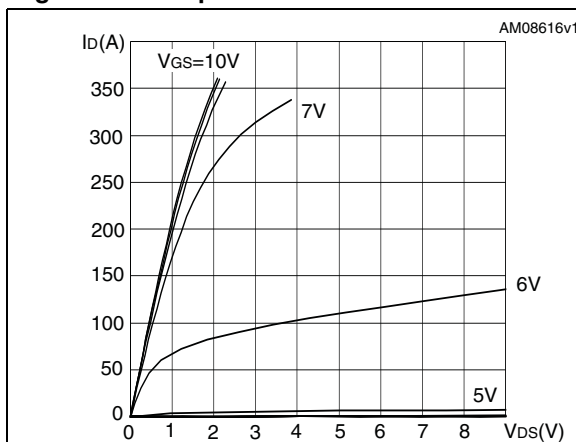
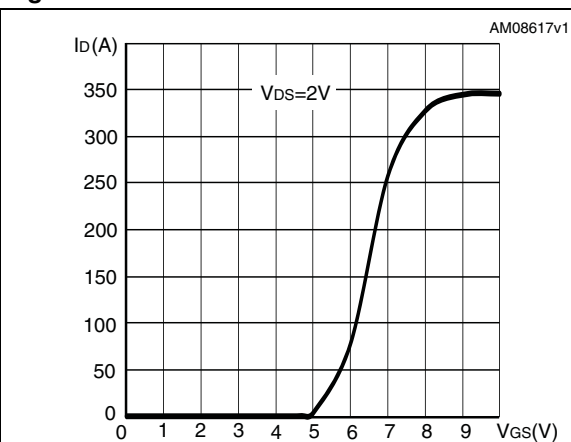
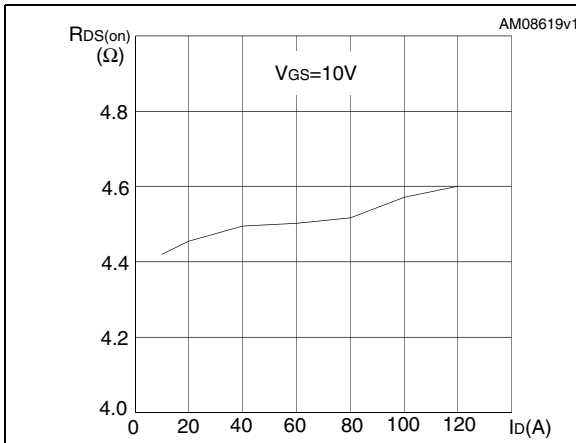


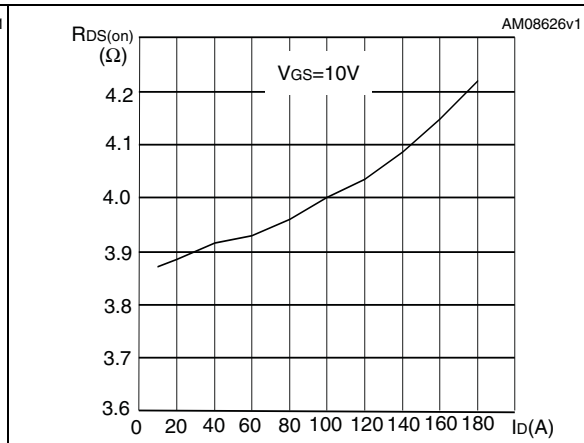
Figure 7. Transfer characteristics



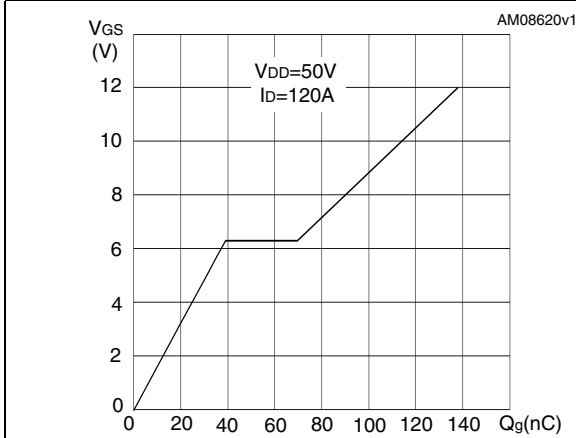
**Figure 8. Static drain-source on resistance for TO-220**



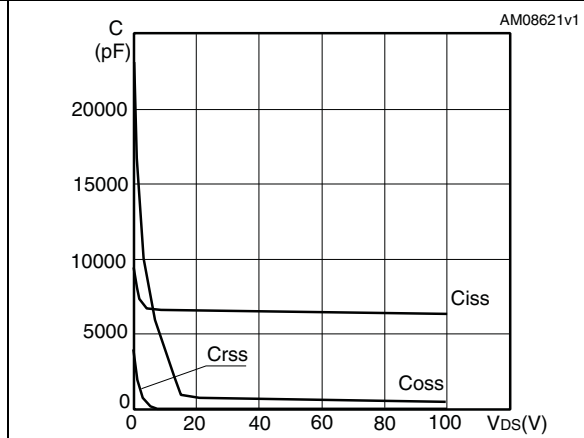
**Figure 9. Static drain-source on resistance for H<sup>2</sup>PAK**



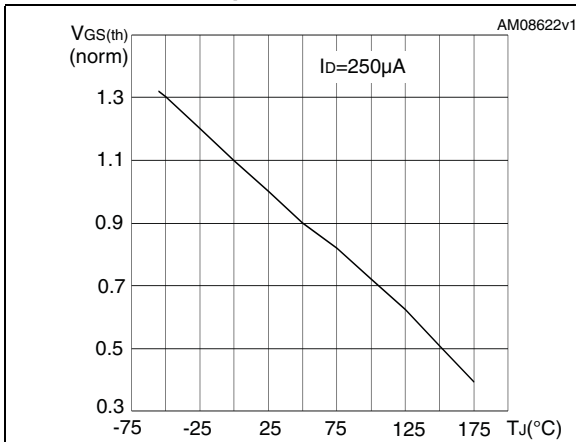
**Figure 10. Gate charge vs gate-source voltage**



**Figure 11. Capacitance variations**



**Figure 12. Normalized gate threshold voltage vs temperature**



**Figure 13. Normalized on resistance vs temperature**

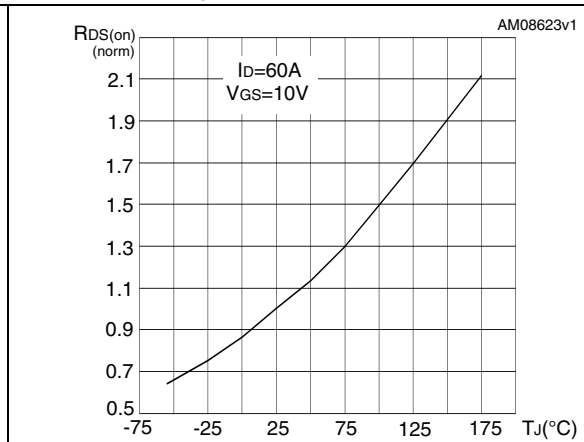


Figure 14. Source-drain diode forward characteristics

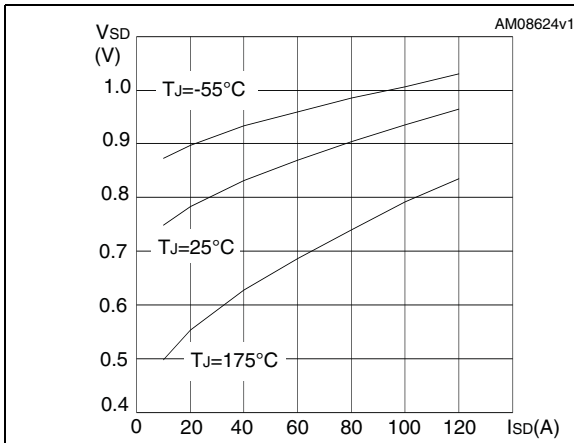
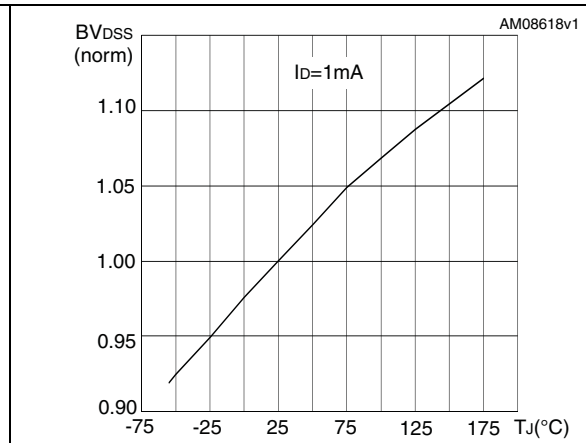


Figure 15. Normalized B<sub>VDSS</sub> vs temperature





### 3 Test circuits

Figure 16. Switching times test circuit for resistive load

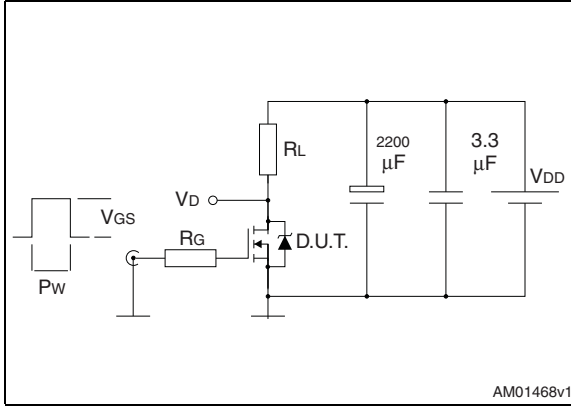


Figure 17. Gate charge test circuit

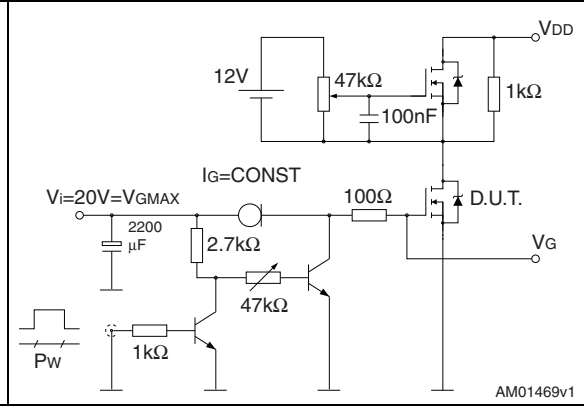


Figure 18. Test circuit for inductive load switching and diode recovery times

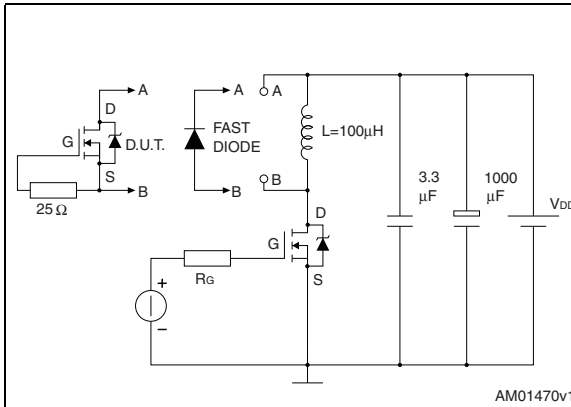


Figure 19. Unclamped inductive load test circuit

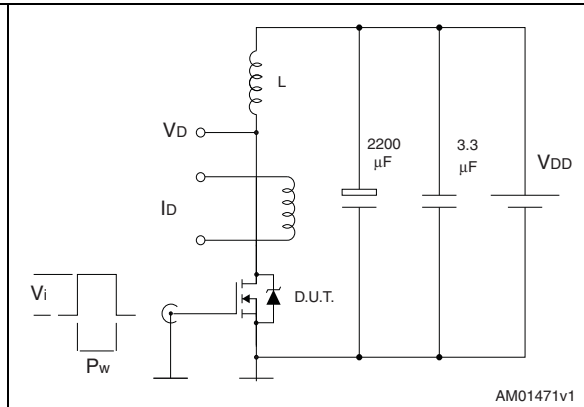


Figure 20. Unclamped inductive waveform

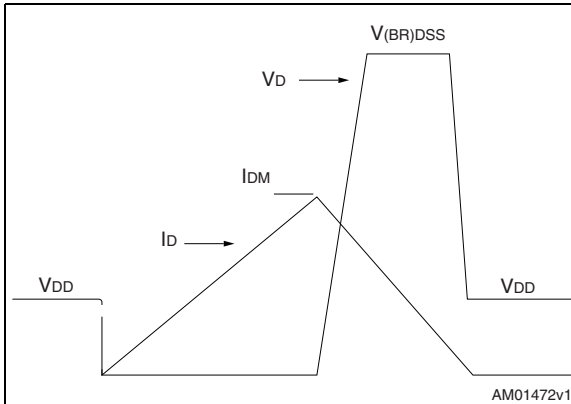
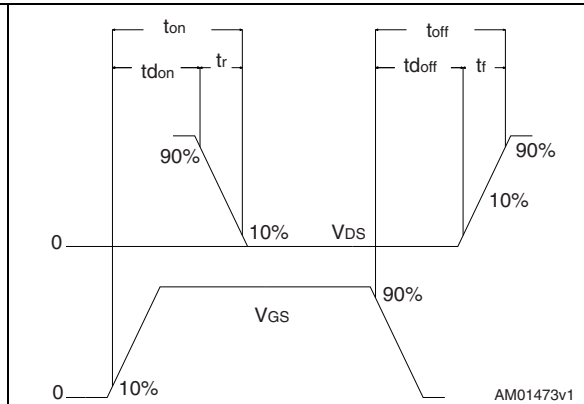


Figure 21. Switching time waveform



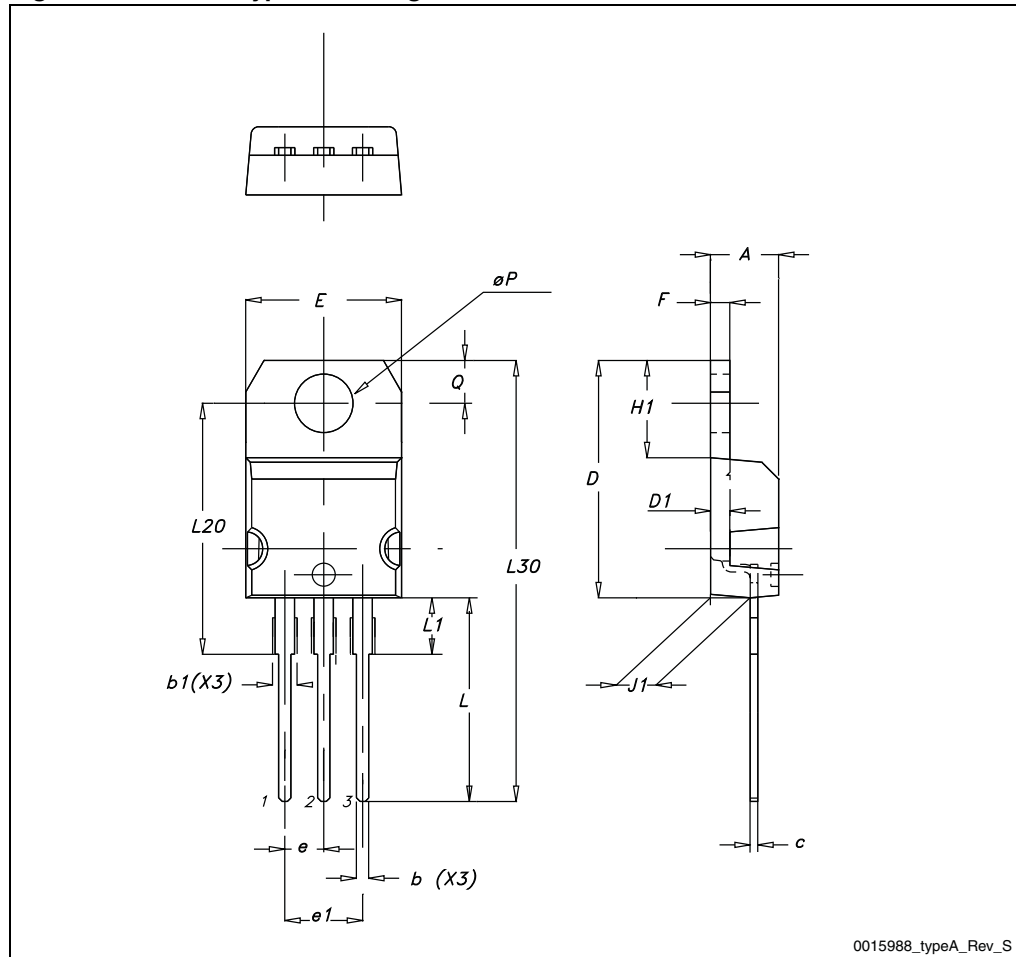
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 22. TO-220 type A drawing



0015988\_typeA\_Rev\_S

Table 9. H<sup>2</sup>PAK 2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 23. H<sup>2</sup>PAK 2 leads drawing

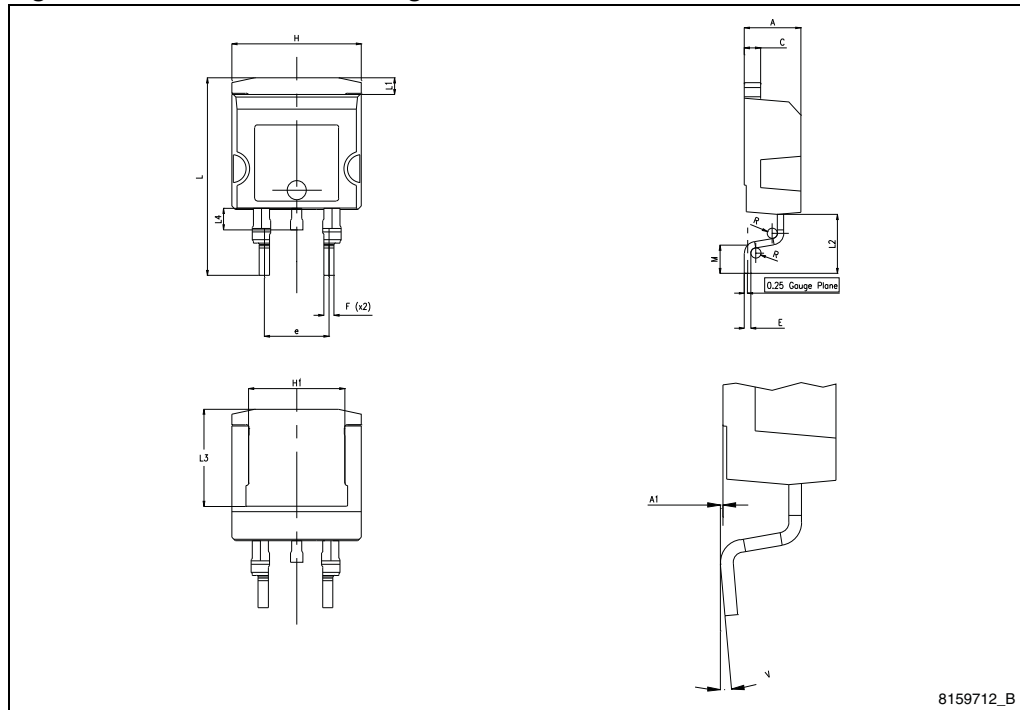
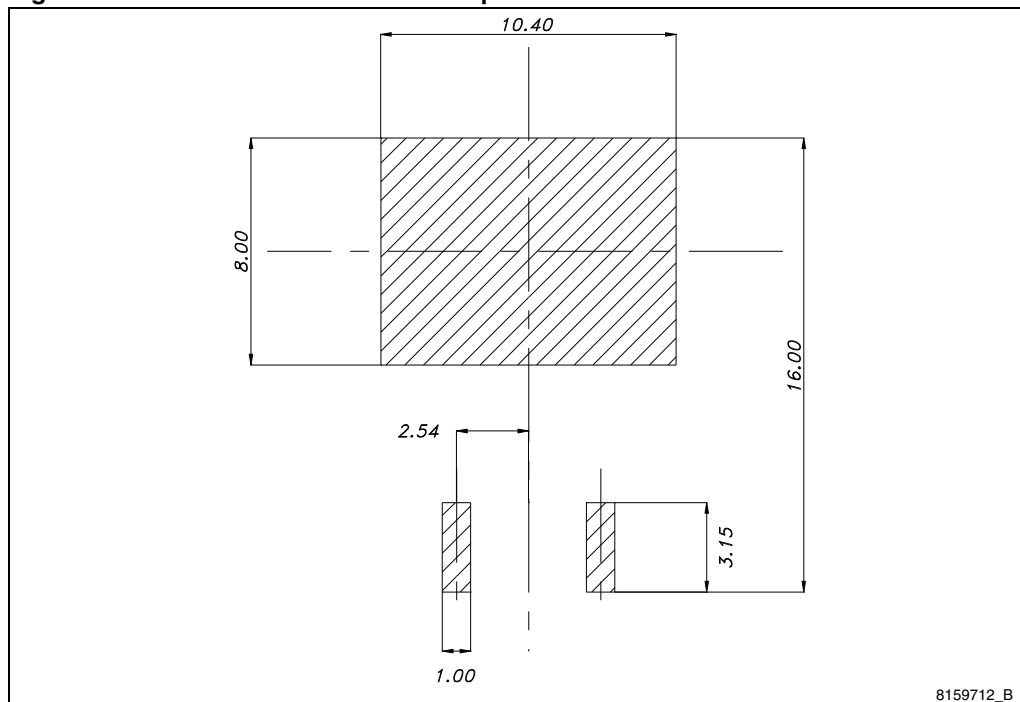


Figure 24. H<sup>2</sup>PAK 2 recommended footprint



## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Aug-2008	1	First version
03-Jun-2010	2	– Removed package, mechanical data: D <sup>2</sup> PAK – Added new package mechanical data: H <sup>2</sup> PAK
10-Mar-2011	3	Document status promoted from preliminary data to datasheet.

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