



STN3N40K3

N-channel 400 V, 3 Ω , 1.8 A SOT-223
SuperMESH3™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D	P _W
STN3N40K3	400 V	< 3.4 Ω	1.8 A	3.3 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Application

- Switching applications

Description

The device is made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH3™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

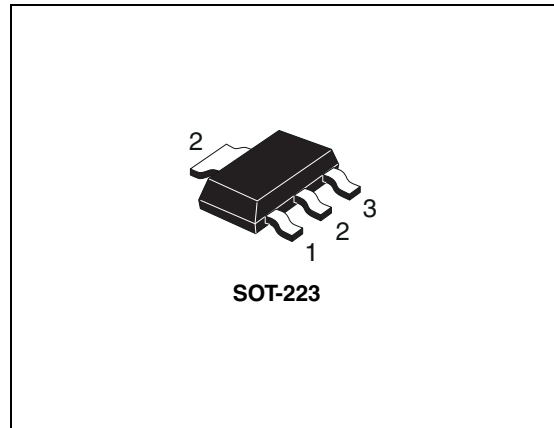


Figure 1. Internal schematic diagram

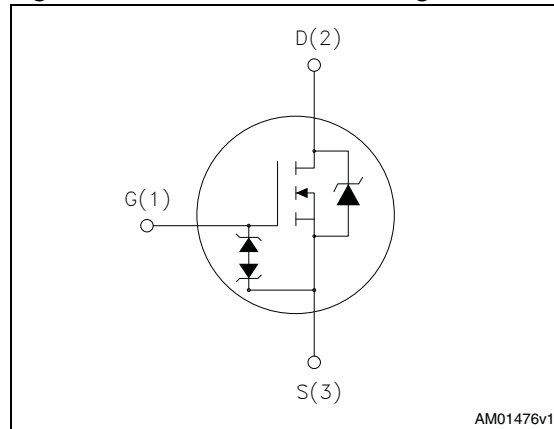


Table 1. Device summary

Order code	Marking	Package	Packaging
STN3N40K3	3N40K3	SOT-223	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics	6
3	Test circuits	9
4	Package mechanical data	10
5	Revision history	12

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	400	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current continuous $T_C = 25\text{ }^\circ\text{C}$	1.8 ⁽¹⁾	A
I_D	Drain current continuous $T_C = 100\text{ }^\circ\text{C}$	1 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current pulsed	7.2	A
I_{AR} ⁽³⁾	Avalanche current, repetitive or not repetitive	0.6	A
E_{AS} ⁽⁴⁾	Single pulse avalanche energy	45	mJ
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	3.3	W
dv/dt ⁽⁵⁾	Peak diode recovery voltage slope	12	V/ns
$V_{esd-(g-s)}$	G-S ESD (HBM C 0 100 pF; R = 1.5 k Ω)	1000	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Drain current limited by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. Pulse width limited by T_{Jmax} .
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.
5. $I_{sd} \leq 1.8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	37.88	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-amb max.	60	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	260	$^\circ\text{C}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	400			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C =125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V, V _{DS} =0			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{GS} = V _{DS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 0.6 A		3	3.4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	165	-	pF
C _{oss}	Output capacitance			17		pF
C _{rss}	Reverse transfer capacitance			3		pF
C _{oss(er)} ⁽¹⁾	Equivalent output capacitance energy related	V _{DS} =0 to 320 V, V _{GS} =0	-	9	-	pF
C _{oss(tr)} ⁽²⁾	Equivalent output capacitance time related			14		pF
R _g	Intrinsic gate resistance	f=1 MHz open drain	-	10	-	Ω
Q _g	Total gate charge	V _{DD} = 320 V, I _D = 1.8 A, V _{GS} = 10 V (see Figure 16)	-	11	-	nC
Q _{gs}	Gate-source charge			2		nC
Q _{gd}	Gate-drain charge			7		nC

1. Is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Is defined as a constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn on delay time	$V_{DD} = 200\text{ V}$, $I_D = 0.6$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)		7		ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn off delay time				18	ns
t_f	Fall time				14	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				7.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.6\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17)	-	145		ns
Q_{rr}	Reverse recovery charge			490		nC
I_{RRM}	Reverse recovery current			7		A
t_{rr}	Reverse recovery time	$I_{SD} = 1.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	166		ns
Q_{rr}	Reverse recovery charge			580		nC
I_{RRM}	Reverse recovery current			7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics

Figure 2. Safe operating area

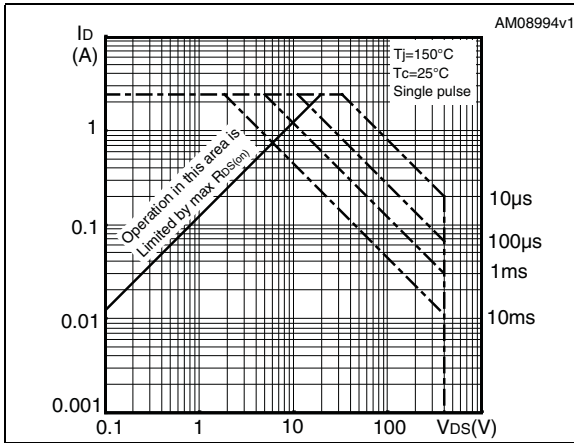


Figure 3. Thermal impedance

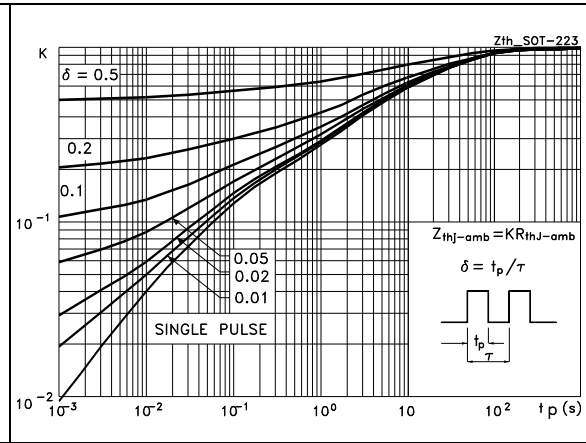


Figure 4. Output characteristics

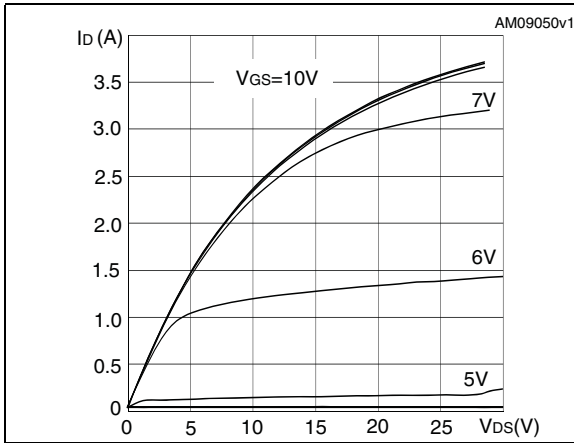


Figure 5. Transfer characteristics

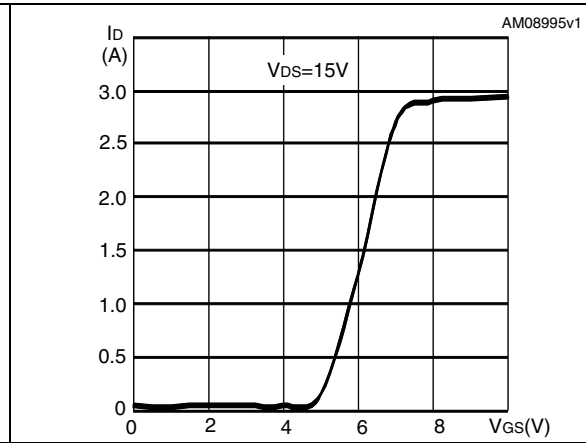


Figure 6. Gate charge vs gate-source voltage

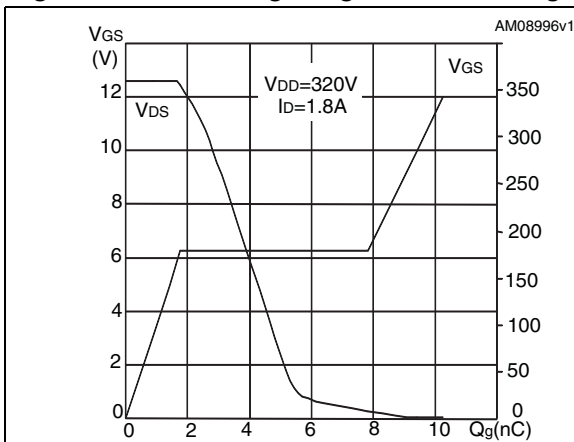


Figure 7. Static drain-source on resistance

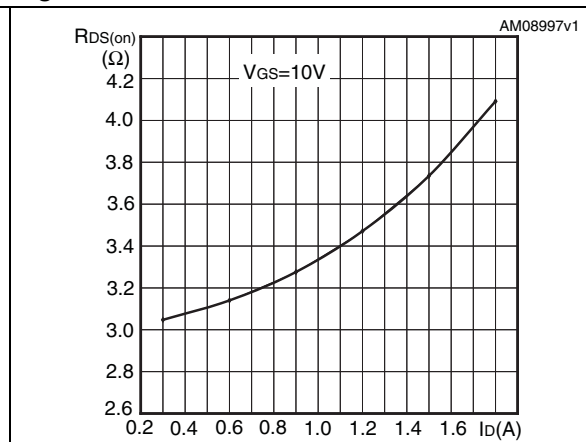


Figure 8. Capacitance variations

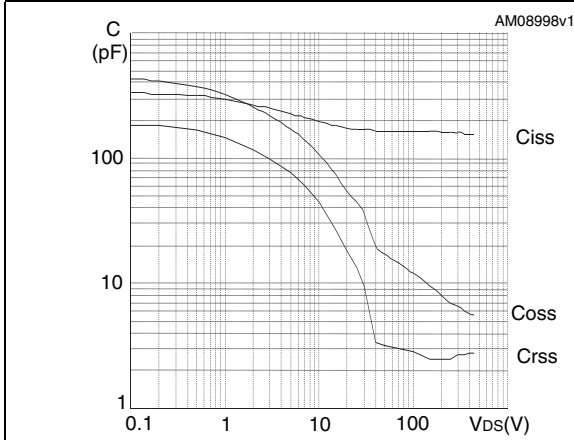


Figure 9. Output capacitance stored energy

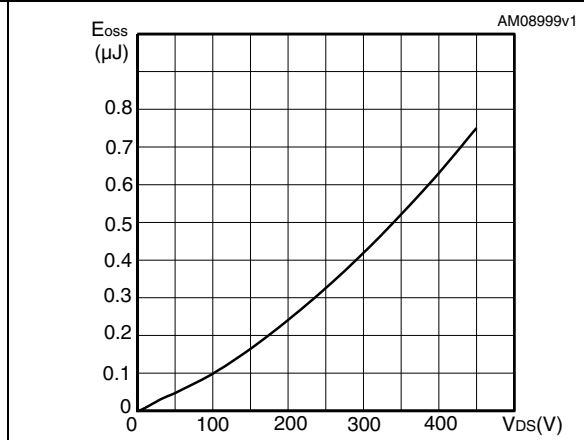


Figure 10. Normalized gate threshold voltage vs. temperature

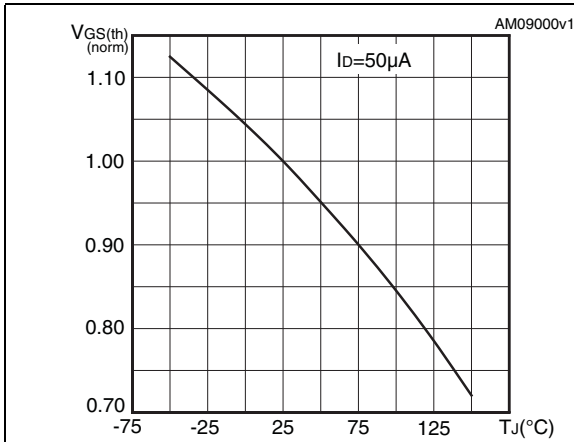


Figure 11. Normalized on resistance vs. temperature

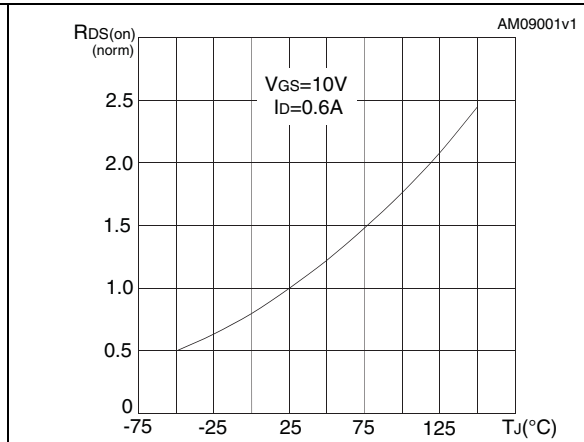


Figure 12. Source-drain diode forward characteristics

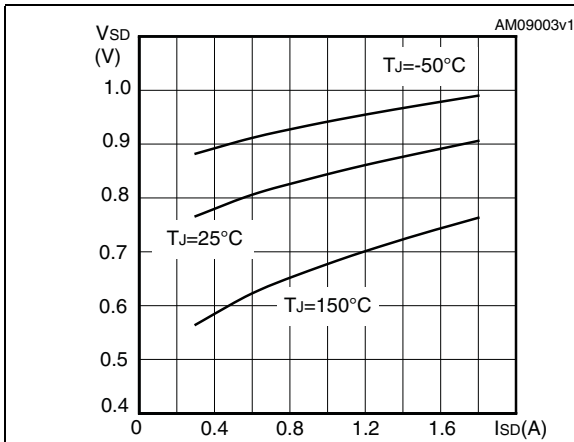


Figure 13. Normalized B_{VDS} vs. temperature

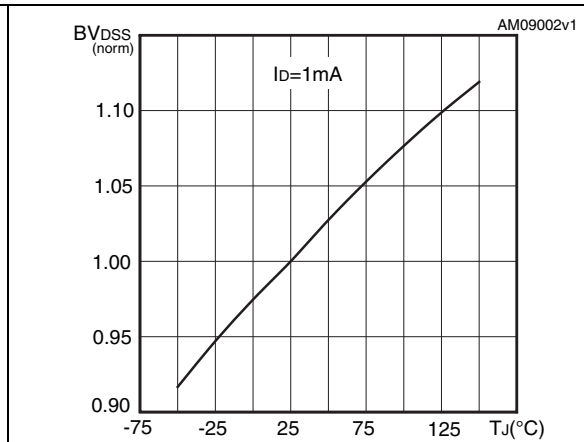
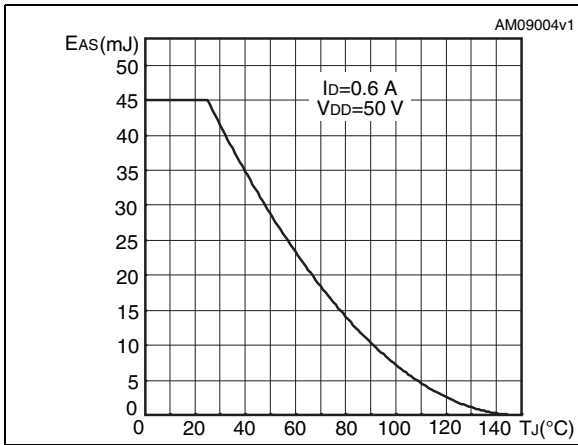


Figure 14. Maximum avalanche energy vs. starting T_j



3 Test circuits

Figure 15. Switching times test circuit for resistive load

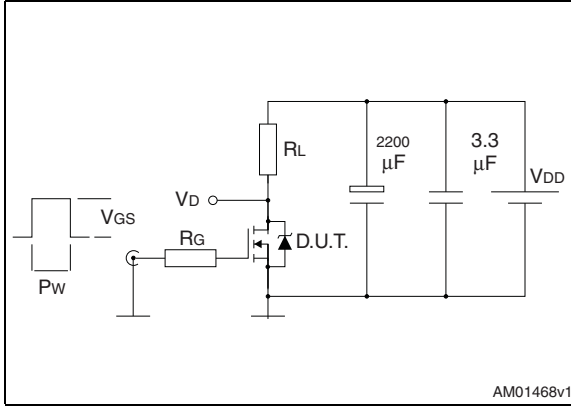


Figure 16. Gate charge test circuit

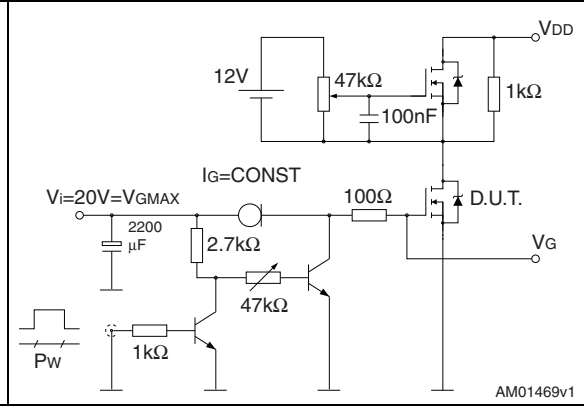


Figure 17. Test circuit for inductive load switching and diode recovery times

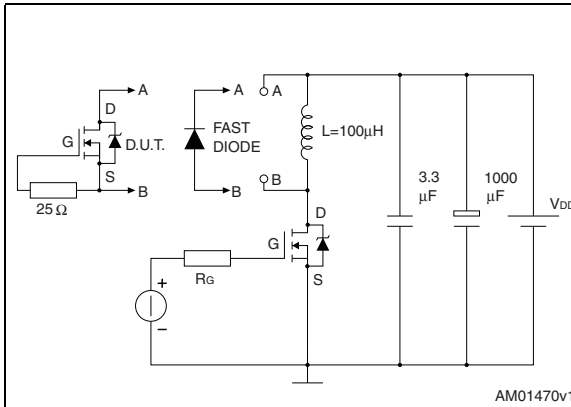


Figure 18. Unclamped inductive load test circuit

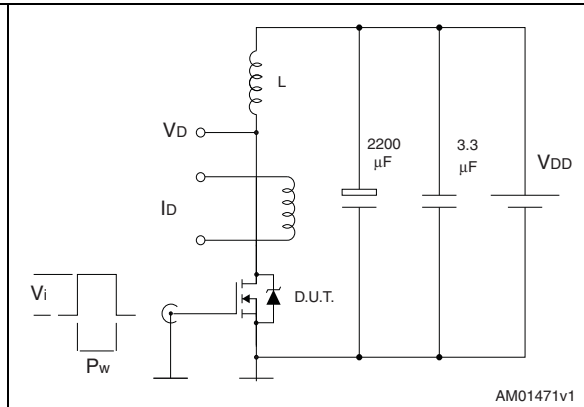


Figure 19. Unclamped inductive waveform

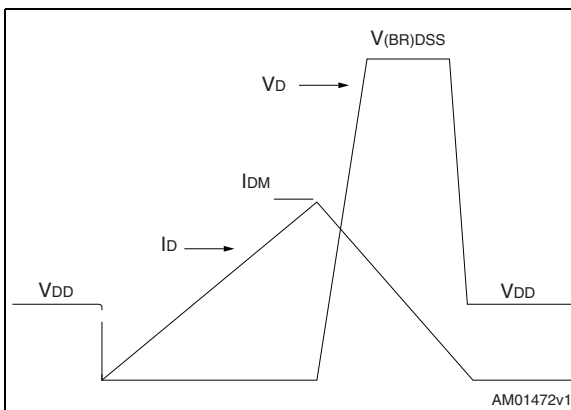
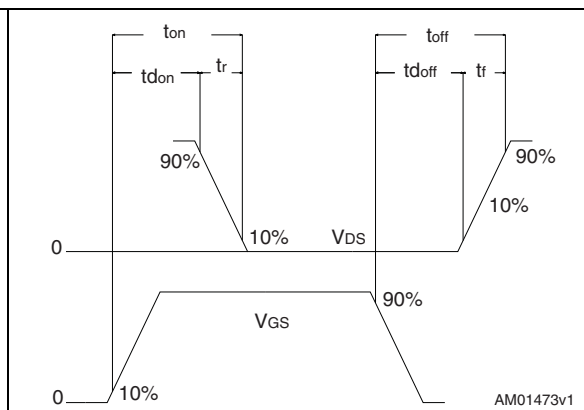


Figure 20. Switching time waveform



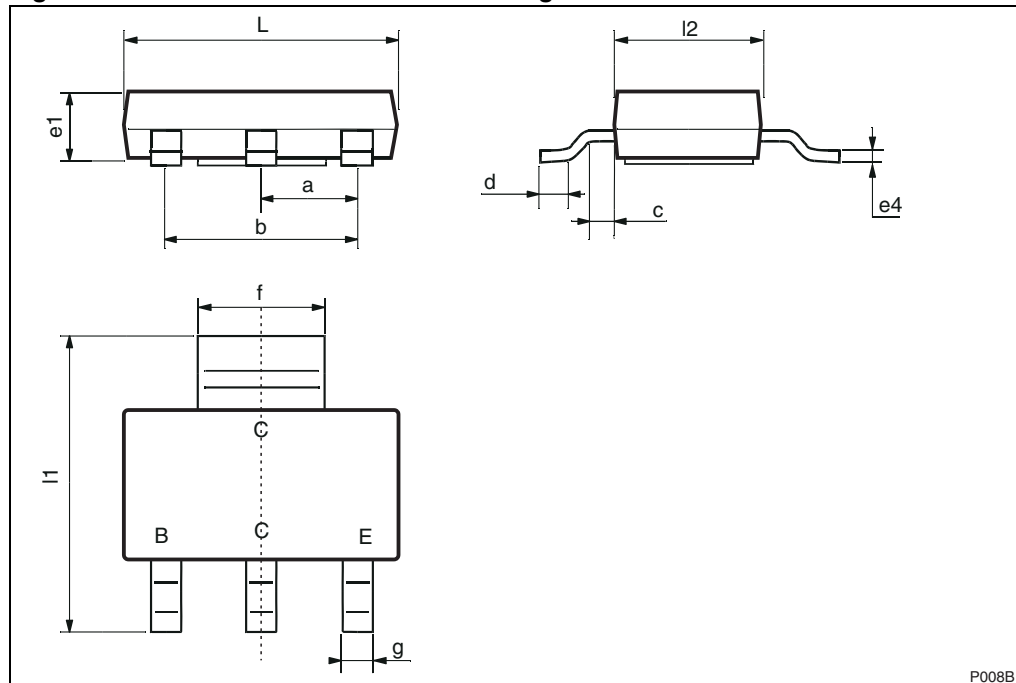
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
a	2.27	2.3	2.33
b	4.57	4.6	4.63
c	0.2	0.4	0.6
d	0.63	0.65	0.67
e1	1.5	1.6	1.7
e4			0.32
f	2.9	3	3.1
g	0.67	0.7	0.73
l1	6.7	7	7.3
l2	3.5	3.5	3.7
L	6.3	6.5	6.7

Figure 21. SOT-223 mechanical data drawing



P008B

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Jun-2010	1	First release.
08-Apr-2011	2	Document status promoted from preliminary data to datasheet.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

