

## 3.125 Gbps LVDS Buffer with Transmit Pre-Emphasis and Receive Equalization

### General Description

The DS25BR100 and DS25BR101 are single channel 3.125 Gbps LVDS buffers optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR100 and DS25BR101 feature transmit pre-emphasis (PE) and receive equalization (EQ), making them ideal for use as a repeater device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR110 features four levels of equalization for use as an optimized receiver device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. On the DS25BR100 the differential input and output is internally terminated with a 100Ω resistor to lower return losses, reduce component count and further minimize board space. For added design flexibility the 100Ω input terminations on the DS25BR101 have been eliminated. This enables a designer to adjust the termination for custom interconnect topologies and layout.

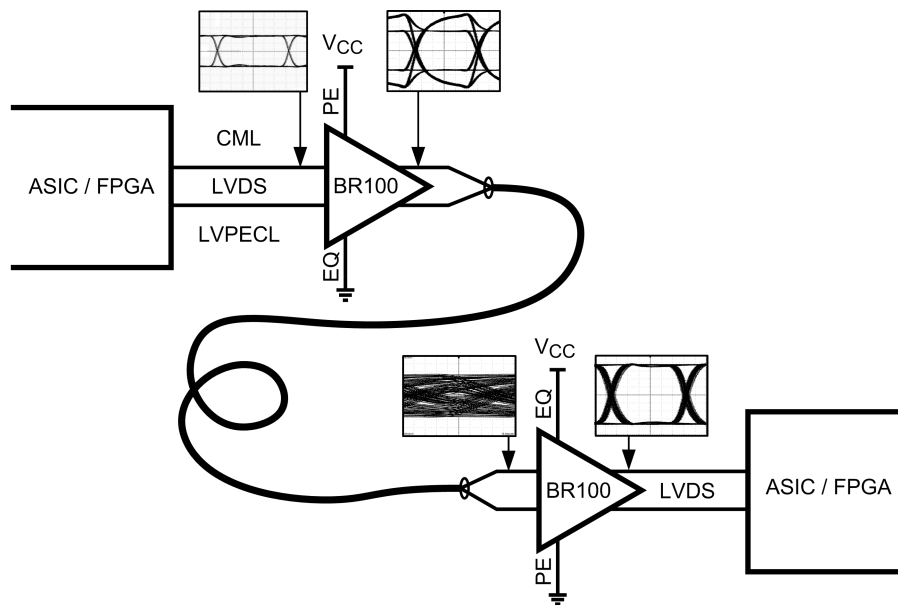
### Features

- DC - 3.125 Gbps low jitter, high noise immunity, low power operation
- Receive equalization reduces ISI jitter due to media loss
- Transmit pre-emphasis drives lossy backplanes and cables
- On-chip 100Ω input and output termination minimizes insertion and return losses, reduces component count and minimizes board space. The DS25BR101 eliminates the on-chip input termination for added design flexibility.
- 7 kV ESD on LVDS I/O pins protects adjoining components
- Small 3 mm x 3 mm LLP-8 space saving package

### Applications

- Clock and data buffering
- Metallic cable driving and equalization
- FR-4 equalization

### Typical Application



20179110

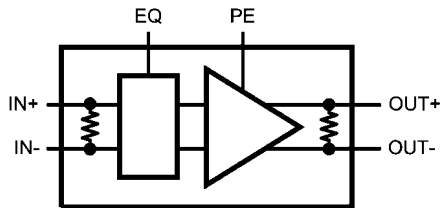
## Device Information

Device	Function	Termination Option	Available Signal Conditioning
DS25BR100	Buffer / Repeater	Internal 100Ω for LVDS inputs	2 Levels: PE and EQ
DS25BR101	Buffer / Repeater	External termination required	2 Levels: PE and EQ
DS25BR110	Receiver	Internal 100Ω for LVDS inputs	4 Levels: EQ
DS25BR120	Driver	Internal 100Ω for LVDS inputs	4 Levels: PE
DS25BR150	Buffer / Repeater	Internal 100Ω for LVDS inputs	None

## Ordering Information

NSID	Package	Tape & Reel QTY	Package Number
DS25BR100TSD	8 Lead LLP Package	1000	SDA08A
DS25BR100TSDX	8 Lead LLP Package	4500	SDA08A
DS25BR101TSD	8 Lead LLP Package	1000	SDA08A
DS25BR101TSDX	8 Lead LLP Package	4500	SDA08A

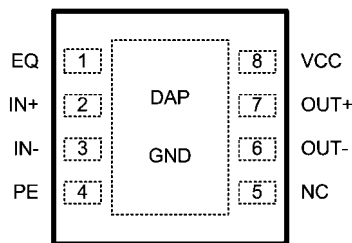
## Block Diagram



20179101

Note: DS25BR101 eliminates 100Ω input termination.

## Pin Diagram



20179104

## Pin Descriptions

Pin Name	Pin Name	Pin Type	Pin Description
EQ	1	Input	Equalizer select pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
PE	4	Input	Pre-emphasis select pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad).

## Control Pins (PE and EQ) Truth Table

EQ	PE	Equalization Level	Pre-emphasis Level
0	0	Low (Approx. 4 dB at 1.56 GHz)	Off
0	1	Low (Approx. 4 dB at 1.56 GHz)	Medium (Approx. 6 dB at 1.56 GHz)
1	0	Medium (Approx. 8 dB at 1.56 GHz)	Off
1	1	Medium (Approx. 8 dB at 1.56 GHz)	Medium (Approx. 6 dB at 1.56 GHz)

## Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V
LVCMOS Input Voltage (EQ, PE)	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Input Voltage (IN+, IN-)	-0.3V to +4V
LVDS Differential Input Voltage (DS25BR100)	0V to 1V
LVDS Differential Input Voltage (DS25BR101)	$V_{CC} + 0.6V$
LVDS Output Voltage (OUT+, OUT-)	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Differential Output Voltage ((OUT+) - (OUT-))	0V to 1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SDA Package	2.08W
Derate SDA Package	16.7 mW/°C above +25°C

Package Thermal Resistance

$\theta_{JA}$	+60.0°C/W
$\theta_{JC}$	+12.3°C/W

ESD Susceptibility

HBM (Note 1)	≥7 kV
MM (Note 2)	≥250V
CDM (Note 3)	≥1250V

**Note 1:** Human Body Model, applicable std. JESD22-A114C

**Note 2:** Machine Model, applicable std. JESD22-A115-A

**Note 3:** Field Induced Charge Device Model, applicable std. JESD22-C101-C

## Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Receiver Differential Input Voltage ( $V_{ID}$ ) (DS25BR100 only)			1.0	V
Operating Free Air Temperature ( $T_A$ )	-40	+25	+85	°C

## DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVCMOS INPUT DC SPECIFICATIONS (EQ, PE)</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$I_{IH}$	High Level Input Current	$V_{IN} = 3.6V$ $V_{CC} = 3.6V$		0	±10	µA
$I_{IL}$	Low Level Input Current	$V_{IN} = GND$ $V_{CC} = 3.6V$		0	±10	µA
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18 \text{ mA}, V_{CC} = 0V$		-0.9	-1.5	V
<b>LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)</b>						
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	350	450	mV
$\Delta V_{OD}$	Change in Magnitude of $V_{OD}$ for Complimentary Output States		-35		35	mV
$V_{OS}$	Offset Voltage	$R_L = 100\Omega$	1.05	1.2	1.375	V
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complimentary Output States		-35		35	mV
$I_{OS}$	Output Short Circuit Current (Note 10)	OUT to GND, PE = 0		-35	-55	mA
		OUT to $V_{CC}$ , PE = 0		7	55	mA
$C_{OUT}$	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
$R_{OUT}$	Output Termination Resistor	Between OUT+ and OUT-		100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVDS INPUT DC SPECIFICATIONS (IN+, IN-)</b>						
$V_{ID}$	Input Differential Voltage (Note 8)	$V_{CM} = +0.05V$ or $V_{CC}-0.05V$	0		1	V
$V_{TH}$	Differential Input High Threshold			0	+100	mV
$V_{TL}$	Differential Input Low Threshold		-100	0		mV
$V_{CMR}$	Common Mode Voltage Range	$V_{ID} = 100$ mV	0.05		$V_{CC} - 0.05$	V
$I_{IN}$	Input Current	$V_{IN} = GND$ or $3.6V$ $V_{CC} = 3.6V$ or $0.0V$		$\pm 1$	$\pm 10$	$\mu A$
$C_{IN}$	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
$R_{IN}$	Input Termination Resistor (Note 9)	Between IN+ and IN-		100		$\Omega$
<b>SUPPLY CURRENT</b>						
$I_{CC}$	Supply Current	EQ = 0, PE = 0		35	43	mA

**Note 4:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

**Note 5:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 6:** Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$  and  $\Delta V_{OD}$ .

**Note 7:** Typical values represent most likely parametric norms for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 8:** Input Differential Voltage ( $V_{ID}$ ) The DS25BR100 limits input amplitude to 1 volt. The DS25BR101 supports any  $V_{ID}$  within the supply voltage to GND range.

**Note 9:** Input Termination Resistor ( $R_{IN}$ ) The DS25BR100 provides an integrated 100 ohm input termination for the high speed LVDS pair. The DS25BR101 eliminates this internal termination.

**Note 10:** Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.

## AC Electrical Characteristics (Note 13)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 11, 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)</b>							
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 100\Omega$		350	465	ps	
$t_{PLHD}$	Differential Propagation Delay Low to High			350	465	ps	
$t_{SKD1}$	Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Note 14)			45	100	ps	
$t_{SKD2}$	Part to Part Skew (Note 15)			45	150	ps	
$t_{LHT}$	Rise Time	$R_L = 100\Omega$		80	150	ps	
$t_{HLT}$	Fall Time			80	150	ps	
<b>JITTER PERFORMANCE WITH PE = OFF AND EQ = LOW (Figures 6, 7)</b>							
$t_{RJ1A}$	Random Jitter (RMS Value) Input Test Channel D (Note 16)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ Clock (RZ) PE = 0, EQ = 0	2.5 Gbps		0.5	1	ps
$t_{RJ2A}$			3.125 Gbps		0.5	1	ps
$t_{DJ1A}$	Deterministic Jitter (Peak to Peak) Input Test Channel D (Note 17)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ K28.5 (NRZ) PE = 0, EQ = 0	2.5 Gbps		1	16	ps
$t_{DJ2A}$			3.125 Gbps		11	31	ps
$t_{TJ1A}$	Total Jitter (Peak to Peak) Input Test Channel D (Note 18)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ PRBS-23 (NRZ) PE = 0, EQ = 0	2.5 Gbps		0.03	0.09	UI <sub>P,P</sub>
$t_{TJ2A}$			3.125 Gbps		0.06	0.14	UI <sub>P,P</sub>
<b>JITTER PERFORMANCE WITH PE = OFF AND EQ = MEDIUM (Figures 6, 7)</b>							
$t_{RJ1B}$	Random Jitter (RMS Value) Input Test Channel E (Note 16)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ Clock (RZ) PE = 0, EQ = 1	2.5 Gbps		0.5	1	ps
$t_{RJ2B}$			3.125 Gbps		0.5	1	ps
$t_{DJ1B}$	Deterministic Jitter (Peak to Peak) Input Test Channel E (Note 17)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ K28.5 (NRZ) PE = 0, EQ = 1	2.5 Gbps		10	29	ps
$t_{DJ2B}$			3.125 Gbps		27	43	ps
$t_{TJ1B}$	Total Jitter (Peak to Peak) Input Test Channel E (Note 18)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ PRBS-23 (NRZ) PE = 0, EQ = 1	2.5 Gbps		0.07	0.12	UI <sub>P,P</sub>
$t_{TJ2B}$			3.125 Gbps		0.12	0.17	UI <sub>P,P</sub>
<b>JITTER PERFORMANCE WITH PE = MEDIUM AND EQ = LOW (Figures 5, 7)</b>							
$t_{RJ1C}$	Random Jitter (RMS Value) Input Test Channel D Output Test Channel B (Note 16)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ Clock (RZ) PE = 1, EQ = 0	2.5 Gbps		0.5	1	ps
$t_{RJ2C}$			3.125 Gbps		0.5	1	ps
$t_{DJ1C}$	Deterministic Jitter (Peak to Peak) Input Test Channel D Output Test Channel B (Note 17)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ K28.5 (NRZ) PE = 1, EQ = 0	2.5 Gbps		29	57	ps
$t_{DJ2C}$			3.125 Gbps		29	51	ps
$t_{TJ1C}$	Total Jitter (Peak to Peak) Input Test Channel D Output Test Channel B (Note 18)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ PRBS-23 (NRZ) PE = 1, EQ = 0	2.5 Gbps		0.10	0.19	UI <sub>P,P</sub>
$t_{TJ2C}$			3.125 Gbps		0.13	0.22	UI <sub>P,P</sub>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>JITTER PERFORMANCE WITH PE = MEDIUM AND EQ = MEDIUM (Figures 5, 7)</b>						
$t_{RJ1D}$	Random Jitter (RMS Value)	$V_{ID} = 350 \text{ mV}$	2.5 Gbps		0.5	1.1 ps
$t_{RJ2D}$	Input Test Channel E Output Test Channel B (Note 16)	$V_{CM} = 1.2\text{V}$ Clock (RZ) PE = 1, EQ = 1	3.125 Gbps		0.5	1 ps
$t_{DJ1D}$	Deterministic Jitter (Peak to Peak)	$V_{ID} = 350 \text{ mV}$	2.5 Gbps		41	77 ps
$t_{DJ2D}$	Input Test Channel E Output Test Channel B (Note 17)	$V_{CM} = 1.2\text{V}$ K28.5 (NRZ) PE = 1, EQ = 1	3.125 Gbps		46	98 ps
$t_{TJ1D}$	Total Jitter (Peak to Peak)	$V_{ID} = 350 \text{ mV}$	2.5 Gbps		0.13	0.20 $U_{I_{P-P}}$
$t_{TJ2D}$	Input Test Channel E Output Test Channel B (Note 18)	$V_{CM} = 1.2\text{V}$ PRBS-23 (NRZ) PE = 1, EQ = 1	3.125 Gbps		0.19	0.30 $U_{I_{P-P}}$

**Note 11:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 12:** Typical values represent most likely parametric norms for  $V_{CC} = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 13:** Specification is guaranteed by characterization and is not tested in production.

**Note 14:**  $t_{SKD1}, |t_{PLHD} - t_{PHLD}|$ , is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

**Note 15:**  $t_{SKD2}$ , Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.

**Note 16:** Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

**Note 17:** Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

**Note 18:** Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

## DC Test Circuits

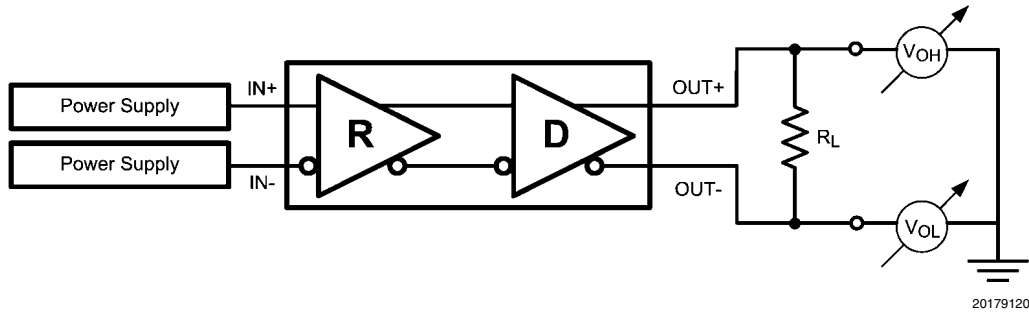


FIGURE 1. Differential Driver DC Test Circuit

## AC Test Circuits and Timing Diagrams

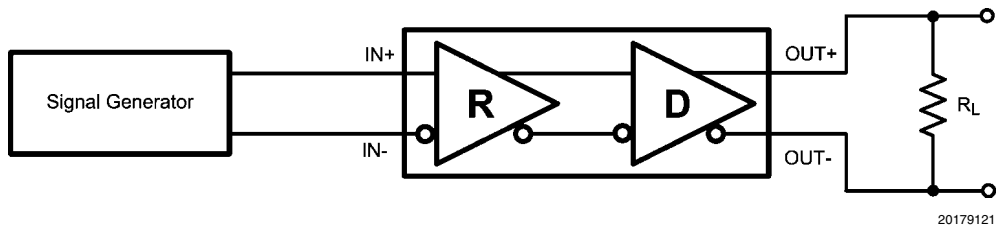


FIGURE 2. Differential Driver AC Test Circuit

Note: DS25BR101 requires external 100Ω input termination.

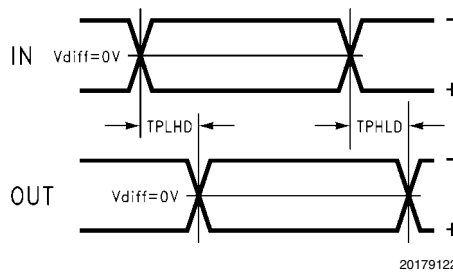


FIGURE 3. Propagation Delay Timing Diagram

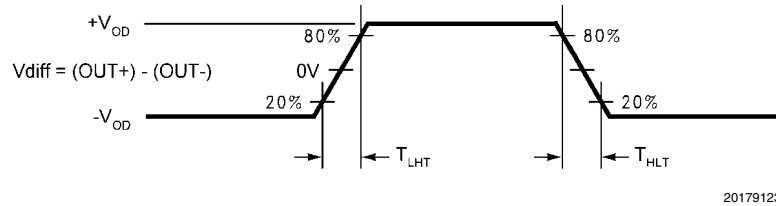
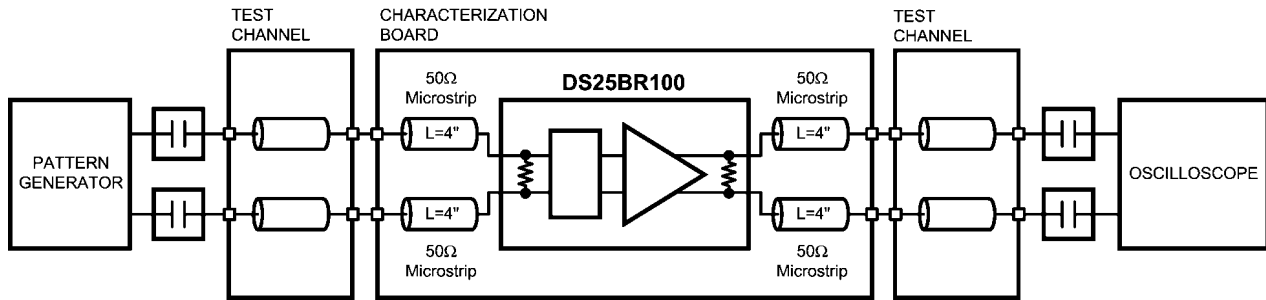


FIGURE 4. LVDS Output Transition Times



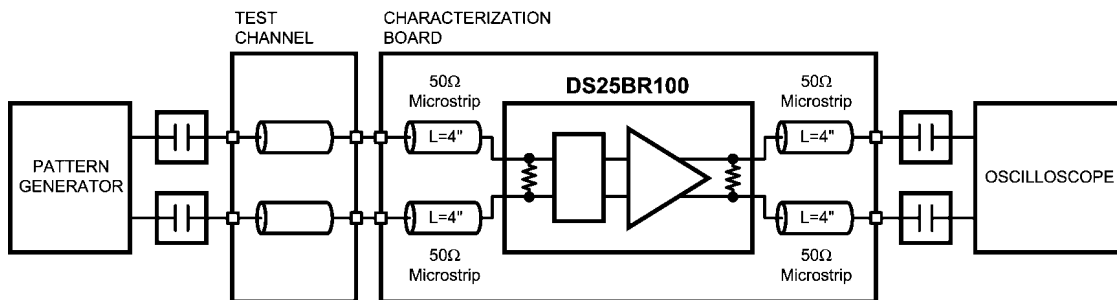
## Pre-Emphasis and Equalization Test Circuits



20179127

FIGURE 5. Pre-emphasis and Equalization Performance Test Circuit

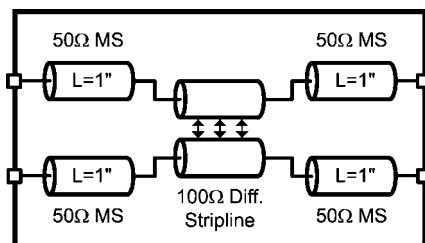
Note: DS25BR101 requires external 100Ω input termination.



20179126

FIGURE 6. Equalization Performance Test Circuit

Note: DS25BR101 requires external 100Ω input termination.



20179128

FIGURE 7. Test Channel Description

### Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric con-

stant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

## Device Operation

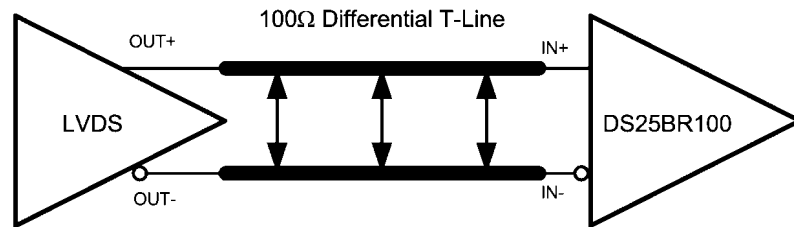
### INPUT INTERFACING

The DS25BR100/101 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR100/101 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.

The DS25BR100 inputs are internally terminated with a 100Ω resistor for optimal device performance, reduced component count, and minimum board space. External input terminations on the DS25BR101 need to be placed as close as possible to the device inputs to achieve equivalent AC per-

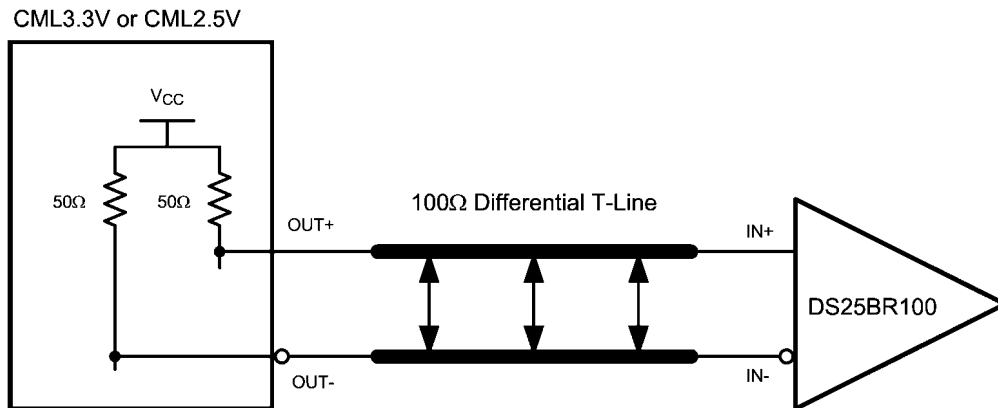
formance. It is recommended that SMT resistors sized 0402 or smaller be used and the mounting distance to the DS25BR101 pins kept under 200 mils.

When using the DS25BR101 in a limited multi-drop topology, any transmission line stubs should be kept very short to minimize any negative effects on signal quality. A single termination resistor or resistor network that matches the differential line impedance should be used. If DS25BR101 input pairs from two separate devices are to be connected to a single differential output, it is recommended that the DS25BR101 devices are mounted directly opposite of each other. One on top of the PCB and the other directly under the first on the bottom of the PCB, this keeps the distance between inputs equal to the PCB thickness.



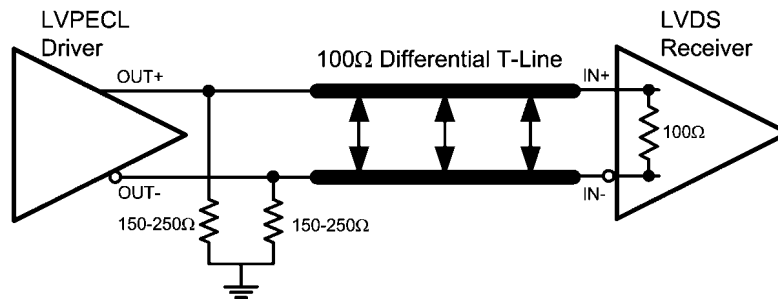
Typical LVDS Driver DC-Coupled Interface to DS25BR100 Input

20179111



Typical CML Driver DC-Coupled Interface to DS25BR100 Input

20179112



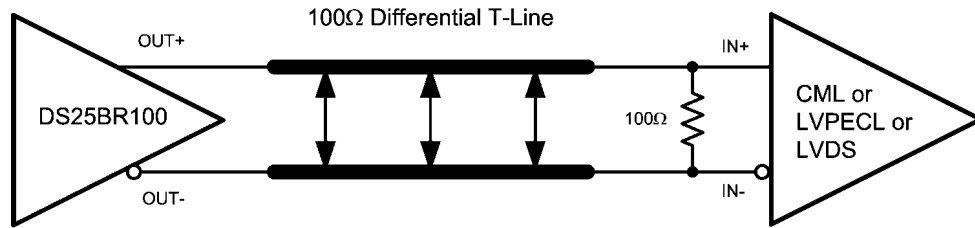
Typical LVPECL Driver DC-Coupled Interface to DS25BR100 Input <sup>20179113</sup>

Note: DS25BR101 requires external 100Ω input termination.

### OUTPUT INTERFACING

The DS25BR100/101 outputs signals compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that

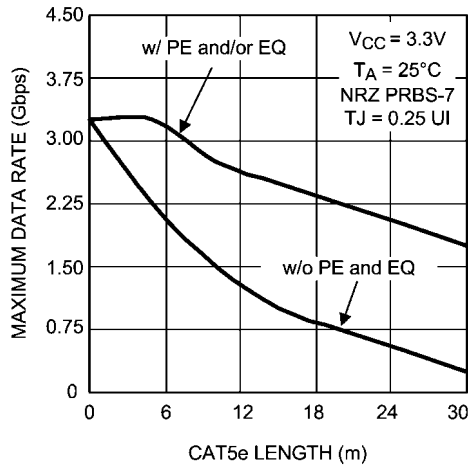
the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



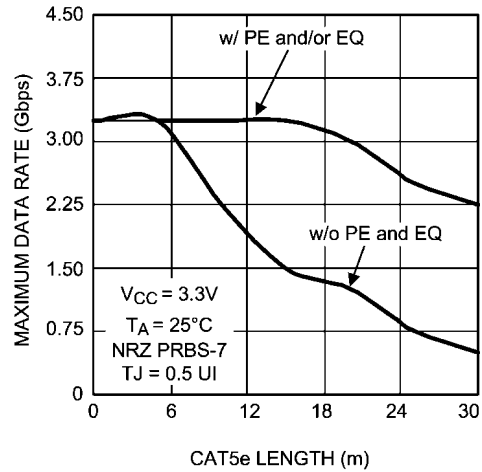
Typical Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

20179114

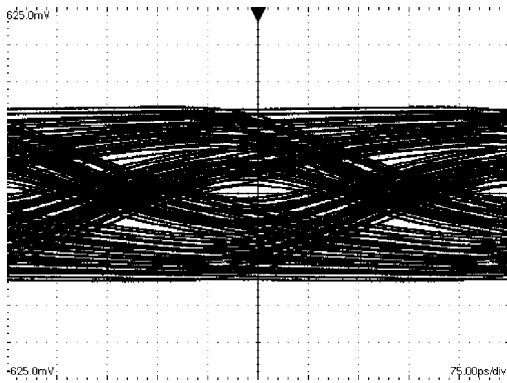
# Typical Performance



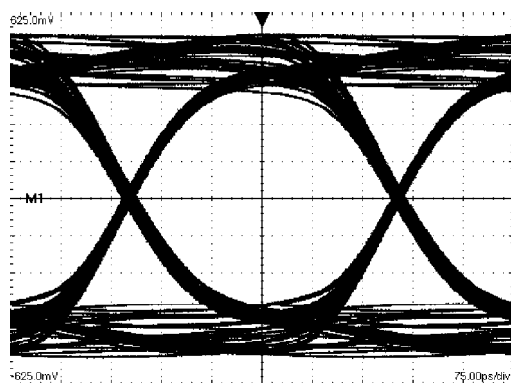
20179134  
**Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length**



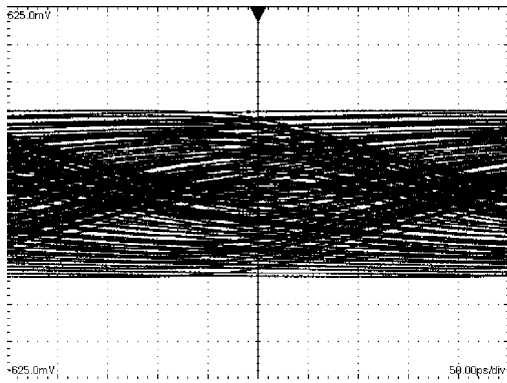
20179135  
**Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length**



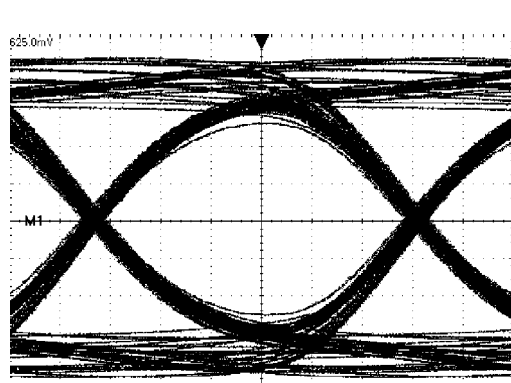
20179130  
**A 2.5 Gbps NRZ PRBS-7 After 60" Differential FR-4 Stripline**  
 V:125 mV / DIV, H:75 ps / DIV



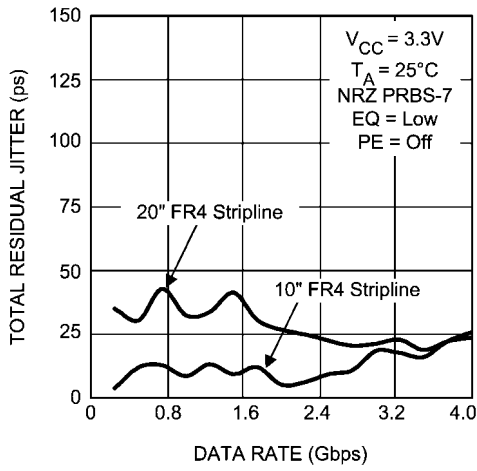
20179131  
**An Equalized (with PE and EQ) 2.5 Gbps NRZ PRBS-7 After The 40" Input and 20" Output Differential Stripline (Figure 5)**  
 V:125 mV / DIV, H:75 ps / DIV



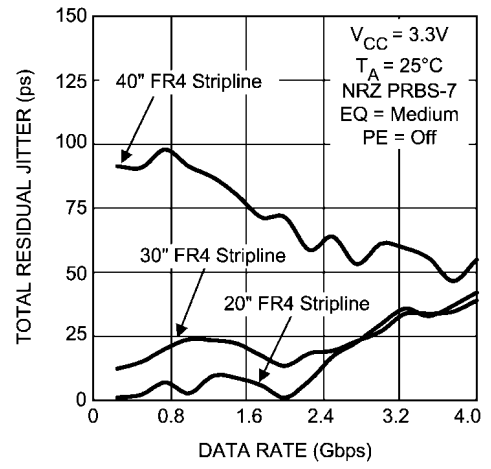
20179132  
**A 3.125 Gbps NRZ PRBS-7 After 60" Differential FR-4 Stripline**  
 V:125 mV / DIV, H:50 ps / DIV



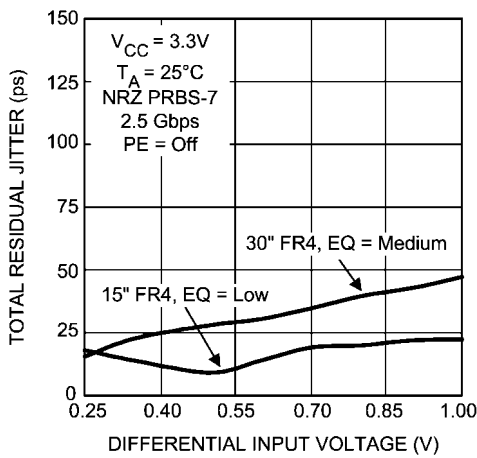
20179133  
**An Equalized (with PE and EQ) 3.125 Gbps NRZ PRBS-7 After The 40" Input and 20" Output Differential Stripline (Figure 5)**  
 V:125 mV / DIV, H:50 ps / DIV



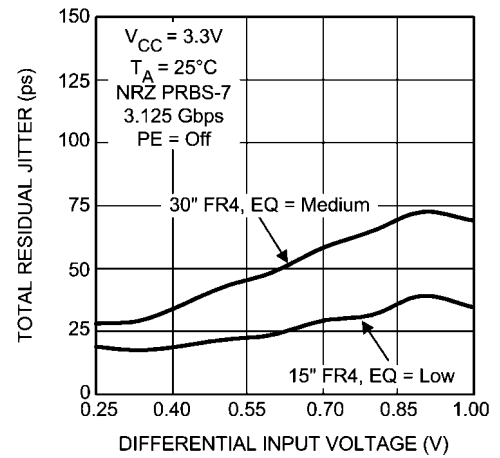
Total Jitter as a Function of Data Rate



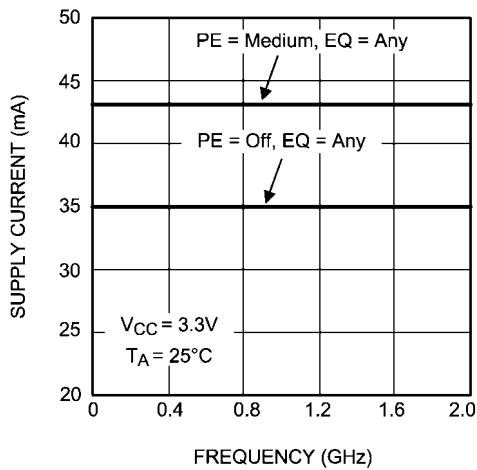
Total Jitter as a Function of Data Rate



Total Jitter as a Function of Input Amplitude

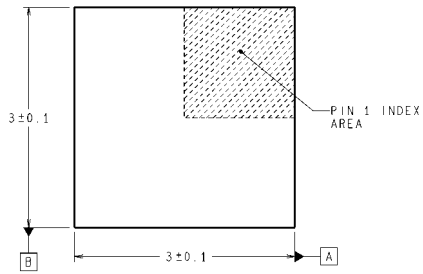
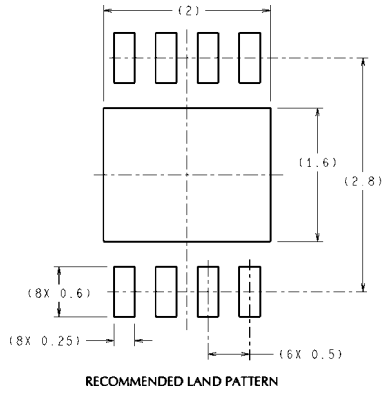


Total Jitter as a Function of Input Amplitude

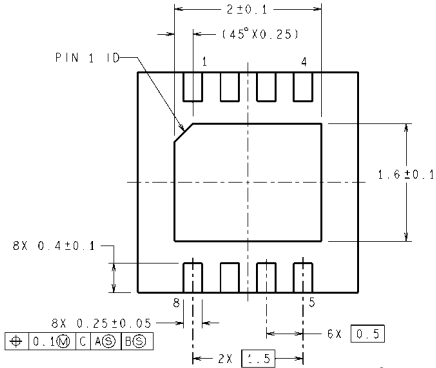
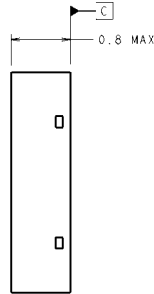


Power Supply Current as a Function of Frequency

**Physical Dimensions** inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



SDA08A (Rev A)

**Order Number DS25BR100TSD**  
**Order Number DS25BR101TSD**  
**NS Package Number SDA08A**  
**(See AN-1187 for PCB Design and Assembly Recommendations)**

## Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	<a href="http://www.national.com/amplifiers">www.national.com/amplifiers</a>	WEBENCH® Tools	<a href="http://www.national.com/webench">www.national.com/webench</a>
Audio	<a href="http://www.national.com/audio">www.national.com/audio</a>	App Notes	<a href="http://www.national.com/appnotes">www.national.com/appnotes</a>
Clock and Timing	<a href="http://www.national.com/timing">www.national.com/timing</a>	Reference Designs	<a href="http://www.national.com/refdesigns">www.national.com/refdesigns</a>
Data Converters	<a href="http://www.national.com/adc">www.national.com/adc</a>	Samples	<a href="http://www.national.com/samples">www.national.com/samples</a>
Interface	<a href="http://www.national.com/interface">www.national.com/interface</a>	Eval Boards	<a href="http://www.national.com/evalboards">www.national.com/evalboards</a>
LVDS	<a href="http://www.national.com/lvds">www.national.com/lvds</a>	Packaging	<a href="http://www.national.com/packaging">www.national.com/packaging</a>
Power Management	<a href="http://www.national.com/power">www.national.com/power</a>	Green Compliance	<a href="http://www.national.com/quality/green">www.national.com/quality/green</a>
Switching Regulators	<a href="http://www.national.com/switchers">www.national.com/switchers</a>	Distributors	<a href="http://www.national.com/contacts">www.national.com/contacts</a>
LDOs	<a href="http://www.national.com/ldo">www.national.com/ldo</a>	Quality and Reliability	<a href="http://www.national.com/quality">www.national.com/quality</a>
LED Lighting	<a href="http://www.national.com/led">www.national.com/led</a>	Feedback/Support	<a href="http://www.national.com/feedback">www.national.com/feedback</a>
Voltage Reference	<a href="http://www.national.com/vref">www.national.com/vref</a>	Design Made Easy	<a href="http://www.national.com/easy">www.national.com/easy</a>
PowerWise® Solutions	<a href="http://www.national.com/powerwise">www.national.com/powerwise</a>	Solutions	<a href="http://www.national.com/solutions">www.national.com/solutions</a>
Serial Digital Interface (SDI)	<a href="http://www.national.com/sdi">www.national.com/sdi</a>	Mil/Aero	<a href="http://www.national.com/milaero">www.national.com/milaero</a>
Temperature Sensors	<a href="http://www.national.com/tempensors">www.national.com/tempensors</a>	SolarMagic™	<a href="http://www.national.com/solarmagic">www.national.com/solarmagic</a>
Wireless (PLL/VCO)	<a href="http://www.national.com/wireless">www.national.com/wireless</a>	PowerWise® Design University	<a href="http://www.national.com/training">www.national.com/training</a>

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

#### LIFE SUPPORT POLICY

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2009 National Semiconductor Corporation

For the most current product information visit us at [www.national.com](http://www.national.com)



**National Semiconductor Americas Technical Support Center**  
 Email: [support@nsc.com](mailto:support@nsc.com)  
 Tel: 1-800-272-9959

**National Semiconductor Europe Technical Support Center**  
 Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)

**National Semiconductor Asia Pacific Technical Support Center**  
 Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor Japan Technical Support Center**  
 Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)