# Ayama™ 10000A
# Network Search Engine

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- Multiple width tables in a single device
- Single-cycle Search operation on 72-/144-bit tables
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- Prioritized blocks with no overhead in table management using programmable Soft Priority™
- Parity support for reliable operation
- Non-Enhanced Mode and Enhanced Mode operation
  - Up to 133 million searches per second in 72-/144-bit configuration
  - Up to 66.5 million searches per second in 36-/288-bit configuration
  - Up to 33.25 million searches per second in 576-bit configuration (Enhanced Mode Only)
- Enhanced Mode with Multi Width MultiSearch™ operation
  - Up to 266 million searches per second in 72-/144-bit configuration
  - Up to 133 million searches per second in 36-/288-bit configuration
  - Up to 66.5 million searches per second in 576-bit configuration
- Cascadable for depth expansion
- Glueless interface to industry-standard SRAMs and SSRAMs
- Simple hardware instruction interface
- IEEE 1149.1 test access port
- 1.2V core voltage supply
- Supports 1.5V HSTL and 1.8V/2.5V LVCMOS I/O standards
- 388-pin BGA package

## 2.0 Overview

Cypress Semiconductor Corporation's (Cypress's) Ayama™ 10000A Network Search Engine (NSE) is designed to be a high-performance, pipelined, synchronous, 512K/256K/128K 36-bit entries NSE. This high-speed, high-capacity Ayama 10000A NSE can be deployed in a variety of networking and communications applications. It can be used to accelerate network protocols such as Longest-Prefix Match (CIDR), ARP, MPLS, and other layer 2, 3, and 4 protocols. The performance and features of the Ayama 10000A make it attractive in applications such as Enterprise LAN switches and routers, and broadband switching and/or routing equipment that supports multiple data rates at OC–48 and beyond. Ayama 10000A can operate at a maximum performance of 266 million searches per second (MSPS).

The Ayama 10000A is designed to be scalable in order to support network database sizes of up to 15872K 36-bit entries specifically for environments that require large network policy databases. It includes features that ease table management, reduce power consumption and improve data integrity. The device can have its features individually enabled or disabled for flexibility based on the needs of the applications. The Ayama 10000A's Data and Mask arrays that make up the Core are organized into blocks that can be individually configured to optimize the device performance and provide even more flexibility.

*Figure 2-1* below shows the block diagram of the Ayama 10000A. (See *Table 3-1* for signal descriptions.)

*Figure 2-2* shows how an NSE subsystem can be formed using a host ASIC, a bank of Ayama 10000A devices and a bank of SRAM devices. (See *Table 3-1* for signal descriptions.) It presents an example of how the NSE subsystem is integrated in a switch or router. The example also shows two possible ways of connecting the devices in the NSE subsystem. In the Associative set-up, the host ASIC sends instructions to the NSE. Where applicable, the NSE drives the SRAM inputs and the SRAM then returns the requested data to the host ASIC. In the Index set-up, the NSE's SRAM address information is routed back to the host ASIC. The host ASIC then interacts with the SRAM bank after it receives the result from the NSE.

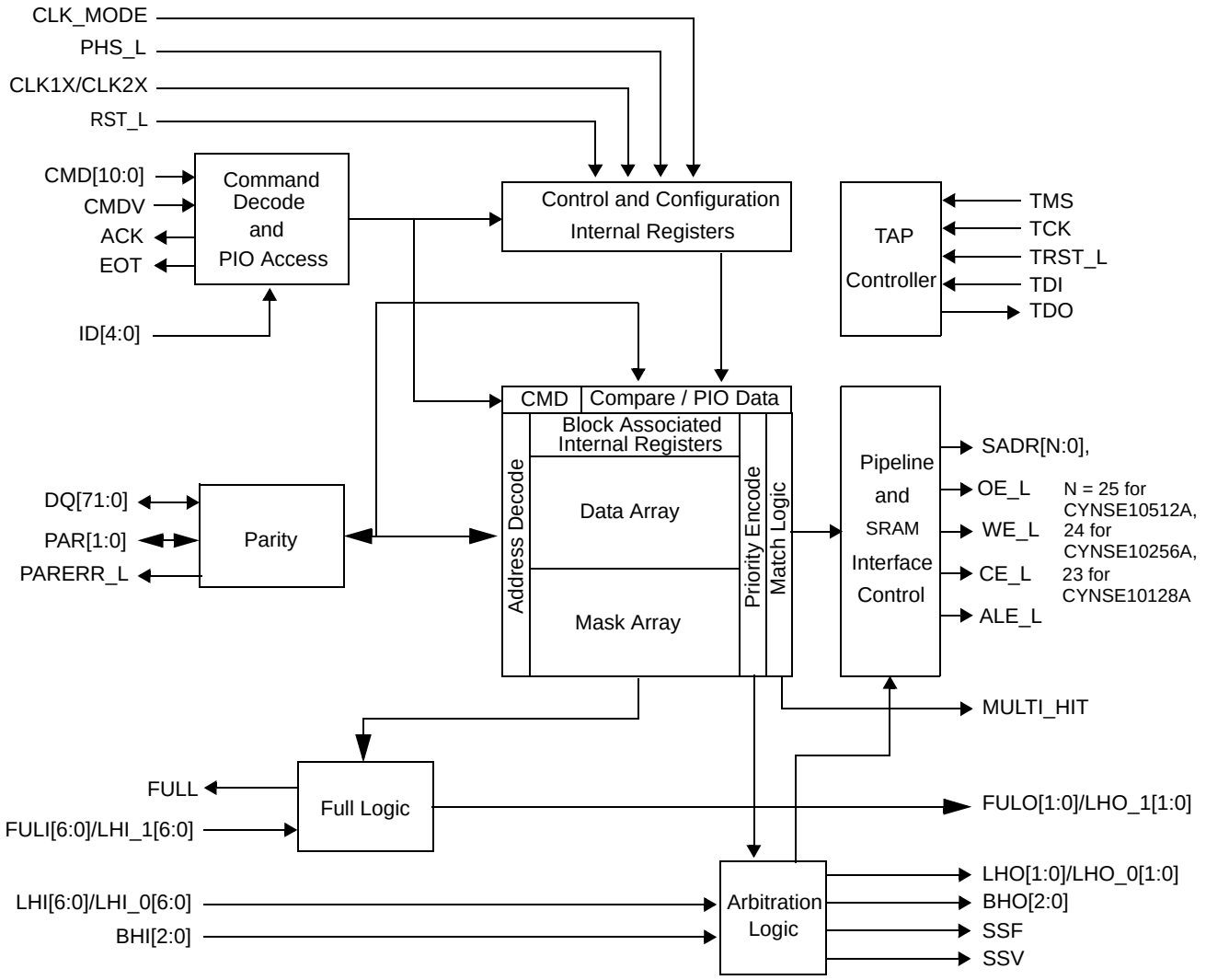



**Figure 2-1. Ayama™ 10000A Block Diagram**

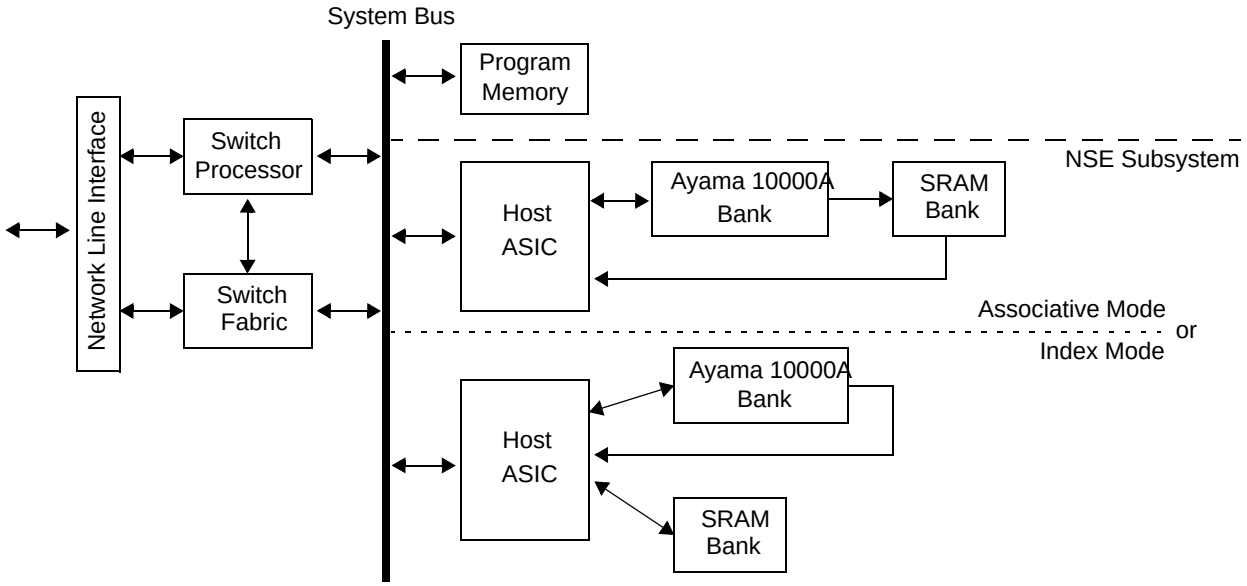



**Figure 2-2. Example of Switch/Router Implementation Using Ayama 10000A**

## 3.0 Signal Description

*Table 3-1* lists and describes all Ayama 10000A signals.

**Table 3-1. Ayama™ 10000A Signal Description**

| Parameter | Type[1], Supply | Description |
|---|---|---|
| **Clocks and Reset** | | |
| CLK_MODE | I, $V_{DDQ\_ASIC}$ | **Clock Mode**. Selects the clock source for the device. When set to Low, the device uses both CLK2X and PHS_L for its clock sources. When pulled High ($V_{DDQ\_ASIC}$), the device uses CLK1X for its clock source (PHS_L must be externally grounded). |
| CLK2X/CLK1X | I, $V_{DDQ\_ASIC}$ | **Master Clock**. CLK_MODE selects either the CLK2X or CLK1X as the clock input signal. CLK1X.<br>Input signals are sampled on both rising and falling edges. Output signals can be driven on both falling and rising depending on the operation and the device configuration.<br>CLK2X<br>Input signals are sampled on the rising edge.Output signals are driven on the rising edge. |
| PHS_L | I, $V_{DDQ\_ASIC}$ | **Phase**. An input signal that must switch at half the frequency of CLK2X. This signal should be pulled LOW when the device is in CLK1X mode. See Section 5.6, “Clocks,” on page 42. |
| RST_L | I, $V_{DDQ\_ASIC}$ | **Reset**. Driving RST_L LOW initializes the device to the default state. The device becomes active stable 4 CLK1X (8 CLK2X) cycles after RST_L is driven High (90% threshold). |
| **Configuration** | | |
| CFG_L | I, $V_{DDQ\_ASIC}$ | **Configuration**. CFG_L is provided for backward compatibility with the older generation of Cypress NSE CYNSE70000 devices, which had DQ bus width of 68-bits.When CFG_L is set to Low, the device will tristate DQ[71:68]. If the Ayama 10000A is being operated as 72-bit NSE, then CFG_L must be tied high to $V_{DDQ\_ASIC}$ |
| ID[4:0] | I, $V_{DDQ\_ASIC}$ | **Device Identification**. The binary-encoded device identification for a depth-cascaded system starts at “00000” and goes up to “11110”. “11111” is reserved as the broadcast address which selects all NSEs in the cascade.<br>On a broadcast Read, only the device with the LDEV bit set to ‘1’ will respond.<br>Any ID bit that is to be set High must be connected to $V_{DDQ\_ASIC}$. |
| ASICSEL | I, $V_{DDQ\_ASIC}$ | **ASIC IO Select**. When this signal is pulled High (1.8V or 2.5V LVCMOS), the Command, Data and Cascade buses will operate in LVCMOS mode. When tied to Low, the buses will operate in HSTL mode.Signals affected by ASICSEL selection:<br>*Clocks*: CLK2X/CLK1X, PHS_L, RST_L<br>*Command and Data*:CMD[10:0], CMDV, DQ[71:0], PAR[1:0], ACK, EOT, SSF, SSV, MULTI_HIT<br>*Cascade Interface*: LHI[6:0], LHO[1:0], BHI[2:0], BHO[2:0], FULI[6:0], FULO[1:0], FULL |
| SRAMSEL | I, $V_{DDQ\_SRAM}$ | **SRAM IO Select**. When this signal is pulled High (1.8V or 2.5V LVCMOS), the SRAM Interface will operate in LVCMOS mode. When tied to Low, the interface will operate in HSTL mode.Signals affected by SRAMSEL selection:SADR[25:0], CE_L, WE_L, OE_L, ALE_L |
| HSVREF0 | I, $V_{DDQ\_ASIC}$ | **HSTL Reference Voltage**. When ASICSEL is set to GND, this signal must be connected to the HSTL reference voltage (VDDQ_ASIC/2). Otherwise, they should be left floating. |
| HSVREF1 | I, $V_{DDQ\_ASIC}$ | **HSTL Reference Voltage**. Refer to HSVREF0 description. |
| PARERR_L[2] | O $V_{DDQ\_ASIC}$ | **Parity Error**. This signal is updated when there is a Core parity error or DQ Bus parity error. It is an Active-Low Open-Drain signal that requires an external pull-up resistor to VDDQ_ASIC. This signal is valid only after the device is fully initialized. |
| **ASIC Interface / Command and Data Buses (LVCMOS or HSTL I/II)** | | |
| CMD[10:0] | I, $V_{DDQ\_ASIC}$ | **Command Bus**. Bit[10:2] contains the command parameters and Bit[1:0] specifies the command. |
| CMDV | I, $V_{DDQ\_ASIC}$ | **Command Valid**. This signal indicates valid command in the CMD bus when set to High. |

**Notes:**
1. I = Input only, I/O = input or output, O = output only (Always driven to 0 or 1, except when JTAG is enabled), OD = open-drain, T = three-state output.
2. The rise time of PARERR_L will depend on the value of the pull-up resistance. Sufficient delay should be allotted for in the error routine after clearing the parity error in the parity control register and before this pin is sampled as part of the next command. Recommended external pull-up resistance range: 4.7KΩ to 47KΩ.

**Table 3-1. Ayama™ 10000A Signal Description** (continued)

| Parameter | Type[1], Supply | Description |
|---|---|---|
| DQ[71:0] | I/O, $V_{DDQ\_ASIC}$ | **Address/Data Bus**. This signal carries the following information:<br>Search operation: Compare Data (Search Key)<br>SRAM PIO operations: SRAM Address<br>Other operations to Register, Data, and Mask Array regions: Address and Data |
| PAR[1:0] | I/O $V_{DDQ\_ASIC}$ | **Parity Bus**. These signals contain the even parity values for the DQ bus. On the Read return data, the NSE generates the parity bits. On all other operations these bits are externally driven. Bit [0] is the parity for all even DQ signals. Bit[1] is the parity for all odd DQ signals. |
| ACK[3] | T, $V_{DDQ\_ASIC}$ | **Read Acknowledge**. This signal indicates that valid data is available on the DQ bus during register, data, and mask array Read operations, or that the data is available on the SRAM data bus during SRAM Read operations. |
| EOT[3] | T, $V_{DDQ\_ASIC}$ | **End of Transfer**. This signal indicates the end of burst transfer to the data or mask array during Read or Write burst operations. |
| SSF[4] | T, $V_{DDQ\_ASIC}$ | **Search Successful Flag**. When asserted, this signal indicates that the device is the global winner in a Search operation. |
| SSV[4] | T, $V_{DDQ\_ASIC}$ | **Search Successful Flag Valid**. When asserted, it indicates valid SSF value. In Enhanced mode, this signal also indicates valid FULL and MULTI_HIT values. |
| MULTI_HIT[4] | O, $V_{DDQ\_ASIC}$ | **Multiple Hit Flag**. In a Search operation, this signal indicates that there are multiple entries in the array or in the selected blocks that match the Search key when it is set to 1. In a Learn operation, it indicates that there are multiple free entries.<br>In Non-Enhanced mode, it becomes valid four CLK1X cycles after the command is issued.<br>In Enhanced mode, it becomes valid when SSV is 1. |
| FULL | T, $V_{DDQ\_ASIC}$ | **Full Flag**. When High, it indicates that the table in the array or in the selected blocks (Enhanced mode) is full.<br>In the Non-Enhanced mode, it becomes valid four CLK1X cycles after the command is issued.<br>In the Enhanced mode, it becomes valid when SSV is 1. The FULL flag is only asserted when there is a Search Miss on a full device. A Search Hit on a full device would not assert the FULL flag. It is not driven when a Write or a Learn takes place. |
| HIGH_SPEED1 | I, $V_{DDQ\_ASIC}$ | **High Speed 1**. This signal must be pulled High ($V_{DDQ\_ASIC}$) when the device operates at CLK2X frequency greater than or equal to 166 MHz but less than 200 MHz. |
| HIGH_SPEED2 | I, $V_{DDQ\_ASIC}$ | **High Speed 2**. This signal must be pulled High ($V_{DDQ\_ASIC}$) when the device operates at CLK2X frequency greater than or equal to 200 MHz, with High Speed 1 tied Low. |
| HIGH_SPEEDI_L | I, $V_{DDQ\_ASIC}$ | **High Speed I_L**. When High ($V_{DDQ\_ASIC}$), High-speed feature disabled. When Low, Highspeed feature is enabled and is configurable through HARDWARE register. |
| **SRAM Interface (LVCMOS or HSTL I/II)** | | |
| SADR[M:0][4] | T, $V_{DDQ\_SRAM}$ | **SRAM Address**. This bus contains address lines to access off-chip SRAMs that contain associative data. In a cascaded system of multiple Ayama 10000A NSEs, each corresponding SADR bit from all cascaded devices must be tied together.<br>M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A. |
| CE_L[4] | T, $V_{DDQ\_SRAM}$ | **SRAM Chip Enable**. This is the chip enable (CE) control for external SRAMs. In a cascaded system of multiple Ayama 10000A NSEs, CE_L of all cascaded devices must be tied together. This signal is then driven by only one of the devices that acts as a master device. |
| WE_L[4] | T, $V_{DDQ\_SRAM}$ | **SRAM Write Enable**. This is the Write enable control for external SRAMs. In a cascaded system of multiple Ayama 10000A NSEs, WE_L of all cascaded devices must be tied together. This signal is then driven by only one of the devices. |
| OE_L[4] | T, $V_{DDQ\_SRAM}$ | **SRAM Output Enable**. This is the output enable (OE) control for external SRAMs. Only the last device drives this signal (the device that has the LRAM bit set). |
| ALE_L[4] | T, $V_{DDQ\_SRAM}$ | **Address Latch Enable**. When this signal is Low, the addresses are valid on the SRAM address bus. In a cascaded system of multiple Ayama 10000As, the ALE_L of all cascaded devices must be tied together. This signal is then driven by only one of the devices. |

**Notes:**

3. Require an external pull-down resistor such as 47KΩ or 100KΩ. For terminated lines, a 70-ohm pull-down and 165-ohm pull-up resistor combination is recommended.
4. These signals will output at the rising edge of CLK2X (both rising and falling edges of CLK1X) in a MultiSearch operation.

**Table 3-1. Ayama™ 10000A Signal Description** (continued)

| Parameter | Type[1], Supply | Description |
|---|---|---|
| **Cascade Interface (LVCMOS and HSTL I/II)** | | |
| LHI[6:0]<br>LHI_0[6:0] (MSE=1) | I, $V_{DDQ\_ASIC}$ | **Local Hit In/Local Hit In Array 0**. These signals are inputs from upstream devices in a cascade that indicate whether there is a hit in the upstream/previous device(s).<br>When MultiSearch is performed, LHI[6:0] becomes LHI_0[6:0] (Local Hit input signals for Array 0). |
| LHO[1:0]<br>LHO_0[1:0] (MSE=1) | O, $V_{DDQ\_ASIC}$ | **Local Hit Out/ Local Hit Out Array 0**. LHO[1] and LHO[0] are logically the same signal. One of these signal is connected to one input on the LHI bus of the downstream devices in a cascade.<br>When MultiSearch is performed, LHO[1:0] becomes LHO_0[1:0] (Local Hit output signals for Array 0). |
| BHI[2:0] | I, $V_{DDQ\_ASIC}$ | **Block Hit In**. These signals are inputs from the last device in the upstream blocks in a cascade that indicate whether there is a hit in the upstream/previous block(s). |
| BHO[2:0] | O, $V_{DDQ\_ASIC}$ | **Block Hit Out**. These signals are logically the same signal. One of these signals is connected to one input on the BHI bus of the downstream devices in the downstream blocks. |
| FULI[6:0]<br>LHI_1_L[6:0] (MSE=1) | I, $V_{DDQ\_ASIC}$ | **Full In/Local Hit In Array 1**. Each signal is driven by an upstream device's FULO output in a block to generate the FULL signal for that block. During a Search operation, these signals indicate whether an upstream device had a free entry for a future Learn.<br>When MultiSearch is performed, FULI[6:0] becomes active Low LHI_1_L[6:0] (Local Hit input signals for Array 1). |
| FULO[1:0]<br>LHO_1_L[1:0] (MSE=1) | O, $V_{DDQ\_ASIC}$ | **Full Out/Local Hit Out Array 1**. FULO[0] and FULO[1] are logically the same signal. One of these signal is connected to one input on the FULO bus of the downstream devices in a cascade.<br>When MultiSearch is performed, FULO[1:0] becomes active Low LHO_0_L[1:0] (Local Hit output signals for Array 1). |
| **Supplies** | | |
| $V_{DD}$ | | **Core Supply**: 1.2V. |
| $V_{DD\_PLL}$ | | **PLL Block Supply**: 1.2V. |
| $V_{DDQ\_ASIC}$ | | **ASIC and Cascade Interface I/O Supply**: 1.5V (HSTL) or 1.8V/2.5V (LVCMOS). |
| $V_{DDQ\_SRAM}$ | | **SRAM Interfaced I/O Supply**: 1.5V (HSTL) or 1.8V/2.5V (LVCMOS). |
| $V_{DDQ\_JTAG}$ | | **JTAG Test Access Port I/O Supply**: 1.8V/2.5V (LVCMOS). |
| **Test Access Port** | | |
| TDI | I, $V_{DDQ\_JTAG}$ | Test access port test data in. |
| TCK | I, $V_{DDQ\_JTAG}$ | Test access port test clock. |
| TDO | T, $V_{DDQ\_JTAG}$ | Test access port test data out. |
| TMS | I, $V_{DDQ\_JTAG}$ | Test access port test mode select. |
| TRST_L | I, $V_{DDQ\_JTAG}$ | Test access port reset. |

## 4.0 Device Architecture Overview

### 4.1 Data Array, Mask Array and Table Widths

The Ayama 10000A device consists of M × 72-bit (M = 256K for CYNSE10512A, 128K for CYNSE10256A, 64K for CYNSE10128A) storage cells referred to as data bits. There is also a mask cell corresponding to each data cell. A database entry includes both the data and mask cells. *Figure 4-1* shows the four possible table width sizes of the data and mask cells and the maximum possible table depth for each width.

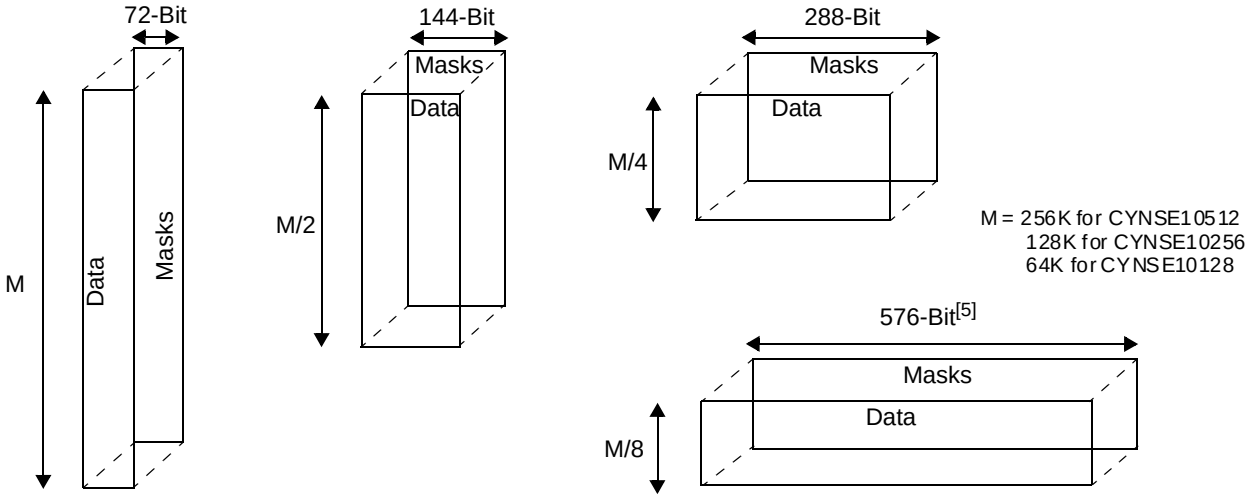



**Figure 4-1. Ayama 10000A Database Table Widths**

The Ayama 10000A can be configured to contain tables of different widths in one device up to a maximum equal to 512K/256K/128K 72-bit entries. For example, a single Ayama 10000A device can have both a 5-Tuple Flow table and an IPv6 forwarding table. *Figure 4-2* shows a sample configuration of multiple table widths in a CYNSE10512A device.

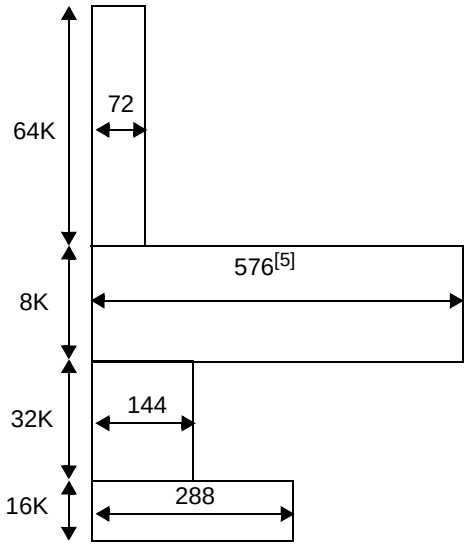



**Figure 4-2. Multi-Width Database Configuration Example**

**Note:**
5. 576-bit table configuration is only supported in the Enhanced mode.

## 4.2 Data and Mask Addressing

Each 72-bit entry in the device can be accessed directly through its address index. With configurations greater than 72-bit entries, the search address results are multiplied accordingly. For example, in 72-bit configurations, the resultant search addresses are 0,1,2,..., N. However, in 144-bit configurations, the resultant search addresses are 0,2,4,...,N-2.

The data and mask arrays addresses are as shown in *Figure 4-3*.

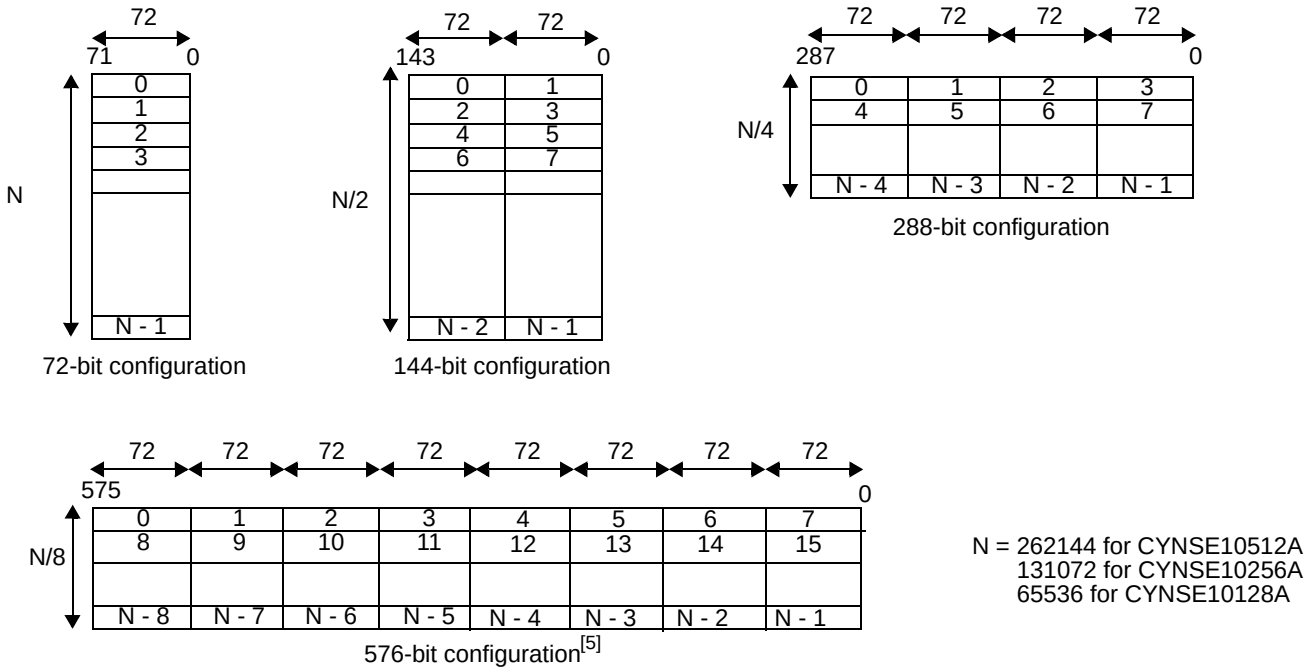



**Figure 4-3. Addressing the Ayama 10000A Data and Mask Arrays**

## 4.3 Successful Search and Multiple Match Arbitration

During a Search operation, the search data bit is masked with the corresponding global mask bit from the selected Global Mask Register and the mask array bit before being compared to the data array entry bit to check for a match at that bit position (see *Table 4-1*). The entry with a match on every bit position results in a successful Search. For example, in order for a successful Search within a device to make the device the local winner, all 72-bit positions must generate a match for a 72-bit entry in 72-bit-configured quadrants. The same applies to 144-bit, 288-bit, and 576-bit searches.

The on-chip priority encoder selects the first matching entry in the database that is nearest to memory address 0. An arbitration mechanism using a cascade bus determines the global winning device among the local winning devices in a Search cycle. The global winning device then drives the output signals. When there is no successful Search, the device designated as the last device will drive the output signals (refer to *Section 5.3* for more information on last device designation).

**Table 4-1. Bit Position Match**

| Global Mask Bit | Mask Array Bit | Data Array Bit | Search Key Bit | Match Result |
|---|---|---|---|---|
| 0 | X | X | X | 1 |
| 1 | 0 | X | X | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

# 5.0 Functional Description

## 5.1 Modes of Operation

Ayama 10000A can operate in two different modes of operation: Non-Enhanced and Enhanced. The Non-Enhanced mode of operation is provided for backward compatibility with the CYNSE70000 device family. The Enhanced mode allows the Ayama 10000A to utilize the features that can be used to lower power consumption, ease table management, increase data integrity and increase Search throughput. These features are Mini-Key, Soft Priority, Parity, and MultiSearch, respectively. The following subsections provide more information on each of the modes and features.

The device powers-up in Non-Enhanced mode. A switch to Enhanced mode and activation of the features require the user to configure internal registers with appropriate values. Refer to *Section 5.4* for detailed information on the internal registers.

*Table 5-1* lists the features and functions that are different between the two modes of operation.

**Table 5-1. Summary of Non-Enhanced and Enhanced Mode Features and Functions Differences**

| Features/Functions | Non-Enhanced | Enhanced |
|---|---|---|
| Maximum Search Throughput | 133 MSPS | 266 MSPS |
| MultiSearch | No | Yes |
| Soft Priority | No | Yes |
| Mini-Key | No | Yes |
| Parity | No | Yes |
| Learn Operation | Data from CMPR Register;<br>Target Data Array;<br>Supports x72 and x144 table widths | Data from CMPR Register or DQ Bus;<br>Target Data or Mask Array;<br>Supports all table widths |
| Where to Configure the Table Width | CONFIG Register | BMR Register |
| Table Widths Supported | x72, x144, x288 | x72, x144, x288, x576 |
| Data and Mask Array Organization | 32/16/8 8Kx72-bit Partitions for CYNSE10512A/256A/128A respectively | 128/64/32 2Kx72-bit Blocks for CYNSE10512A/256A/128A respectively |

### *5.1.1 Non-Enhanced Mode*

In the Non-Enhanced mode of operation, the Ayama 10000A device is organized into 32/16/8 partitions (corresponds to CYNSE10512A/256A/128A, respectively) that each can be configured to be 8K x 72, 4K x 144, or 2K x 288. The 576-bit table width configuration is not supported in this operation mode. The LSB of each 72-bit is designated to indicate whether that entry is used or not. When the entry is empty, that bit must be set to 0. When the entry is used, that bit must be set to 1. For example, in a 288-bit table a used entry will have bit[0], bit[72], bit[144], and bit[216] set to 1. When all bit[0] are set to 1, the Ayama 10000A will assert FULO[1:0] to “11.”

References are present throughout this document to indicate features that are applicable when device is in this mode.

Internal registers for configuration: CONFIG and CMD.

### *5.1.2 Enhanced Mode*

In Enhanced mode, Ayama 10000A is organized into 128/64/32 blocks (corresponds to CYNSE10512A/256A/128A respectively) of 2K x 72 which can also be configured into 1K x 144, 512 x 288, or 256 x 576. The Mini-Key, Soft Priority, Parity, and MultiSearch features can also be activated. Each block has internal block registers associated to it that needs to be initialized before the device goes into normal operation. *Figure 5-1* shows the general overview of the block registers association.

References are present throughout this document to indicates features that are applicable when the device is in this mode.

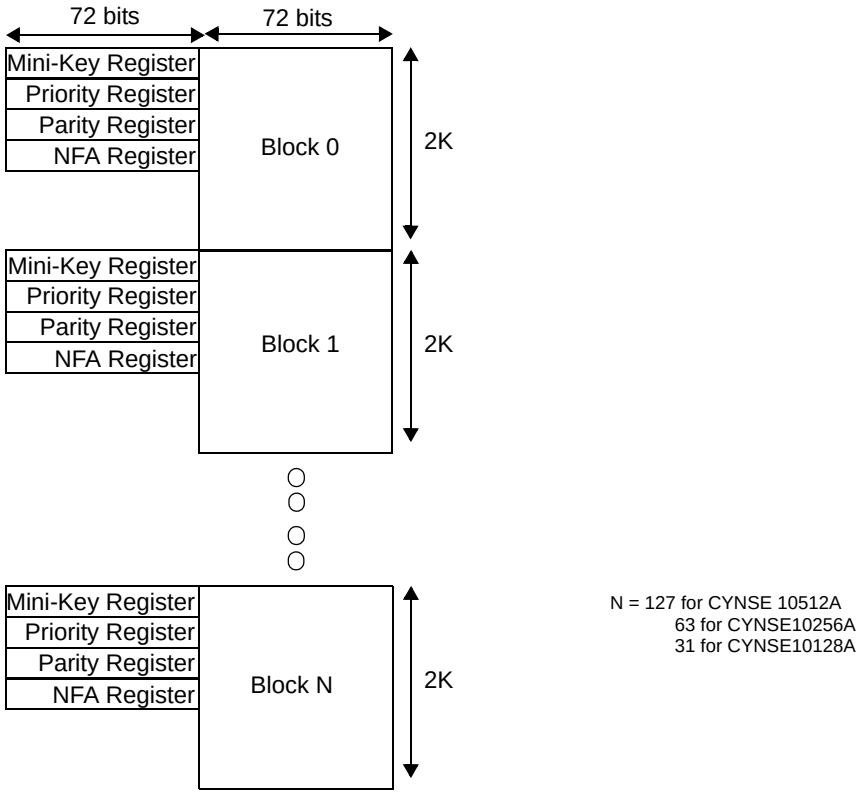



**Figure 5-1. Blocks and Block Registers Association**

*5.1.2.1 Mini-Key*

The Mini-Key feature allows the device to power down blocks within the device that are not being selected to participate in the search operation. This results in lower power consumption. When a device has multiple tables, the block architecture of the device combined with Mini-Key can be used to ease table expansion or reorganization. There are four Mini-Keys that can be associated with each block (*Figure 5-2*), which supports each block to be a member of up to four logical tables. The block register that holds the Mini-Key values also includes the field that configures the block to be of a certain table width.

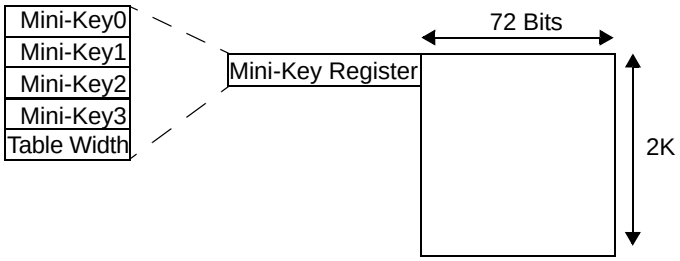



**Figure 5-2. Mini-Key Register Contents**

During a Search operation, the Search key width as well as the Search Mini-Key are used to selectively activate certain blocks. A block will participate in the Search operation only when the Search width matches the block's table width and the Search Mini-Key matches one of the four Mini-Keys of the block.

Internal registers for configuration: CMD, CPR and BMR.

*5.1.2.2 Soft Priority*

Table management can become a time consuming process and slow down the performance of the system. In an edge router with multiple table of same widths in one or more Ayama 10000A devices, that constantly update the entries, one table may become full very quickly. The time it takes to process table expansion and data reorganization can be critical in a system that requires high performance and quality of service. Soft Priority feature in the Ayama 10000A can help avoid that problem. For Soft Priority purposes, each 2Kx72 block of Data/Mask array is arranged into four 512 x 72 sub-blocks. Each sub-block has a user-program-

mable Soft Priority value that becomes part of the search key when Soft Priority feature is enabled. This feature eases the management of the tables, especially for table expansion. Each sub-block also has a Priority Valid bit that can be used to set the Soft Priority value of the sub-block to invalid state which will also prevent the sub-block from participating in a search operation.

*Figure 5-3* shows the associations of the sub-blocks and Soft Priority.

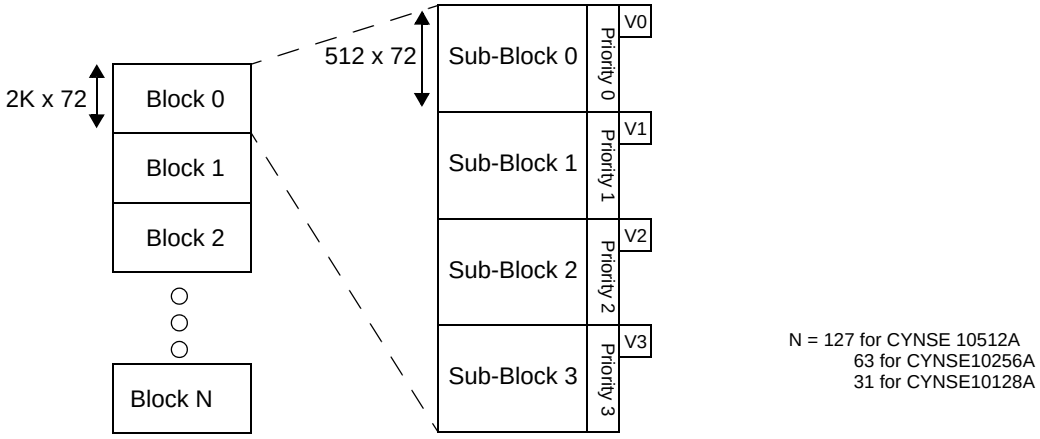



**Figure 5-3. Sub-Blocks and Soft Priority Associations**

Internal registers for configuration: CMD, CPR and BPR.

*5.1.2.3 Parity*

Ayama 10000A introduces parity to provide additional protection for data integrity. Parity checking can be performed both on the data transmission that passes through DQ bus and the data stored in the Core (data and mask arrays). The Parity feature can be enabled through the PARITY register. DQ Bus and Core parity checking can be independently enabled. When parity checking is enabled, a Write operation ignores any masking and all bits are written as presented in the DQ bus.

Even Parity is used in the parity checking. For example, if there is an odd number of logic-1 bits in a word, the corresponding parity bit will be set High in order for the combination (word and parity bit) to have even parity.

When an error is detected, the device will update the PARITY register and set the parity error flag (PARERR_L) to report the error. Parity status is not cascaded. However, PARERR_L is an open-drain signal to allow signals from cascaded Ayama 10000A devices to be connected together and provide cascaded parity error detection. Therefore, the AC timing parameters associated with the signal (rise time/fall time) will be dependent on the loading conditions. Note that all parity status fields in PARITY and BPAR registers needs to be cleared by the ASIC after fixing the errors.

Internal registers for configuration: PARITY and BPAR.

*DQ Bus Parity*

The DQ bus is divided into even-bits and odd-bits groups for parity checking. Parity bits of both even- and odd-bits groups are provided in the bidirectional PAR[1:0]. When the ASIC is driving the DQ bus, the ASIC must generate the parity bits. When the NSE is driving the DQ bus, the NSE will generate the parity bits.

When the ASIC is driving the DQ bus, the NSE will calculate the data stream parity and compare it to PAR[1:0]. When there is an error, the NSE will update the PARITY register and set PARERR_L to 0. PARERR_L is valid on the $(3+T)^{th}$ cycle of latency for a Read operation and $(4+T)^{th}$ cycle of latency for the other operations. T is the cycle where the bus parity error is detected. When a DQ bus parity error is detected, the NSE must be reset and reinitialized.

*Figure 5-4* shows the timing diagram of a DQ Bus Parity error during a 288-bit Search instruction. In cycle 1B the parity of the odd DQ bits is shown to be ‘1’ while the corresponding parity bit (PAR[1]) is ‘0’ (should be High for parity check to result in a ‘0’).The PARERR_L signal goes Low 4 cycles after the error is detected.

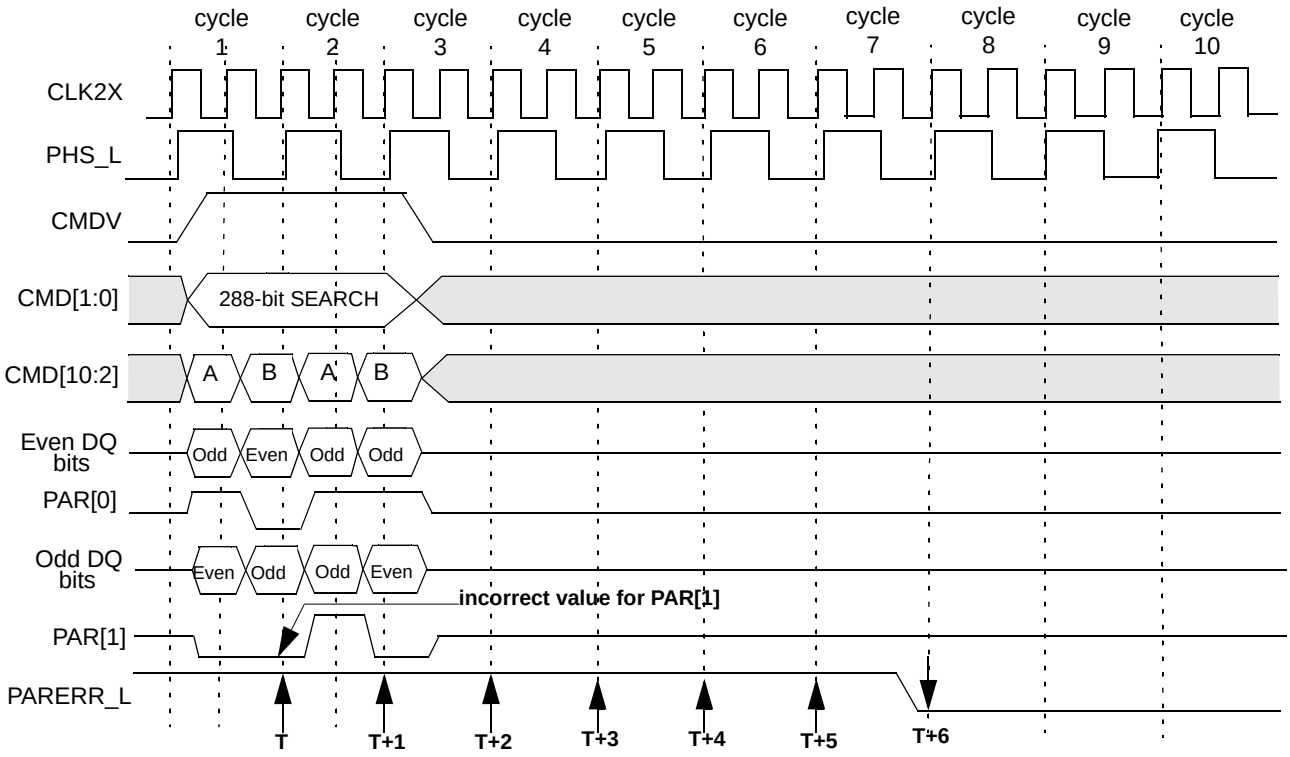



**Figure 5-4. Timing Diagram of a DQ Bus Parity Error (288-bit Search, TLSZ=10)**

*Core Parity*

The Core includes a one-bit parity for each 72-bit entry in the data and mask arrays. When writing into the data or mask array, the NSE will calculate and generate the one-bit parity for each 72-bit data. Each block also has a block-associated internal register to enable the parity checking for the block (BPAR). When disabled, the block will ignore the Read Parity command.

To issue the Read Parity command, the ASIC issues a Read command and sets the Parity field in the parameters sent through the DQ bus as described in *Table 5-28*. Core parity checking is performed in parallel on four adjacent 72-bit entries per pair of blocks. At the beginning of each parity operation, an internal address counter is incremented. The new incremented address is then used for the parity check operation.

It will cycle through the data and mask arrays as well as odd and even blocks for both arrays for each Read Parity issued. If one or more parity errors are detected, the error is reported in the block's BPAR register. Then all errors are prioritized through an arbiter to select the highest priority parity error, which is then reported in the PARITY register. PARERR_L will also be set to 0 when there is a parity error. PARERR_L is valid on the $(5+TLSZ)^{th}$ cycle of latency. For example, with TLSZ = 10 (binary) and the command is issued at Cycle1, PARERR_L will be valid on Cycle8. Read Parity also responds to broadcast CHIPID selection.

*Figure 5-5* shows the timing diagram of a Core Parity error during a Read Parity instruction. The PARERR_L signal goes Low five cycles after the error is detected.

There are two basic flows for parity error recovery. The first flow is by reading the highest priority parity error address stored in the PARITY register, fix the error, decrement the internal address counter and reissue Read Parity. The second flow is by reading the PARITY register to obtain the location, reading the BPAR registers to locate blocks that has the error and then fixing those locations.

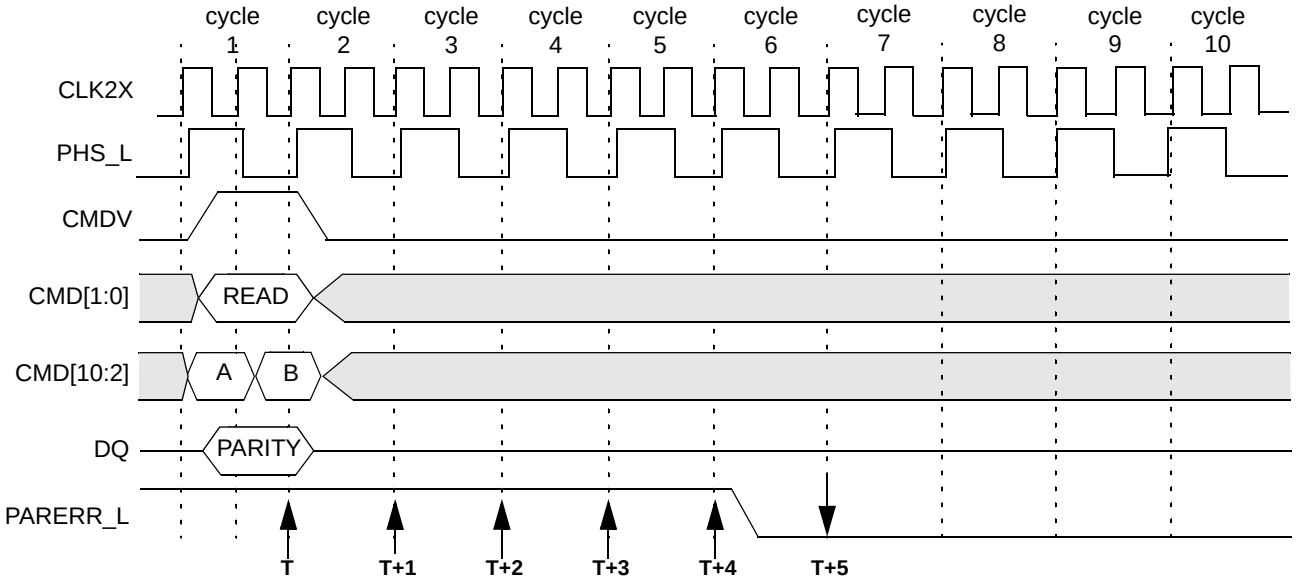



**Figure 5-5. Timing Diagram of a Core Parity Error (TLSZ=00)**

*5.1.2.4 MultiSearch*

When MultiSearch is activated, the Core is divided into two separate arrays. Each array is organized into 64/32/16 blocks (corresponds to CYNSE10512A/CYNSE10256A/CYNSE10128A, respectively) of 2K 72-bit entries. Each block can be configured to be of width x72, x144, x288, or x576. This separation allows a Search operation to simultaneously perform the search across both arrays. The output signals will run at double data rate to effectively increase the throughput to a maximum of 266 million searches per second. Each array can have multiple tables with different widths. Single-Search operation outputs are driven at the rising edge of CLK1X. When the device has the MultiSearch feature enabled and MultiSearch operation is issued (Single-Search can still be issued even when MultiSearch is enabled), the output is driven at both rising and falling edges of CLK1X (rising edge of CLK2X). Output from Array 0 is driven at the rising edge while output from Array 1 is driven at the falling edge of CLK1X. *Figure 5-6* shows an illustration of the MultiSearch operation.

Both arrays will use the same Search key except for search operation on 72-bit wide tables. Multisearching across tables of different widths is possible. *Table 5-2* contains a summary of possible multisearching combinations.

**Note**. Throughout this document, the search that is issued through the command (CMD) bus is called the leading search. Similarly, the trailing search is the second search that uses a subset of the data presented for the leading search. This data subset is aligned with the least significant (trailing) 72-bit word. For 144-bit and 288-bit searches, the leading search needs to be greater than or equal to the width of the trailing search.

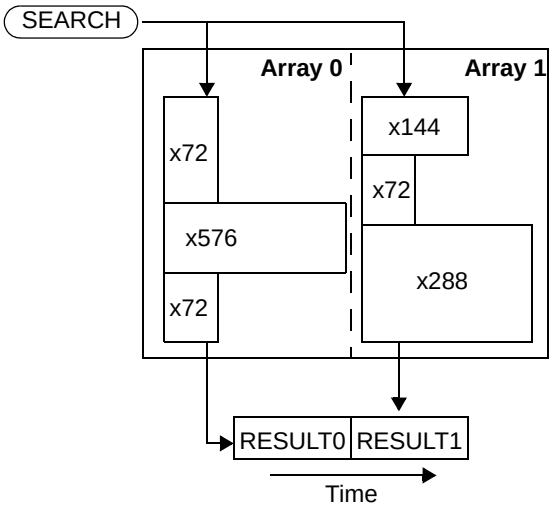



**Figure 5-6. MultiSearch Operation Overview**

**Table 5-2. Summary of Supported Trailing Searches**

| Leading Search Width | 576-bit Trailing Search Supported | 288-bit Trailing Search Supported | 144-bit Trailing Search Supported | 72-bit Trailing Search Supported |
|---|---|---|---|---|
| 576-bit | Yes | Yes | Yes | Yes |
| 288-bit | No | Yes | Yes | Yes |
| 144-bit | No | No | Yes | Yes |
| 72-bit | No | No | No | Yes |

MultiSearch operations use different CPR registers (different Mini-Key, Soft Priority, and width configuration values) for the two searches. Depending on the location of the leading search in the data array (Array 0 or Array 1), the GMR/CPR selection will vary.

Leading search in Array 0: By indicating the GMR used for the leading search width in the MultiSearch, the corresponding CPR is automatically selected (GMR0 selects CPR0). The trailing search (must be smaller or equal width) is automatically assigned the configuration specified in the CPR immediately following the one specified for the leading search. Therefore, if the leading search specifies CPR3, the trailing search will use CPR4. With respect to the GMR, the GMR registers specified for the leading search will automatically select the subsequent GMR registers for the trailing search. This is best shown in *Table 5-3*.

**Table 5-3. GMR and CPR Selection When Leading Search is in Array 0**

| Search Size Presented on CMD | GMRs Presented on CMD | Leading Search GMR Usage | Leading Search CPR Usage | Trailing Search Size | Trailing Search GMR Usage | Trailing Search CPR Usage |
|---|---|---|---|---|---|---|
| 576-bit | GMR[a], GMR[b], GMR[c], GMR[d] | GMR[a], GMR[b], GMR[c], GMR[d] | CPR[a] | 576-bit | GMR[a+1], GMR[b+1], GMR[c+1], GMR[d+1] | CPR[a+1] |
| | | | | 288-bit | GMR[c+1], GMR[d+1] | |
| | | | | 144-bit | GMR[d+1] | |
| | | | | 72-bit | GMR[d+1] | |
| 288-bit | GMR[a], GMR[b] | GMR[a], GMR[b] | CPR[a] | 288-bit | GMR[a+1], GMR[b+1] | CPR[a+1] |
| | | | | 144-bit | GMR[b+1] | |
| | | | | 72-bit | GMR[b+1] | |
| 144-bit | GMR[a] | GMR[a] | CPR[a] | 144-bit | GMR[a+1] | CPR[a+1] |
| | | | | 72-bit | GMR[a+1], | |
| 72-bit | GMR[a] | GMR[a] | CPR[a] | 72-bit | GMR[a+1] | CPR[a+1] |

Leading search is located in Array 1: The GMR/CPR selection process changes slightly. Specifically, the GMR usage specified on the CMD bus at the time of the search is used for the trailing search, and not the leading search. Otherwise, the reverse of *Table 5-3* is true. The new GMR/CPR selection matrix is presented in *Table 5-4*.

**Table 5-4. GMR and CPR Selection when Leading Search is in Array 1**

| Search Size Presented on CMD | GMRs Presented on CMD | Leading Search GMR Usage | Leading Search CPR Usage | Trailing Search Size | Trailing Search GMR Usage | Trailing Search CPR Usage |
|---|---|---|---|---|---|---|
| 576-bit | GMR[a], GMR[b], GMR[c], GMR[d] | GMR[a+1] GMR[b+1] GMR[c+1] GMR[d+1] | CPR[a+1] | 576-bit | GMR[a], GMR[b], GMR[c], GMR[d] | CPR[a] |
| | | | | 288-bit | GMR[c], GMR[d] | |
| | | | | 144-bit | GMR[d] | |
| | | | | 72-bit | GMR[d] | |
| 288-bit | GMR[a], GMR[b] | GMR[a+1], GMR[b+1] | CPR[a+1] | 288-bit | GMR[a], GMR[b] | CPR[a] |
| | | | | 144-bit | GMR[b] | |
| | | | | 72-bit | GMR[b] | |
| 144-bit | GMR[a] | GMR[a+1] | CPR[a+1] | 144-bit | GMR[a] | CPR[a] |
| | | | | 72-bit | GMR[a] | |
| 72-bit | GMR[a] | GMR[a+1] | CPR[a+1] | 72-bit | GMR[a] | CPR[a] |

In order to successfully use a MultiSearch in the Ayama 10000A NSE, the logical tables need to be wholly stored in either Array 0 or Array 1. Any table that has entries in both Array 0 and Array 1 can not be MultiSearch-ed. The address space is shown in *Table 5-5*.

**Table 5-5. Address Spaces for Array 0 and Array 1**

| Device | Array 0 Addresses (hexadecimal) | Array 1 Addresses (hexadecimal) |
|---|---|---|
| CYNSE10512A | [0:1FFFF] | [20000:3FFFF] |
| CYNSE10256A | [0:FFFF] | [10000:1FFFF] |
| CYNSE10128A | [0:7FFF] | [8000:FFFF] |

During the MultiSearch operation, the trailing search uses a subset of the data presented (least significant) for the leading search as its search key. The size is dependent on the width of the trailing search. For example, in a multisearch command with a 288-bit leading search and 144-bit trailing search, the least significant 144-bit of the leading search key will be used for the 144-bit trailing. In the 72-bit trailing search case, the location of the 72-bit table (Array 0 or Array 1) will cause the data sample window to change (Cycle A of the last clock cycle or Cycle B of the last clock cycle). See *Section 6.0* for timing diagrams of multisearch commands.

Internal register for configuration: CPR, BPR, CMD.

#### *5.1.2.5 Enhanced Learn Operation*

Ayama 10000A extends the capability of the Learn function to allow users to select the data source for the operation. The data can be from the DQ bus or one of the Comparand (CMPR) registers. It also allows the data to be written to both the mask and data array while in Non-Enhanced mode it allows the data to be written only to the data array.

Internal register for configuration: CMD.

## 5.2 I/O Interfaces

Data flows in and out of the device through three separate I/O interfaces: ASIC, SRAM and Cascade Interface. Section 3.0, “Signal Description,” on page 12 lists the signals that are part of each interface. Input signals are registered on the rising edge and falling edge of CLK1X or rising edge of CLK2X. Output signals are driven out on the rising edge of CLK1X or rising edge of CLK2X when PHS_L is Low. An exception is when MultiSearch operation is activated, the output will be driven out on both edges of CLK1X or rising edge of CLK2X. Refer to *Section 5.6* for more information on clock signals. *Figure 5-7* shows an example of ASIC, NSEs and SRAMs I/O interconnects. The SRAM Interface outputs may be connected to SRAM devices in associative applications mode or back to the ASIC in index applications mode.

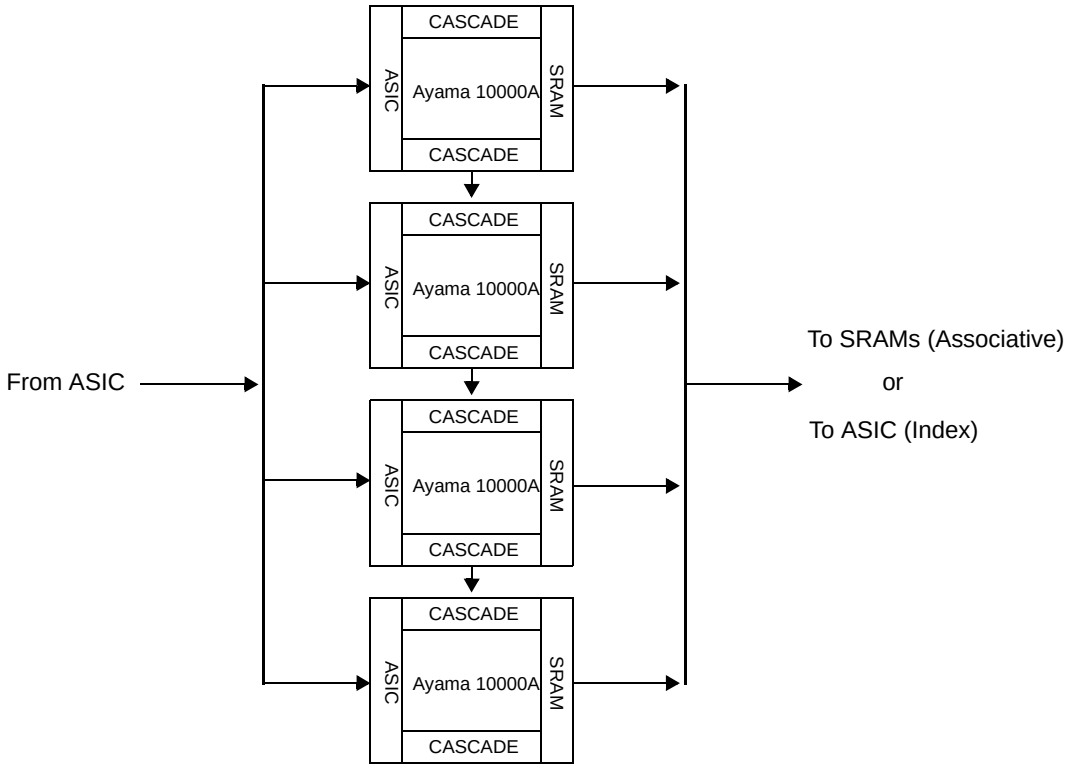



**Figure 5-7. Ayama 10000A I/O Interfaces**

Internal register for configuration: HARDWARE.

### *5.2.1 ASIC Interface*

The ASIC Interface includes all signals for data that comes in from and out to a system's processing unit, which could be an application specific (ASIC) or a more generic network processing unit (NPU and NCP). It supports LVCMOS and HSTL I/O standards. LVCMOS allows the I/O signals to run at a rate of up to 100 MHz (CLK1X; Double data rate in MultiSearch operation). With HSTL, the I/O signals can run at a rate of up to 133 MHz (CLK1X; Double data rate in MultiSearch operation).

The ASIC Interface includes the Command and DQ bus signal group. CMD[10:0] carries the command and its associated parameter. DQ[71:0] is used for data transfer to and from the database entries, which are comprised of data and mask fields that are organized as data and mask arrays. The DQ bus carries Search data (of the data and mask arrays and internal registers) during the Search command as well as the address and data during Read and/or Write operations. The DQ bus also carries address information for the direct accesses to the external SRAM.

### *5.2.2 SRAM Interface*

The SRAM Interface includes output only signals that are used to interact with SRAM memory devices. As with the ASIC Interface, it supports LVCMOS and HSTL I/O standards. LVCMOS allows the I/O signals to run at a rate of up to 100 MHz (200-MHz double data rate with MultiSearch operation). With HSTL, the I/O signals can run at a rate of up to 133 MHz (266-MHz double date rate with MultiSearch operation).

### *5.2.3 Cascade Interface*

The Cascade Interface is used for cascading multiple Ayama 10000A devices in a system. It supports LVCMOS and HSTL I/O standards that can run up to 133 MHz in all operation modes. The Cascade Interface power supply is the same power supply that the ASIC Interface uses. Thus the selection of the I/O standard used for the Cascade Interface depends on the I/O Standard selected for the ASIC Interface.

When multiple NSEs are cascaded to create large databases, the data being searched is presented to all NSEs in the cascaded system simultaneously. If multiple matches occur, arbitration logic on the NSEs will enable the winning device (the one with a matching entry closest to address 0 of the cascaded database) to drive the SRAM bus. User can set the default device to respond to an operation when a Search operation does not result in a Search Hit. Refer to *Section 5.3* for more information.

## 5.3 Output Signals Default Driver/Last Device Designation (LRAM and LDEV)

When NSEs are cascaded using multiple Ayama 10000A devices, the SADR, CE_L, and WE_L (three-state signals) are all tied together. In order to eliminate external pull-up and pull-downs, one device in a bank is designated the default driver. For non-search or non-learn cycles (see *Subsection 6.6, "Learn Command"*) or Search cycles with a global miss, the SADR, CE_L, and WE_L signals are driven by the device with the LRAM bit set. It is important that only one device in a bank of cascaded NSEs have this bit set. Failure to do so will cause contention on the SADR, CE_L, and WE_L, and can potentially cause damage to the device(s).

Similarly, when NSEs using multiple Ayama 10000A devices are cascaded, SSF and SSV (also three-state signals) are tied together. In order to eliminate external pull-up and pull-downs, one device in a bank is designated as the default driver. For non-search cycles or Search cycles with a global miss, the SSF and SSV signals are driven by the device with the LDEV bit set. It is important that only one device in a bank of cascaded NSEs have this bit set. Failure to do so will cause contention on the SSV and SSF, and can potentially cause damage to the device(s).

## 5.4 Registers

*Table 5-6* provides an overview of all the Ayama 10000A internal registers. Each register is 72 bits wide. The Ayama 10000A contains sixteen pairs of comparand storage registers, sixteen pairs of global mask registers, eight Search status index registers, sixteen Search control parameters registers, sixteen Search result registers and one each of command, information, burst Read, burst Write, next-free address register, partition configuration, hardware and parity control registers. Each of the blocks in the NSE device (128/64/32 2Kx72 blocks in CYNSE10512A/256A/128A respectively) also has one each of Block Mini-Key, Block Priority, Block Parity and Block Next-free Address registers. There are also four Block Priority Register Aliases registers for each Block Priority register that allows an alternative way to update the Block Priority registers. The registers are presented in ascending address order. Each register group is then described in the following subsections. Reserved fields in the registers are read as 0s. When writing to the registers, all Reserved fields must be written with 0s, unless specified otherwise in the field's description.

**Table 5-6. List of Internal Registers**

| Address (decimal) | Address (Hexadecimal) | Abbreviation | Type (Read/Write) | Description |
|---|---|---|---|---|
| 0–31 | 000 - 01F | CMPR0–15 | R | **Comparand Register**. Sixteen CMPR pairs (144 bits per pair) that store comparands from the DQ bus during a Search operation for later use with the Learn command. See *Section 5.4.1*. |
| 32–47<br>96–111 | 020 - 02F<br>060 - 06F | GMR0–7<br>GMR8–15 | R/W | **Global Mask Register**. Sixteen GMR pairs (144 bits per pair) used for global mask bits on the DQ bus for all commands. See *Section 5.4.2*. |
| 48–55 | 030 - 037 | SSR0–7 | R | **Search Successful Register**. These registers store the result of Search operations. See *Section 5.4.3*. |
| 56 | 038 | COMMAND | R/W | **Command Register**. This register contains control fields that determine how the NSE operates. See *Section 5.4.4*. |
| 57 | 039 | INFO | R | **Information Register**. This Read-only register contains static information about the NSE device. See *Section 5.4.5*. |
| 58 | 03A | RBURREG | R/W | **Burst-Read Register**. This register contains the starting address and count for a Read Burst operation. See *Section 5.4.6*. |
| 59 | 03B | WBURREG | R/W | **Burst-Write Register**. This register contains the starting address and count for a Write Burst operation. See *Section 5.4.7*. |
| 60 | 03C | NFA | R | **Next-free Address Register**. This register contains the index of the next-free entry when the device is in the Non-Enhanced mode (Enhanced mode uses SRR registers to store the next-free entry information). See *Section 5.4.8*. |
| 61 | 03D | CONFIG | R/W | **Partition Configuration Register**. This register contains the partition type bits when the NSE device operates in the Non-Enhanced mode. It is not used in the Enhanced mode. See *Section 5.4.9*. |
| 62 | 03E | HARDWARE | R/W | **Hardware Register**. This register contains I/O drive strength settings. See *Section 5.4.10*. |
| 63 | 03F | PARITY | R/W | **Parity Control Register**. This register contains the control and address for parity checking of the Core and registers. See *Section 5.4.11*. |

**Table 5-6. List of Internal Registers** (continued)

| Address (decimal) | Address (Hexadecimal) | Abbreviation | Type (Read/Write) | Description |
|---|---|---|---|---|
| 64–79 | 040 - 04F | CPR0–15 | R/W | **Control Register**. These registers provide Mini-Key and Soft Priority for the associated operation. See *Section 5.4.12*. |
| 80–95 | 050 - 05F | SRR0–15 | R | **Search Result Register**. These registers provide information of the next-free entry when the device is in the Enhanced mode. (Non-Enhanced mode uses the NFA register to store the next-free entry information.) See *Section 5.4.13*. |
| 112–1023 | 070 - 3F0 | – | – | **Reserved**. |
| 1024 | 400 | BMRx | R/W | **Block Mini-Key Register**. This register holds the four Mini-Keys associated with a block. There is one BMR per block. See *Section 5.4.14*. |
| 1025 | 401 | BPRx | R/W | **Block Priority Register**. This register holds the four sub-block priorities. There is one BPR per block. See *Section 5.4.15*. |
| 1026 | 402 | BPARx | R/W | **Block Parity Register**. This register contains the control and status bits for controlling and detecting parity errors for a block. There is one BPAR per block. See *Section 5.4.16*. |
| 1027 | 403 | BNFAx | R | **Block Next-free Address Register**. This register contains the next-free entry information for the block that it is associated with. There is one BNFA per block. See *Section 5.4.17*. |
| 1028–1031 | 404 - 407 | BPRA0x–BPRA3x | R/W | **Block Priority Register Aliases**. These locations are aliases for the corresponding BPRx. See *Section 5.4.18*. |

**Note**: For BMR, BPR, BPAR, BNFA, and BPRA0-3, the block (0- N, where N = 127 for CYNSE10512, N = 63 for CYNSE10256 and N = CYNSE10128) that will participate in the operation must be encoded in the BLKNUM field of the internal register address space. Also, the addresses in *Table 5-6* must be encoded in the REGSEL field of the internal register address space. See *Section 5.9.2*.

### *5.4.1 Comparand Register (CMPR)*

The device contains 16 pairs of comparand registers (one pair is 144 bits) dynamically selected in every Search operation to store the comparand presented on the DQ bus. The device may later use these registers when it executes a Learn operation. Search and Learn commands specify the comparand registers in pairs. The Ayama 10000A device stores the Search command's cycle A comparand in the even-numbered register and the cycle B comparand in the odd-numbered register, as shown in *Figure 5-8*. For wider width keys, pairs of comparand registers are concatenated together. The concatenation of the registers must be done by the user. On a 72-bit operation, both halves of the comparand register must be loaded with the same value. When performing MultiSearch operation, the comparand registers specified in the search command will be used for the leading search. For the trailing searches, the NSE automatically selects the comparand register one index higher than the ones specified in the command bus. When the device powers-up, the CMPR registers are initialized to 0.

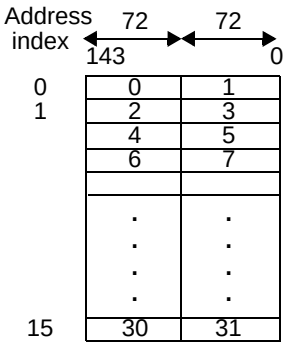



**Figure 5-8. Comparand Register Selection During Search and Learn Instructions**

### *5.4.2 Global Mask Register (GMR)*

The device contains 16 pairs of GMRs (one pair is 144 bits) dynamically selected in every Search operation to select the Search subfield. The addressing of these registers is shown in *Figure 5-9*. The GMR index supplied on the command bus selects one of

the sixteen pairs of global masks during Search and Write operations. In 72-bit Search and Write operations, the host ASIC must program both the even and odd mask registers with the same values. For a MultiSearch operation, see section 5.1.2.4 for details.

Each mask bit in the GMRs is used during Search and Write operations. In a Search operation, setting the mask bit to 1 enables while setting the mask bit to 0 disables compares at the corresponding bit position (forced match). In Write operations to the data or mask array, setting the mask bit to 1 enables Write while setting the mask bit to 0 disables Write at the corresponding bit position. Write operation to internal registers does not use the GMR to mask the data and ignores the GMR selection when the command is issued.

When the device powers-up, the GMR registers are initialized to 0. *Figure 5-9* below shows each portion (Even, Odd) of each GMR, and what address (in decimal) is required to access that register.

| GMR Index | Even 72 (143) | Odd 72 (0) |
|---|---|---|
| 0 | 32 | 33 |
| 1 | 34 | 35 |
| 2 | 36 | 37 |
| 3 | 38 | 39 |
| 4 | 40 | 41 |
| 5 | 42 | 43 |
| 6 | 44 | 45 |
| 7 | 46 | 47 |
| 8 | 96 | 97 |
| 9 | 98 | 99 |
| 10 | 100 | 101 |
| 11 | 102 | 103 |
| 12 | 104 | 105 |
| 13 | 106 | 107 |
| 14 | 108 | 109 |
| 15 | 110 | 111 |

**Figure 5-9. Addressing the Global Mask Register Array**

### *5.4.3 Search Successful Register (SSR)*

The device contains eight Search Successful Registers (SSR) to hold the index of the location at which a successful search occurred. The format of each SSR is described in *Table 5-7*. The Search command specifies which SSR stores the index of a specific Search command in cycle B of the Search instruction. Subsequently, the host ASIC can use this register to access that data array, mask array, or external SRAM using the index as part of the indirect access address. The selected register is updated when the device performs a Search operation regardless of the operation modes.

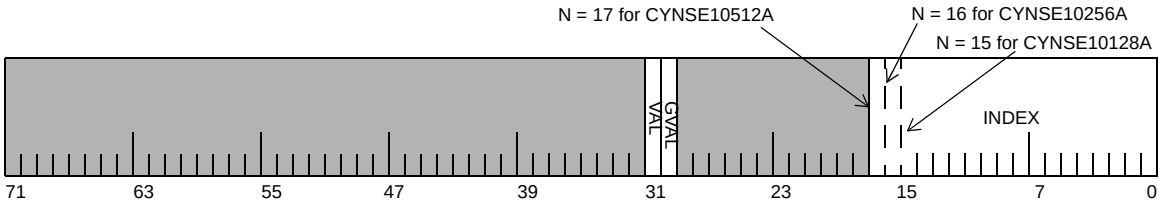



**Figure 5-10. Search Successful Register**

**Table 5-7. Search Successful Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| INDEX | [N:0] | 0 | **Index**. This is the address of the 72-bit entry where a successful search occurs. This index is updated if the device is either a local or global winner in a Search operation. N = 17 for CYNSE10512A, 16 for CYNSE10256A, 15 for CYNSE10128A.<br>If a hit occurs in a 144-bit table, the least-significant bit (LSB) is cleared to 0.<br>If a hit occurs in a 288-bit table, the two LSBs are cleared to 0.<br>If a hit occurs in a 576-bit table, the three LSBs are cleared to 0. |
| | [29:N + 1] | | **Reserved**. |
| GVAL | [30] | 0 | **Global Valid**. Valid only in Enhanced mode. It is updated when the device performs a Search operation. It is set to 1 when there is no hit anywhere in the cascade and this device is the last one in the cascade (LDEV field in CMD register is set to 1). Otherwise it is cleared to 0. When set to 1, the device is responsible for responding to broadcast PIO operation. |
| VAL | [31] | 0 | **Valid**. This field is updated when the device performs a Search operation. It is set to 1 only when the device is a global winner. Otherwise it will be cleared to 0. |
| | [71:32] | | **Reserved**. |

### *5.4.4 Command Register (COMMAND)*

*Table 5-8* describes the command register fields. This register is expected to be initialized by the user right after reset before performing any Read, Write, Learn, Search, or Parity operations and thereafter not changed during normal operation. The user must also wait for at least 32 CLK2X cycles after a write to the COMMAND register before issuing the next command.

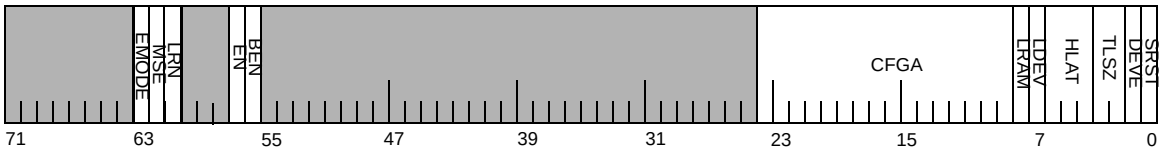



**Figure 5-11. Command Register**

**Table 5-8. Command Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| SRST | [0] | 0 | **Software Reset**. If set to 1, this bit resets the device with the same effect as a hardware reset. Internally, it generates a reset pulse lasting for eight CLK2X cycles. This bit automatically resets to 0 after the reset pulse is deasserted. |
| DEVE | [1] | 0 | **Device Enable**. If 0, it keeps the SRAM bus (SADR, WE_L, CE_L, OE_L and ALE_L), SSF, and SSV signals in a three-state condition and forces the cascade interface output signals LHO[1:0] and BHO[2:0] to 0. It also keeps the DQ bus in input mode. The purpose is to make sure that there are no bus contentions when the device powers up. Set this bit to 1 when the device is ready for operation. |
| TLSZ | [3:2] | 10 | **Table Size**. This field increases the pipeline latency of the Search and Learn operations as well as the Read and Write accesses to the SRAM. Once programmed, it is expected to not be changed.<br>Affected signals in both Enhanced and Non-Enhanced Modes:<br>SADR, CE_L, OE_L, WE_L, ALE_L, SSV, SSF, and ACK.<br>Affected signals only in Enhanced Mode:<br>FULL and MULTI_HIT.<br>Latency in number of CLK cycles:<br>“00”: 4 cycles<br>“01”: 5 cycles<br>“10”: 6 cycles<br>“11”: Reserved/Invalid |

**Table 5-8. Command Register Description** (continued)

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| HLAT | [6:4] | 000 | **Latency of Hit Signals**. This field adds latency to the SSF, SSV, FULL and MULTI_HIT signals (in addition to the latency of TLSZ) during a Search operation and ACK signal during SRAM Read accesses to control the SRAM access time. In case of associative data mode, this field can always programmed to be 000. Different latency values are as listed below:<br><br>000: 0 100: 4<br>001: 1 101: 5<br>010: 2 110: 6<br>011: 3 111: 7 |
| LDEV | [7] | 0 | **Last Device in the Cascade**. When set, the device is the last device in a cascaded and is the default driver for the SSF and SSV signals. In the event of a Search failure, the device with this bit set drives the hit signals as follows: SSF = 0 (binary), SSV = 1 (binary). In an operation other than Search, the device with this bit set drives the hit signals as follows: SSF = 0 (binary), SSV = 0 (binary). When multiple devices are cascaded, one of the devices must have LDEV set to 1. |
| LRAM | [8] | 0 | **Last Device on the SRAM Bus**. When set to 1, this is the last device on the SRAM bus in a cascade and is the default driver for the SADR, CE_L, WE_L, and ALE_L signals.<br>In cycles where none of the Ayama 10000A devices in a cascade drive these signals, this device drives the signals as follows:<br>For CYNSE10512A: SADR = 0x1FFFFFF<br>For CYNSE10256A: SADR = 0xFFFFFF<br>For CYNSE10128A: SADR = 0x7FFFFF<br>For CYNSE10512A/256A/128A:<br>CE_L = 1<br>WE_L = 1<br>ALE_L = 1<br>The device with this field set to 1 always drives OE_L. When multiple devices are cascaded, one of the devices must have LRAM set to 1. |
| CFGA | [24:9] | 0 | **Database Configuration**. The field is an alias for the first eight pairs of partition configuration bits of the configuration register. Reading and writing this field is reflected in the configuration register and vice versa. This field is only used when the device operates in the Non-Enhanced mode. |
| | [55:25] | | **Reserved**. |
| BEN | [56] | 0 | **DQ Bus Parity Enable**. When set to 1, it enables parity checking on the data transferred through DQ bus. |
| EN | [57] | 0 | **Core Parity Enable**. When set to 1, it enables Core parity checking. |
| | [60:58] | | **Reserved**. |
| LRN | [61] | 0 | **Enhanced LEARN Enable**. When set to 1, it allows the user to select the data source for the Learn operation from either the DQ bus or one of the CMPRs. It also allows the user to select whether the write is to the data or the mask array. This field is valid in the Enhanced mode. |
| MSE | [62] | 0 | **MultiSearch Enable**. When set to 1, it activates support for MultiSearch operation. The SRAM output operates at CLK2X rate instead of CLK1X. This field is valid only when the EMODE field of COMMAND register is set to 1. |
| EMODE | [63] | 0 | **Enhanced Mode**. When set to 1, the device operates in the Enhanced mode. When cleared to 0, the device operates in the Non-Enhanced mode. |
| | [71:64] | | **Reserved**. |

### 5.4.5 *Information Register (INFO)*

*Table 5-9* describes the information register fields.

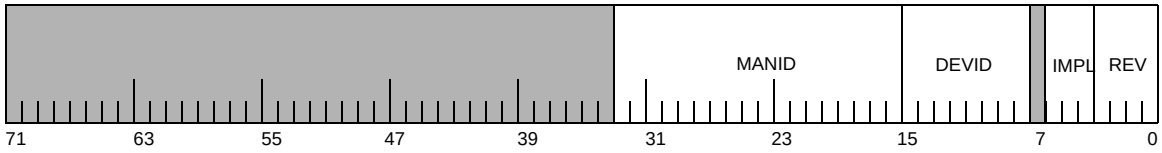



**Figure 5-12. Information Register**

**Table 5-9. Information Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| REV | [3:0] | 0110 | **Device Revision Number**. |
| IMPL | [6:4] | 001 | **Implementation Number**. |
| Reserved | [7] | 0 | **Reserved**. |
| DEVID | [15:8] | 0001 0100 | **Device Identification Number for CYNSE10128A**. |
| | | 0001 0101 | **Device Identification Number for CYNSE10256A**. |
| | | 0001 0110 | **Device Identification Number for CYNSE10512A**. |
| MANID | [33:16] | 00 00000 000 1101 1100 | **Manufacturer ID**. |
| Reserved | [71:34] | | **Reserved**. |

### 5.4.6 *Read Burst Address Register (RBURREG)*

*Table 5-10* shows the Read Burst Address register fields. These must be programmed before issuing a Burst-Read operation.

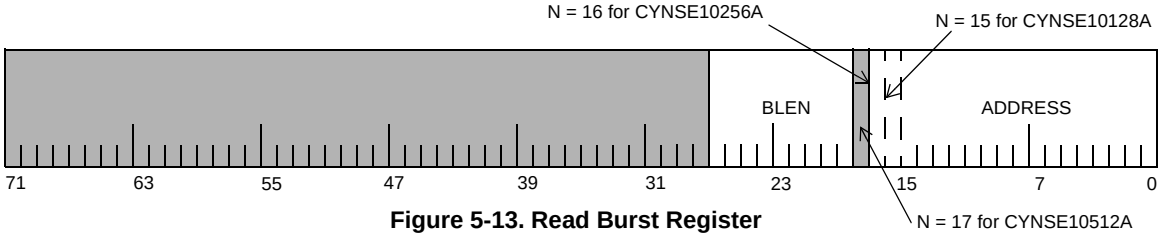



**Figure 5-13. Read Burst Register**

**Table 5-10. Read Burst Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| ADDRESS | [N:0] | 0 | **Address**. This field is used to identify the starting address of the data or mask array in a Burst-Read operation. The NSE will automatically increment the value by one after each successive Read of the data or mask array. It must be reinitialized before the next Burst-Read operation. N = 17 for CYNSE10512A, 16 for CYNSE10256A, 15 for CYNSE10128A. |
| | [18:M] | | **Reserved**. M = 18 for CYNSE10512A, 17 for CYNSE10256A, 16 for CYNSE10128A. |
| BLEN | [27:19] | 0 | **Length of Burst Access**. The device provides the capability to Read from 4 to 511 locations in a single burst. The NSE automatically decrements the value by one after each successive reading of the data or mask array. It must be reinitialized before the next Burst-Read operation. |
| | [71:28] | | **Reserved**. |

### 5.4.7 *Write Burst Address Register (WBURREG)*

*Table 5-11* describes the Write Burst Address register fields. These must be programmed before issuing a Burst-Write operation.

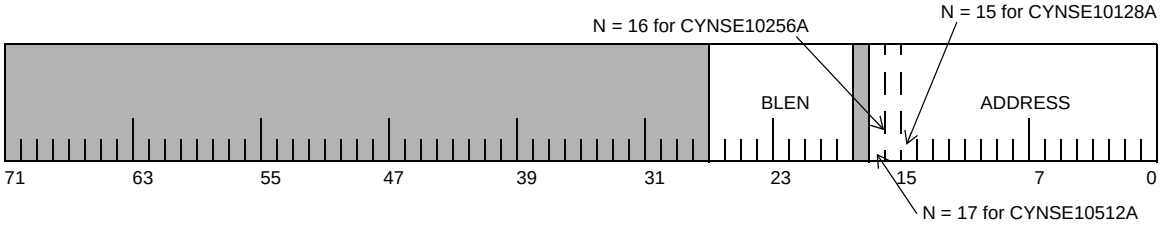



**Figure 5-14. Write Burst Address Register**

**Table 5-11. Write Burst Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| ADDRESS | [N:0] | 0 | **Address**. This field is used to identify the starting address of the data or mask array in a Burst-Write operation. The NSE will automatically increment the value by one after each successive Write of the data or mask array. It must be reinitialized before the next Burst-Write operation. N = 17 for CYNSE10512A, 16 for CYNSE10256A, 15 for CYNSE10128A. |
| | [18:M] | | **Reserved**. M = 18 for CYNSE10512A, 17 for CYNSE10256A, 16 for CYNSE10128A. |
| BLEN | [27:19] | 0 | **Length of Burst Access**. The device provides the capability to Write from 4 to 511 locations in a single burst. The NSE automatically decrements the value by one after each successive writing of the data or mask array. It must be reinitialized before the next Burst-Write operation. |
| | [71:28] | | **Reserved**. |

### 5.4.8 *Next-free Address Register (NFA)*

The NFA register is used only when the device operates in the Non-Enhanced mode. The NFA register's Index field (*Table 5-12*) holds the address of the highest priority free entry in the table. When the table is full, the Index field will be set to all 1s. When all entries in the device is full, the Ayama 10000A will assert FULO[1:0] to "11".

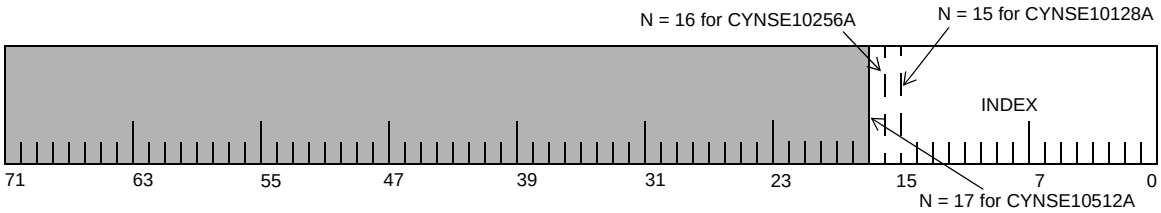



**Figure 5-15. Next-free Address Register**

**Table 5-12. NFA Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| Index | [N:0] | 0 | **Index**. The address index of the next-free entry location. N = 17 for CYNSE10512A, 16 for CYNSE10256A, 15 for CYNSE10128A. |
| | [71:M] | | **Reserved**. M = 18 for CYNSE10512A, 17 for CYNSE10256A, 16 for CYNSE10128A. |

### 5.4.9 Configuration Register (CONFIG)

The CONFIG register is valid only when the device operates in the Non-Enhanced mode. *Table 5-13* describes the information register fields.

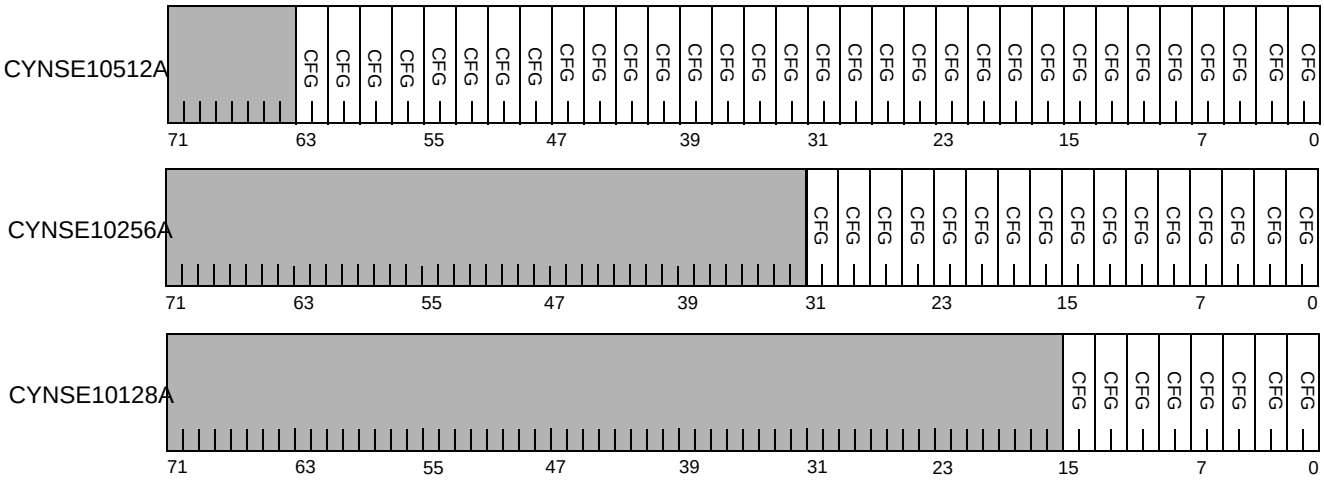



**Figure 5-16. Configuration Register**

**Table 5-13. Configuration Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| CFG | [N:N-1]<br>[N-2:N-3]<br>...<br>[1:0]<br><br>N = 63 for CYNSE10512A, 31 for CYNSE10256A, 15 for CYNSE10128A. | 0 | **Partition Configuration**. In the Non-Enhanced mode, Ayama 10000A is internally divided into 32/16/8 partitions corresponding to CYNSE10512A/256A/128A respectively. Each two bits configures one partition as encoded below:<br>00: 8K × 72<br>01: 4K × 144<br>10: 2K × 288<br>11: Disabled (does not reduce power consumption in a Search operation)<br>Bit[1:0] configures the first partition, Bit[3:2] configures the second partition and so on. Bit [15:0] of this register is aliased in Bit[24:9] of the Command register. Modification to Bit[15:0] of this field will affect the CFGA field in the Command register and vice versa. |
| Reserved | [71:N + 1] | | **Reserved**. |

### *5.4.10 Hardware Register (HARDWARE)*

The Hardware register controls the drive strength of the groups of signals as listed in *Section 6.0*. *Table 5-14* shows the fields that control each of the group and the output signals associated with it.

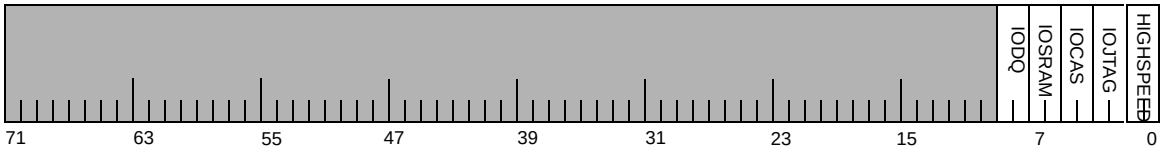



**Figure 5-17. Hardware Register**

**Table 5-14. Hardware Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| HIGHSPEED | [1:0] | 11 | **HIGHSPEED Settings**.<br>The encoding for Highspeed is listed below:<br>11: HIGHSPEED disabled. Use this setting for CLK1x <= 100Mhz<br>10: Reserved<br>01: Reserved<br>00: HIGHSPEED enabled. Use this setting for CLK1x > 100Mhz |
| IOJTAG | [3:2] | 11 | **JTAG I/Os**. Sets the drive strength for the I/O. By default it is set to “11”. The following output signal is part of this group: TDO.<br>The LVCMOS I/O drive strength for encoding is as listed below:<br>00: 2 mA<br>01: 8 mA<br>10: 16 mA<br>11: 24 mA ($V_{DDQ}$ = 2.5V); 20 mA ($V_{DDQ}$ = 1.8V)<br>The HSTL I/O drive strength for encoding is as listed below:<br>00: 8 mA (HSTL I)<br>01: Reserved<br>10: Reserved<br>11: 17 mA (HSTL II) |
| IOCAS | [5:4] | 11 | **Cascade I/Os**. The following output signals are part of this group:<br>LHO, BHO and FULO.<br>Refer to IOJTAG above for I/O drive strength encoding. |
| IOSRAM | [7:6] | 11 | **SRAM I/Os**. The following output signals are part of this group:<br>SADR, CE_L, WE_L, OE_L and ALE_L.<br>Refer to IOJTAG above for I/O drive strength encoding. |
| IODQ | [9:8] | 11 | **Command and DQ Bus I/Os**. The following output signals are part of this group:<br>DQ, ACK, EOT, SSF, SSV, PAR, PARERR_L, MULTI_HIT, and FULL.<br>Refer to IOJTAG above for I/O drive strength encoding. |
| | [63:10] | | **Reserved**. |
| | [71:64] | 0 | **Reserved**. This field must be set to 0. |

### 5.4.11 Parity Control Register (PARITY)

*Table 5-15* describes the Parity Control Register fields. This register is only active when the device is in the Enhanced mode.

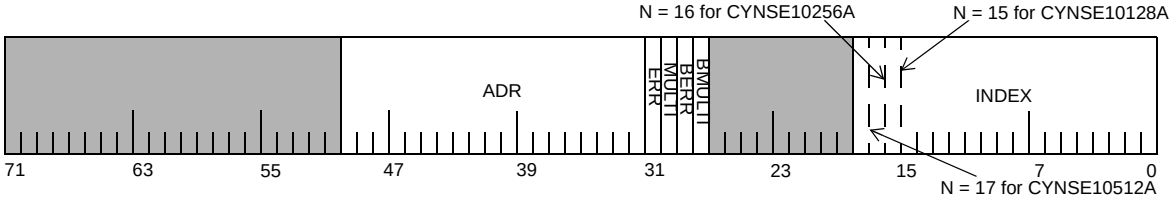



**Figure 5-18. Parity Control Register**

**Table 5-15. Parity Control Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| INDEX | [18, N:0] | 0 | **Index**. This field contains the highest priority parity error index. When a parity error is detected, the global priority encoder selects the highest priority parity error out of the entire Core.<br>Note that if another Parity operation is performed, this field is updated based upon that operation.<br>N = 17 for CYNSE10512A, 16 for CYNSE10256A (bit [17] is reserved), 15 for CYNSE10128A (bits [17:16] are reserved). Bit[18] is used to indicate whether a mask (=1) or data (=0) entry contained the error. |
| | [27:19] | | **Reserved**. |
| BMULTI | [28] | 0 | **Multi DQ Parity Error Status Bit**. This field is set to 1 when multiple errors were detected during a bus transfer. It is also set to 1 when new parity error occurs and BERR is set. This bit can only be cleared by a user Write. |
| BERR | [29] | 0 | **DQ Parity Error Status Bit**. This bit is set when a parity error is detected during a data transfer across the DQ bus. This bit can only be cleared by a user Write. |
| MULTI | [30] | 0 | **Multi-Parity Error Status Bit**. This bit is set when more than one parity error in the Core is detected during the Parity operation. It also updates when a new parity error occurs and ERR is set. This bit can only be cleared by a user Write. |
| ERR | [31] | 0 | **Parity Error Status Bit**. This bit is set when any parity error in the Core is detected during the Parity operation. This bit can only be cleared by a user Write. |
| ADR | [50, M:32] | 0 | **Current Address**. After a parity check, the address in this field is incremented and is ready for the next address to check for parity. When the Parity operation finishes and an error is detected, assuming no intervening new Parity operations, this field will point to the next entry address to be checked. Bit[50] selects between mask (=1) or data (=0) array. As the address is incremented, this bit is treated as the LSB and toggles before Bit[34]. Bit[33:32] are always 0 because Read Parity operation checks 4 adjacent 72-bit entries. M = 49 for CYNSE10512A, 48 for CYNSE10256A (bit [49] is reserved), 47 for CYNSE10128A (bits [49:48] are reserved). |
| | [71:51] | | **Reserved**. |

### 5.4.12 Control Register (CPR[0:15])

These registers are active only when the device is in the Enhanced Mode. During a Search operation, selecting a GMR will automatically select one of the CPRs to participate in the search as shown in *Figure 5-19*.

| GMR Index | CPR Addr | CPR Index |
|---|---|---|
| 0 | 64 | 0 |
| 1 | 65 | 1 |
| 2 | 66 | 2 |
| 3 | 67 | 3 |
| 4 | 68 | 4 |
| 5 | 69 | 5 |
| 6 | 70 | 6 |
| 7 | 71 | 7 |
| 8 | 72 | 8 |
| 9 | 73 | 9 |
| 10 | 74 | 10 |
| 11 | 75 | 11 |
| 12 | 76 | 12 |
| 13 | 77 | 13 |
| 14 | 78 | 14 |
| 15 | 79 | 15 |

**Figure 5-19. Selection of the CPR through GMR Index**

*Table 5-16* shows the fields of the CPR.

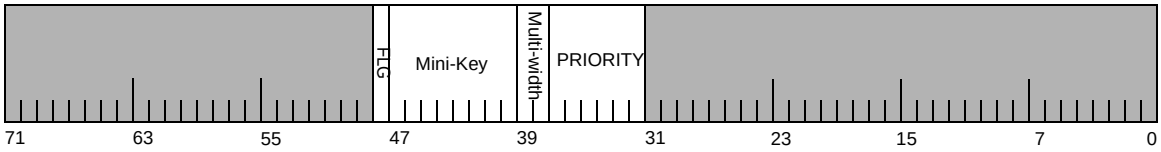



**Figure 5-20. Control Register**

**Table 5-16. Control Register**

| Field | Index (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| | [31:0] | | **Reserved**. |
| PRIORITY | [37:32] | 0 | **Software Priority (Soft Priority)**. This field contains the software priority for the associated command. Smaller numeric value is higher in priority. 0x00 is the highest priority and 0x3F is the lowest priority. |
| Multi-width Configuration | [39:38] | 0 | **Multi-width Configuration**. This field determines the width of the search when used in a MultiSearch command.<br>00 - 72-bit<br>01 - 144-bit<br>10 - 288-bit<br>11 - 576-bit<br>For a single search this field is a don't care. |
| Mini-Key | [47:40] | 0 | **Mini-Key**. This field contains the Mini-Key to be used for the associated command. |
| FLG | [48] | 0 | **Soft Priority Comparison Flag**. When set to 1, Search comparison is with entries that has Soft Priority value equal to or higher (lower priority) than PRIORITY. When set to 0, comparison is only with equal value. |
| | [71:49] | | **Reserved**. |

### 5.4.13 Search Result Register (SRR[15:0])

The SRR register is only active when the device is in the Enhanced mode. It contains status information about where the next-free entry is and what kind of entry it is. There are sixteen SRRs; one SRR associated with one CMPR. The SRR is updated on a Search operation regardless of hit or miss. Two SRRs are used in one Search operation when MSE is set. The second SRR is automatically selected to be the register one index higher. *Table 5-17* below details the SRR fields.

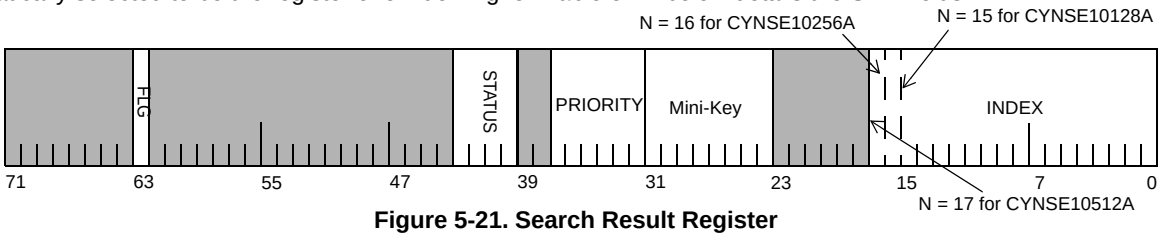



**Figure 5-21. Search Result Register**

**Table 5-17. Search Result Register**

| Field | Index (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| INDEX | [N:0] | 0 | **Index**. This field contains the Hit or Miss index inside the Core. N = 17 for CYNSE10512A, 16 for CYNSE10256A, 15 for CYNSE10128A. |
| | [23:M] | | **Reserved**. M = 18 for CYNSE10512A, 17 for CYNSE10256A, 16 for CYNSE10128A. |
| Mini-Key | [31:24] | 0 | **Mini-Key**. This field contains a copy of the Mini-Key value selected for the Search operation. The value comes from the selected CPR. |
| PRIORITY | [37:32] | 0 | **Soft Priority**. This field holds the priority value of the sub-block where a successful search occurs. Otherwise it holds the priority of the next-free entry sub-block. If there are no free entries, this field is set to the selected CPR's Soft Priority value. This field is not valid when STATUS value is Taken. |
| | [39:38] | | ***Reserved.*** |
| STATUS | [43:40] | 0 | **Next-free Entry Status**. This field contains the status information for the next-free entry.<br>The STATUS value is encoded as described below:<br>0000: Single match. Search hit and there is a single match.<br>0010: Single free entry. Search miss and there is a single free entry.<br>0100: Single free sub-block. Search miss and there is a single free sub-block.<br>0110: Single free block. Search miss and there is a single free block.<br>0001: Multiple matches. Search hit and there are multiple matches.<br>0011: Multiple free entries. Search miss and there are multiple free entries<br>0101: Multiple free sub-blocks. Search miss and there are multiple free sub-blocks.<br>0111: Multiple free blocks. Search miss and there are multiple free blocks.<br>1000: Taken. Search miss and there are no free entries. |
| | [62:44] | | **Reserved**. |
| FLG | [63] | 0 | **Flag**. When set to 1, this flag indicates that a Search operation resulted in a miss, this device has a free entry and the upstream devices in a cascade have a Search miss with no free entries reported. Note that a device with no free entries can still have free blocks or sub-blocks. |
| | [71:64] | | **Reserved**. |

*Table 5-18* below shows the different parts of the INDEX field of the SRR.

**Table 5-18. SRR's INDEX Composition Based on STATUS**

| STATUS | INDEX[17:11] | INDEX[10:9] | INDEX[8:0] |
|---|---|---|---|
| Hit | Block ID | Sub-block ID | Hit Entry Index |
| Free Entry | Block ID | Sub-block ID | Free Entry Index |
| Free Sub-block | Block ID | Sub-block ID | All zeros |
| Free Block | Block ID | All zeros | All zeros |
| Taken | Undefined | Undefined | Undefined |

### 5.4.14 Block Mini-Key Register (BMR)

The BMR is only accessible when the device is in the Enhanced mode. There is one BMR for each block in the device. The following table (*Table 5-19*) shows the BMR fields.

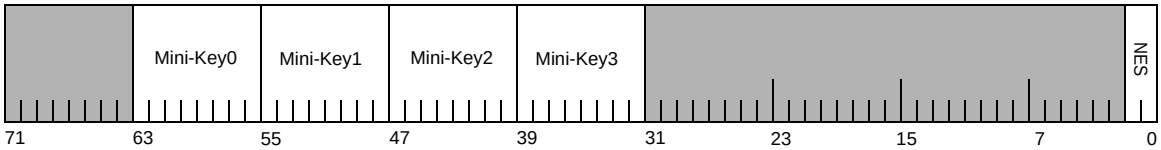



**Figure 5-22. Block Mini-Key Register**

**Table 5-19. Block Mini-Key Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| NES | [1:0] | 0 | **NSE Entry Size**. This field selects the entry width for the associated block. A Search operation that is of different size than the NES will cause the block to not participate in the search.<br>The NES encoding is as follows:<br>00: 72-bit<br>01: 144-bit<br>10: 288-bit<br>11: 576-bit<br>For proper free-entry address computation, this NES field must be set before initializing the entries in a block. The entries of a block must then be initialized to a known value before accessing the block. |
| | [31:2] | | **Reserved**. |
| Mini-Key3 | [39:32] | 0 | **Mini-Key #3**. There are four Mini-Key fields in each BMR. When an operation occurs, all four fields are checked against the Mini-Key in the selected CPR by the command. If there is a match, the associated block is enabled to participate in the operation. |
| Mini-Key2 | [47:40] | 0 | **Mini-Key #2**. See Mini-Key #3 description. |
| Mini-Key1 | [55:48] | 0 | **Mini-Key #1**. See Mini-Key #3 description. |
| Mini-Key0 | [63:56] | 0 | **Mini-Key #0**. See Mini-Key #3 description. |
| | [71:64] | | **Reserved**. |

### 5.4.15 Block Priority Register (BPR)

The BPR is only accessible when the device is in the Enhanced mode. There is one BPR for each block in the device. For each Priority in the BPR, there is an alias address (Block Priority Register Address) which allows individual priorities to be updated. *Table 5-20* shows the BPR fields.

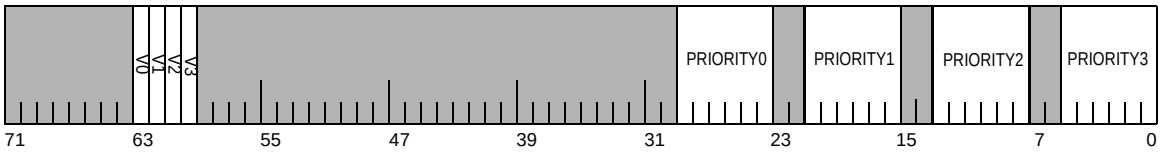



**Figure 5-23. Block Priority Register**

**Table 5-20. Block Priority Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| PRIORITY3 | [5:0] | 0 | **Soft Priority #3**. There are four Priority fields in each BPR. Each Priority represents the priority of a sub-block located within the block associated with this register. Priority value of 00 (hex) is highest and 3F (hex) is lowest in priority.<br>The addresses in a block associated with each Soft Priority is as follows:<br>Entry Index 0 to 511: Priority0<br>Entry Index 512-1023: Priority1<br>Entry Index 1024-1535: Priority2<br>Entry Index 1536-2047: Priority3 |
| | [7:6] | 0 | **Reserved** |
| PRIORITY2 | [13:8] | 0 | **Soft Priority #2**. See Soft Priority #3 description. |
| | [15:14] | 0 | **Reserved** |
| PRIORITY1 | [21:16] | 0 | **Soft Priority #1**. See Soft Priority #3 description. |
| | [23:22] | 0 | **Reserved** |
| PRIORITY0 | [29:24] | 0 | **Soft Priority #0**. See Soft Priority #3 description. |
| | [59:30] | | **Reserved**. |
| V3 | [60] | 0 | **V #3**. There are four V fields in each BPR. Each field represent the valid bit for a sub-block within the block associated with this register. If this bit is set to 1 and the Soft Priority in the CPR selected by the operation matches, the associated sub-block will participate in the operation. If this bit is set to 0, the associated sub-block will not participate in a Search operation. |
| V2 | [61] | 0 | **V #2**. See V #3 description. |
| V1 | [62] | 0 | **V #1**. See V #3 description. |
| V0 | [63] | 0 | **V #0**. See V #3 description. |
| | [71:64] | | **Reserved**. |

### 5.4.16 Block Parity Register (BPAR)

The BPAR is only accessible when the device is in the Enhanced mode. There is one BPAR for each block in the device. *Table 5-21* shows the BPR fields.

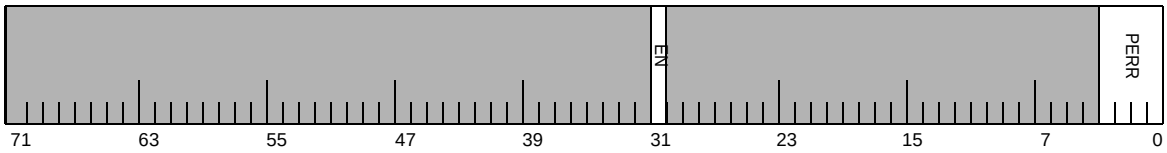



**Figure 5-24. Block Parity Register**

**Table 5-21. Block Parity Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| PERR | [3:0] | 0000 | **Parity Error**. This field contains the status of a Parity operation. It is set to 1 when any parity error is detected during the Parity operation on the associated block. Each bit corresponds to one of the four x72 entries checked during the Parity operation. Bit[0] corresponds to the lowest address. This field is sticky, i.e., it can only be cleared by a user write to the register. This field contains only this block's status. To clear this bit, the user must write a "1" to this bit location. Writing a "0" will preserve the old value. |
| | [30:4] | | **Reserved**. |
| EN | [31] | 0 | **Enable Parity Checking**. This field enables parity checking for the associated block. When set to 1, the associated block will participate in Parity operation. |
| | [71:32] | | **Reserved**. |

### 5.4.17 Block NFA Register (BNFA)

The BNFA is only accessible when the device is in the Enhanced mode. There is one BNFA for each block in the device. *Table 5-22* shows the BNFA fields.

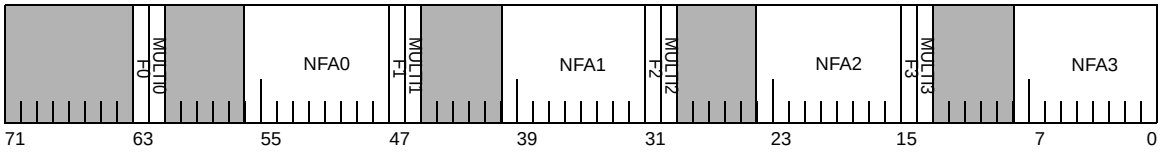



**Figure 5-25. Block NFA Register**

**Table 5-22. Block NFA Register Description**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| NFA3 | [8:0] | 0 | **Next-free Address for Sub-block #3**. This field contains the address/index of the next-free entry within the sub-block of the block associated with this register. If the entry size is larger than x72, the least significant bits will be set to 0 as follows:<br>x144: NFAx[0] = '0',<br>x288: NFAx[1:0] = "00",<br>x576: NFAx[2:0] = "000". |
| | [13:9] | | **Reserved**. |
| MULTI3 | [14] | 1 | **Multiple Free Entries in Sub-block #3**. This field contains the multiple free entry status. If there are multiple free entries in the sub-block, this bit is set to 1. |
| F3 | [15] | 0 | **Free Entry in Sub-block #3**. This field indicates the sub-block full status. If this field is set to 1, the sub-block is full and there are no free entries. If the field is set to 0, the sub-block is not full and there is a free entry. |
| NFA2 | [24:16] | 0 | **Next-free Address for Sub-block #2**. See NFA3 description. |
| | [29:25] | | **Reserved**. |
| MULTI2 | [30] | 1 | **Multi Free Entry in Sub-block #2**. See MULTI3 description. |
| F2 | [31] | 0 | **Free Entry in Sub-block #2**. See F3 description. |
| NFA1 | [40:32] | 0 | **Next-free Address for Sub-block #1**. See NFA3 description. |

**Table 5-22. Block NFA Register Description** (continued)

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| | [45:41] | | **Reserved**. |
| MULTI1 | [46] | 1 | **Multi Free Entry in Sub-block #1**. See MULTI3 description. |
| F1 | [47] | 0 | **Free Entry in Sub-block #1**. See F3 description. |
| NFA0 | [56:48] | 0 | **Next-free Address for Sub-block #0**. See NFA3 description. |
| | [61:57] | | **Reserved**. |
| MULTI0 | [62] | 1 | **Multi Free Entry in Sub-block #0**. See MULTI3 description. |
| F0 | [63] | 0 | **Free Entry in Sub-block #0**. See F3 description. |
| | [71:64] | | **Reserved**. |

### *5.4.18 Block Priority Register Aliases (BPRA)*

The BPRA is only accessible when the device is in the Enhanced mode. There are four BPRAs for each block. These pseudo registers provide an alternate means to update the associated block's BPR. The fields of these BPRAs exactly match the BPR fields. Please see the corresponding BPR fields for the descriptions of the BPRAs fields.

*Table 5-23* shows the BPRA fields for BPR's Priority0.

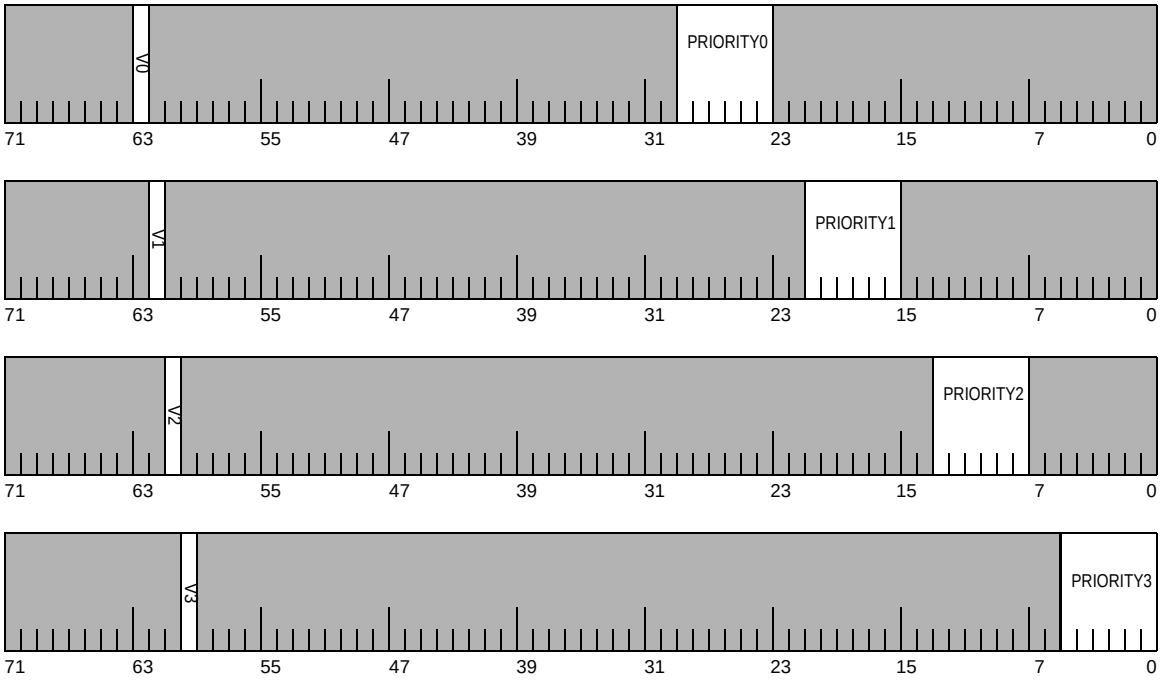



**Figure 5-26. Block Priority Register Aliases**

**Table 5-23. Block Priority Register Alias for Priority #0 Fields**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| | [23:0] | | **Reserved**. |
| PRIORITY0 | [29:24] | 0 | **Priority #0**. |
| | [62:30] | | **Reserved**. |
| V0 | [63] | 0 | **V #0**. |
| | [71:64] | | **Reserved**. |

*Table 5-24* shows the BPRA fields for BPR's Priority1.

**Table 5-24. Block Priority Register Alias for Priority #1 Fields**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| | [15:0] | | **Reserved**. |
| PRIORITY1 | [21:16] | 0 | **Priority #1**. |
| | [61:22] | | **Reserved**. |
| V1 | [62] | 0 | **V #1**. |
| | [71:63] | | **Reserved**. |

*Table 5-25* shows the BPRA fields for BPR's Priority2.

**Table 5-25. Block Priority Register Alias for Priority #2 Fields**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| | [7:0] | | **Reserved**. |
| PRIORITY2 | [13:8] | 0 | **Priority #2**. |
| | [60:14] | | **Reserved**. |
| V2 | [61] | 0 | **V #2**. |
| | [71:62] | | **Reserved**. |

*Table 5-26* shows the BPRA fields for BPR's Priority3.

**Table 5-26. Block Priority Register Alias for Priority #3 Fields**

| Field | Range (decimal) | Initial Value (binary) | Description |
|---|---|---|---|
| PRIORITY3 | [5:0] | 0 | **Priority #3**. |
| | [59:6] | | **Reserved**. |
| V3 | [60] | 0 | **V #3**. |
| | [71:61] | | **Reserved**. |

## 5.5 Multi-Hit Description

For a Search operation, Multi-Hit is set when there are multiple matching entries in the array (Non-Enhanced) or in the selected blocks (Enhanced). For a Learn operation, Multi-Hit is set when there are multiple free entries in the array (Non-Enhanced) or in the selected blocks (Enhanced). Multi-Hit maintains its value until another operation changes it.

In the Non-Enhanced mode, the Multi-Hit signal is valid four cycles after the command is issued, regardless of the setting of TLSZ and HLAT. In the Enhanced mode, the Multi-Hit signal is valid at the same time as SSV.

## 5.6 Clocks

If the CLK_MODE pin is LOW, Ayama 10000A receives the CLK2X and PHS_L signals. It uses the PHS_L signal to divide CLK2X and generate an internal clock (CLK[6]), as shown in *Figure 5-27*. If the CLK_MODE pin is HIGH, Ayama 10000A receives CLK1X only. Ayama 10000A uses an internal phase-locked loop (PLL) to lock the frequency of CLK1X and generates the internal clock CLK, as shown in *Figure 5-28*. Also noted on these figures are cycles A and B. In CLK2X mode, cycle A begins on the rising edge of CLK2X, when PHS_L is Low, and ends on the next rising edge. Cycle B begins on the rising edge of CLK2X when PHS_L is High, and ends on the subsequent CLK2X rising edge. For CLK1X mode, the falling edge of CLK1X is considered the end of cycle A, while the rising edge after that is considered the end of cycle B. Valid data must be available for the NSE at the END of any cycle. **Note**. For the purpose of showing timing diagrams, all such diagrams in this document will be shown in CLK2X mode. For a timing diagram in CLK1X mode, the following substitution can be made (see *Figure 5-29*).

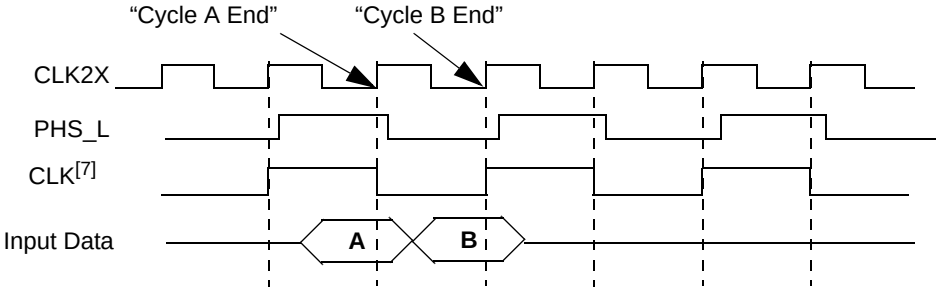



**Figure 5-27. Ayama 10000A Clocks (CLK2X and PHS_L)**

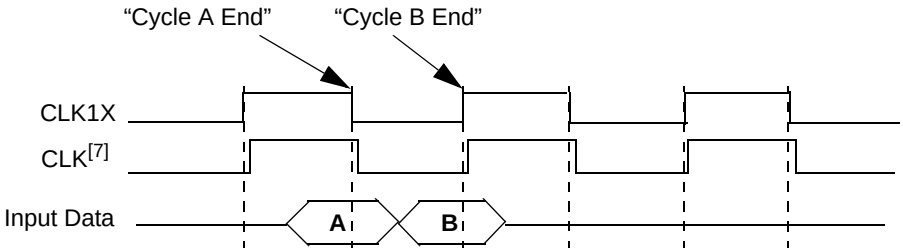



**Figure 5-28. Ayama 10000A Clocks (CLK1X)**

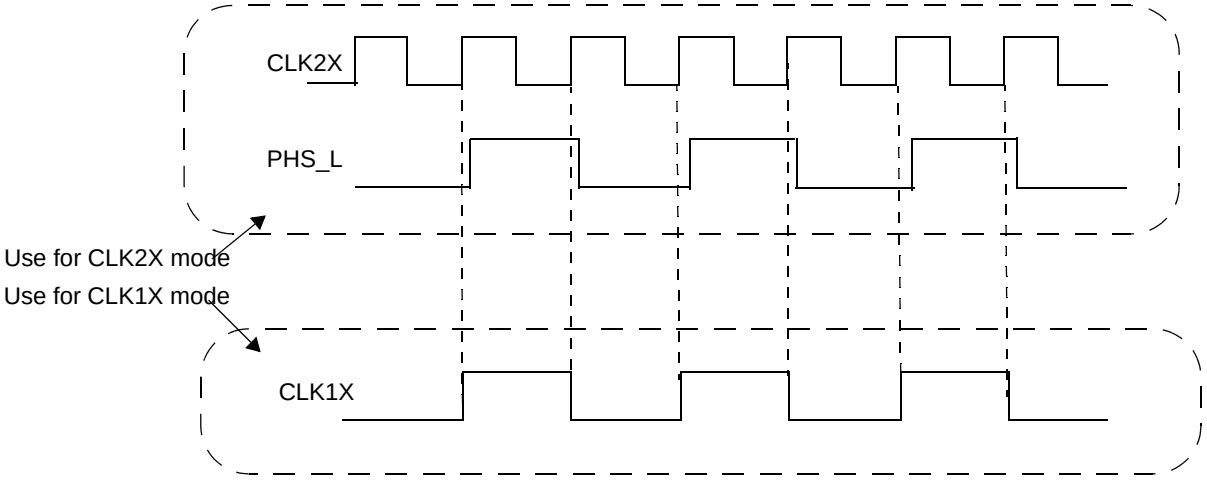



**Figure 5-29. Ayama 10000A Clocks for All Timing Diagrams**

**Notes:**
6. "CLK" is an internal clock signal.
7. Any reference to "CLK" cycles means one cycle of CLK.

## 5.7 Phase-Locked Loop

When the device first powers up, it takes 0.5 milliseconds (ms) after the power supplies are stable to lock the internal PLL. During this time period, the RST_L must be held LOW for proper power-up. All signals to the device in CLK1X mode are sampled by a clock that is generated by multiplying CLK1X by two. Since the PLL has a locking range, the device will only work between the range of frequencies specified in the timing specification wave form section of this data sheet (see Section 10.0, “AC Timing Parameters, Waveforms and Test Conditions,” on page 130).

## 5.8 Pipeline Latency

Pipeline latency is used to give enough time for a cascaded system’s arbitration logic to determine the device that will drive the output of an operation on the SRAM bus. The Ayama 10000A has a default of 4 CLK1X pipeline latencies but more latency can be added as necessary. The number of additional pipeline stages is set in the TLSZ and HLAT fields of the COMMAND Register. The number of pipeline stages also controls the maximum operating speed for a single Ayama 10000A NSE. *Table 5-27* lists the additional pipeline stages and the maximum operating speed.

**Table 5-27. Pipeline Stages and Maximum Operating Speed**

| TLSZ | Additional CLK1X Cycle Latency | Total Search CLK1X Cycle Latency | Maximum Operating Speed (CLK1X/CLK2X) |
|---|---|---|---|
| 00 | 0 | 4 | 83/166 MHz |
| 01 | 1 | 5 | 100/200 MHz |
| 10 | 2 | 6 | 133/266 MHz |
| 11 | Invalid | Invalid | Invalid |

Internal register for configuration: CMD

## 5.9 DQ Bus Encoding of Ayama 10000A Address Space

A set of parameters for an operation must be provided in the DQ bus to the NSE along with the command sent in the CMD bus. This section covers the encoding of the parameters expected in the DQ bus. There are two ways of addressing an entry location or an internal register within the device: Direct and Indirect. The internal registers can only use Direct addressing while Data array, Mask array and SRAM access operations can use either Direct or Indirect. Indirect addressing allows the use of the SSR register INDEX field as the address for a Read, Write and Learn operations. Indirect Read operation on the internal registers will return undefined values.

### 5.9.1 *Addressing the Data Array, Mask Array and External SRAM*

The following table (*Table 5-28*) lists the parameters for addressing the Data array, Mask array and external SRAM.

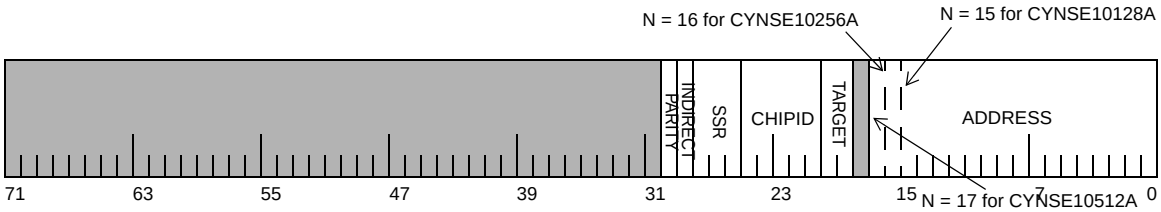



**Figure 5-30. Data Array, Mask Array and External SRAM Address Space Encoding**

**Table 5-28. Data Array, Mask Array and External SRAM Address Space Encoding**

| Field | Range (decimal) | Description |
|---|---|---|
| ADDRESS | [N:0] | **Address**. This field contains the location of the entry to be accessed on Direct Addressing operations. N = 17 for CYNSE10512A, 16 for CYNSE10256A, 15 for CYNSE10128A. Note that on a burst Read or Write operation, the appropriate burst register (WBURADR or RBURADR) INDEX field is used as the address. |
| | [M] | **Reserved**. M = 18 for CYNSE10512A, [18:17] for CYNSE10256A, [18:16] for CYNSE10128A. |
| TARGET | [20:19] | **Target Area Select**. This field indicates in what context the access takes place. It is encoded as follows:<br>00: Access the Data array<br>01: Access the Mask array<br>10: Access the external SRAM<br>11: Access the Internal Registers (Refer to*Section 5.9.2*) |
| CHIPID | [25:21] | **Device ID**. This field indicates which NSE device should respond to the READ or WRITE operation. CHIPID value “11111” indicates a broadcast operation. |
| SSR | [28:26] | **SSR Index**. This field selects the SSR for Indirect accesses. |
| INDIRECT | [29] | **Indirect Addressing Enable**.<br>1: Indirect.<br>When DQ[30] is 0, the selected SSR register INDEX field is used to generate the address as follow: {SSR[17:3], SSR[2] \| DQ[2], SSR[1] \| DQ[1], SSR[0] \| DQ[0]}.<br>To issue a Read Parity command, this bit must be set to 1. The address of the entry location to be checked is taken from the PARITY control register’s ADR field. Note that Read Parity command can be issued only on a Read command. Issuing an Indirect Write with Bit[30] set to 1 will result in No-Operation.<br>0: Direct. DQ[17:0] contains the address for the operation. |
| PARITY | [30] | **Read Parity**. This bit must be set to 1 to issue a Read Parity command. It is valid only when DQ[29] is also set to 1. |
| | [71:31] | **Reserved**. |

The address generation of the SADR bits varies depending on the operation being performed. The following table (*Table 5-29*) shows the SRAM address generation for the various operations.

**Table 5-29. SRAM Address Generation**

| Command | SRAM Operation | SADR[M+8:M+6][8] | SADR[M+5:M+1] | SADR[M:0][8,9] |
|---|---|---|---|---|
| Search | Read | EADR[2:0] | ID[4:0] | Index[M:0] |
| Learn | Write | EADR[2:0] | ID[4:0] | NFA/SRR[M:0][10] |
| SRAM PIO Read | Read | EADR[2:0] | ID[4:0] | DQ[M:0] |
| SRAM PIO Write | Write | EADR[2:0] | ID[4:0] | DQ[M:0] |
| Indirect Read | Read | EADR[2:0] | ID[4:0] | SSR[M:0] \| DQ[2:0][11] |
| Indirect Write | Write | EADR[2:0] | ID[4:0] | SSR[M:0] \| DQ[2:0][11] |

**Notes:**
8. When MultiSearch feature is enabled, SADR[M+8] is not used and SADR[M] will be 0 to indicate Array0 output or 1 to indicate Array 1 output.
9. M = 17 for CYNSE10512A; M = 16 for CYNSE10256A; M = 15 for CYNSE10128A.
10. Non-Enhanced mode uses NFA register. Enhanced mode uses SRR register.
11. SSR[2:0] is OR-ed with DQ[2:0] to generate the SADR[2:0] values.

### 5.9.2 Addressing the Internal Registers

The following table (*Table 5-30*) details the parameters expected (in DQ bus) to access the internal registers of the NSE.

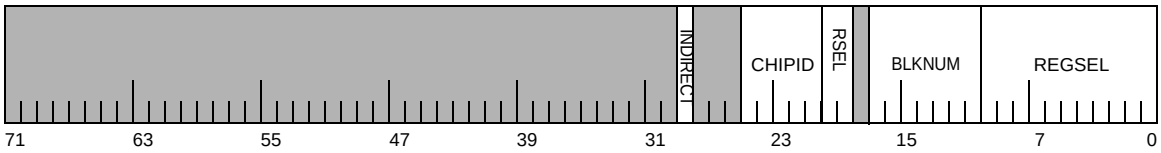



**Figure 5-31. Internal Register Address Space Encoding**

**Table 5-30. Internal Register Address Space Encoding**

| Field | Range (decimal) | Description |
|---|---|---|
| REGSEL | [10:0] | **Register Address Selected**. This field selects which internal register to address.*Table 5-6* lists the registers that are available. |
| BLKNUM | [17:11] | **Block Number**. This field selects the block within the device that will participate in the operation. It is only used when accessing block specific internal registers (BMR, BPR, BPAR, BNFA and BPRA0-3). For other internal register accesses, this field must be set to 0. |
| | [18] | **Reserved**. |
| RSEL | [20:19] | **Register Area Select**. This field indicates in what context the access takes place. It must be set to “11”. |
| CHIPID | [25:21] | **Device ID**. This field indicates which NSE device should respond to the READ or WRITE operation. CHIPID value “11111” indicates a broadcast operation. |
| | [28:26] | **Reserved**. |
| INDIRECT | [29] | **Indirect Addressing Enable**. This bit must be cleared to 0. |
| | [71:30] | **Reserved**. |

## 5.10 Depth Cascading

The NSE application can depth-cascade the devices to various table sizes of different widths (72-bit, 144-bit, 288-bit or 576-bit). The devices perform all the necessary arbitration to decide which device will drive the SRAM bus. Some operations and features are not cascadable, which means that the operation or feature is on a device-by-device basis and the results are not propagated to the next device. *Table 5-31* lists those operations and features. The following subsections covers the interconnects when the devices in a cascade operates in the Non-Enhanced mode or Enhanced Mode with MSE set to 0 (MultiSearch disabled). For device interconnects when operating in Enhanced mode with MultiSearch enabled, please refer to *Figure 6-43*.

**Table 5-31. Cascadability of Operations and Features**

| Operations/# of Devices | Non-Enhanced | | | Enhanced Mode with MSE = 0 | | | Enhanced Mode with MSE = 1 | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2-8 | 9-31 | 1 | 2-8 | 9-31 | 1 | 2-8 | 9-31 |
| MultiSearch Command | No | No | No | No | No | No | Yes | Yes | No |
| Learn Command | Yes | Yes | No | Yes | Yes | No[12] | Yes | No[12] | No[12] |
| Soft Priority | No | No | No | Yes | No[12] | No[12] | Yes | No[12] | No[12] |
| FULL | Yes | Yes | No | Yes | Yes | No | Yes | No | No |
| MULTI_HIT | Yes | No | No | Yes | No | No | Yes | No | No |

### 5.10.1 Depth Cascading up to Eight Devices in One Block

*Figure 5-32* shows the interconnection of up to eight devices in a cascade to form 2M × 72, 1M × 144, 512K × 288, or 256K x 576 tables. Each NSE asserts the LHO[1] and LHO[0] signals to inform downstream devices of its result. LHI[6:0] signals for a device are connected to LHO signals of the upstream devices. The host ASIC must program the TLSZ = 01 (binary) for each of up to eight devices in a block. Only a single device drives the SRAM bus in any single cycle.

**Note:**
12. Software solutions are possible for these cases. Please refer to specific application notes.

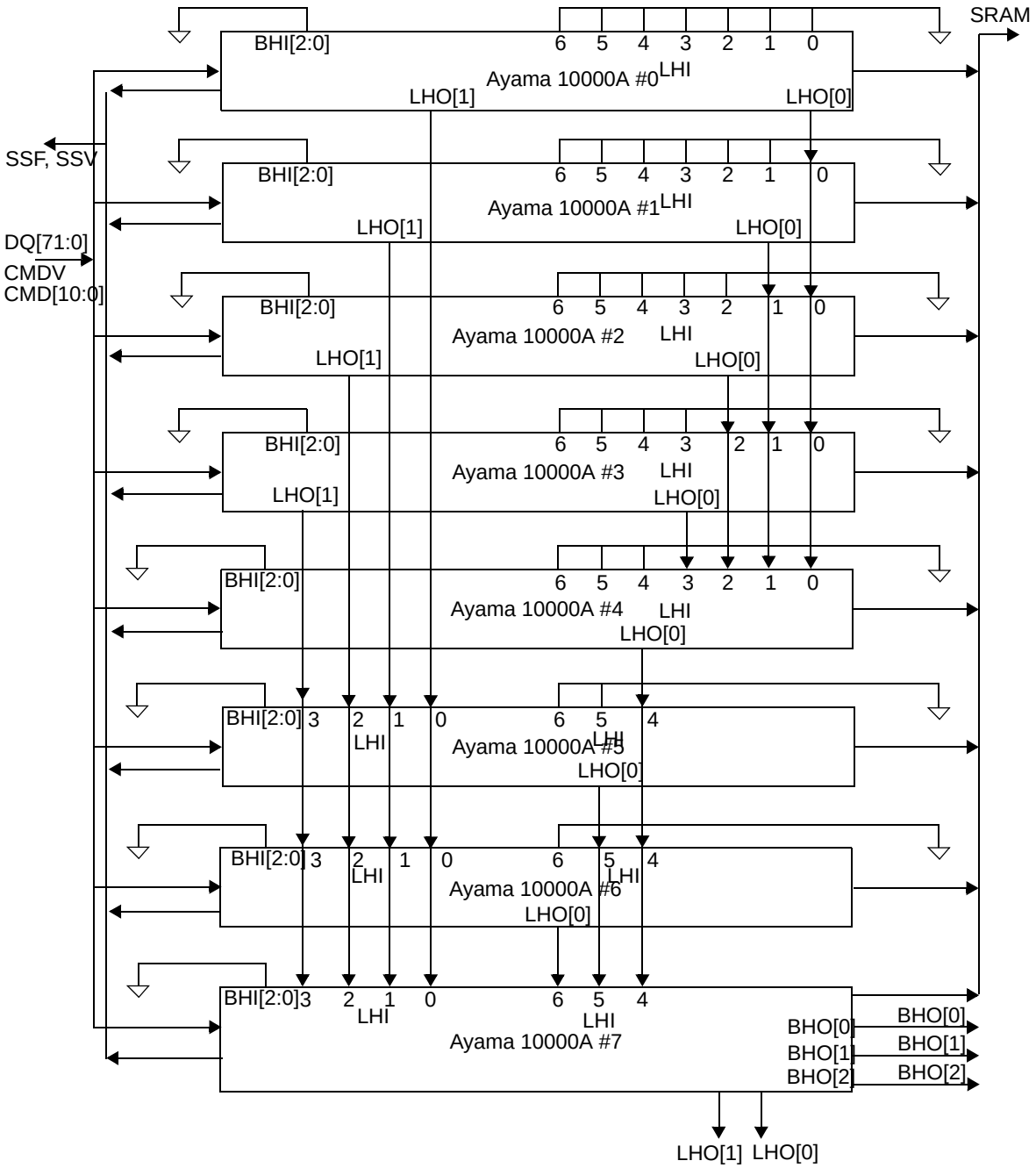



**Figure 5-32. Depth Cascading in a Single Block**

### 5.10.2 Depth Cascading up to 31 Devices in 4 Blocks

*Figure 5-33* shows the cascading of up to four blocks. Each block except the last contains up to eight Ayama 10000A devices, and the interconnection within each with the cascading of up to eight devices in a block was shown in the previous subsection.

**Note**. The interconnection between blocks for depth cascading is important. For each Search, a block asserts BHO[2], BHO[1], and BHO[0]. The BHO[2:0] signals for a block are taken only from the last device in that block. For all other devices within that block, these signals stay open. The host ASIC must program TLSZ = 10 (binary) in each of the devices for cascading up to 31 devices (in up to four blocks).

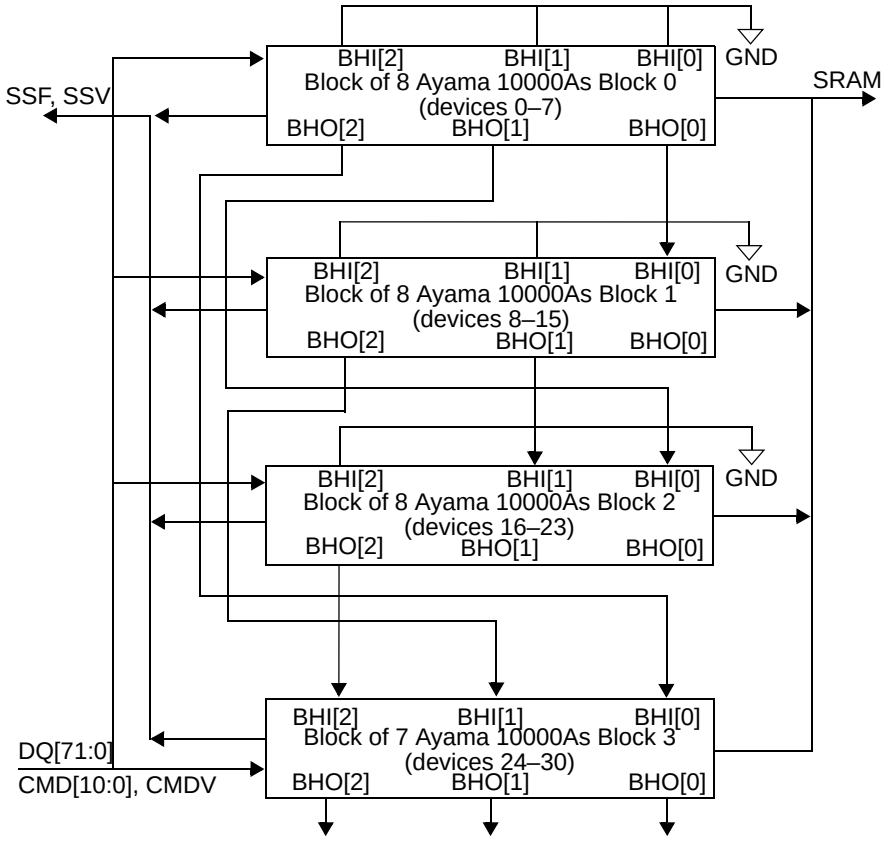



**Figure 5-33. Depth Cascading 4 Blocks**

### 5.10.3 Depth Cascading for a FULL Signal

Bit[0] of each of the 72-bit entries is designated as a special bit (1 = occupied, 0 = empty). For each Learn or PIO Write to the data array, each device asserts FULO[1] or FULO[0] depending on whether or not it has any empty locations within it (see *Figure 5-34*). Each device combines the FULO signals from the devices above it with its own full status to generate a FULL signal that gives the full status of the table up to the device asserting the FULL signal. *Figure 5-34* shows the hardware connection diagram for generating the FULL signal that goes back to the ASIC. In a depth-cascaded block of up to eight devices, the FULL signal from the last device should be fed back to the ASIC controller to indicate the fullness of the table. The FULL signal of the other devices should be left open. **Note**. The Learn instruction is supported for only up to eight devices, whereas FULL cascading is allowed only for one block in tables containing more than eight devices. In tables for which a Learn instruction is not going to be used, the bit[0] of each 72-bit entry should always be set to 1.

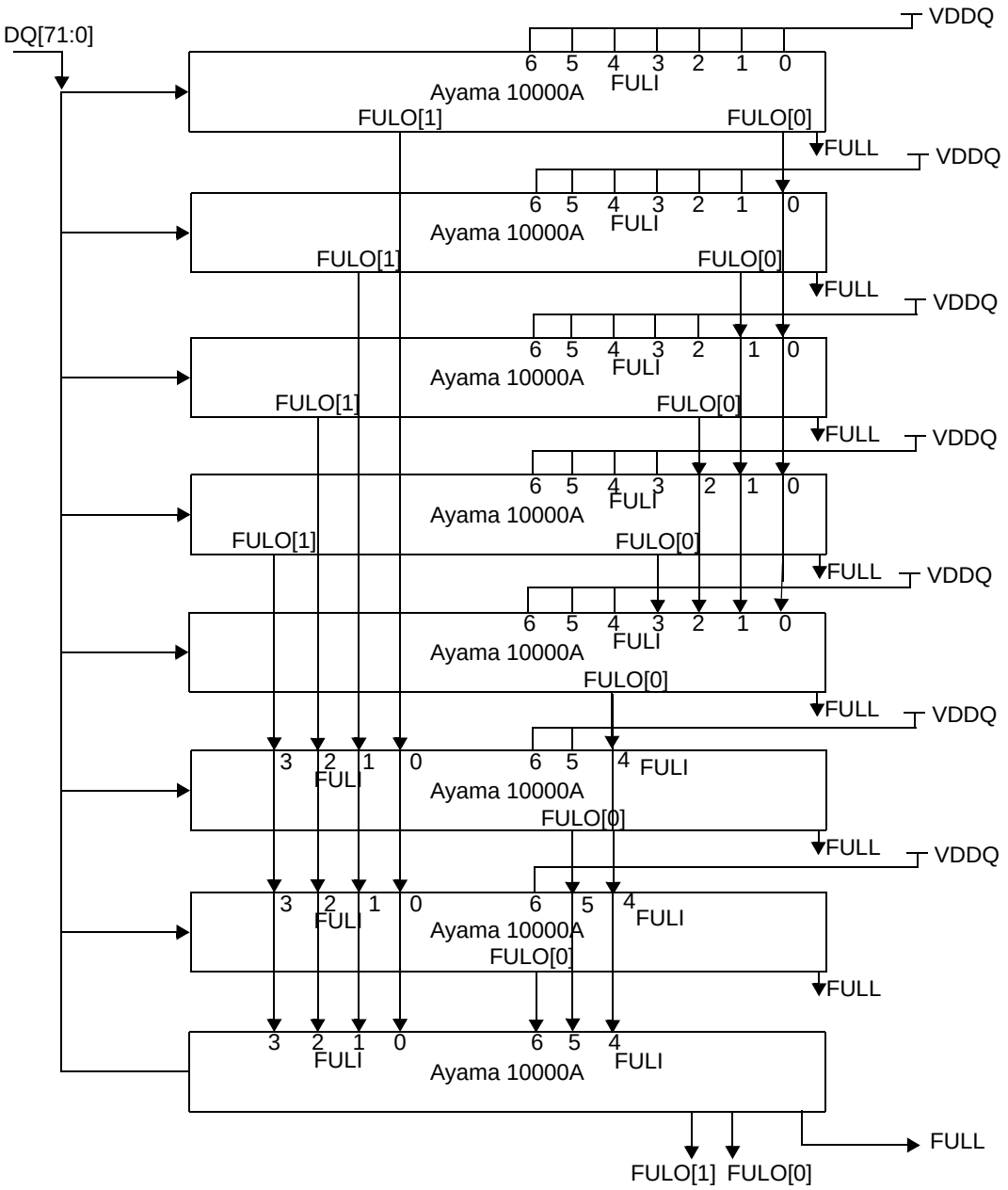



**Figure 5-34. FULL Signal Generation in a Cascaded Table**

## 5.11 Device Selection in a Cascaded System

On a Direct Read operation, if the CHIPID field matches the current device's ID[4:0], this device will respond to the read request. If the CHIPID field does not match, the device will not respond. Note that if the CHIPID does not match any device in the cascade, no read acknowledge will be generated. If the CHIPID is set to broadcast ("11111", binary), the device with the LDEV bit set to 1 will respond to the read request.

On an Indirect Read operation, if the CHIPID field matches the current device's ID[4:0], this device will respond to the read request. If the CHIPID field does not match, the device will not respond. Note that if the CHIPID does not match any device in the cascade, no read acknowledge will be generated. If the CHIPID is set to broadcast ("11111"), each device examines its SSR register's VAL and GVAL bits. The device with one of these bits set responds to the read request. If none of these bits are set (this occurs when a Search has not been done after a reset), no read acknowledge will be returned.

On a Direct Write operation, if the CHIPID field matches the current device's ID[4:0], this device will perform the write request. If the CHIPID field does not match, the device will not respond. If the CHIPID is set to broadcast, all devices write to the desired location.

On an Indirect Write operation, if the CHIPID field matches the current device, this device will perform the write request. If the CHIPID field does not match, the device will not respond. If the CHIPID is set to broadcast, different actions occur based upon the target. If the target is an internal register, the write request is ignored. If the target is a Data or Mask array, the device with the VAL field of the SSR register set performs the write request. If the target is external SRAM, the device with the LRAM field set will drive the SRAM signals.

### 5.12 Power-up Sequence

Ayama 10000A requires that the power supplies follow a known sequence to ensure successful device power-up to set the device to its initial state. RST_L should be held Low before the power supplies ramp-up and must be held Low for a duration of time afterward. Clock signals (CLK1X/CLK2X and PHS_L) should start running after the power supplies become stable. All IO voltages ($V_{DDQ}$, which includes $V_{DDQ\_ASIC}$ and $V_{DDQ\_SRAM}$) should only ramp up only after the core voltage ($V_{DD}$) level reaches 90% point.

The following describes the proper power-up sequence required to correctly initialize the Cypress Network Search Engines before functional access to the device can begin. The following steps are presented in order of priority.

1. Hold RST_L and TRST_L signals low and power up $V_{DD}$. Then power up $V_{DDQ}$ when $V_{DD}$ is stable. TRST_L can be tied to RST_L, tied low permanently, or driven asynchronously (more information on resetting JTAG in the JTAG section of the data sheet).
2. Start running CLK2X/CLK1X and PHS_L (if applicable) after $V_{DDQ}$ powers up.
3. Hold RST_L low for at least 0.5 ms + $t_{RSTL}$ after the clock signal is stable, then drive high.
4. Allow device 4 CLK1X/8 CLK2X cycles of idle time before issuing functional accesses.

RST_L should be set High with sufficient hold time with respect to CLK2X. Following steps 1 through 4 will power up the device gracefully and ensure proper operation of the device. *Figure 5-35* illustrates the proper sequences of the power-up operation.

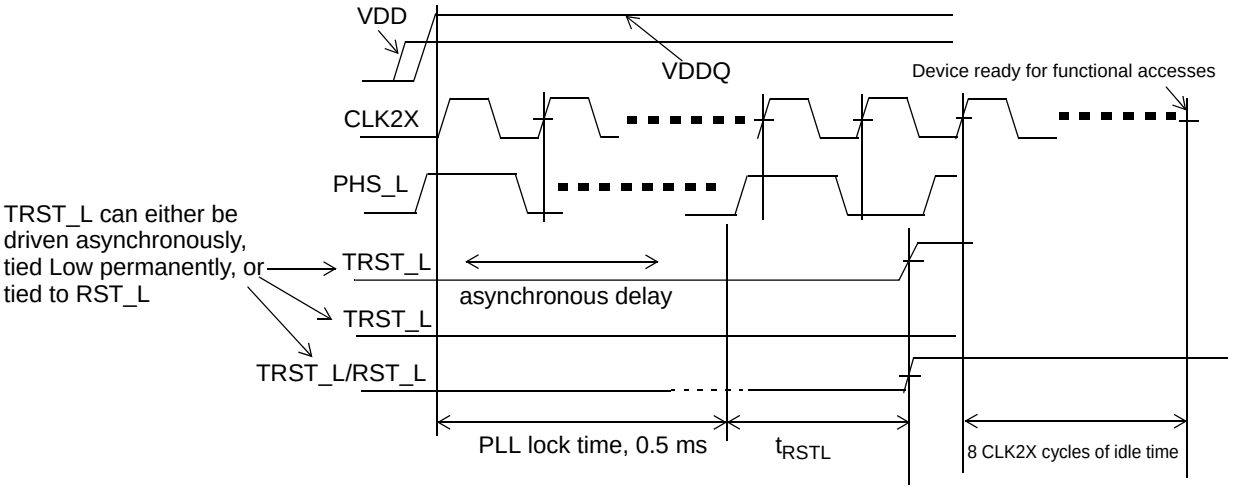



**Figure 5-35. Proper Power-up Sequence**

Note: The PLL will lose lock if the CLK2X/CLK1X or PHS_L (if applicable) stop transitioning.

# 6.0 Operations and Timing Diagrams

A master device, such as an ASIC controller, issues commands to the Ayama 10000A device using the CMD bus and CMDV signals. The following subsections describe the operation of these commands.

## 6.1 Command Encoding

The Ayama 10000A device implements four basic commands, as shown in *Table 6-1*. The Search command is a non-blocking operation which allows another operation to be issued immediately on the following cycle. Read, Write and Learn are blocking operations. There are also other derivative commands that the device supports. The operation of basic commands as well as the derivative commands are explained in more detail in the following sections.

The command code must be presented to CMD[1:0] while keeping the CMDV signal HIGH for two CLK2X cycles (cycles A and B) when the CLK_MODE pin is LOW. In CLK2X mode, the controller ASIC must align the instructions using the PHS_L signal. The command code must be presented to CMD[1:0] while keeping the CMDV signal HIGH for one CLK1X cycle when the CLK_MODE pin is HIGH. In CLK1X mode, cycle A ends on the falling edge of CLK1X and cycle B ends on the rising edge of CLK1X. Valid data must be present at the edge ending any given cycle for valid inputs. The CMD[10:2] field passes command parameters in cycles A and B. All commands must begin with cycle A operations.

**Table 6-1. Command Codes**

| Command Code (binary) | Command | Description |
|---|---|---|
| 00 | Read | Reads from one of the following: data array, mask array, device registers, or external SRAM. Read command is also used to issue Read Parity command. |
| 01 | Write | Writes to one of the following: data array, mask array, device registers, or external SRAM. |
| 10 | Search | Searches the data array for a desired pattern using the specified register from the GMR array and local mask associated with each data cell. |
| 11 | Learn | The device has internal storage for up to sixteen comparands that it can learn. The device controller can insert these entries at the next-free address (as specified by the NFA register) using the Learn instruction. |

## 6.2 Command Bus Parameters

### *6.2.1 Extended Address (EADR)*

The EADR field of the CMD bus, CMD[8:6], allows flexibility in the accessing of associated data SRAM. For all operations, the EADR field is mapped to the most significant bits of the SADR output bus. SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, and SADR[23:21] for CYNSE10128A.

This field allows for the specific region of the associated data address space to be targeted for an operation. One practical application of this is when two 36-bit keys are packed into a single 72-bit NSE entry. This is because the Ayama 10000A NSE is 72-bit addressable and outputs a single index for each 72-bit entry. In this case, the EADR field is used to differentiate between the two keys.

### *6.2.2 Enhanced Mode and Non-Enhanced Mode Parameters*

*Table 6-2*, *Table 6-3*, and *Table 6-4* list the command bus fields that contain the Ayama 10000A command parameters and their respective cycles.

**Table 6-2. Non-Enhanced Mode (EMODE = 0)**

| Cmd | Cycle | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| READ | A | X | X | EADR[2:0][13] | | | 0 | | | 0 = Single | 0 | 0 |
| | B | | | 0 | | | | | | 1 = Burst | | |
| WRITE | A | GMR[3] | 0=Normal | EADR[2:0][13] | | | GMR[2:0] | | | 0 = Single | 0 | 1 |
| | B | | 1=Parallel | 0 | | | | | | 1 = Burst | | |
| SEARCH | A | GMR[3] | 0=x72 | EADR[2:0][13] | | | GMR[2:0] | | | 0=x72 or x144 | 1 | 0 |
| | | | 1=x144 | | | | | | | 1=x288 (first cycle) | | |
| | | | X=x288 | | | | | | | 0=x288 (last cycle) | | |
| | B | X | X | SSR[2:0] | | | CMPR[3:0] | | | | | |
| LEARN | A | X | X | EADR[2:0][13] | | | CMPR[3:0] | | | | 1 | 1 |
| | B | | | 0 | | 0=x72 | | | | | | |
| | | | | | | 1=x144 | | | | | | |

**Table 6-3. Enhanced Mode (EMODE = 1) with MultiSearch Disabled (MSE = 0)**

| Cmd | Cycle | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| READ | A | X | X | EADR[2:0][13] | | | 0 | | | 0 = Single | 0 | 0 |
| | B | | | 0 | | | | | | 1 = Burst | | |
| WRITE | A | GMR[3] | 0=Normal | EADR[2:0][13] | | | GMR[2:0] | | | 0 = Single | 0 | 1 |
| | B | | 1=Parallel | 0 | | | | | | 1 = Burst | | |
| SEARCH | A | GMR[3] | 0=x72 | EADR[2:0][13] | | | GMR[2:0] | | | 0=x72 or x144 | 1 | 0 |
| | | | 1=x144 | | | | | | | 1=x288/x576 (all except last cycle) | | |
| | | | X=x288/x576 | | | | | | | 0=x288/x576 (last cycle) | | |
| | B | X | X | SSR[2:0] | | | CMPR[3:0] | | | | | |
| LEARN | A | 0=Data 1=Mask | 0=CMPR 1=DQ | EADR[2:0][13] | | | CMPR[3:0] | | | | 1 | 1 |
| | B | 0 | 0 | 0 | 00: x72; 01: x144; 1X:x288/x576 (all except last cycle); 0X:x288/x576 (last cycle) | | | | | | | |

**Table 6-4. Enhanced Mode (EMODE = 1) with MultiSearch Enabled (MSE = 1)**

| Cmd | Cycle | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| READ | A | X | X | 0 | EADR[1:0][13] | | 0 | | | 0 = Single | 0 |
| | B | | | 0 | | | | | | 1 = Burst | |
| WRITE | A | GMR[3] | 0=Normal | 0 | EADR[1:0][13] | | GMR[2:0] | | | 0 = Single | 0 |
| | B | | 1=Parallel | 0 | | | | | | 1 = Burst | |
| SEARCH | A | GMR[3] | 0=x72 | 0=Single-Search 1=Multi-Search | EADR[1:0][13] | | GMR[2:0] | | | 0=x72 or x144 | 1 |
| | | | 1=x144 | | | | | | | 1=x288/x576 (all except last cycles) | |
| | | | X=x288/x576 | | | | | | | 0=x288/x576 (last cycle) | |
| | B | X | X | SSR[2:0] | | | CMPR[3:0] | | | | |
| LEARN | A | 0=Data 1=Mask | 0=CMPR 1=DQ | 0 | EADR[1:0][13] | | CMPR[3:0] | | | | 1 |
| | B | 0 | 0 | 0 | 00: x72; 01: x144; 1X:x288/x576 (all except last cycle); 0X:x288/x576 (last cycle) | | | | | | |

**Note:**

13. The NSE density determines to which SADR field EADR[2:0] is mapped. In Ayama10128, SADR[23:21] gets EADR[2:0]; In Ayama10256, SADR[24:22] gets EADR[2:0]; In Ayama10512, SADR[25:23] gets EADR[2:0].
14. When issuing x288 and x576 searches, there are multiple A and B cycle. In this scenario the CMPR[3:0] must change for every B-cycle of the x288/x576 search, if that key is to be learnt at a later stage. If the search key need not be learnt, the CMPR[3:0] is a don't care. Similarly GMR values could vary depending which part of the key needs to be masked for x288 and x576 searches.

## 6.3 Read Command

In both the Non-Enhanced and Enhanced mode, the Read command can be issued to read data from the data array, mask array, NSE-associated SRAMs or internal registers. The Read can be a single or burst Read (*Table 6-5*). Burst Read can only be issued for accesses to the data or mask array locations. SRAM Read operation is covered in *Section 6.7.1* to *Section 6.7.3*. In the Enhanced mode, the Read command is also used to issue the Read Parity command, which is issued to perform parity check on the data and mask array entries.

Read is a blocking operation and must be completed before the next operation can be issued.

**Table 6-5. Single/Burst Read Command Parameters**

| CMD Parameter CMD[2] | Read Command | Description |
|---|---|---|
| 0 | Single Read | Reads a single location of the data array, mask array, NSE-associated SRAM or internal registers. All access information is applied on the DQ bus. |
| 1 | Burst Read | Reads a block of locations from the data or mask array as a burst. RBURREG specifies the starting address and the length of the data transfer from the data or mask array; it also auto-increments the address for each access. All other access information is applied on the DQ bus. |

### *6.3.1 Single Read*

A single Read operation lasts six cycles (CLK1X) with the data driven out by the NSE on cycle 5 as illustrated in *Figure 6-1*.

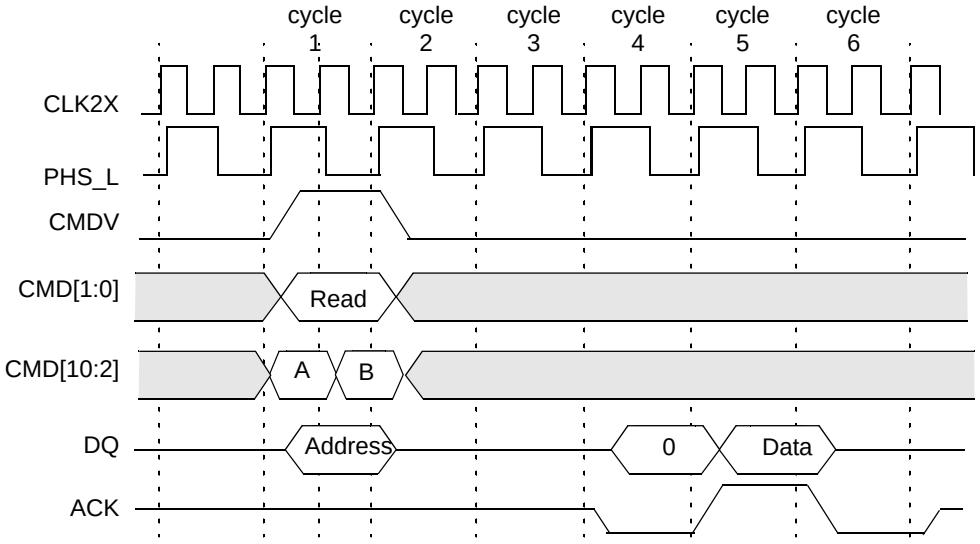



**Figure 6-1. Single-Location Read Cycle Timing**

Read operation sequence:

- **Cycle 1**: The host ASIC applies the Read instruction on CMD[1:0] (CMD[2] = 0) using CMDV = 1, and the DQ bus supplies the address. The host ASIC selects the Ayama 10000A device for which ID[4:0] matches the DQ[25:21] lines. If DQ[25:21] = 11111, the host ASIC selects the Ayama 10000A with the LDEV bit set. The host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6] in cycle A of the Read instruction if the Read is directed to the external SRAM.
- **Cycle 2**: The host ASIC floats DQ[71:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[71:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive the DQ[71:0] bus and drives the ACK signal from Z to LOW.
- **Cycle 5**: The selected device drives the Read data from the addressed location on the DQ[71:0] bus, and drives the ACK signal HIGH.
- **Cycle 6**: The selected device floats the DQ[71:0] to a three-state condition and drives the ACK signal LOW.

At the termination of cycle 6, the selected device releases the ACK line to a three-state condition. The Read instruction is complete and the next operation can begin.

### 6.3.2 Burst Read

The burst Read operation lasts 4 + 2n CLK1X cycles, where n is the number of the burst length as specified by the BLEN field of the RBURREG. The BLEN field is automatically decremented after each Read of the burst, so the register must be reinitialized before another burst Read is issued. Instead of the address provided by the user, the address in the INDEX field of the RBURREG is used and incremented each cycle.

*Figure 6-2* illustrates the timing diagram for the burst Read of the data or mask array.

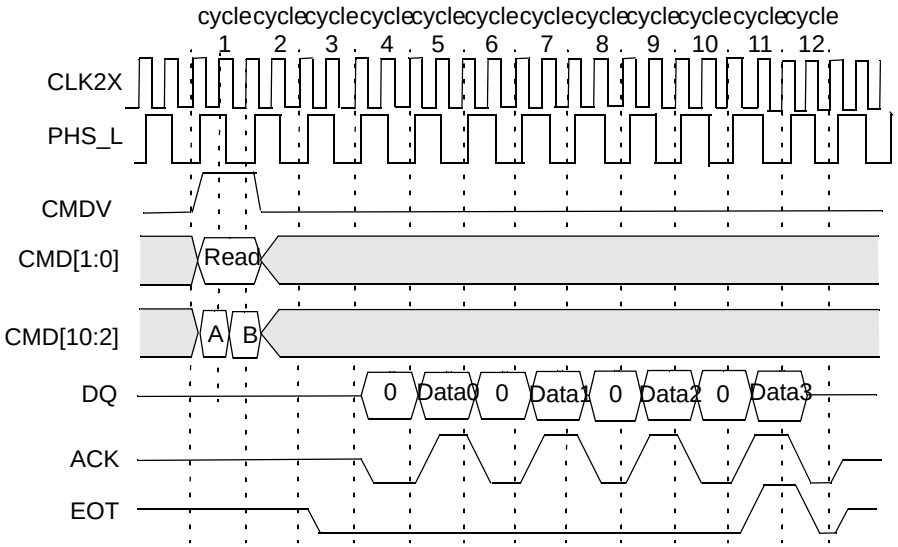



**Figure 6-2. Burst Read of the Data and Mask Arrays (BLEN = 4)**

Burst Read operation sequence:

- **Cycle 1**: The host ASIC applies the Read instruction on CMD[1:0] (CMD[2] = 1) using CMDV = 1, and the start address is provided in the RBURREG register. The host ASIC selects the Ayama 10000A device where ID[4:0] matches the DQ[25:21] lines. If DQ[25:21] = 11111, the host ASIC selects the Ayama 10000A device with the LDEV bit set.
- **Cycle 2**: The host ASIC floats DQ[71:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[71:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive the DQ[71:0] bus and drives ACK and EOT from Z to LOW.
- **Cycle 5**: The selected device drives the Read data from the address location on the DQ[71:0] bus and drives the ACK signal HIGH.

Cycles 4 and 5 repeat for each additional access until all the accesses specified in the BLEN field of RBURREG are complete. On the last data transfer, the Ayama 10000A drives the EOT signal HIGH.

**Cycle (4 + 2n)**: The selected device drives the DQ[71:0] to a three-state condition, and drives ACK and EOT signals LOW.

At the termination of cycle (4 + 2n), the selected device floats ACK and EOT to a three-state condition. The burst Read operation is complete and the next operation can begin.

### 6.3.3 Read Parity

Data output of the Read Parity command should be ignored. Read Parity is a blocking operation only on cycles equivalent to a regular Read operation, ignoring the fact that the parity status signal (PARERR) is valid TLSZ cycles later.

## 6.4 Write Command

The Write command can be issued to write to the data array, mask array, NSE-associated SRAMs or internal registers. The Write can be a single or burst Write (*Table 6-6*). Burst Write can only be issued for accesses to the data or mask array locations. SRAM Write operation is covered in *Section 6.7.4* to *Section 6.7.6*. The Write command is also used to issue the Parallel Write command. When a Write command is issued, a GMR needs to be specified. This GMR will be used to mask out bits written to the data or mask array. The upper 72-bit and lower 72-bit of the selected GMR MUST be the exact copy of each other.

**Note that when Parity feature is enabled masks will be ignored and all bits will be written as presented in the DQ bus.**

Write is a blocking operation and must be completed before the next operation can be issued.

**Table 6-6. Single/Burst Write Command Parameters**

| CMD Parameter CMD[2] | Write Command | Description |
|---|---|---|
| 0 | Single Write | Writes a single location of the data array, mask array, NSE-associated SRAM or internal registers. All access information is applied on the DQ bus. |
| 1 | Burst Write | Writes a block of locations to the data or mask array as a burst. WBURREG specifies the starting address and the length of the data transfer from the data or mask array; it also auto-increments the address for each access. All other access information is applied on the DQ bus. |

### *6.4.1 Single Write*

A single Write operation lasts 3 cycles (CLK1X) as illustrated in *Figure 6-3*.

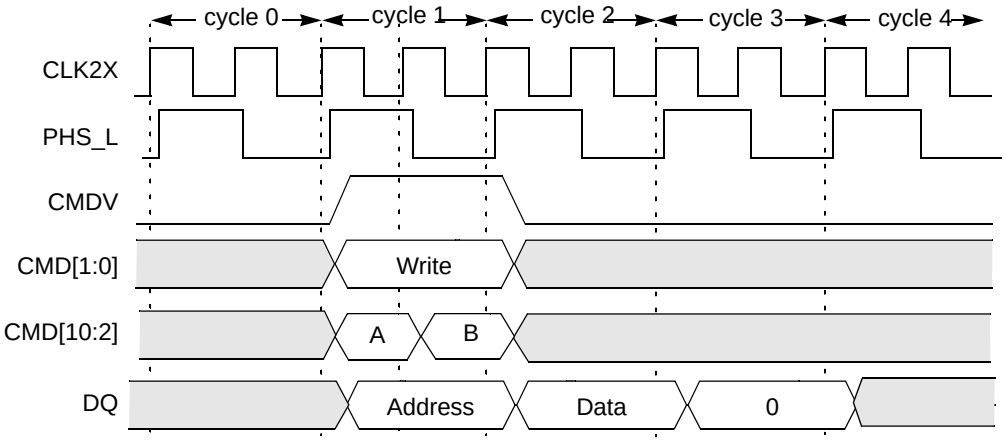



**Figure 6-3. Single Write Cycle Timing**

Write operation sequence:

- **Cycle 1A**: The host ASIC applies the Write instruction to CMD[1:0] (CMD[2] = 0) using CMDV = 1, and the target address supplied on the DQ bus. The host ASIC also supplies the GMR index to mask the Write to the data or mask array location on {CMD[10], CMD[5:3]}. For SRAM WRITEs, the host ASIC must supply the SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6]. The host ASIC sets CMD[9] to 0 for a normal Write.
- **Cycle 1B**:The host ASIC continues to apply the Write instruction to CMD[1:0] (CMD[2] = 0) using CMDV = 1, and the address supplied on the DQ bus. The host ASIC continues to supply the GMR index to mask the Write to the data or mask array locations in {CMD[10], CMD[5:3]}. The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.
- **Cycle 2**: The host ASIC drives DQ[71:0] with the data to be written to the data array, mask array, or register location of the selected device.
- **Cycle 3**: Idle cycle. DQ bus should be driven to 0.

At the termination of cycle 3, another operation can begin.

### *6.4.2 Burst Write*

The burst Write operation lasts 2 + n CLK1X cycles, where n is the number of the burst length as specified by the BLEN field of the WBURREG. The BLEN field is automatically decremented after each Write of the burst, so the register must be re-initialized before another burst Write is issued. Instead of the address provided by the user, the address in the INDEX field of the WBURREG is used and incremented each cycle.

*Figure 6-4* illustrates the timing diagram for the burst Write to the data or mask array.

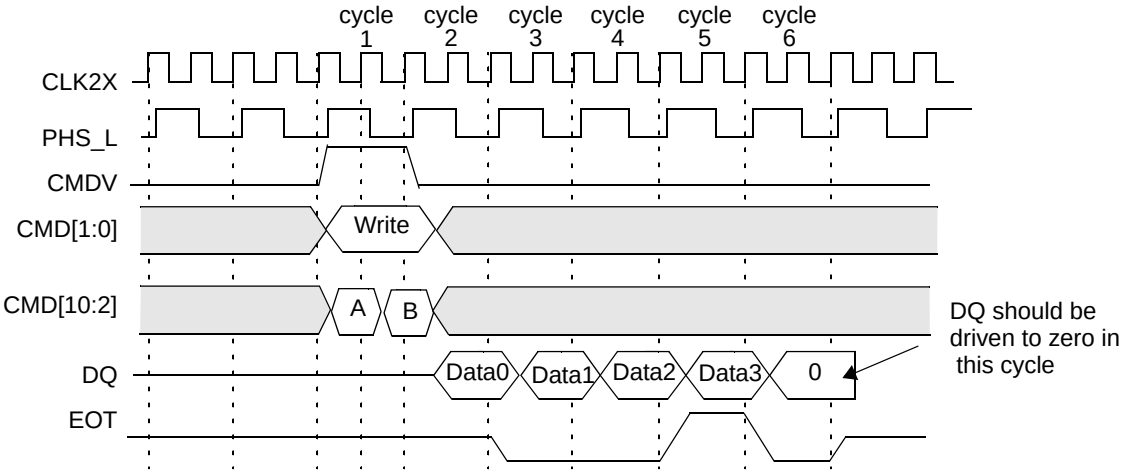



**Figure 6-4. Burst Write of the Data and Mask Arrays (BLEN = 4)**

Burst Write operation sequence:

- **Cycle 1A**: The host ASIC applies the Write instruction to CMD[1:0] (CMD[2] = 1) using CMDV = 1, and the start address is provided in the WBURREG register. The host ASIC also supplies the GMR index to mask the Write to the data or mask array locations in {CMD[10], CMD[5:3]}. The host ASIC sets CMD[9] to 0 for the normal Write.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] (CMD[2] = 1) using CMDV = 1, and the address supplied on the DQ bus. The host ASIC continues to supply the GMR index to mask the Write to the data or mask array locations in {CMD[10], CMD[5:3]}. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. It selects all devices when DQ[25:21] = 11111.
- **Cycle 2**: The host ASIC drives the DQ[71:0] with the data to be written to the data or mask array location of the selected device. The Ayama 10000A device writes the data from the DQ[71:0] bus only to the subfield with the corresponding mask bit set to 1 in the GMR that is specified by the index {CMD[10],CMD[5:3]} supplied in cycle 1.
- **Cycles 3 to n + 1**: The host ASIC drives the DQ[71:0] with the data to be written to the next data or mask array location of the selected device (addressed by the auto-increment ADR field of the WBURREG register).

The Ayama 10000A device writes the data on the DQ[71:0] bus only to the subfield that has the corresponding mask bit set to 1 in the GMR specified by the index supplied in cycle 1 {CMD[10],CMD[5:3]}. The Ayama 10000A device drives the EOT signal LOW from cycle 3 to cycle n; the Ayama 10000A device drives the EOT signal HIGH in cycle n + 1 (n is specified in the BLEN field of the WBURREG).

- **Cycle n + 2:** The Ayama 10000A device drives the EOT signal LOW.

At the termination of cycle n + 2, the Ayama 10000A device floats the EOT signal to a three-state operation and the next instruction can be issued.

### *6.4.3 Parallel Write*

In order to write the Data or Mask array faster for initialization, testing, or diagnostics, the user can issue a Parallel Write command. Parallel Write allows the user to specify one address and write multiple locations in the Core with the same data. Parallel Write only works with Direct addressing. If Indirect addressing is used, the operation will result in No-Operation. Parallel Write can also be done in burst operation.

In Non-Enhanced Mode, address bits DQ[10:1] specify which location to perform parallel write. DQ[17:11] defines a set of partitions, all of which write two x72 entries (DQ[0] is ignored). For Ayama 10512, this corresponds to 64 parallel locations (32 8Kx72 partitions, two locations per partition).

In Enhanced Mode, address bits DQ[10:0] specify the location within a block. Parallel write only occurs on those blocks which match the Mini-Key(s) selected by the GMR field. For Ayama 10512, this corresponds to 128 parallel locations (128 blocks, 1 location per block).

## 6.5 Search Command

One of the key parameters that controls SEARCH operation is TLSZ (Statically programmed in Command Register). TLSZ controls the maximum number of devices that can be cascaded and the latency of SEARCH instruction, as shown in *Table 6-7*.

**Table 6-7. TLSZ[1:0] Description**

| TLSZ[1:0] | Max. # Devices in Cascade | Max frequency (CLK1X Cycles | Search Latency (CLK1X Cycles) | Max. Table Size (with max. number of devices |
|---|---|---|---|---|
| 00 | 1 | 83 MHz | 4 | N x 72<br>N/2 x 144<br>N/4 x 288<br>N/8 x 576<br>N = 256k for CYNSE10512A, 128k for CYNSE10256A, 64k for CYNSE10128A |
| 01 | 8 | 100 MHz | 5 | N x 72<br>N/2 x 144<br>N/4 x 288<br>N/8 x 576<br>N = 2048k for CYNSE10512A, 1024k for CYNSE10256A, 512k for CYNSE10128A |
| 10 | 31 (in single-search mode, 8 in multisearch mode) | 133 MHz | 6 | N x 72<br>N/2 x 144<br>N/4 x 288<br>N/8 x 576<br>N = 7936k for CYNSE10512A, 3968k for CYNSE10256A, 1984k for CYNSE10128A |
| 11 | Reserved | Reserved | Reserved | Reserved |

The following is a list of SEARCH operations described in the data sheet:

- Mixed-size Single Search for a single device on tables configured with different widths (TLSZ[1:0] = 10)
- Mixed-size MultiSearch for a single device on tables configured with different widths (TLSZ[1:0] = 10)
- 72-bit Single Search for single device or cascade up to eight devices (TLSZ[1:0] = 01)
- 144-bit Single Search for cascade up to 31 devices (TLSZ[1:0] = 10)
- 576-bit Single Search for single device or cascade up to eight devices (TLSZ[1:0] = 01)
- Mixed-size Single Search for cascade up to 31 devices on tables configured with different widths (TLSZ[1:0] = 10)
- Mixed-size MultiSearch for cascade up to eight devices on tables configured with different widths (TLSZ[1:0] = 01).

### DQ bus format and Addressing during Search Operations

The Ayama10000 family of search engine is addressable on x72-bit word boundaries. For tables that are 72-bit wide, every entry gets written into an addressable entry. For tables that are x144, x288 or x576 per entry, it is up to the user to organize the NSE using the Big-Endian approach or Little-Endian approach. The decision of using a x72 Big-Endian organization or a x72 Little-Endian approach will affect the way to send in search keys during a search operation. Since the Ayama10000 has a x72 bit DQ interface, search keys that are longer then 72-bits will require multiple bus cycles to get transferred into the NSE. For tables that are organized with the x72 Big-Endian approach, make sure the search key also appears as x72 Big-Endian on the DQ bus (i.e., First transfer cycle contains the most significant 72 bits). Likewise for a Little-Endian organization, Search key on the DQ bus must appear as Little-Endian (i.e., First transfer cycle contains the least significant 72 bits). Here is another way to represent the relationship between the data presented on the different clock cycles during a search command and the entry in the NSE that it will get compared to:

During a x144, x288 or x576 single search:

- Data presented on DQ bus during the 1st CLK2X cycle will be compared to the lowest 72-bit word of the NSE entry
- Data presented on DQ bus during the 2nd CLK2X cycle will be compared to the 2nd lowest 72-bit word of the NSE entry
- Data presented on DQ bus during the nth CLK2X cycle will be compared to the nth lowest 72-bit word of the NSE entry

See *Figure 6-5* for graphical explanation of a 288-bit search example.

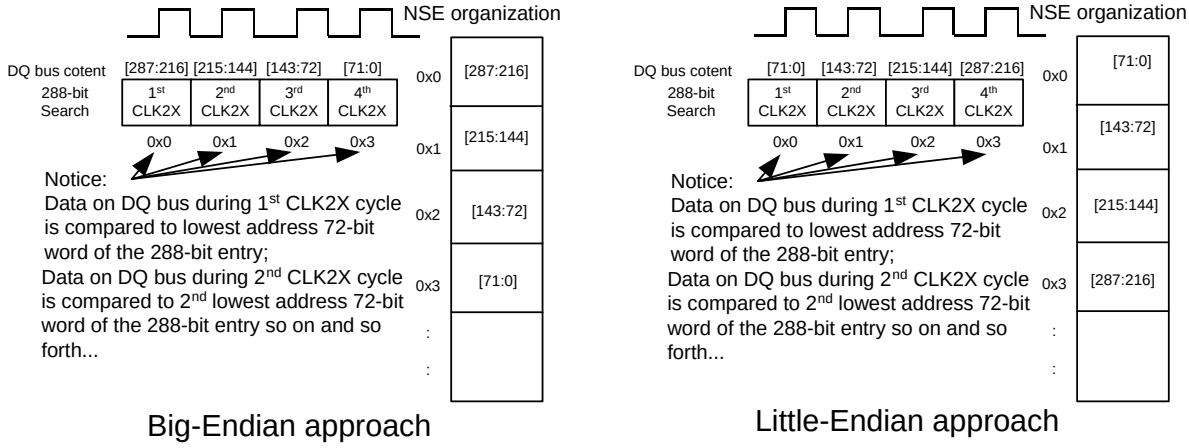


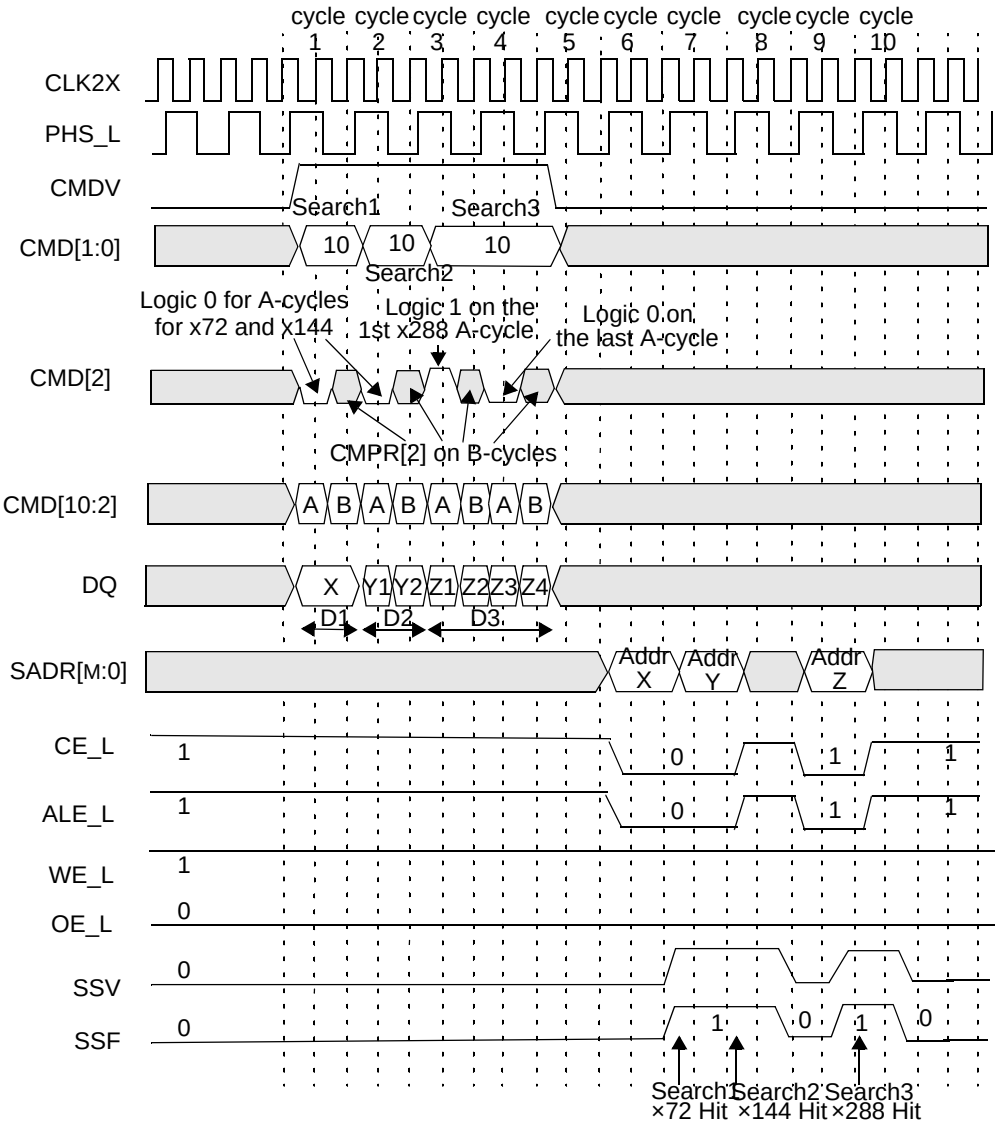

**Figure 6-5. Search Key format on DQ bus for a 288-bit search**

### *6.5.1 Mixed-size Single Searches with One Device on Tables Configured with Different Widths*

This subsection covers single-searches with a single device configured with tables of different widths (×72, ×144, ×288). *Figure 6-6* shows three sequential searches: first, a 72-bit Search on a ×72-configured table; a 144-bit Search on a ×144-configured table; and a 288-bit Search on a ×288-configured table that each results in a hit. *Figure 6-7* shows the sample table.

**Note**: If the mixed-size tables include a 576-bit table, then the device can only operate in the Enhanced Mode, as the maximum table width allowed in the Non-Enhanced Mode is 288 bits.

One way to create multiple tables of different widths in an NSE is by having table designation bits. It is assumed that bits [71:70] for each entry will be assigned such table designation bits. DQ[71:70] will be 00 in each of the two A and B cycles of the ×72-bit Search (Search1). DQ[71:70] is 01 in each of the A and B cycles of the ×144-bit Search (Search2). DQ[71:70] is 10 in each of the A, B, C, and D cycles of the ×288-bit Search (Search3).




HLAT = 001 (binary), TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary).
M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-6. Timing Diagram for Mixed Single Search (One Device)**

The following is the sequence of operation for a single Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = 10. The CMD[2] and CMD[9] signals must be driven to logic 0 for the 72-bit search, but for 144-bit search, CMD[9] = 1 and CMD [2] = 0. For 288-bit search, CMD[9] is don't care, whereas CMD[2] = 1 for the first "A" cycle and 0 for the last "A" cycle. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A if it has a hit. If Enhanced Mode and MultiSearch Enable bits are both set to 1in the Command Resister, CMD[8] has to be set to 0 for Single Searches. For 288-bit and 576-bit Single Searches, all Cycle A CMD[8] bits have to be set to 0's.
  - **DQ Bus**: At the same time in cycle A, DQ[71:0] must be driven with the 72-bit data to be compared.

- **Cycle B**:
  - **Command Bus**: The host ASIC continues to drive CMDV HIGH and to apply Search command CMD[1:0] = 10. CMD[5:2] must now be driven by the index of the comparand register pair for storing the search key presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 27 for a description of SSR[0:7]). CMD[10:9] are don't cares for this cycle.
  - **DQ Bus**: The DQ[71:0] continues to carry the search key to be compared.

**Note**. For 72-bit searches, the host ASIC must supply the same 72-bit data on DQ[71:0] during both cycles A and B. Also, the even and odd pairs of GMRs selected for the comparison must be programmed with the same value. For 144-bit, 288-bit or 576-bit searches, each 72-bit presented on each cycle A and B will together form the 144-bit or 288-bit or 576-bit search key respectively.

When an N-bit search key, K, is presented on the DQ bus, the entire table of N-bit entries is compared to the search key using the GMR and local mask bits. The GMR is selected by the GMR Index in the command's cycle A. K is also stored in both even and odd comparand register pairs (selected by the comparand register index in command cycle B). K is compared with each entry in the table, starting at location 0. A matching entry that satisfies the Soft Priority and Mini-Key scheme (for Enhanced Mode) will be the winning entry, and its location address L will be driven as part of the SRAM address on the SADR[N:0] lines (see Section 6.7, "SRAM PIO Access," on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A.

The latency of the Search from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ[1:0] = 01). SSV and SSF also shift further to the right for different values of HLAT, as specified in *Table 6-8*.

*Figure 6-7* shows an example of multiple table configuration with a CYNSE10512A device.

**Table 6-8. Shift of SSF and SSV from SADR**

| HLAT (binary) | Number of CLK Cycles | HLAT | Number of CLK Cycles |
|---|---|---|---|
| 000 | 0 | 100 | 4 |
| 001 | 1 | 101 | 5 |
| 010 | 2 | 110 | 6 |
| 011 | 3 | 111 | 7 |

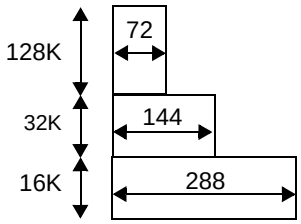



**Figure 6-7. Multiwidth Configurations Using CYNSE10512A as an Example**

Referring to *Figure 6-7*, if the CYNSE10512A device is used in the Non-Enhanced Mode, the CFG field in the Configuration Register should be configured to "AAAA555500000000" (hex) in order to have three individual tables within a device. If the device is used in the Enhanced Mode, the NES field in the Block Mini-Key Register (BMR) should be configured as follows:

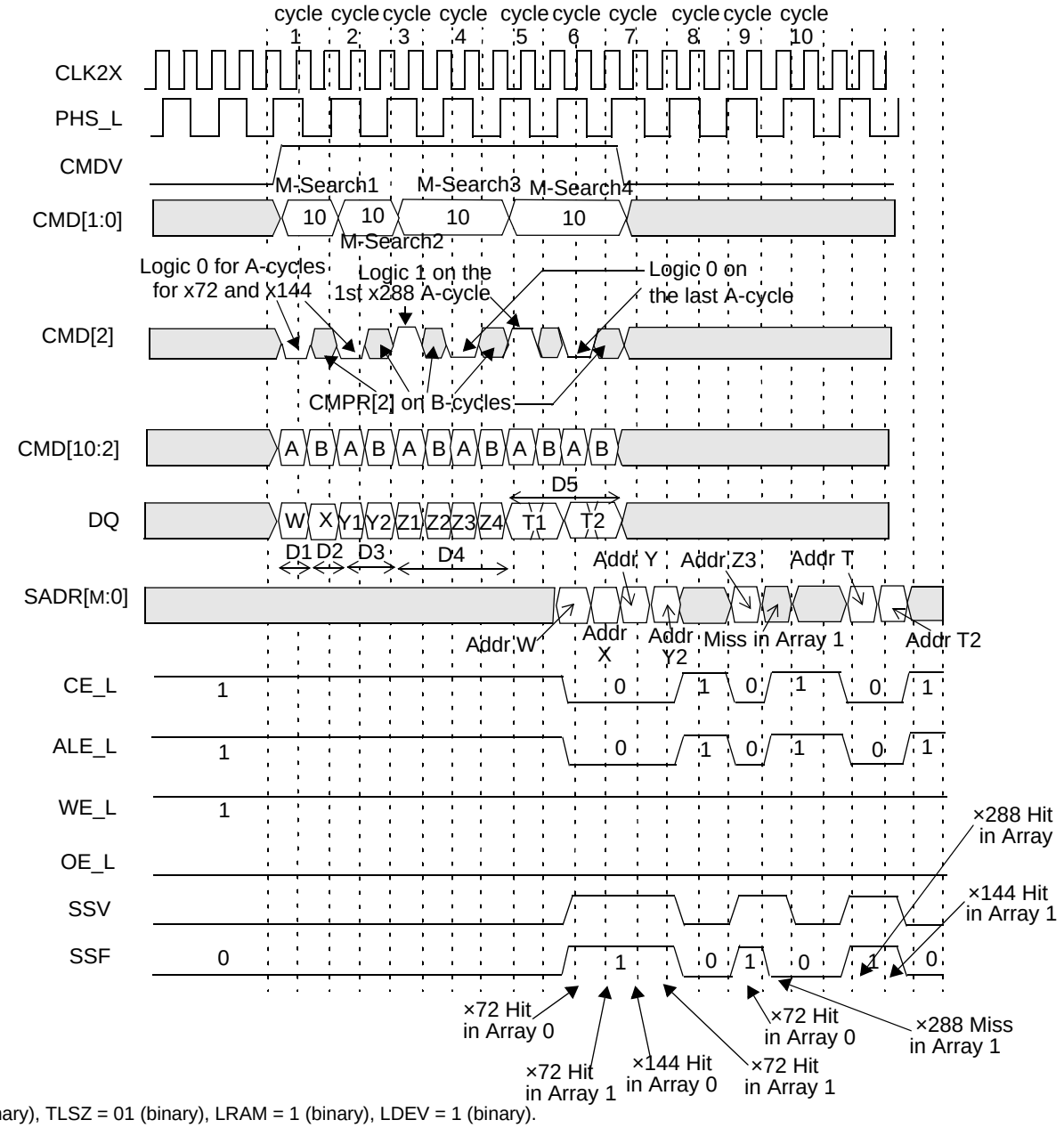
- For the first 64 blocks in the data array, NES = 00 for 72-bit table width.
- For the next 32 blocks, NES = 01 for 144-bit table width.
- For the final 32 blocks, NES = 10 for 288-bit table width.

### *6.5.2 Mixed-size Multi Searches with One Device on Tables Configured with Different Widths*

The multiple search operates the search commands in parallel on the upper half (array 0) and lower half (array 1) of the data array in the device. The results from the two parallel searches are then driven on the SRAM bus at twice that rate relative to single-search. This subsection covers multi searches with a single device configured with tables of different widths (×72, ×144, ×288) in each of the two arrays. *Figure 6-8* shows four sequential searches:

1. A 72-bit - 72bit MultiSearch
2. A 144-bit -72-bit MultiSearch
3. A 288-bit - 72-bit MultiSearch (leading search in array 1)
4. A 288-bit -144bit MultiSearch.

**Note**: MultiSearch is only available in the Enhanced Mode, not in the Non-Enhanced Mode. *Figure 6-9* shows the sample table.




HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary).
M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-8. Timing Diagram for Mixed MultiSearch (One Device)**

The MSE bit in the Command Register must be set high to enable the MultiSearch feature. The same with the Enhanced Mode (EMODE) bit. TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary) for a single-device configuration. HLAT = 000 (binary) for this example. The following is the sequence of operation for a single Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = "10". The CMD[2] and CMD[9] signals must be driven to logic 0 for the 72-bit search, but for 144-bit search, CMD[9] = 1 and CMD [2] = 0. For 288-bit and 576-bit searches, CMD[9] is don't care, whereas CMD[2] = 1 for the first "A" cycle and 0 for the last "A" cycle. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. CMD[7:6] signals must be driven with the same bits that will be driven on SADR[24:23] for CYNSE10512A, SADR[23:22] for CYNSE10256A, SADR[22:21] for CYNSE10128A by this device if it has a hit. CMD[8] must be driven high on all Cycle A's in a command for MultiSearch operation. Note, CMD[8] must be driven low for all Cycle A's of Single Search operations if Enhanced mode and MultiSearch Enabled bits are set to 1 in the Command Register.

— **DQ Bus**: At the same time in cycle A, DQ[71:0] must be driven with the 72-bit data to be compared.

- **Cycle B**:
  — **Command Bus**: The host ASIC continues to drive CMDV HIGH and to apply Search command CMD[1:0] = “10”. CMD[5:2] must now be driven by the index of the comparand register pair for storing the search key presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 27 for a description of SSR[0:7]). CMD[10:9] are don’t cares for this cycle.
  — **DQ Bus**: The DQ[71:0] continues to carry the search key to be compared.

**Notes**.

1. For 72-bit leading + 72-bit trailing MultiSearches, the host ASIC can supply different 72-bit data on DQ[71:0] during both cycles A and B to be compared with the tables in array 0 and 1 of the data array. The even and odd pairs of GMRs selected for the comparison need not be programmed with the same value.
2. For all other Multisearch commands that contain a 72-bit trailing search, you must pay special attention to which part of the entire search key is used for the 72-bit trailing search. An example of this situation is illustrated in M-search 2 and M-search 3 in *Figure 6-7*. M-search 2 is a 144-bit leading search on Array 0 plus a 72-bit trailing search on Array 1. Notice that the Y2 portion of the entire key is used during the 72-bit search. Different behavior is observed for a leading search in Array 1 instead of Array 0. M-search 3 is a 288-bit leading search on Array 1 plus a 72-bit trailing search on Array 0. In this example, Z3 is used as the 72-bit key for the trailing 72-bit search. The difference between M-search 2 and M-search 3 is the trailing 72-bit search (Array 0 and Array 1 respectively). This behavior is summarized as follows:
   - 72-bit trailing search on Array 0: Data on DQ during the last Cycle A of the entire Search command will be used as search key
   - 72-bit trailing search on Array 1: Data on DQ during the last Cycle B of the entire Search command will be used as search key
3. For all other Multisearches, the N-bit search key used for the N-bit trailing search is simply the last N-bits presented on the DQ bus when the Multisearch command is issued.
4. GMR and CPR selection also deserve special attention, please see *Section 5.1.2.4* for details.
5. A matching entry from each array that satisfies the Soft Priority and Mini-Key scheme will be the winning entries, and their location addresses La and Lb, will be driven as part of the SRAM address on the SADR[N:0] lines (see Section 6.7, “SRAM PIO Access,” on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A.
6. Reading CMPR registers after Multisearches: You can only do this if your leading and trailing searches are of same width.
7. Learning from CMPR is only supported if your leading and trailing searches are of same width.

The latency of the Search from command to SRAM access cycle is 5 for a single device (or up to eight devices) configuration in the table (TLSZ[1:0] = 01). SSV and SSF also shift further to the right for different values of HLAT, as specified in *Table 6-8*.

*Figure 6-9* shows a multiwidth configuration when multisearch is enabled using CYNSE10512A as an example.

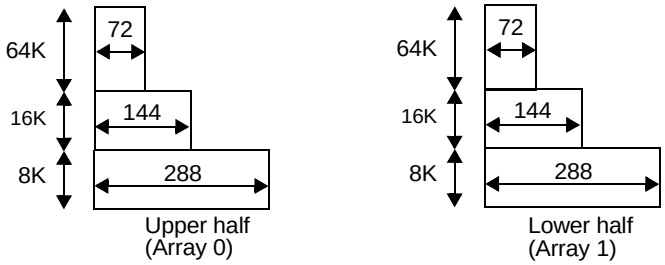



**Figure 6-9. Multiwidth Configurations Using CYNSE10512A as an Example**

The NES field in the Block Mini-Key Register (BMR) should be configured as follows:

- For the first 32 blocks in the data array, NES = 00 (binary) for 72-bit table width. For the next 16 blocks, NES = 01 (binary) for 144-bit table width. For the following 16 blocks, NES = 10 (binary) for 288-bit table width. These will configure the tables in array 0.
- Setting NES = 00 (binary) for the next 32 blocks will configure those blocks to be 72-bit table in array 1. Setting NES = 01 (binary) for the next 16 blocks will configure those blocks to be 144-bit table. Setting the final 16 blocks’ NES field will configure those blocks to be 288-bit table.

### *6.5.3 72-bit Single Search for 1 device or cascade up to eight devices*

The hardware diagram of the Search subsystem of up to eight devices is shown in *Figure 6-10*. The MultiSearch Mode (MSE) bit in the Command Register must be set LOW to perform single-search. The following are the rest of the parameters programmed into the eight devices.

- In Non-Enhanced Mode, first seven devices (devices 0–6) must reset all bits of the CFG field in Configuration register to zeroes. In Enhanced Mode, these devices should have the NES field of each block within a device configured to 00 for 72-bit table width. TLSZ = 01 (binary), HLAT = 010 (binary), LRAM = 0 (binary), and LDEV = 0 (binary) for both modes.

- In Non-Enhanced Mode, the eighth device (device 7) should still reset all bits of the CFG field in Configuration register to zeroes. In Enhanced Mode, NES should still be 00 (binary). But TLSZ = 01 (binary), HLAT = 010 (binary), LRAM = 1 (binary), and LDEV = 1 (binary) for the last device.

**Note**: The device receiving all the LHO signals from the other devices is the last device.

For a single-device configuration, the parameters are the same as device 7. BHI[2:0] and LHI[6:0] should be tied to ground.

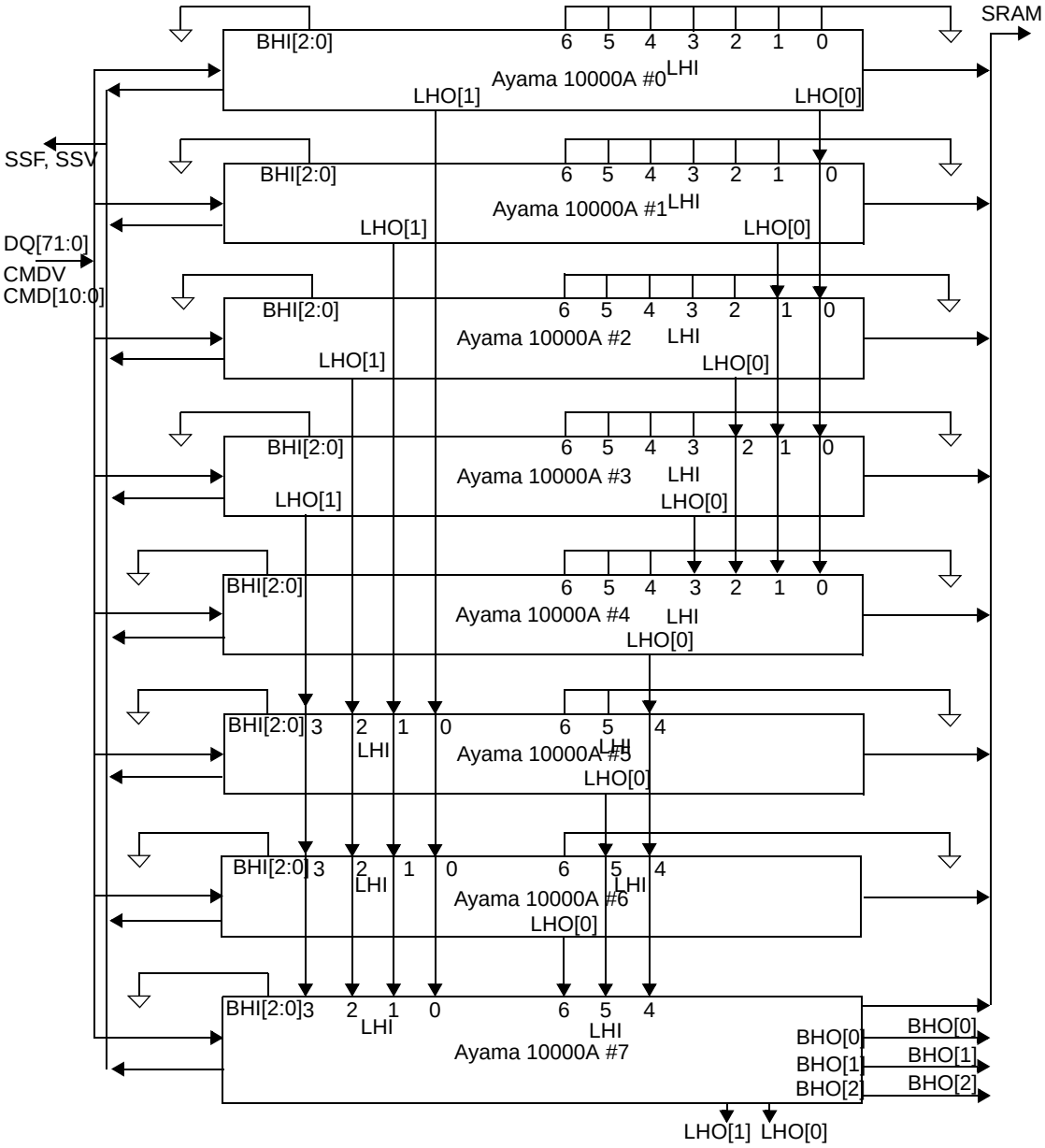


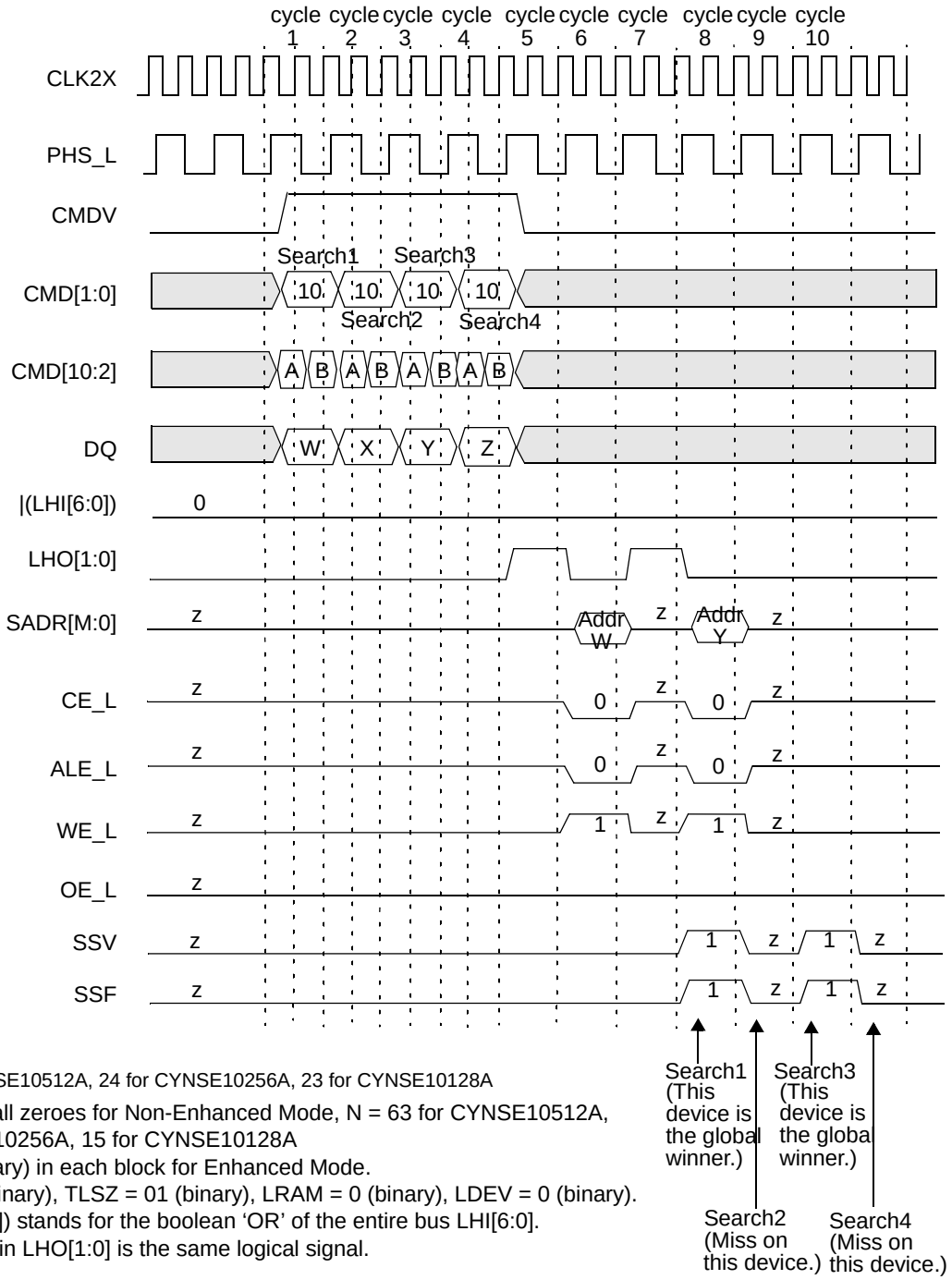

**Figure 6-10. Hardware Diagram for a Table with Eight Devices**

The following three figures show the response of three of the eight devices having a hit at different time according to a Hit/Miss assumption shown below in *Table 6-9*. For these timing diagrams, four 72-bit searches are performed sequentially. *Figure 6-11* shows the timing diagram for a Search command in the 72-bit-configured table of eight devices for device number 0. *Figure 6-12* and *Figure 6-13* shows the same for device number 1 and number 7 (the last device in this specific table) respectively.

**Note**: All the shared signals showing tri-stated condition (“z”) indicate that, that particular device is not driving the shared signals. The shared signals are not three-stated in a real life because other devices will be driving them.

**Table 6-9. Hit/Miss Assumptions**

| Search Number | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Device 0 | Hit | Miss | Hit | Miss |
| Device 1 | Miss | Hit | Hit | Miss |
| Devices 2–6 | Miss | Miss | Miss | Miss |
| Device 7 | Miss | Miss | Hit | Hit |




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

CFG[N:0] are all zeroes for Non-Enhanced Mode, N = 63 for CYNSE10512A, 31 for CYNSE10256A, 15 for CYNSE10128A

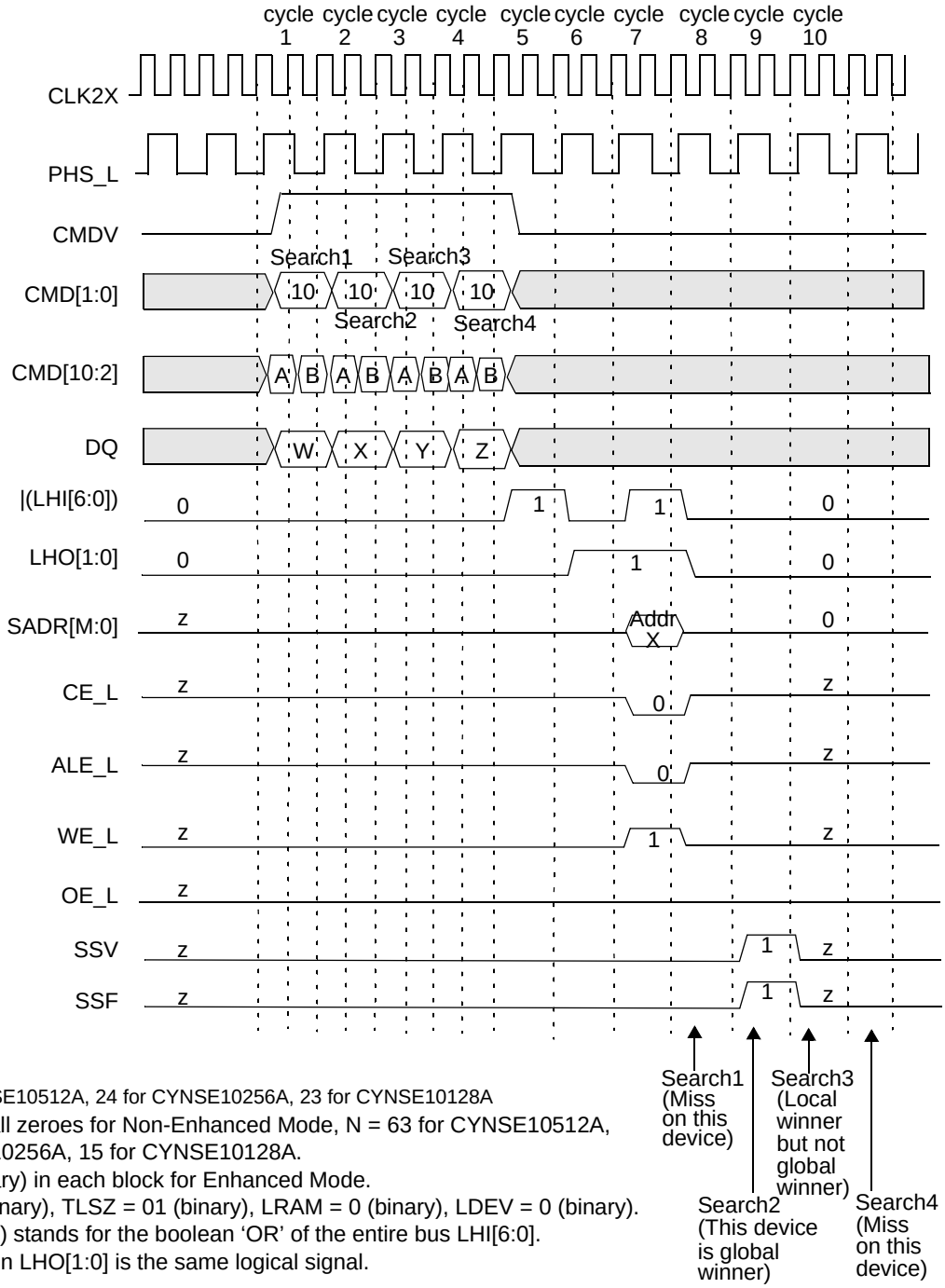
NES = 00 (binary) in each block for Enhanced Mode.

HLAT = 010 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].

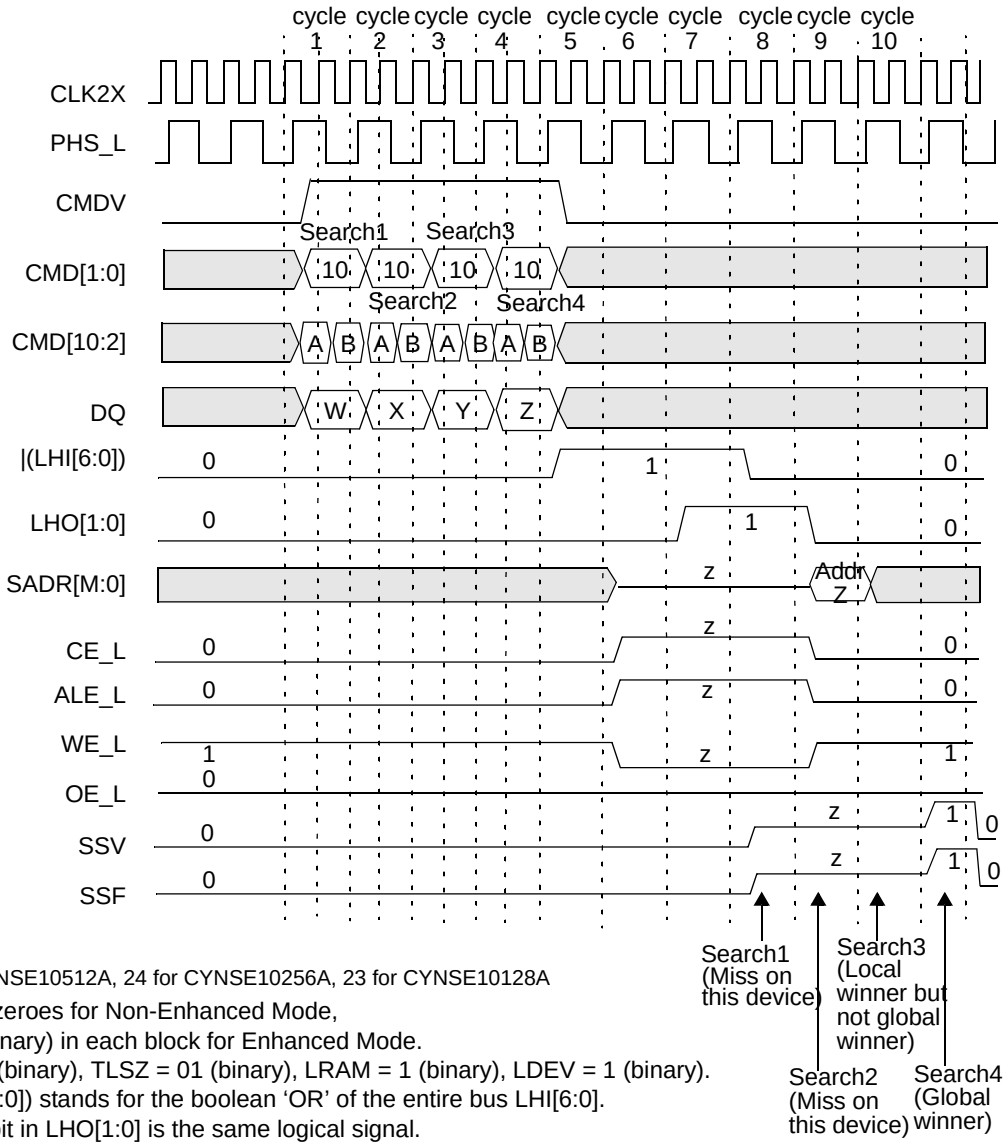
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-11. Timing Diagram for 72-bit Search Device Number 0**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
CFG[N:0] are all zeroes for Non-Enhanced Mode, N = 63 for CYNSE10512A, 31 for CYNSE10256A, 15 for CYNSE10128A.
NES = 00 (binary) in each block for Enhanced Mode.
HLAT = 010 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-12. Timing Diagram for 72-bit Search Device Number 1**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
CFG are all zeroes for Non-Enhanced Mode,
NES = 00 (binary) in each block for Enhanced Mode.
HLAT = 010 (binary), TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary).
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-13. Timing Diagram for 72-bit Search Device Number 7 (Last Device)**

The following is the sequence of operation for a single 72-bit Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = "10". The CMD[2] and CMD[9] signals must be driven to logic 0 for this 72-bit search. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A by this device if it has a hit. If Enhanced Mode and MultiSearch Enable bits are both set to 1in the Command Resister, CMD[8] has to be set to 0 for Single Searches. For 288-bit and 576-bit Single Searches, all Cycle A CMD[8] bits have to be set to 0's.
  - **DQ Bus**: At the same time in cycle A, DQ[71:0] must be driven with the 72-bit data to be compared.
- **Cycle B**:
  - **Command Bus**: The host ASIC continues to drive CMDV HIGH and to apply Search command CMD[1:0] = "10". CMD[5:2] must now be driven by the index of the comparand register pair for storing the two 72-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 27 for a description of SSR[0:7]). CMD[10:9] are don't cares for this cycle.
  - **DQ Bus**: The DQ[71:0] continues to carry the 72-bit data to be compared.

**Note**. For 72-bit searches, the host ASIC must supply the same 72-bit data on DQ[71:0] during both cycles A and B. Also, the even and odd pairs of GMRs selected for the comparison must be programmed with the same value.

The logical 72-bit Search operation is shown in *Figure 6-14*. The entire table of 72-bit entries (eight devices) is compared to a 72-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and local mask bits. The effective GMR is the 72-bit word specified by the identical value in both even and odd GMR pairs, in each of the eight devices, and selected by the GMR Index in the command's cycle A. The 72-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs (selected by the comparand register index in command cycle B) in each of the eight devices. In the ×72 configuration, only the even comparand register can subsequently be used by the Learn command in one of the devices (the first non-full device only). The word K (presented on the DQ bus in both cycles A and B of the command) is compared with each entry in the table, starting at location 0. A matching entry that satisfies the Soft Priority and Mini-Key scheme (for Enhanced Mode) will be the winning entry, and its location address L will be driven as part of the SRAM address on the SADR[N:0] lines (see Section 6.7, "SRAM PIO Access," on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A. The global winning device will drive the bus in a specific cycle. On a global miss cycle, the device with LRAM = 1 (default driving device for the SRAM bus) and LDEV = 1 (default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 72-bit searches in ×72-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 72-bit Search command cycle (two CLK2X cycles) is shown in *Table 6-7*.

The latency of the Search from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ = 01). SSV and SSF also shift further to the right for different values of HLAT, as specified in *Table 6-8*.

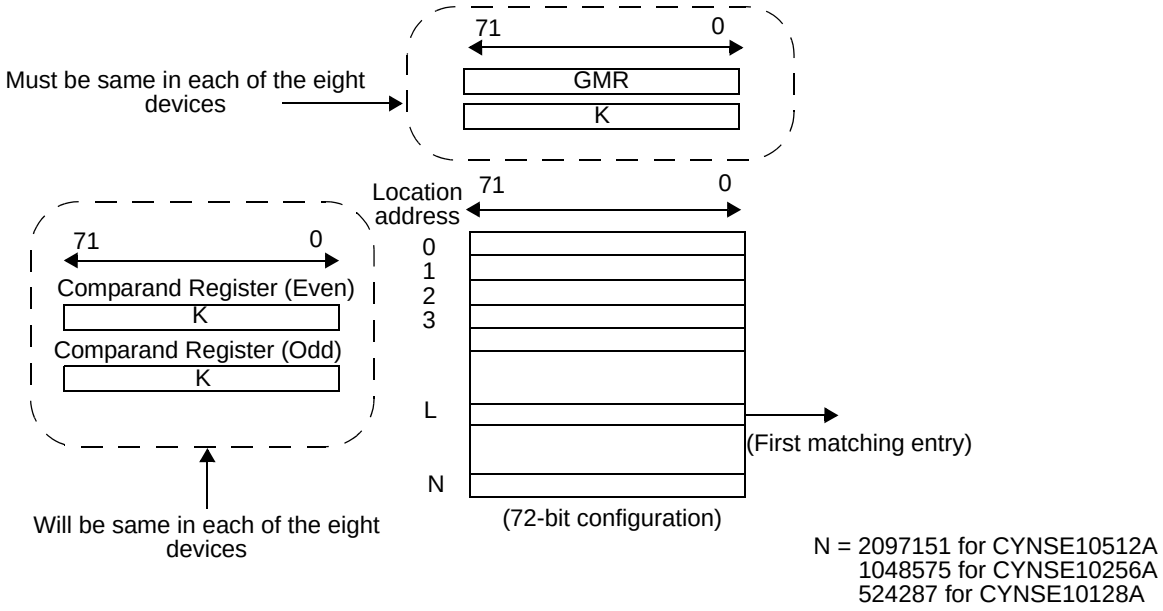



**Figure 6-14. ×72 Table with Eight Devices**

### 6.5.4 144-bit Single Search for Cascade Up to 31 Devices

The hardware diagram of the Search subsystem of 31 devices is shown in *Figure 6-15*. Each of the four blocks in the diagram represents eight Ayama 10000A devices (except the last, which has seven devices). The diagram for a block of eight devices is very similar to the hardware diagram in *Figure 6-10*, except that the BHI[2:0] signals are connected to BHO of the previous block (rather than being grounded) as shown in *Figure 6-10*. The following are the parameters programmed into the 31 devices:

- First thirty devices (devices 0–29): TLSZ = 10 (binary), HLAT = 001 (binary), LRAM = 0 (binary), and LDEV = 0 (binary).
- Thirty-first device (device 30): TLSZ = 10 (binary), HLAT = 001 (binary), LRAM = 1 (binary), and LDEV = 1 (binary).
- For Non-Enhanced Mode, CFG[63:0] = 5555555555555555 (hex) for all devices for CYNSE10512A. CFG[31:0] = 55555555 (hex) for all devices for CYNSE10256A, and CFG[15:0] = 5555 (hex) for all devices for CYNSE10128A. For Enhanced Mode, NES in each block for all devices should be set to “01” to create 144-bit table.
- The device receiving all the LHO signals from the other devices is considered the last device.
- All the shared signals showing tri-stated condition (“z”) indicate that, that particular device is not driving the shared signals. The shared signals are not three-stated in a real life because other devices will be driving them.
- Comparing the hardware diagrams shown in *Figure 6-10* and *Figure 6-43*, enabling MultiSearch does not mean that a board layout change is required. The LHO_1_L and LHI_1_L share the same pin with the Full In and Full Out signals, which are not shown in *Figure 6-10*. Cascading multiple devices together still allow the user to configure the devices through software to perform single-search or MultiSearch operations without any board change.

The timing diagrams referred to in this paragraph reference the Hit/Miss assumptions defined in *Table 6-10*. For the purpose of illustrating the timings, it is further assumed that there is only one device with a matching entry in each of the blocks. *Figure 6-16* shows the timing diagram for a Search command in the 144-bit-configured table of 31 devices for each of the eight devices in block number 0. *Figure 6-17* shows the same for the all the devices in block number 1 (above the winning device in that block). *Figure 6-18* shows the timing diagram for the globally winning device (defined as the final winner within its own and all blocks) in block number 1. *Figure 6-19* shows the timing diagram for all the devices below the globally winning device in block number 1. *Figure 6-20*, *Figure 6-21*, and *Figure 6-22* show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device, respectively, for block number 2. *Figure 6-23*, *Figure 6-24*, *Figure 6-25*, and *Figure 6-26* show the timing diagrams of the devices above globally winning device, the globally winning device, and the devices below the globally winning device except the last device (device 30), respectively, for block number 3.

The 144-bit Search operation is pipelined and executes as follows:

- Four cycles from the Search command, each of the devices knows the outcome internal to it for that operation.
- On the fifth cycle, the devices arbitrate for a winner within a block (a “block” is defined as less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism).
- On the sixth cycle after the Search command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for a Search operation.

**Table 6-10. Hit/Miss Assumptions**

| Search Number | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Block 0 | Miss | Miss | Miss | Miss |
| Block 1 | Miss | Miss | Hit | Miss |
| Block 2 | Miss | Hit | Hit | Miss |
| Block 3 | Hit | Hit | Miss | Miss |

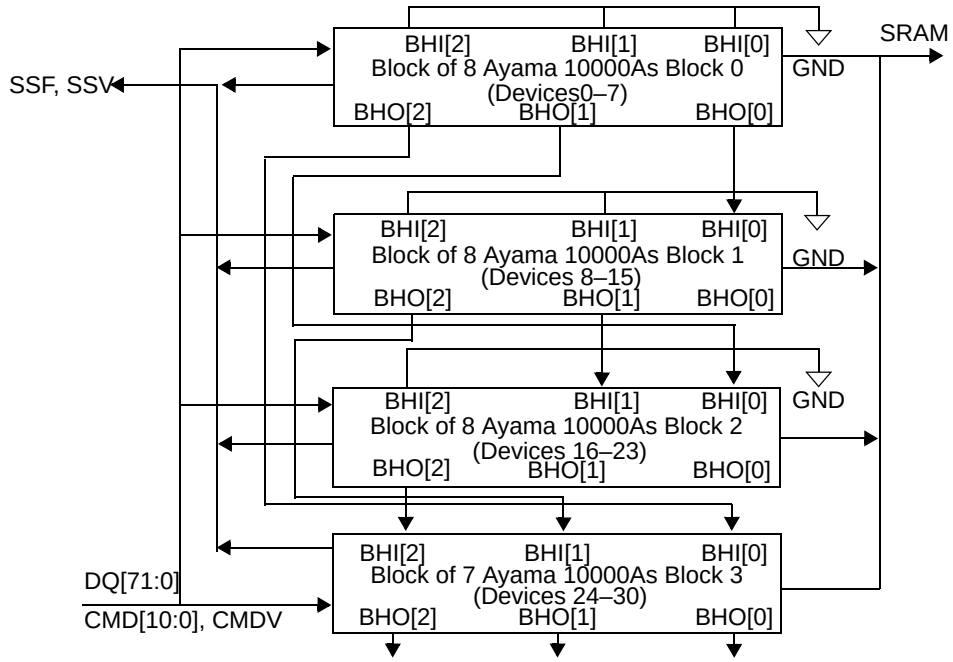
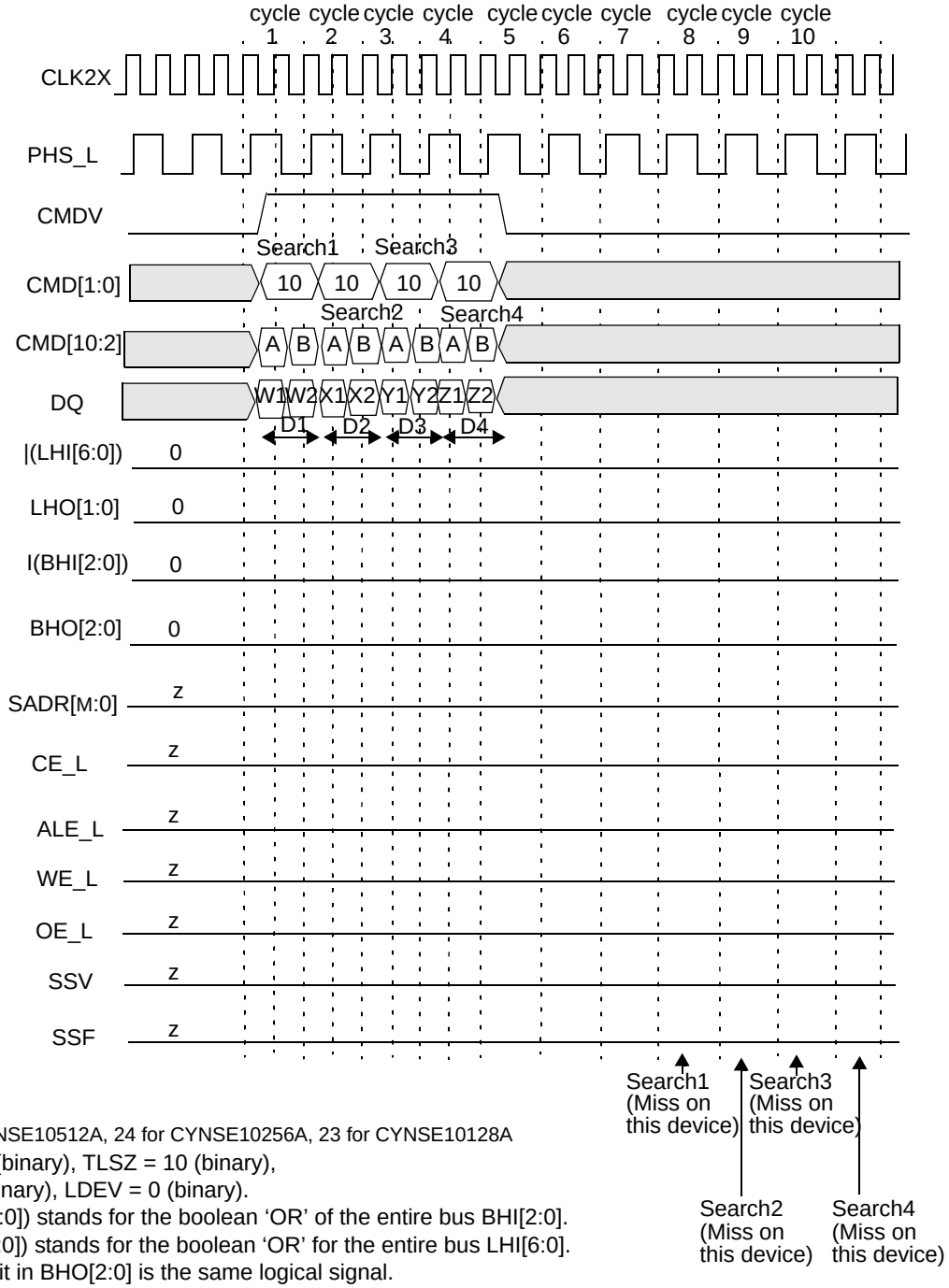
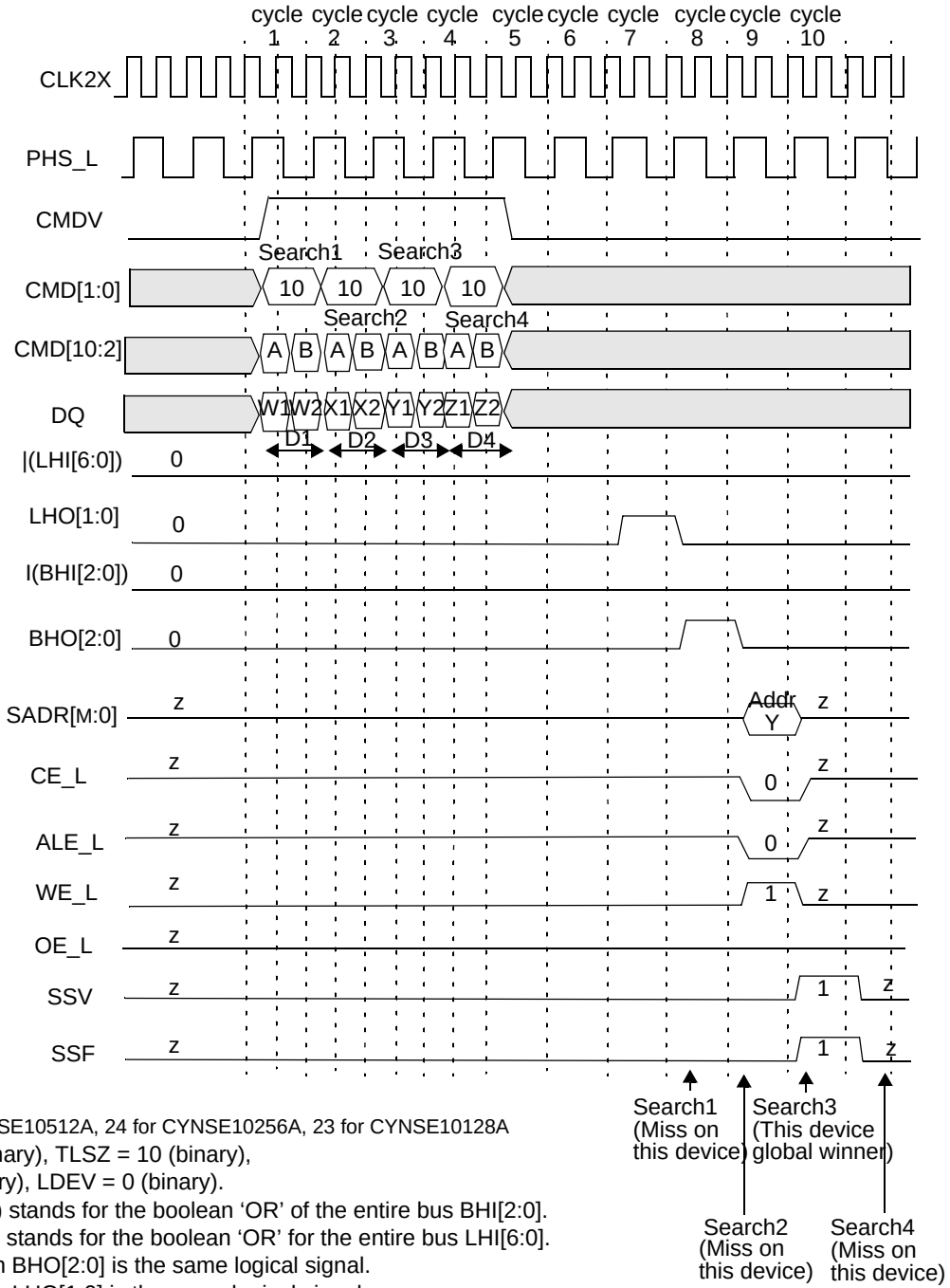



**Figure 6-15. Hardware Diagram for a Table with 31 Devices**



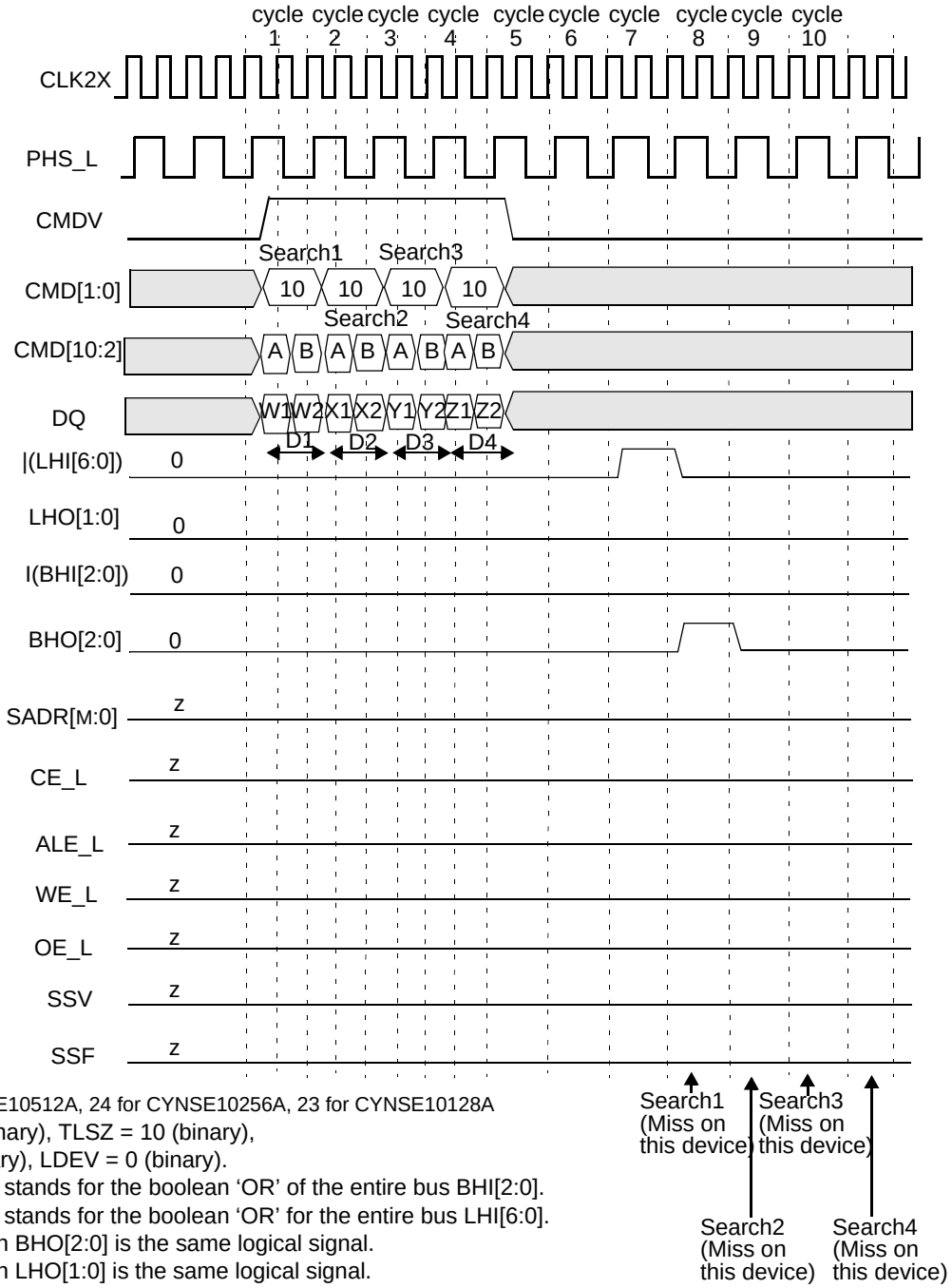

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-16. 144-bit Search for Devices in Block #0 and Above Block #1 Winning Device**



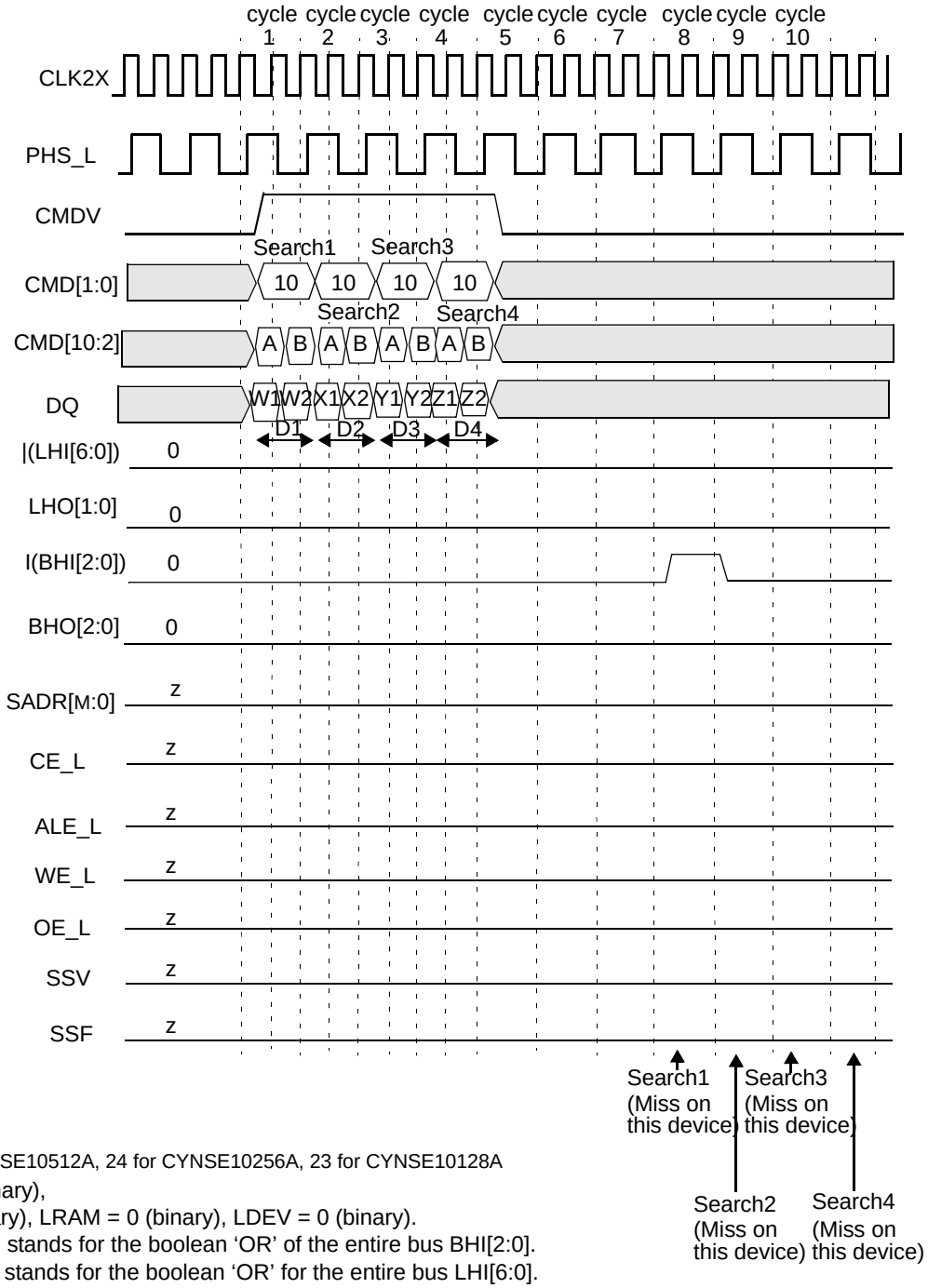

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-17. 144-bit Search Timing Diagram for Block #1 Global Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI(6:0) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

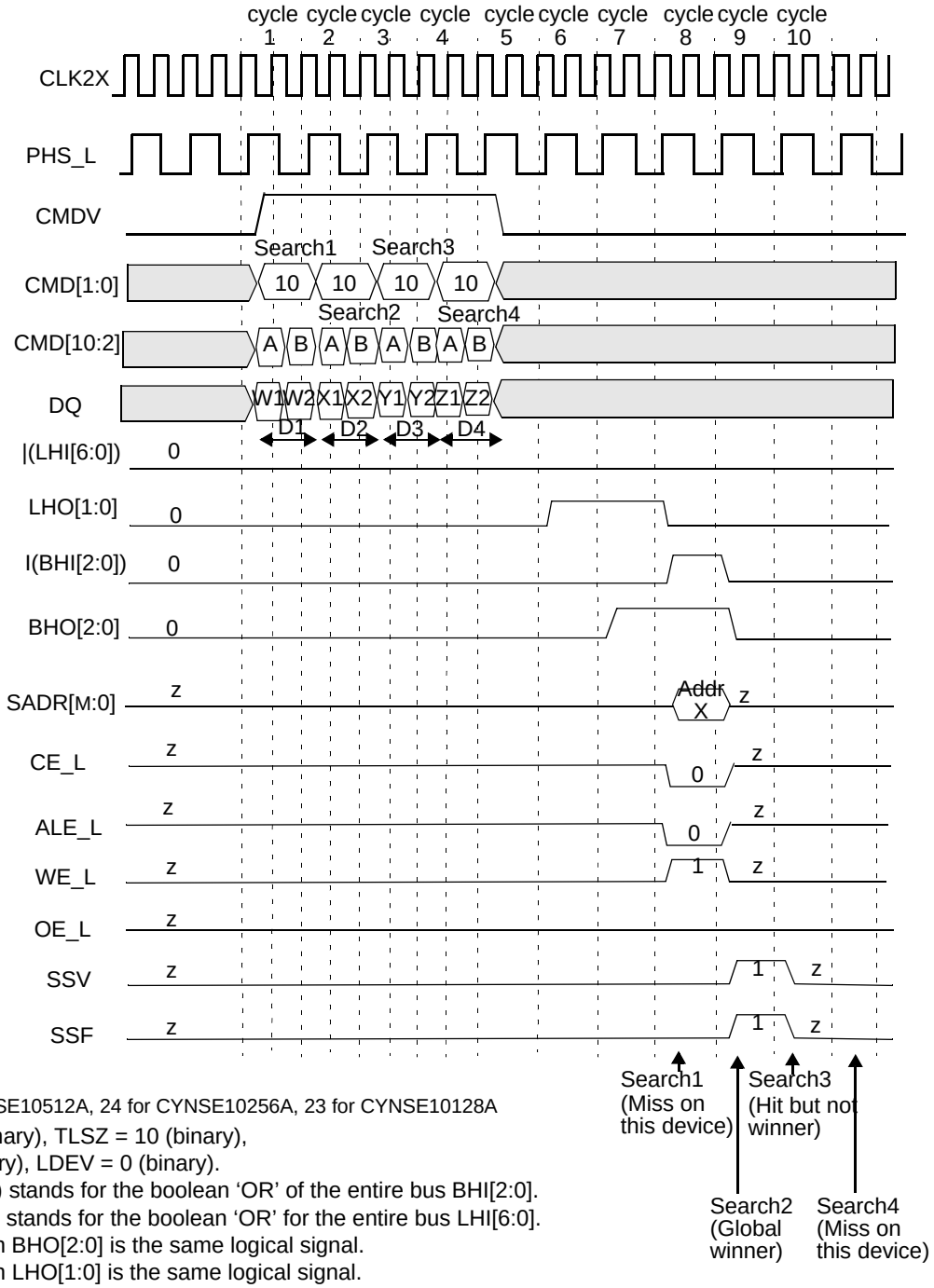
**Figure 6-18. 144-bit Search Timing Diagram for Devices Below Block #1 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

HLAT = 001 (binary),
TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

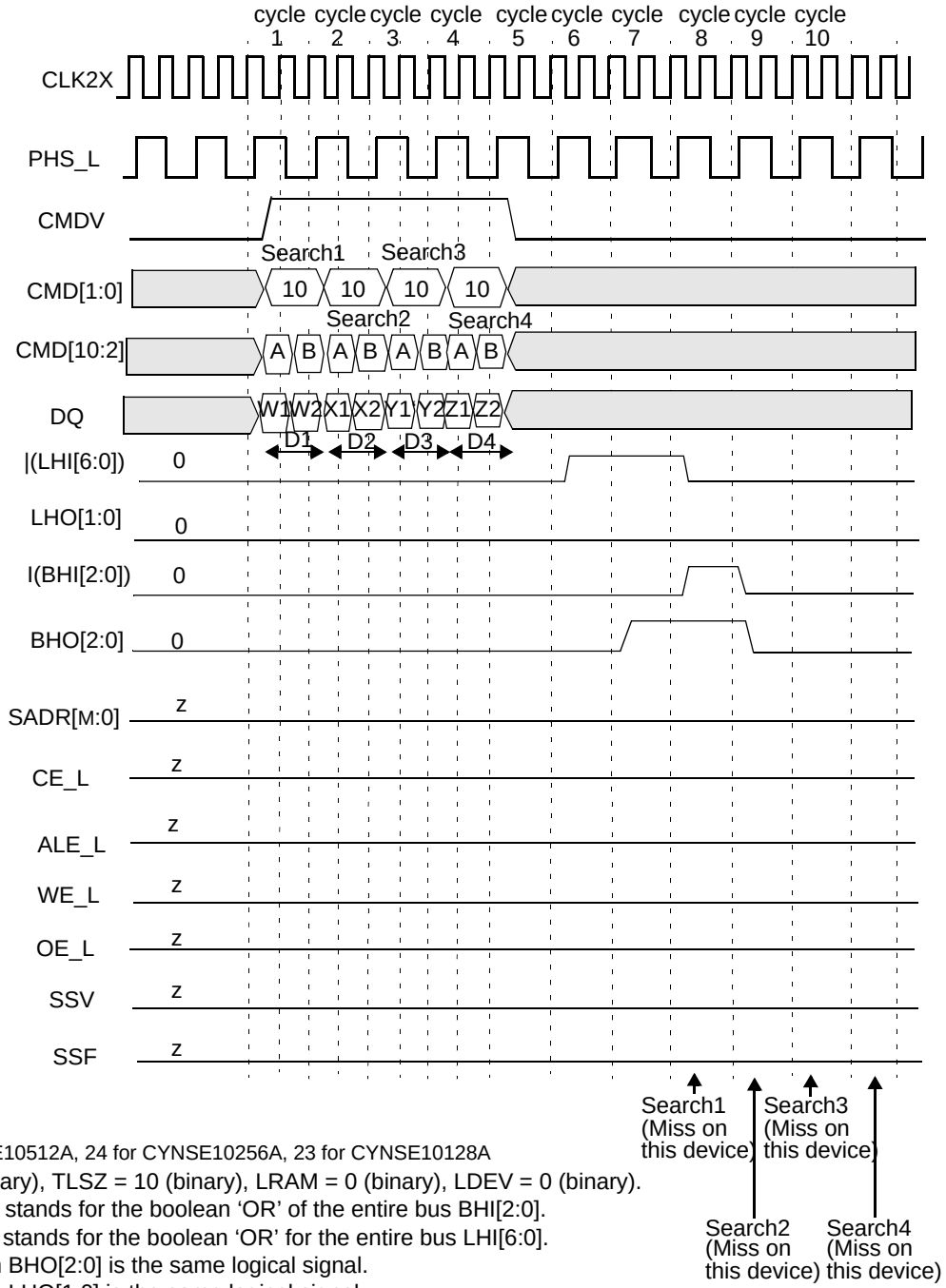
**Figure 6-19. 144-bit Search Timing Diagram for Devices Above Block #2 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

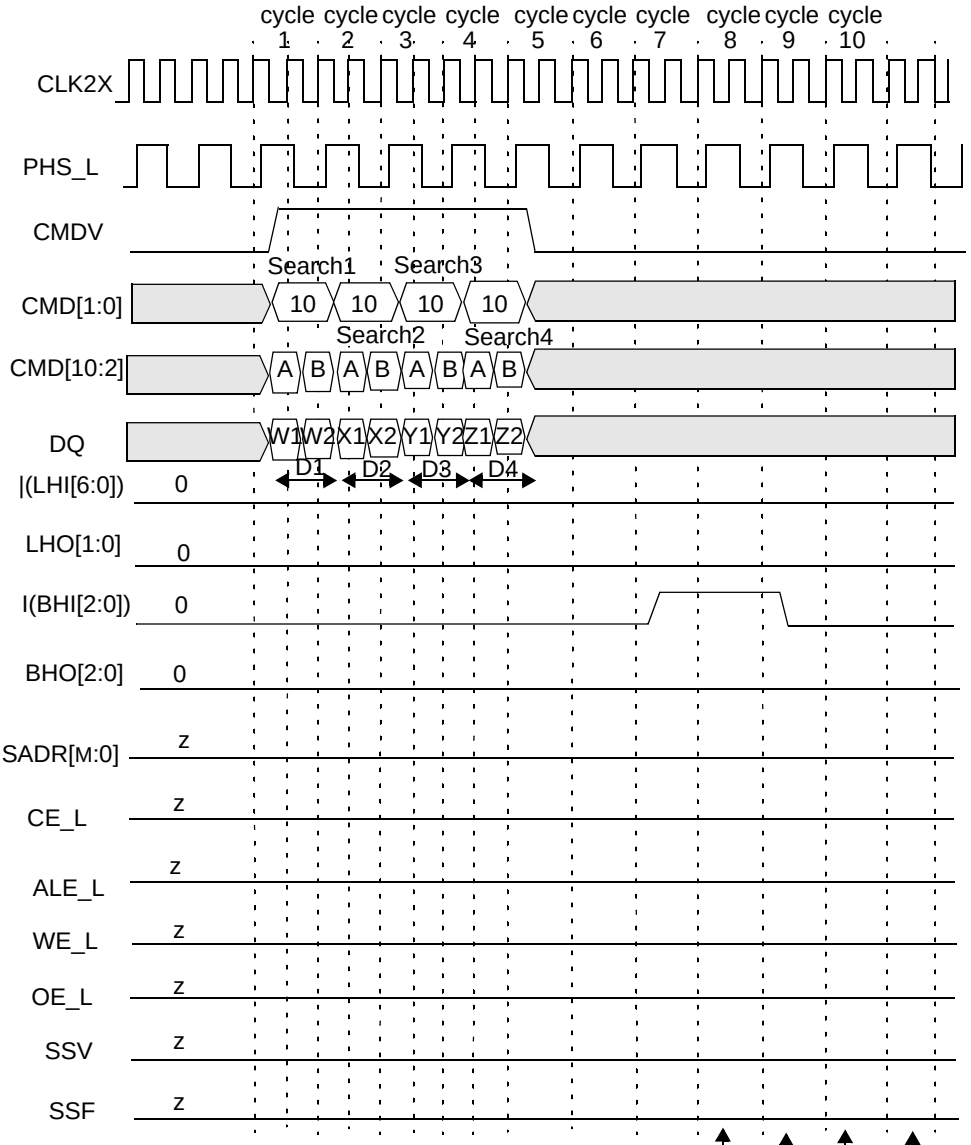
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-20. 144-bit Search Timing Diagram for Block #2 Global Winning Device**



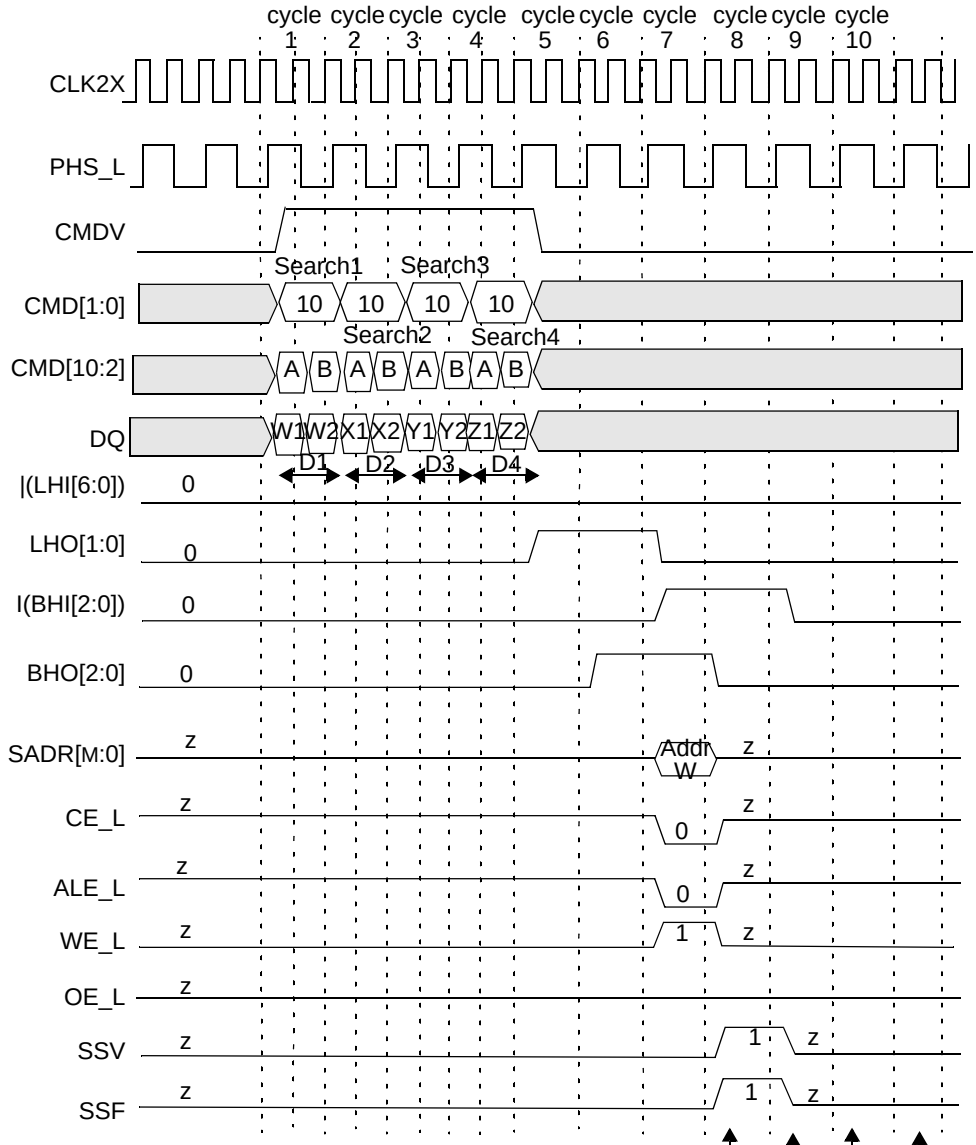

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-21. 144-bit Search Timing Diagram for Devices Below Block #2 Winning Device**



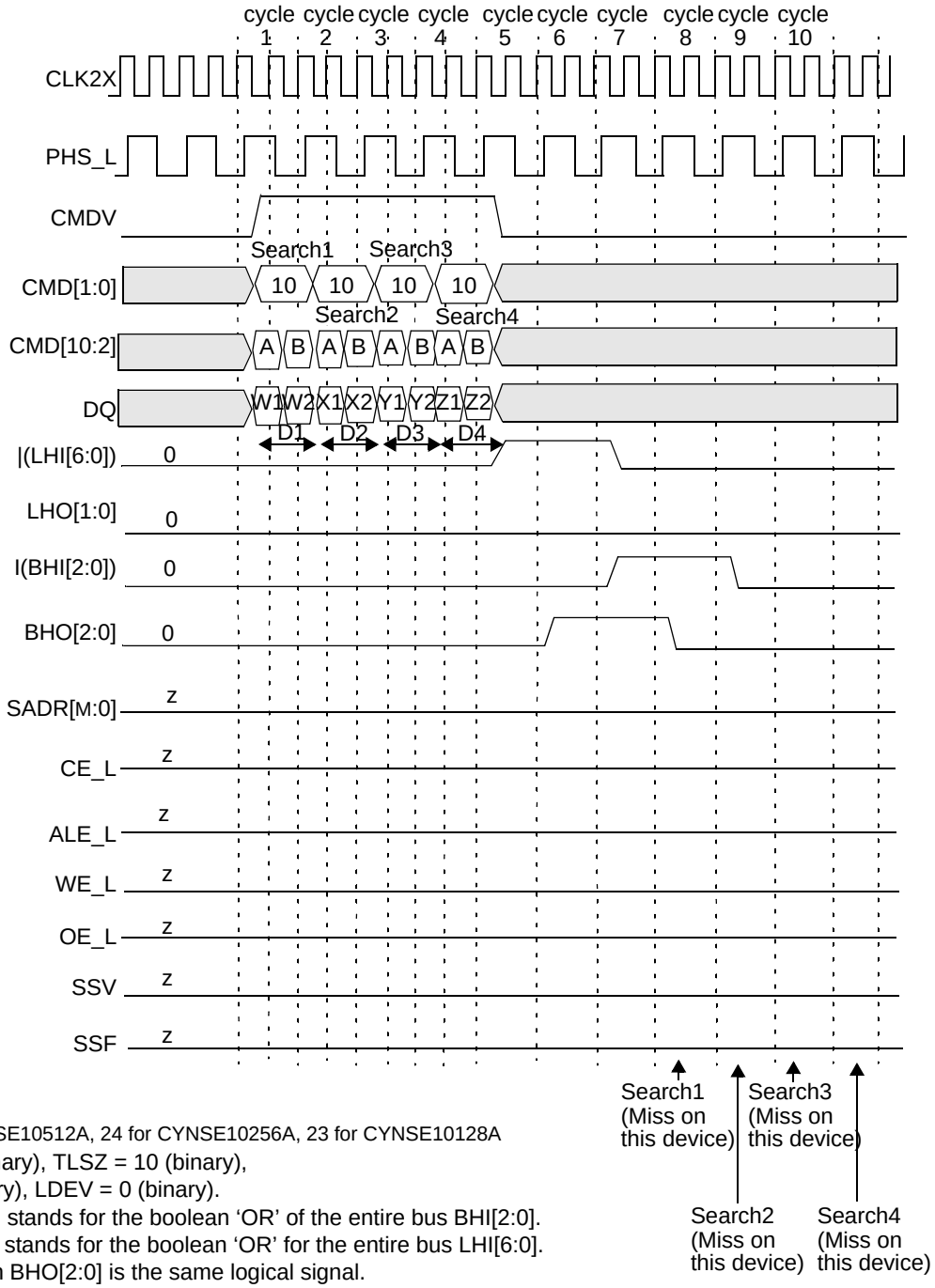

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-22. 144-bit Search Timing Diagram for Devices Above Block #3 Winning Device**



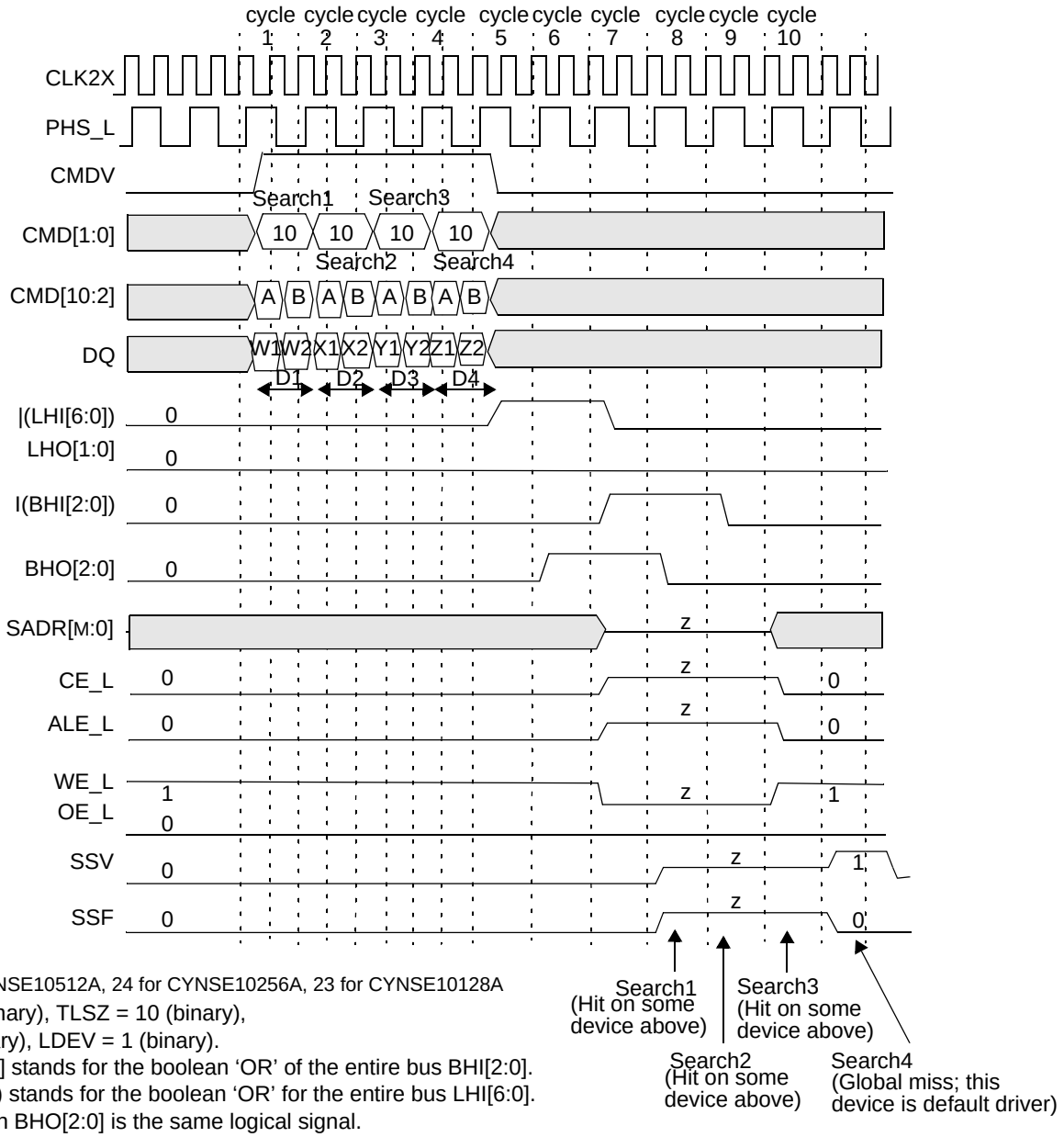

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-23. 144-bit Search Timing Diagram for Block #3 Global Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-24. 144-bit Search Diagram Below Block #3 Winning Device Except the Last Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 001 (binary), TLSZ = 10 (binary),
LRAM = 1 (binary), LDEV = 1 (binary).
Note: |(BHI[2:0)] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-25. 144-bit Search Timing Diagram for Device Number 6 in Block #3**

The following is the sequence of operation for a single 144-bit Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = "10" (binary). CMD[2] must be driven to logic low. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A by this device if it has a hit. CMD[9] must be driven to logic high to indicate a 144-bit search. If Enhanced Mode and MultiSearch Enable bits are both set to 1in the Command Resister, CMD[8] has to be set to 0 for Single Searches. For 288-bit and 576-bit Single Searches, all Cycle A CMD[8] bits have to be set to 0's.
  - **DQ Bus**: DQ[71:0] must be driven with the 72-bit data to be compared.

- **Cycle B**:
  - **Command Bus**: The host ASIC continues to drive CMDV HIGH and applies Search command CMD[1:0] = “10” (binary). CMD[5:2] must be driven by the index of the comparand register pair for storing the 144-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 27 for the description of SSR[0:7]). CMD[10:9] are don’t cares in this cycle.
  - **DQ Bus**: The DQ[71:0] continues to carry the 72-bit data to be compared.

The logical 144-bit Search operation is shown in *Figure 6-26*. The entire table of 31 devices (consisting of 72-bit entries) is compared to a 144-bit word K presented on the DQ bus in both cycles A and B of the command using the GMR and local mask bits. The GMR is the 144-bit word specified by the even and odd GMR pairs selected by the GMR index in the command’s cycle A. The 144-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the comparand register index in command cycle B. In the ×144 configuration, the even and odd comparand register can be subsequently used by the Learn command only in the first non-full device.

**Note**. The Learn command is supported for only one of the blocks consisting of up to eight devices in a depth-cascaded table of more than one block.

The word K (presented on the DQ bus in both cycles A and B of the command) is compared with each entry in the table, starting at location 0 (decimal). A matching entry that satisfies the Soft Priority and Mini-Key scheme (for Enhanced Mode) will be the winning entry, and its location address L will be driven as part of the SRAM address on the SADR[N:0] lines (see “SRAM PIO Access” on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A. The global winning device will drive the bus in a specific cycle. On global miss cycles, the device with LRAM = 1 (binary) and LDEV = 1 (binary) will be the default driver for such missed cycles.

**Note**. During 144-bit searches of 144-bit-configured tables, the Search hit will always be at an even address.

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 144-bit searches in ×144-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 144-bit Search command cycle (two CLK2X cycles) is shown in *Table 6-7*.

For up to 31 devices in the table (TLSZ = 10 (binary)), Search latency is 6 from command to SRAM access cycle. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 6-8*.

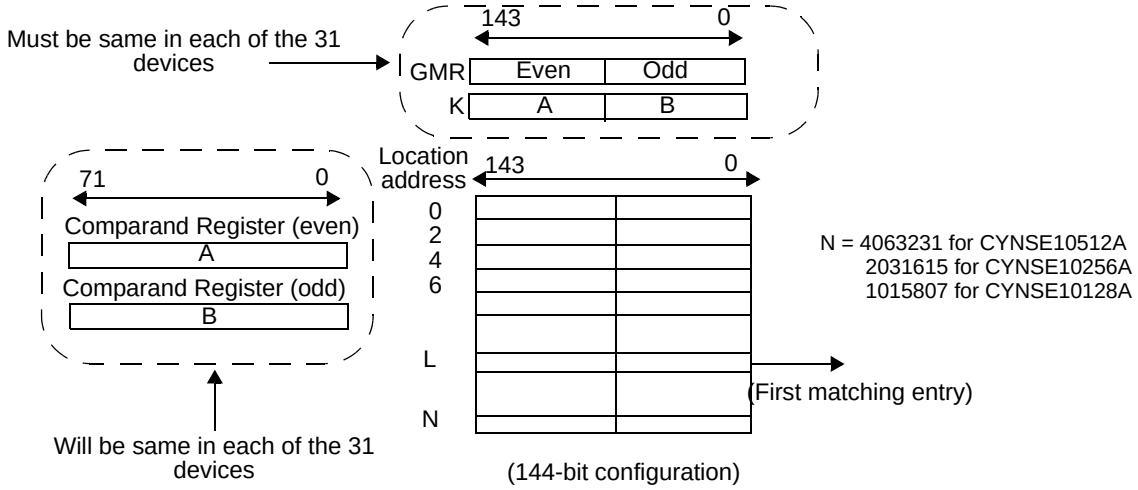



**Figure 6-26. ×144 Table with 31 Devices**

### 6.5.5 576-bit Single Search for One Device or Cascade up to Eight Devices

The hardware diagram of the Search subsystem of up to eight devices is shown in *Figure 6-10*. The MultiSearch Enable (MSE) bit in the Command Register must be set LOW to perform single-search. The following are the rest of the parameters programmed into the eight devices.

- First seven devices (devices 0–6): TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 0 (binary), and LDEV = 0 (binary).
- Eighth device (device 7): TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 1 (binary), and LDEV = 1 (binary).
- 576-bit search is only available in the Enhanced Mode, not in the Non-Enhanced Mode. NES should be set to “11” (binary) in all blocks of all devices to create a 576-bit table.

For a single-device configuration, all parameters will be the same as device 7. BHI[2:0] and LHI[6:0] should be tied to ground.

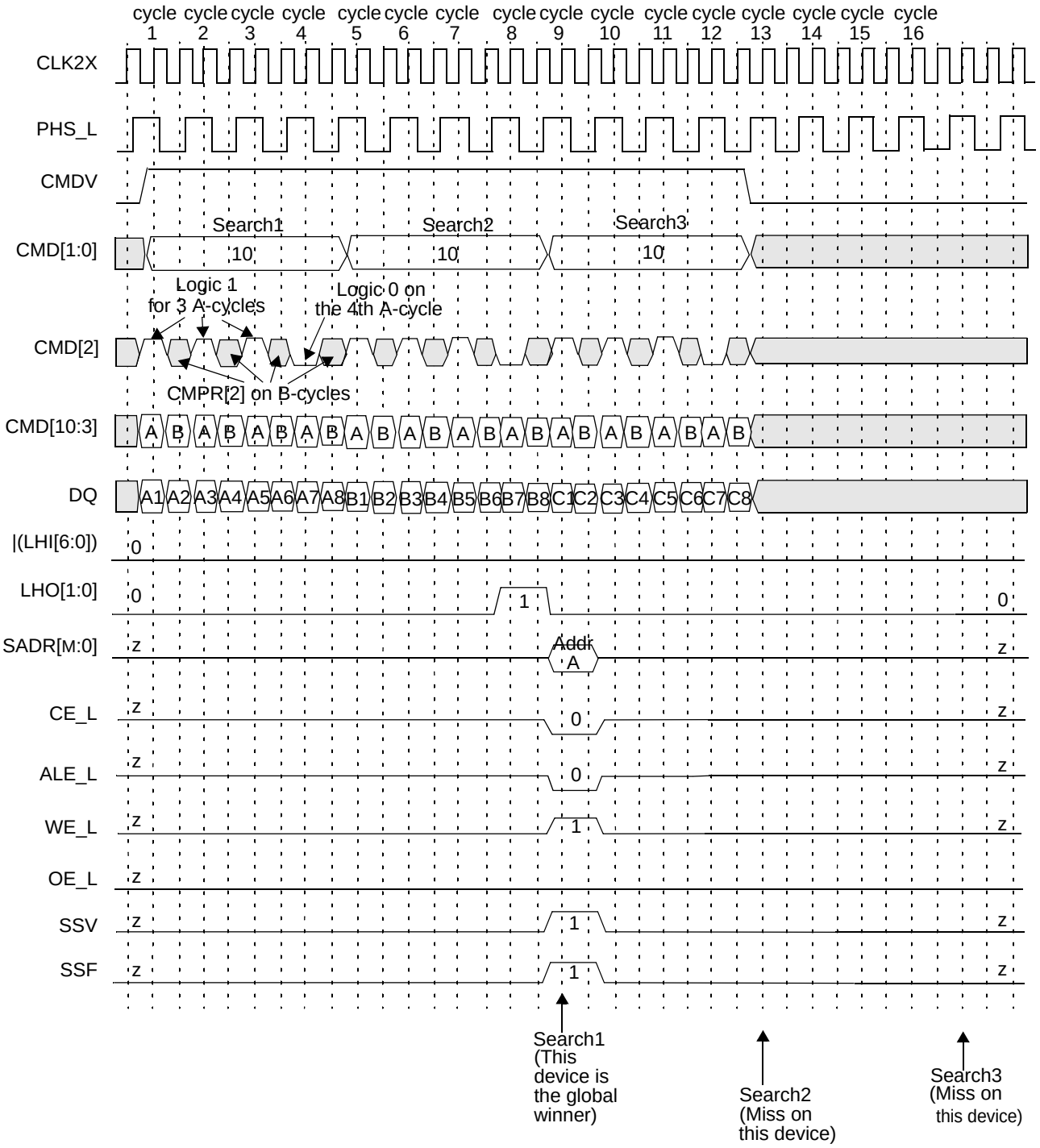
***Notes***:

- All eight devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table (device number 7 in this case) must be programmed with LRAM = 1 (binary) and LDEV = 1 (binary). All other upstream devices (devices 0 through 6 in this case) must be programmed with LRAM = 0 (binary) and LDEV = 0 (binary).
- The device receiving all the LHO signals from the other devices is considered the last device.
- All the shared signals in the following timing diagrams showing tri-stated condition (“z”) indicate that, that particular device is not driving the shared signals. The shared signals are not three-stated in a real life because other devices will be driving them.
- Comparing the hardware diagrams shown in *Figure 6-10* and *Figure 6-43*, enabling MultiSearch does not mean that a board layout change is required. The LHO_1_L and LHI_1_L share the same pin with the Full In and Full Out signals, which are not shown in *Figure 6-10*. Cascading multiple devices together still allow the user to configure the devices through software to perform single-search or MultiSearch operations without any board change.

The following three figures show the response of three of the eight devices having a hit at different time according to a Hit/Miss assumption shown below in *Table 6-11*. For these timing diagrams, three 576-bit searches are performed sequentially. *Figure 6-27* shows the timing diagram for a Search command in the 576-bit-configured table of eight devices for device number 0. *Figure 6-28* and *Figure 6-29* shows the same for device number 1 and number 7 (the last device in this specific table) respectively.

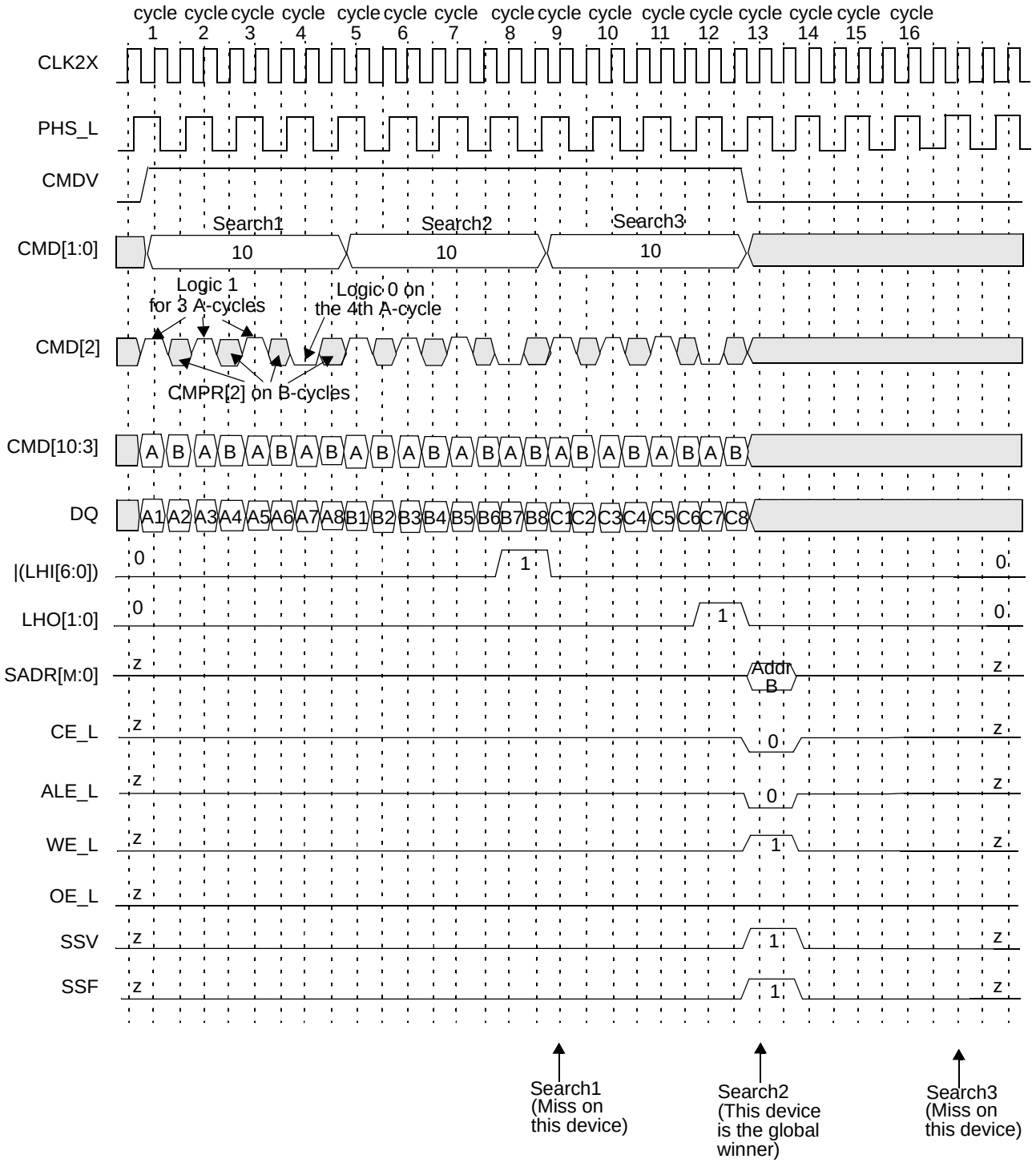
**Table 6-11. Hit/Miss Assumptions**

| Search Number | 1 | 2 | 3 |
|---|---|---|---|
| Device 0 | Hit | Miss | Miss |
| Device 1 | Miss | Hit | Miss |
| Devices 2–6 | Miss | Miss | Miss |
| Device 7 | Miss | Miss | Miss |



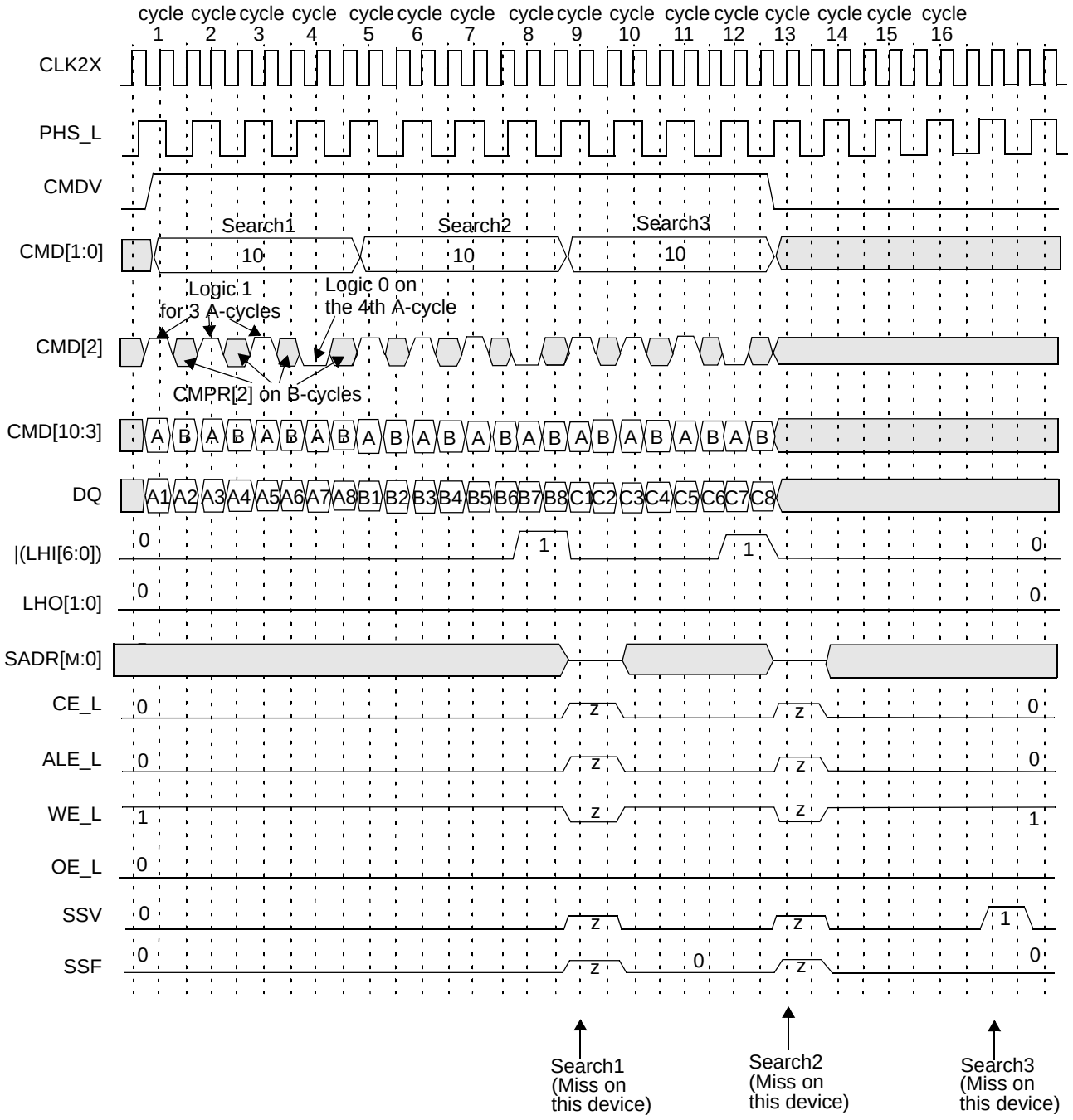

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-27. Timing Diagram for 576-bit Single Search Device Number 0**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-28. Timing Diagram for 576-bit Single Search Device Number 1**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary).

Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].

Note: Each bit in LHO[1:0] is the same logical signal.

**Figure 6-29. Timing Diagram for 576-bit Single Search Device Number 7 (Last Device)**

The following is the sequence of operation for a single 576-bit Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = "10" (binary). CMD[2] must be driven to logic 1 for the first three A-cycles and then driven to logic 0 for the final A-cycle for 576-bit search. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. Each of the four A-cycles provide a GMR index to mask 144 bits of the data to be compared (each A-cycle provide a pair of GMR, which is 144 bits, four A-cycles will result in a total of 576 bits of GMR). CMD[8:6] signals must be driven with the same bits that will be driven on SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A by this device if it has a hit. If Enhanced Mode and MultiSearch Enable bits are both set to 1in the Command Resister, CMD[8] has to be set to 0 for Single Searches. For 288-bit and 576-bit Single Searches, all Cycle A CMD[8] bits have to be set to 0's. CMD[9] is don't care for this cycle.
  - **DQ Bus**: At the same time in cycle A, DQ[71:0] must be driven with 72-bit data (which is part of the 576-bit data) to be compared.
- **Cycle B**:
  - **Command Bus**: The host ASIC continues to drive CMDV HIGH and to apply Search command CMD[1:0] = "10" (binary). CMD[5:2] must now be driven by the index of the comparand register pair for storing the two 72-bit word presented on the DQ bus during cycles A and B. Each of the four B-cycles provide an index for a pair of comparand register. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 27 for a description of SSR[0:7]). CMD[10:9] are don't cares for this cycle.
  - **DQ Bus**: The DQ[71:0] continues to carry the 72-bit data (which is part of the 576-bit data) to be compared.

**Note**. For 576-bit searches, the host ASIC must supply individual 72-bit data on DQ[71:0] during cycles A and B. Also, four individual pairs of GMR and CMPR registers may be involved in the comparison.

The logical 576-bit Search operation is shown in *Figure 6-30*. The entire table of 576-bit entries (eight devices) is compared to a 576-bit word K that is presented on the DQ bus in eight cycles using the GMR and local mask bits. The GMR is the 576-bit word specified by four pairs of GMRs selected by GMR indices in each of the eight devices. The 576-bit word K (presented on the DQ bus in all eight cycles of the command) is also stored in both even and odd comparand register pairs (selected by the comparand register index in command cycle B) in each of the eight devices. The word K is compared with each entry in the table, starting at location 0 (decimal). A matching entry that satisfies the Soft Priority and Mini-Key scheme will be the winning entry, and its location address L will be driven as part of the SRAM address on the SADR[N:0] lines (see Section 6.7, "SRAM PIO Access," on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A. The global winning device will drive the bus in a specific cycle. On a global miss cycle, the device with LRAM = 1 (binary) (default driving device for the SRAM bus) and LDEV = 1 (binary) (default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

The Search command is a pipelined operation and executes a Search at one-eighth the rate of the frequency of CLK2X for 576-bit searches in ×576-configured tables. The latency of the Search from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ = 01 (binary)). SSV and SSF also shift further to the right for different values of HLAT, as specified in *Table 6-8*.

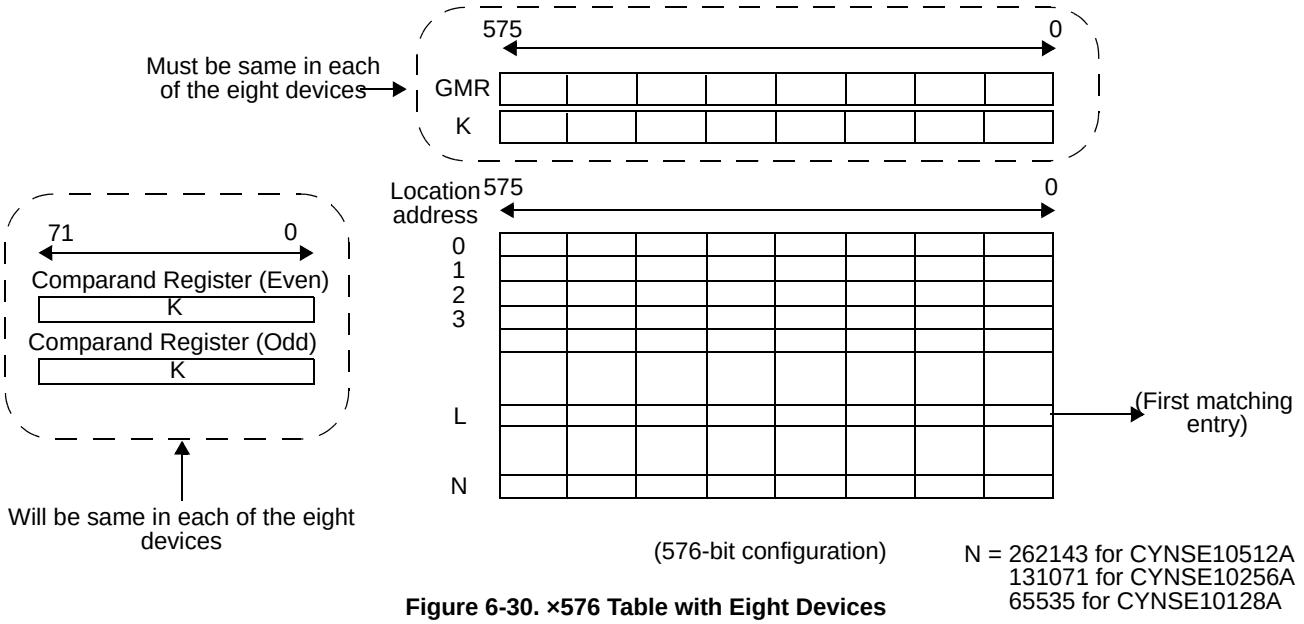



**Figure 6-30. ×576 Table with Eight Devices**

### 6.5.6 *Mixed-size Single Searches with 31 Devices on Tables Configured with Different Widths*

This subsection will cover mixed searches (×72, ×144, and ×288) with tables of different widths (×72, ×144, ×288). ***Note***: Non-Enhanced Mode does not support 576-bit tables. The sample operation shown is for 31 devices, with devices 0 to 7 containing x72 tables (CFG field in Command register all zeroes for Non-Enhanced Mode, NES = “00” (binary) for all blocks for Enhanced Mode), devices 8 to 15 containing x144 tables (CFG[63:0] field in Command register for CYNSE10512A = 5555555555555555 (hex), CFG[31:0] = 55555555 (hex) for CYNSE10256A, CFG[15:0] = 5555 (hex) for CYNSE10128A for Non-Enhanced Mode, NES = “01” (binary) in all blocks for Enhanced Mode), and the rest of the devices containing x288 tables (CFG[63:0] = AAAAAAAAAAAAAAAA (hex) for CYNSE10512A, CFG[31:0] = AAAAAAAA (hex) for CYNSE10256A, CFG[15:0] = AAAA (hex) for CYNSE10128A for Non-Enhanced Mode, NES = “10” (binary) in all blocks for Enhanced Mode). The following figures show three sequential searches: first, a 72-bit Search on a ×72-configured table; a 144-bit Search on a ×144-configured table; and a 288-bit Search on a ×288-configured table that each results in a hit.

The 31 cascaded devices can be viewed as three blocks of 8 devices and a fourth block of 7 devices, as shown in *Figure 6-15*. Each individual block of 8 or 7 devices is connected very similarly to the connection shown in *Figure 6-10*, except that the BHI[2:0] signals are connected to BHO of the previous block rather than being grounded. *Figure 6-31* shows a graphical example of the tables using CYNSE10512As.

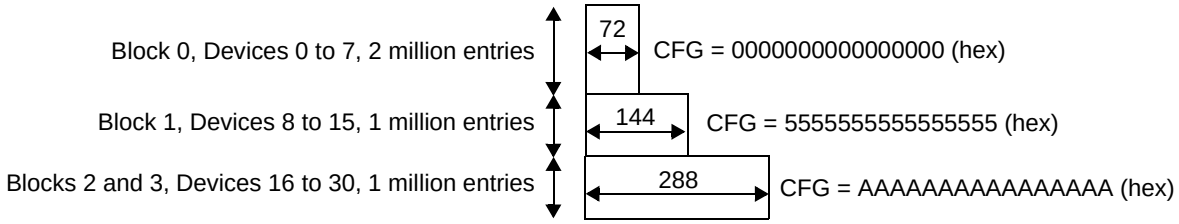



**Figure 6-31. Multiwidth Configurations Example with CYNSE10512As**

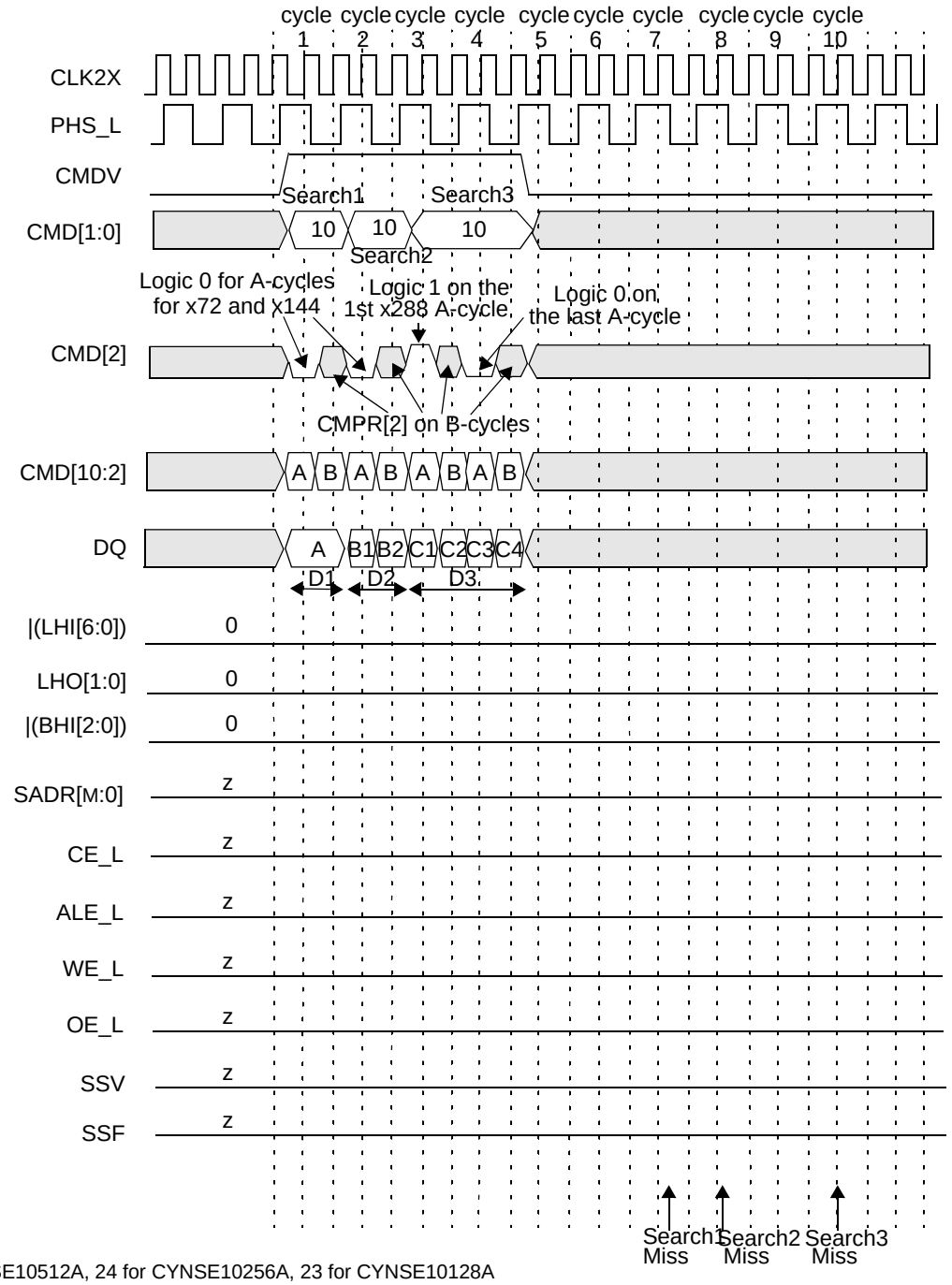
**Notes**:

- The “Block” in the figure above refers to a block of 8 devices, not a block within a single device.
- All 31 devices must be programmed with the same values for TLZ (“10” (binary)) and HLAT (“000” (binary) in this example). Only the last device in the table must be programmed with LRAM = 1 (binary) and LDEV = 1 (binary) (device 30 in this case). All other upstream devices must be programmed with LRAM = 0 (binary) and LDEV = 0 (binary) (devices 0 through 29 in this case).
- The device receiving all the LHO signals from the other devices is considered the last device.
- All the shared signals in the following timing diagrams showing tri-stated condition (“z”) indicate that, that particular device is not driving the shared signals. The shared signals are not three-stated in a real life because other devices will be driving them.
- One way to create many tables of different widths in a bank of NSEs is by having table designation bits. It is assumed that bits [71:70] for each entry will be assigned such table designation bits. DQ[71:70] will be 00 in each of the two A and B cycles of the ×72-bit Search (Search1). DQ[71:70] is 01 in each of the A and B cycles of the ×144-bit Search (Search2). DQ[71:70] is 10 in each of the A, B, C, and D cycles of the ×288-bit Search (Search3).

The timing diagrams below corresponds to the Hit/Miss assumptions defined in *Table 6-12*. For the purpose of illustrating the timings, it is further assumed that there is only one device with a matching entry in each of the blocks.

**Table 6-12. Hit/Miss Assumptions**

| Search Number | #1 (x72) | #2 (x144) | #3 (x288) |
|---|---|---|---|
| Block 0 | Hit | Miss | Miss |
| Block 1 | Miss | Hit | Miss |
| Block 2 | Miss | Miss | Hit |
| Block 3 | Miss | Miss | Miss |



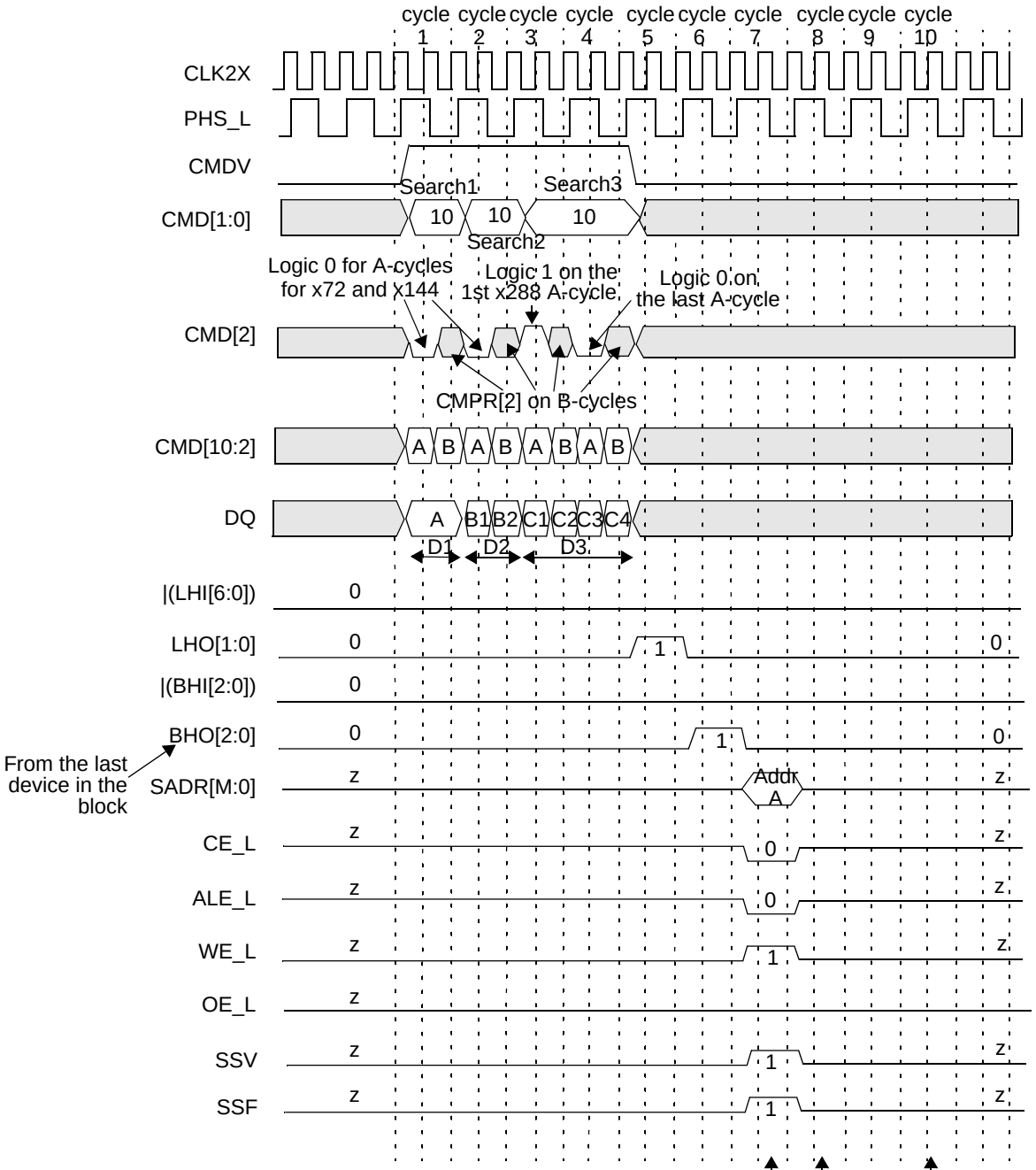

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode, CFG = all zeroes

NES = 00 (binary) in all blocks for Enhanced Mode, x72 search

HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-32. Timing Diagram for Mixed Search for Devices Above Block 0 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

CFG = all zeroes for Non-Enhanced Mode

NES = 00 (binary) in all blocks for Enhanced Mode, x72 search

HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-33. Timing Diagram for Mixed Search for Block 0 Winning Device**

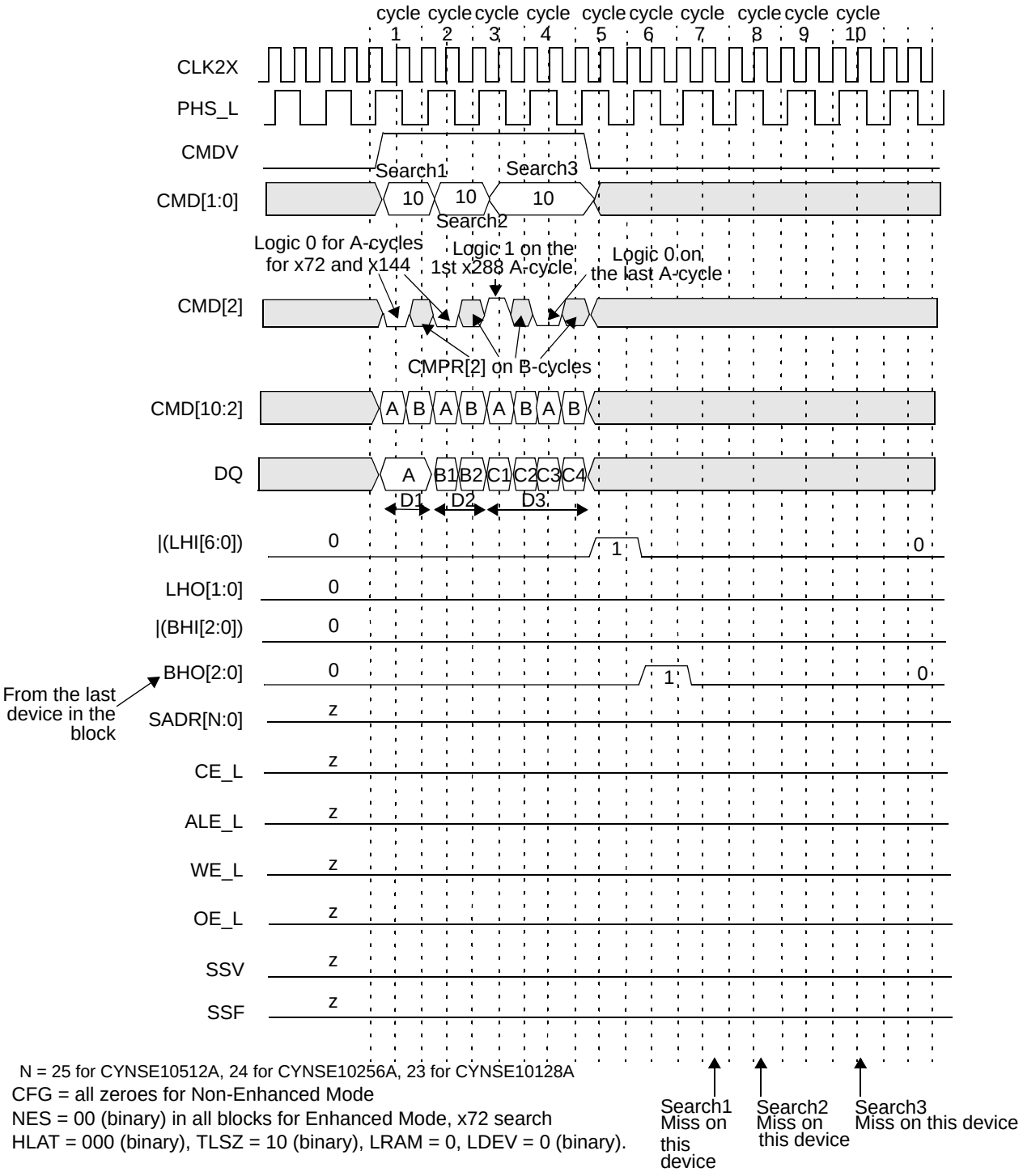
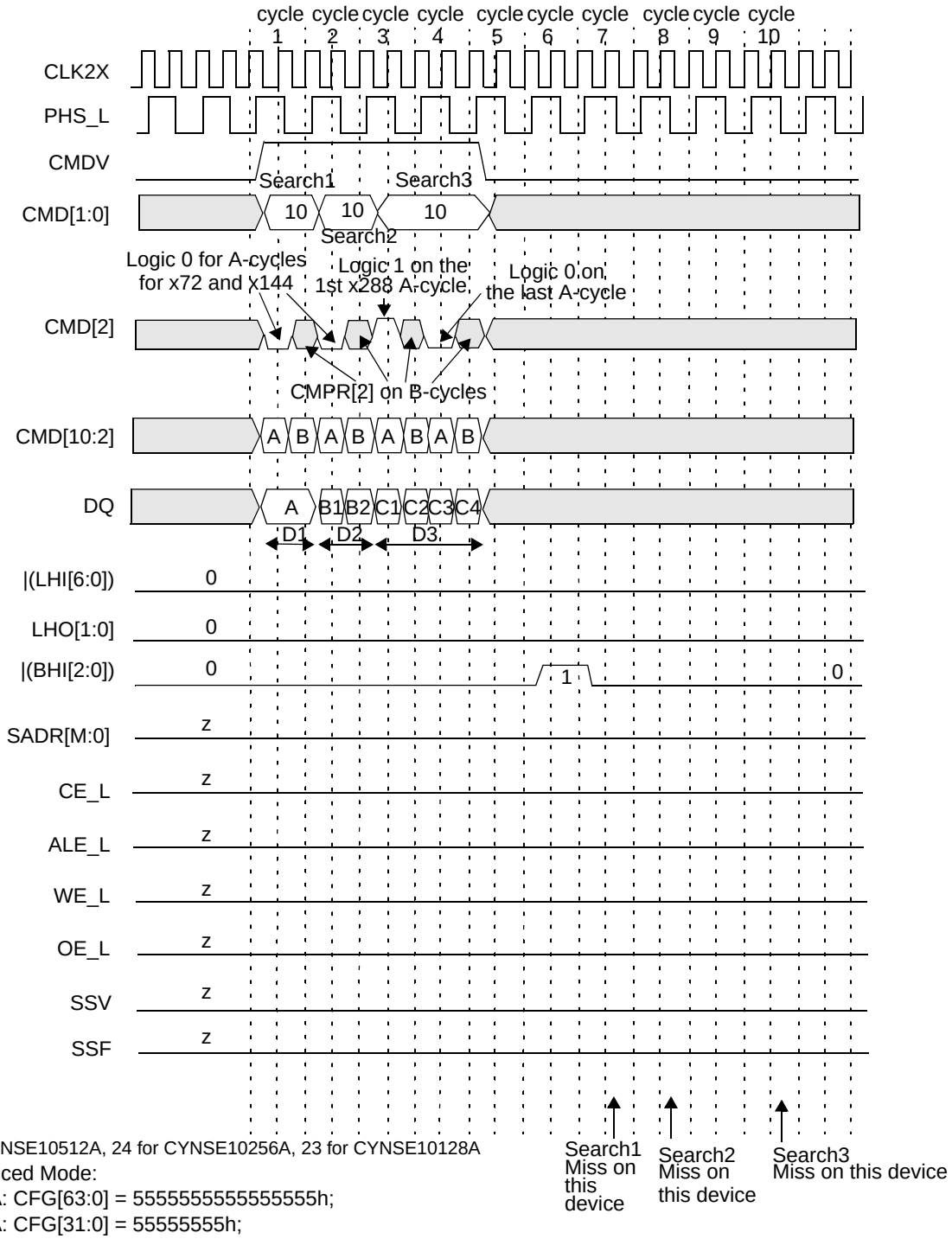


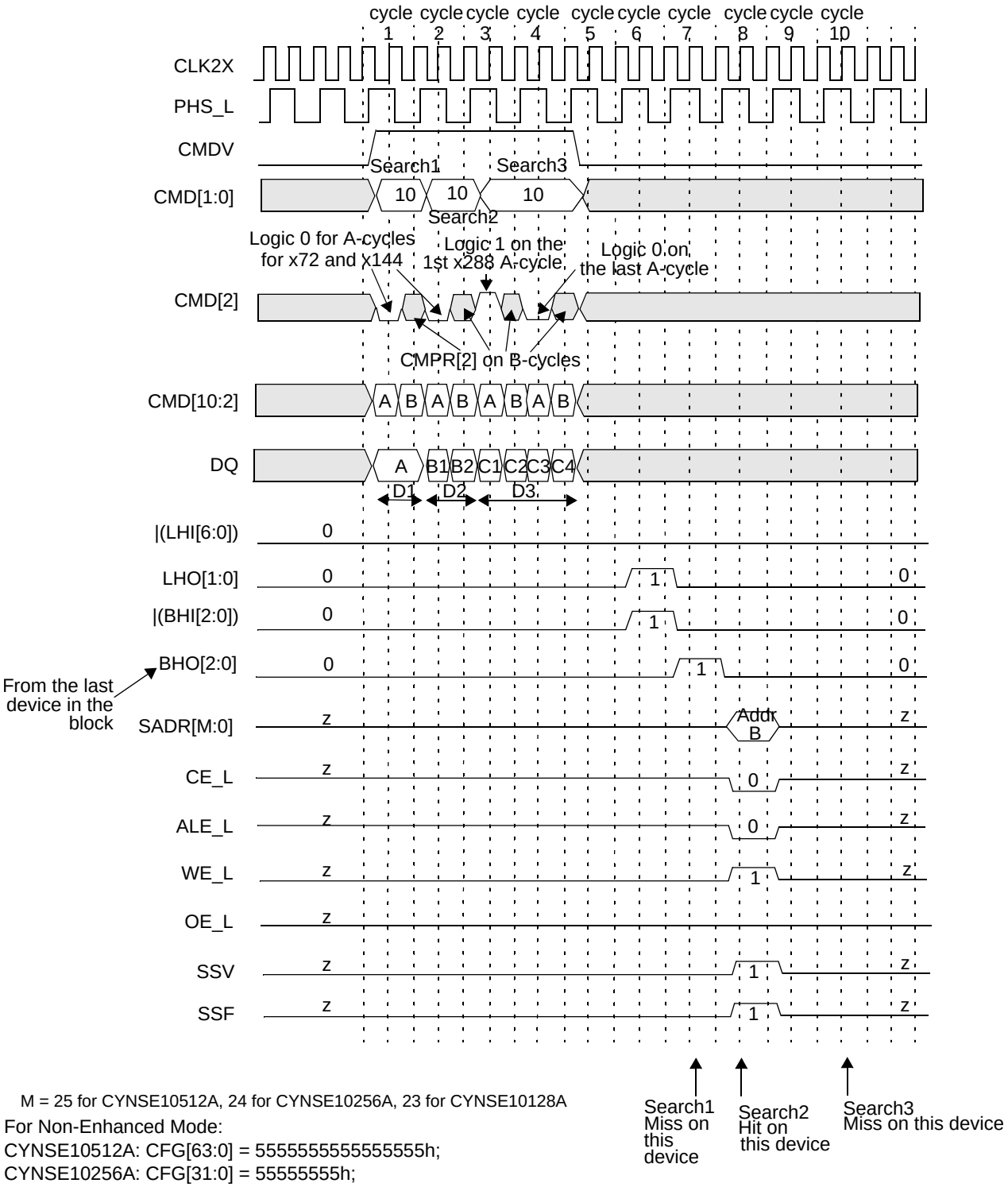

**Figure 6-34. Timing Diagram for Mixed Search for Devices Below Block 0 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode:
CYNSE10512A: CFG[63:0] = 5555555555555555h;
CYNSE10256A: CFG[31:0] = 55555555h;
CYNSE10128A: CFG[15:0] = 5555h.
NES = 01 (binary) in all blocks for Enhanced Mode, x144 search
HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

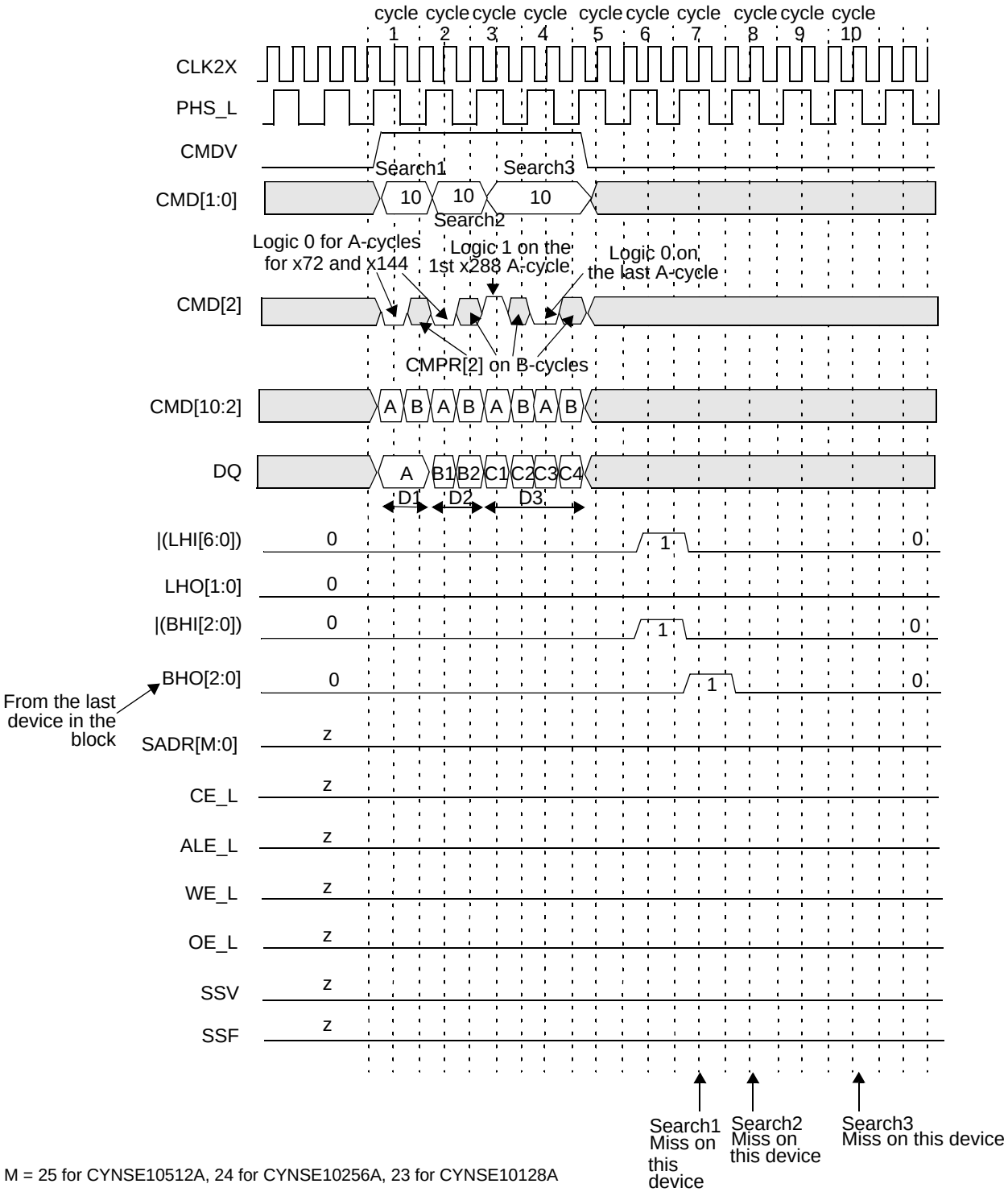
**Figure 6-35. Timing Diagram for Mixed Search Above Block 1 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode:
CYNSE10512A: CFG[63:0] = 5555555555555555h;
CYNSE10256A: CFG[31:0] = 55555555h;
CYNSE10128A, CFG[15:0] = 5555h.
NES = 01 (binary) in all blocks for Enhanced Mode, x144 search
HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

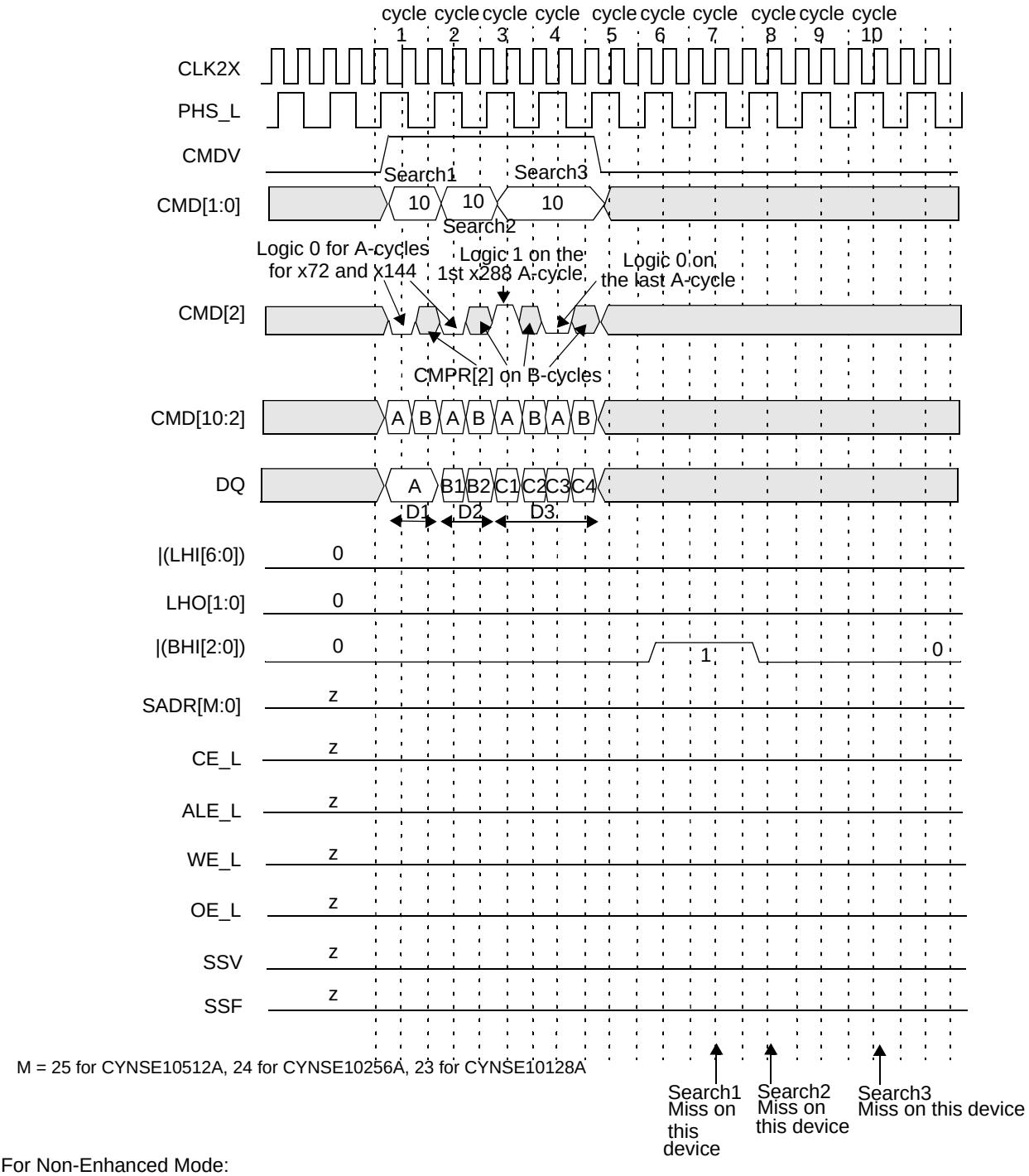
**Figure 6-36. Timing Diagram for Mixed Search for Block 1 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode:
CYNSE10512A: CFG[63:0] = 5555555555555555h;
CYNSE10256A: CFG[31:0] = 55555555h;
CYNSE10128A, CFG[15:0] = 5555h.
NES = 01 (binary) in all blocks for Enhanced Mode, x144 search
HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-37. Timing Diagram for Mixed Search Below Block 1 Winning Device**




For Non-Enhanced Mode:
CYNSE10512A: CFG[63:0] = AAAAAAAAAAAAAAAAh;
CYNSE10256A: CFG[31:0] = AAAAAAAAh;
CYNSE10128A, CFG[15:0] = AAAAh.
NES = 10 (binary) in all blocks for Enhanced Mode, x288 search
HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-38. Timing Diagram for Mixed Search Above Block 2 Winning Device**

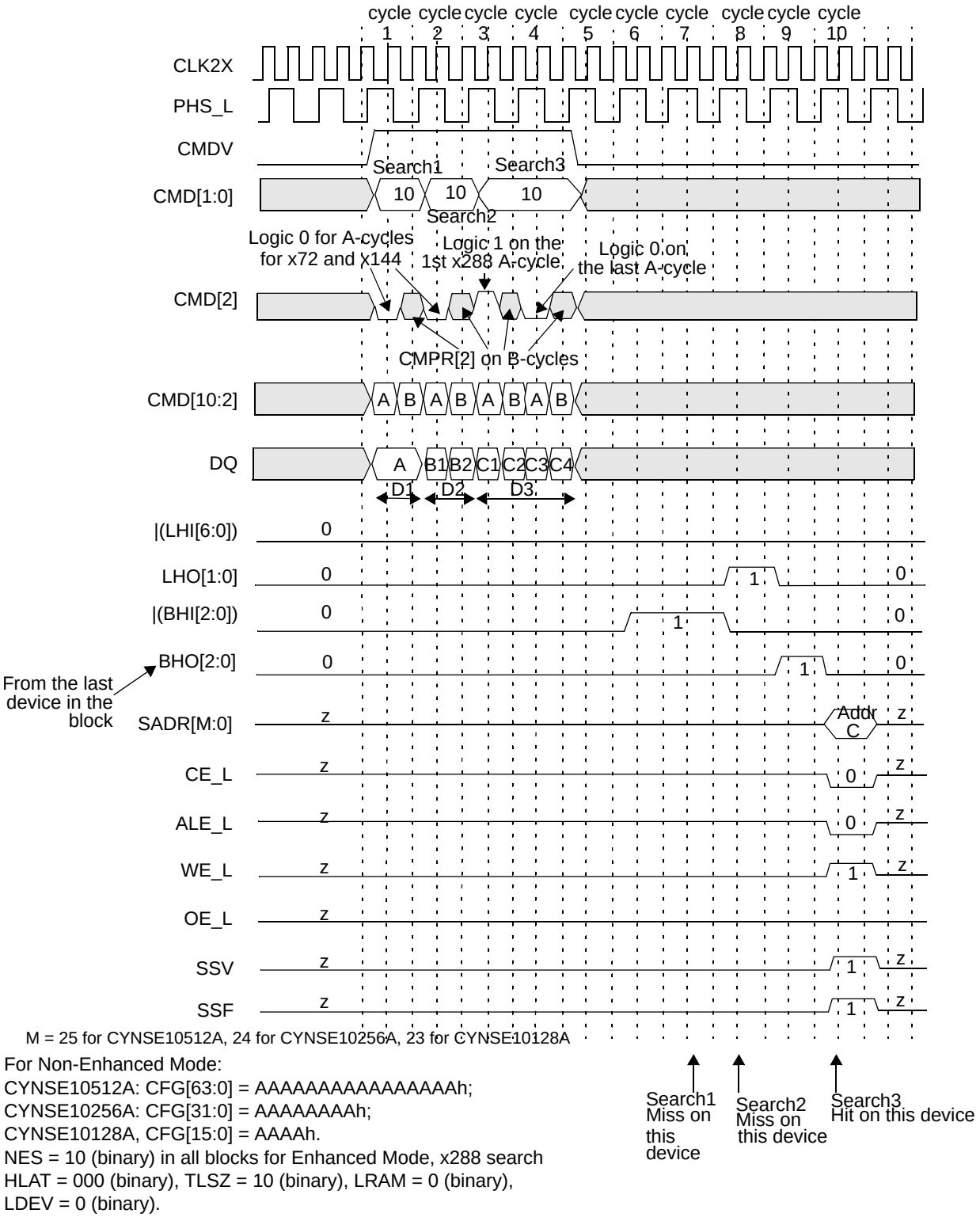
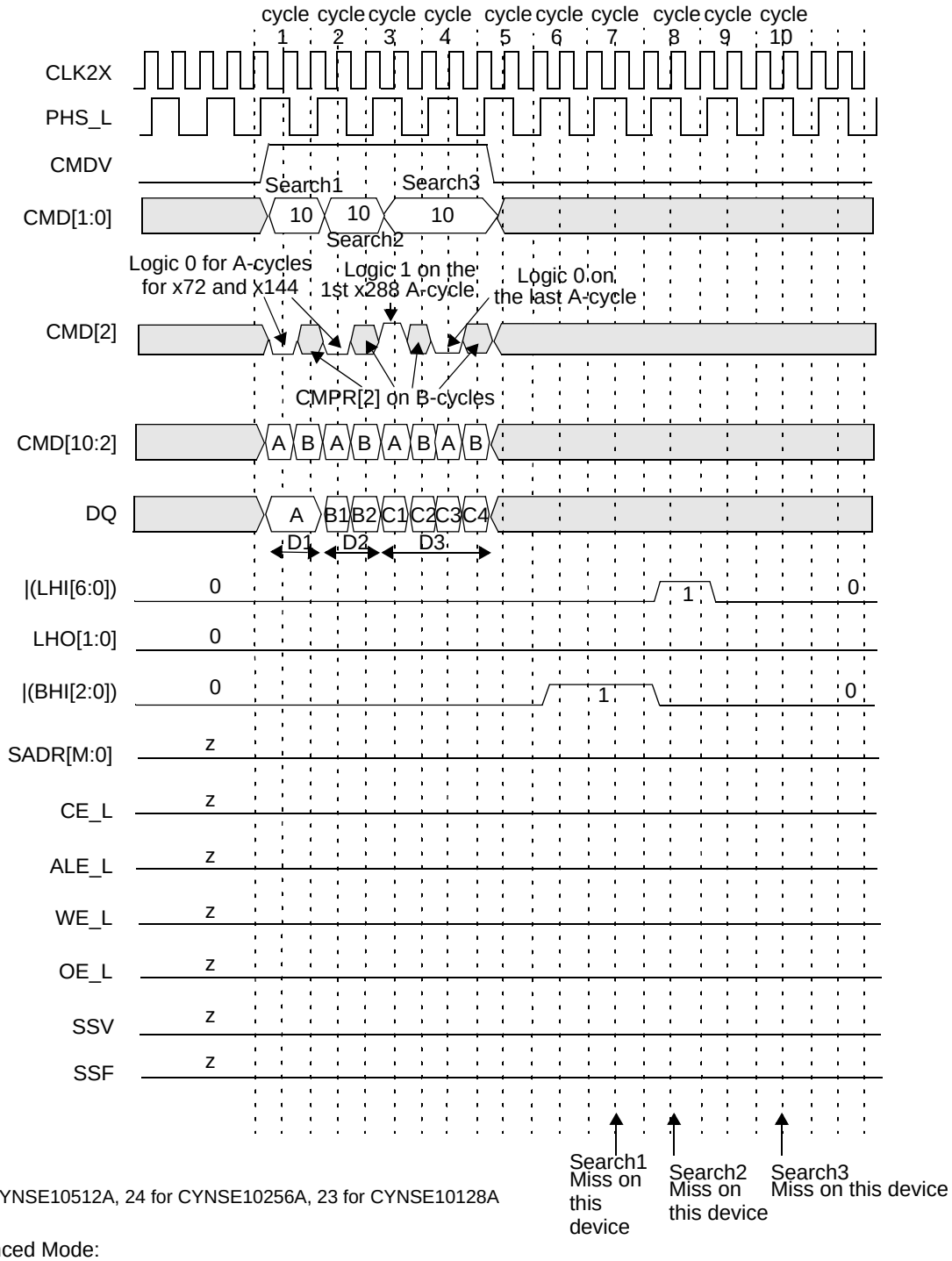


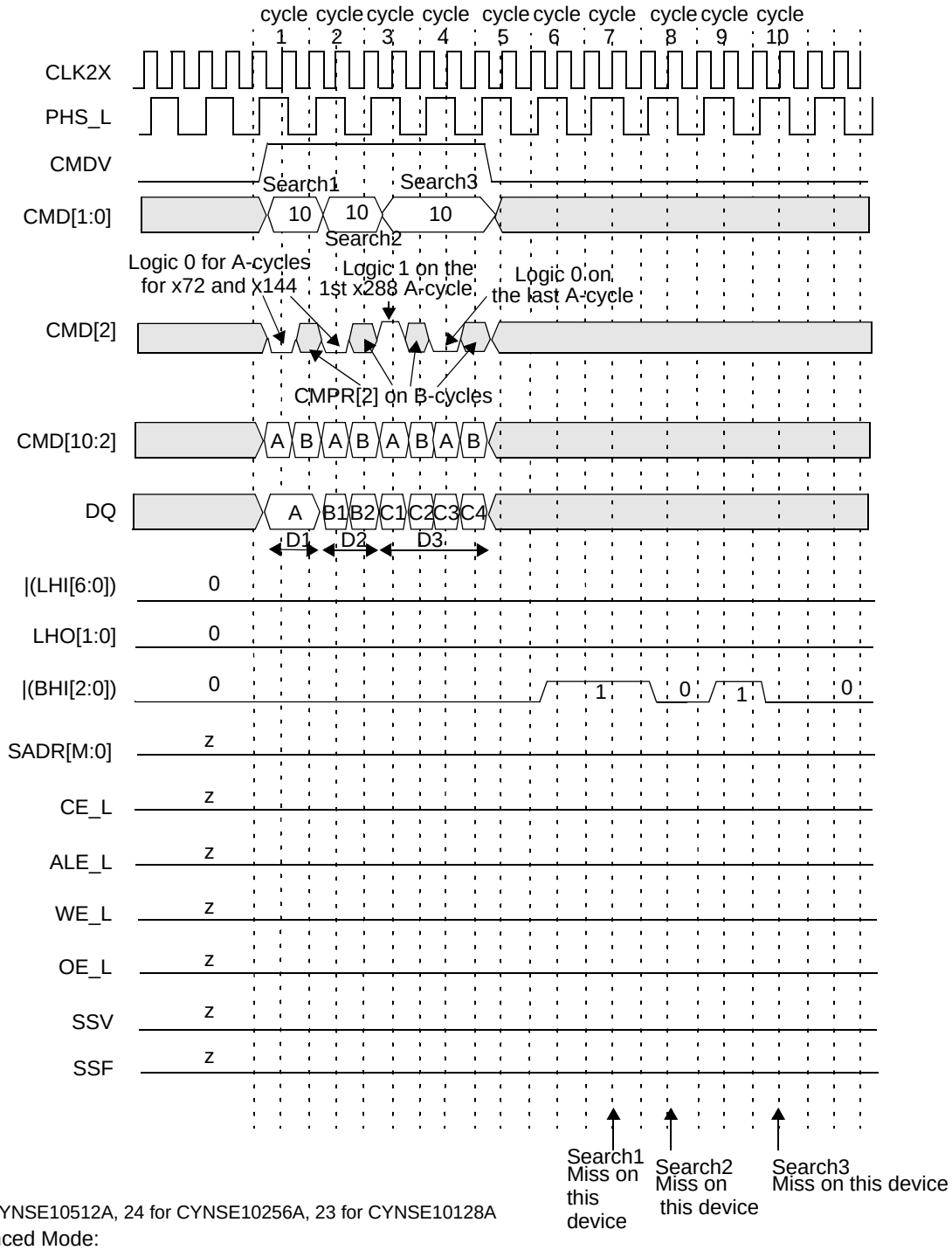

**Figure 6-39. Timing Diagram for Mixed Search for Block 2 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode:
CYNSE10512A: CFG[63:0] = AAAAAAAAAAAAAAAAh;
CYNSE10256A: CFG[31:0] = AAAAAAAAh;
CYNSE10128A, CFG[15:0] = AAAAh.
NES = 10 (binary) in all blocks for Enhanced Mode, x288 search.
HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

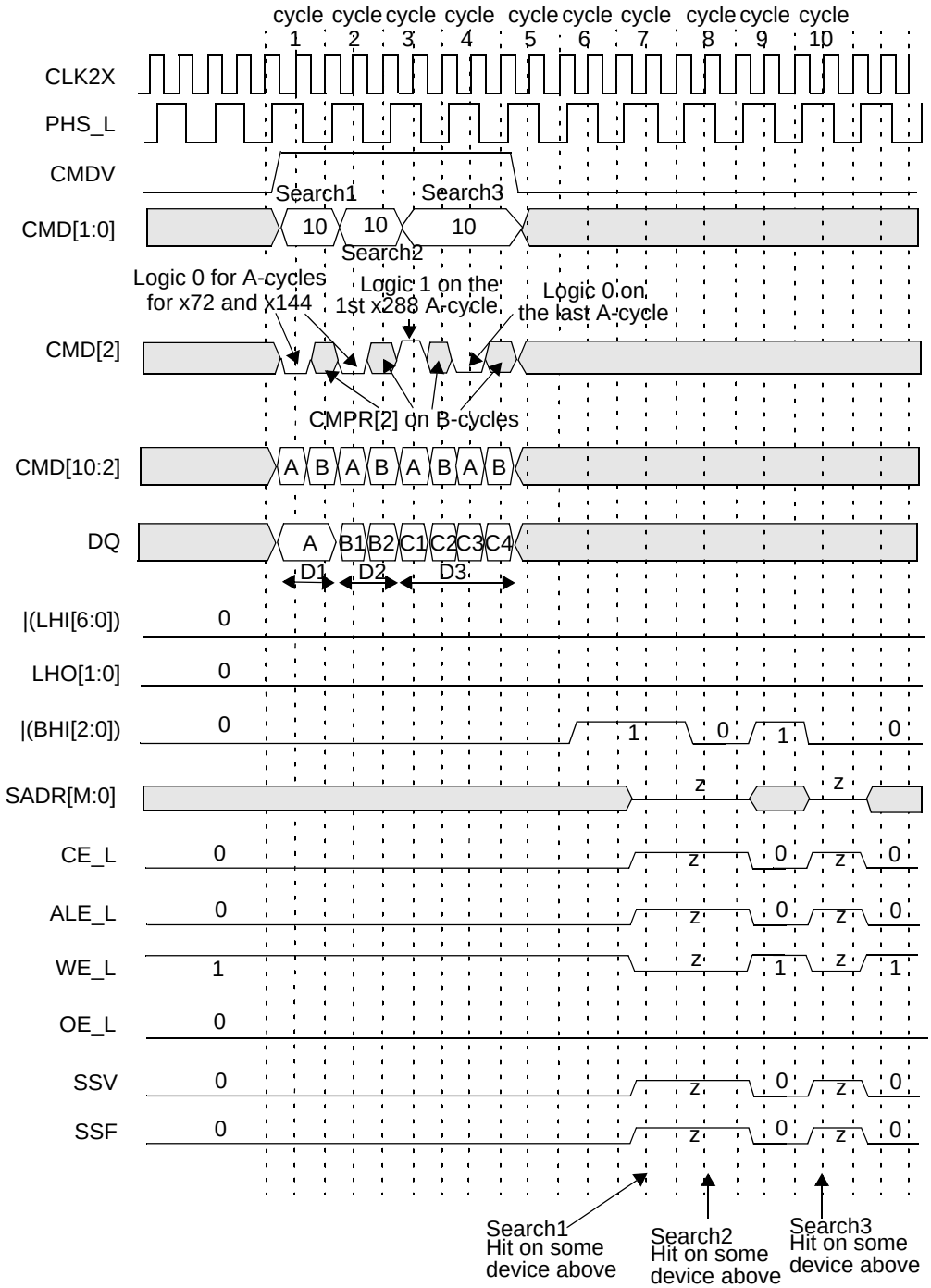
**Figure 6-40. Timing Diagram for Mixed Search Below Block 2 Winning Device**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode:
CYNSE10512A: CFG[63:0] = AAAAAAAAAAAAAAAAh;
CYNSE10256A: CFG[31:0] = AAAAAAAAh;
CYNSE10128A, CFG[15:0] = AAAAh.
NES = 10 (binary) in all blocks for Enhanced Mode, x288 search.
HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-41. Timing Diagram for Mixed Search for All Except the Last Device in Block 3**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

For Non-Enhanced Mode:

CYNSE10512A: CFG[63:0] = AAAAAAAAAAAAAAAAh;

CYNSE10256A: CFG[31:0] = AAAAAAAAh;

CYNSE10128A, CFG[15:0] = AAAAh.

NES = 10 (binary) in all blocks for Enhanced Mode, x288 search

HLAT = 000 (binary), TLSZ = 10 (binary), LRAM = 1 (binary), LDEV = 1 (binary).

**Figure 6-42. Timing Diagram for Mixed Search for the Last Device in Block 3**

The following is the sequence of operation for a single mixed-width Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = "10" (binary). The CMD[2] and CMD[9] signals must be driven to logic 0 for the 72-bit search, but for 144-bit search, CMD[9] = 1 and CMD [2] = 0. For 288-bit search, CMD[9] is don't care, whereas CMD[2] = 1 for the first "A" cycle and 0 for the last "A" cycle. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A by this device if it has a hit. If Enhanced Mode and MultiSearch Enable bits are both set to 1in the Command Resister, CMD[8] has to be set to 0 for Single Searches. For 288-bit and 576-bit Single Searches, all Cycle A CMD[8] bits have to be set to 0's.
  - **DQ Bus**: At the same time in cycle A, DQ[71:0] must be driven with the 72-bit data to be compared.
- **Cycle B**:
  - **Command Bus**: The host ASIC continues to drive CMDV HIGH and to apply Search command CMD[1:0] = "10" (binary). CMD[5:2] must now be driven by the index of the comparand register pair for storing the search key presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 27 for a description of SSR[0:7]). CMD[10:9] are don't cares for this cycle.
  - **DQ Bus**: The DQ[71:0] continues to carry the search key to be compared.

**Note**. For 72-bit searches, the host ASIC must supply the same 72-bit data on DQ[71:0] during both cycles A and B. Also, the even and odd pairs of GMRs selected for the comparison must be programmed with the same value. For 144-bit, 288-bit or 576-bit searches, each 72-bit presented on each cycle A and B will together form the 144-bit or 288-bit or 576-bit search key respectively.

When an N-bit search key, K, is presented on the DQ bus, the entire table of N-bit entries is compared to the search key using the GMR and local mask bits. The GMR is selected by the GMR Index in the command's cycle A. K is also stored in both even and odd comparand register pairs (selected by the comparand register index in command cycle B). K is compared with each entry in the table, starting at location 0. A matching entry that satisfies the Soft Priority and Mini-Key scheme (for Enhanced Mode) will be the winning entry, and its location address L will be driven as part of the SRAM address on the SADR[N:0] lines (see Section 6.7, "SRAM PIO Access," on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A. **Note**. The Learn command is supported for only one of the blocks consisting of up to eight devices in a depth-cascaded table of more than one block.

For up to 31 devices in the table (TLSZ = 10 (binary)), Search latency is 6 from command to SRAM access cycle. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 6-8*.

### *6.5.7 Mixed-size Multi Searches with 8 Devices on Tables Configured with Different Widths*

The multiple search operates the search commands in parallel on the upper half (array 0) and lower half (array 1) of the data array in the device. The results from the two parallel searches are then driven on the SRAM bus at twice that rate relative to single-search. The hardware diagram of the Search subsystem of up to eight devices is shown in *Figure 6-43* below.

***Note***:

- MultiSearch feature is only available in the Enhanced Mode, not in the Non-Enhanced Mode.
- When MultiSearch is enabled, the maximum number of devices that can be cascaded is 8 if CLK2x is less than or equal to 200 MHz. The number of devices will be 4 if CLK2x operates above 200 MHz but up to 266 MHz.
- Comparing the hardware diagrams shown in *Figure 6-10* and *Figure 6-43*, enabling MultiSearch does not mean that a board layout change is required. The LHO_1_L and LHI_1_L share the same pin with the Full In and Full Out signals, which are not shown in *Figure 6-10*. Cascading multiple devices together still allow the user to configure the devices through software to perform single-search or MultiSearch operations without any board change.
- All eight devices must be programmed with the same values for TLZ ("01" (binary)) and HLAT ("000" (binary) in this example). Only the last device in the table must be programmed with LRAM = 1 (binary) and LDEV = 1 (binary) (device 7 in this case). All other upstream devices must be programmed with LRAM = 0 (binary) and LDEV = 0 (binary) (devices 0 through 6 in this case).
- The device receiving all the LHO signals from the other devices is considered the last device.
- All the shared signals in the following timing diagrams showing tri-stated condition ("z") indicate that, that particular device is not driving the shared signals. The shared signals are not three-stated in a real life because other devices will be driving them.
- Comparing the hardware diagrams shown in *Figure 6-10* and *Figure 6-43*, enabling MultiSearch does not mean that a board layout change is required. The LHO_1_L and LHI_1_L share the same pin with the Full In and Full Out signals, which are not shown in *Figure 6-10*. Cascading multiple devices together still allow the user to configure the devices through software to perform single-search or MultiSearch operations without any board change.

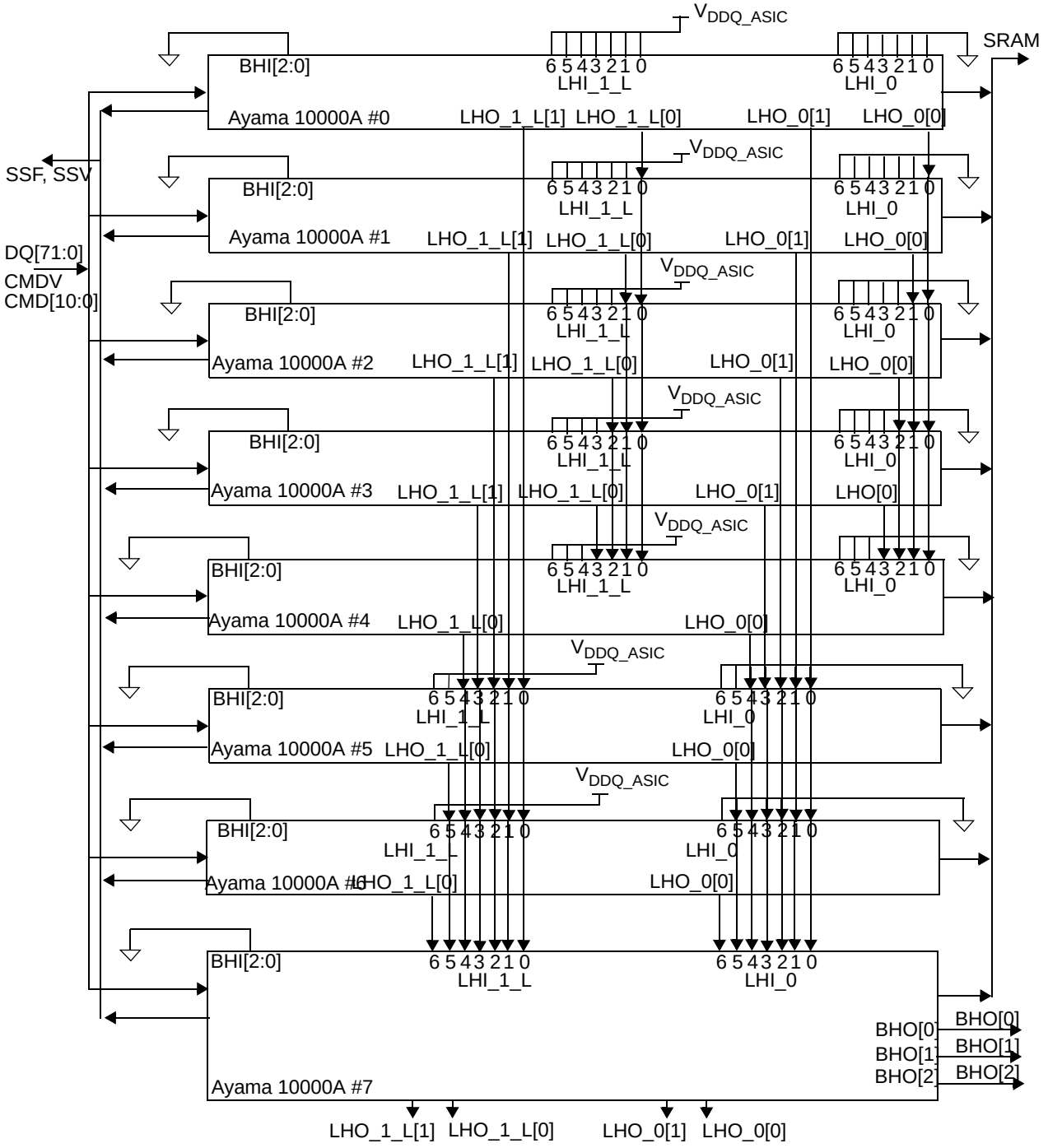



**Figure 6-43. Hardware Diagram for a Table with Eight Devices for MultiSearch**

**Notes**:

- In MultiSearchMode, there is a separate set of the LHO and LHI signals corresponding to memory array 0 and array 1. LHO_0[1:0] and LHI_0[6:0] corresponds to array 0 whereas LHO_1_L[1:0] and LHI_1_L[6:0] corresponds to array 1. The latter share the same pins as FULO[1:0] and FULI[6:0] respectively.
- Both LHO_0[1] and LHO_0[0] are exact same signals so that the loads can be shared by two outputs. The same is true for LHO_1_L[1] and LHO_1_L[0].
- Unused LHI_0 signals should be tied to ground whereas unused LHI_1_L signals should be tied to $V_{DDQ\_ASIC}$, which is either 1.8V or 2.5V only.

- LHI_1_L signals are active LOW while LHI_0 are active HIGH.

The MultiSearch Enable (MSE) bit in the Command Register must be set HIGH when the Command Register is programmed. The same with the Enhanced Mode (EMODE) bit.

The sample operation shown is for 8-device-cascade, with devices 0 and 1 containing x72 tables (NES = 00 (binary) in all blocks), devices 2 and 3 containing x144 tables (NES = 01 (binary) in all blocks), and devices 4 to 7 containing x288 tables (NES = 10 (binary) in all blocks). The following figures show three sequential searches:

1. A 72-bit - 72-bit MultiSearch
2. A144-bit - 144-bit MultiSearch
3. A288-bit - 288-bit MultiSearch.

The hardware connection of the 8 cascaded devices is shown in *Figure 6-43*. A graphical representation of the tables is shown in *Figure 6-44* using CYNSE10512As as an example.

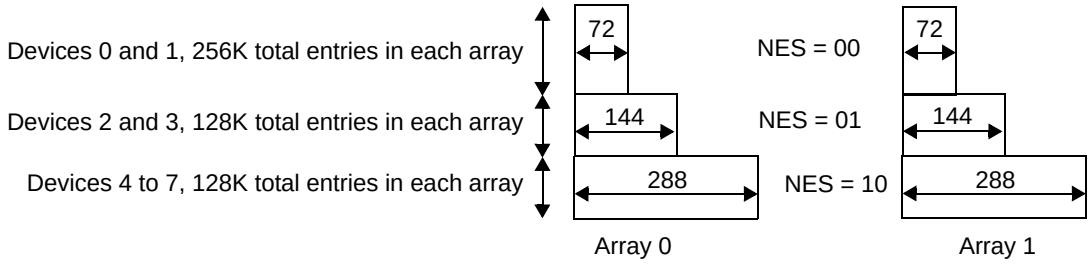
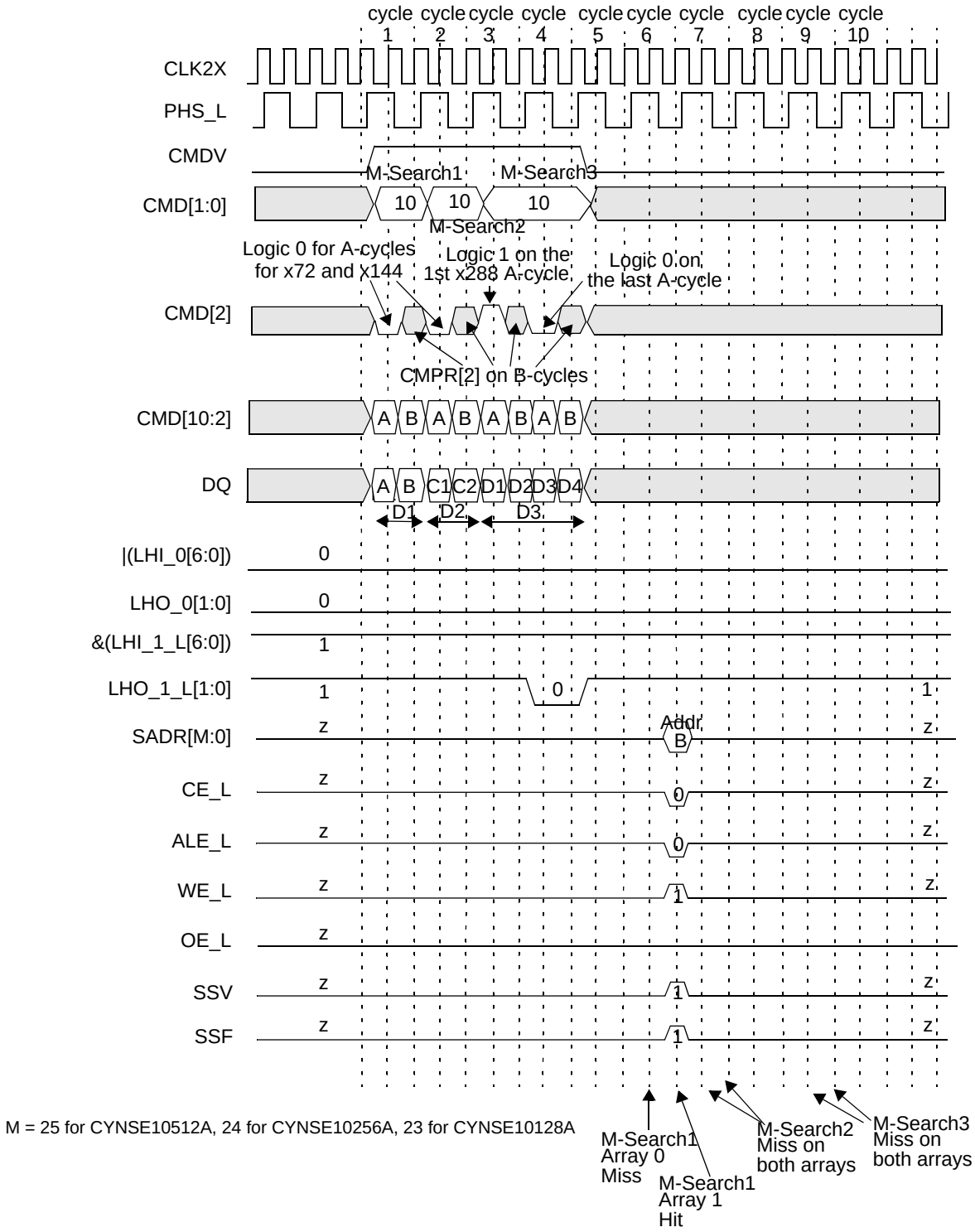



**Figure 6-44. Multiwidth Configurations Example for MultiSearch with CYNSE10512As**

- The timing diagrams below correspond to the Hit/Miss assumptions defined in *Table 6-13*.

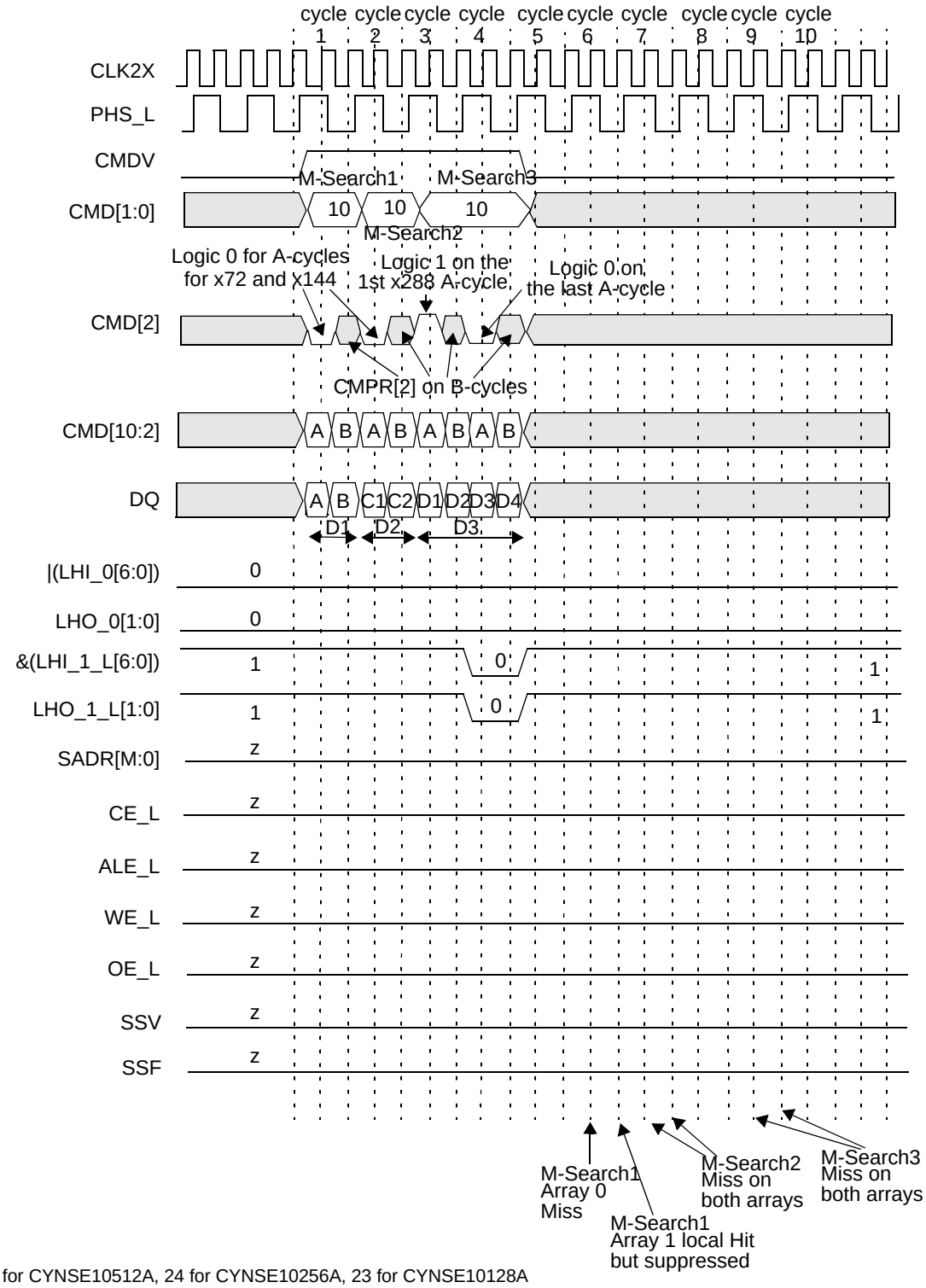
**Table 6-13. Hit/Miss Assumptions in MultiSearchMode**

| Search Number | #1 (x72–x72) | | #2 (x144–x144) | | #3 (x288–x288) | |
|---|---|---|---|---|---|---|
| Device 0 | Miss | Hit | Miss | Miss | Miss | Miss |
| Device 1 | Miss | Hit | Miss | Miss | Miss | Miss |
| Device 2 | Miss | Miss | Miss | Hit | Miss | Miss |
| Device 3 to 6 | Miss | Miss | Miss | Miss | Miss | Miss |
| Device 7 | Miss | Miss | Miss | Miss | Hit | Miss |




NES = 00 (binary) in all blocks for Enhanced Mode, x72 search.
HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-45. Timing Diagram for Mixed MultiSearch (Eight Devices) for Device 0**

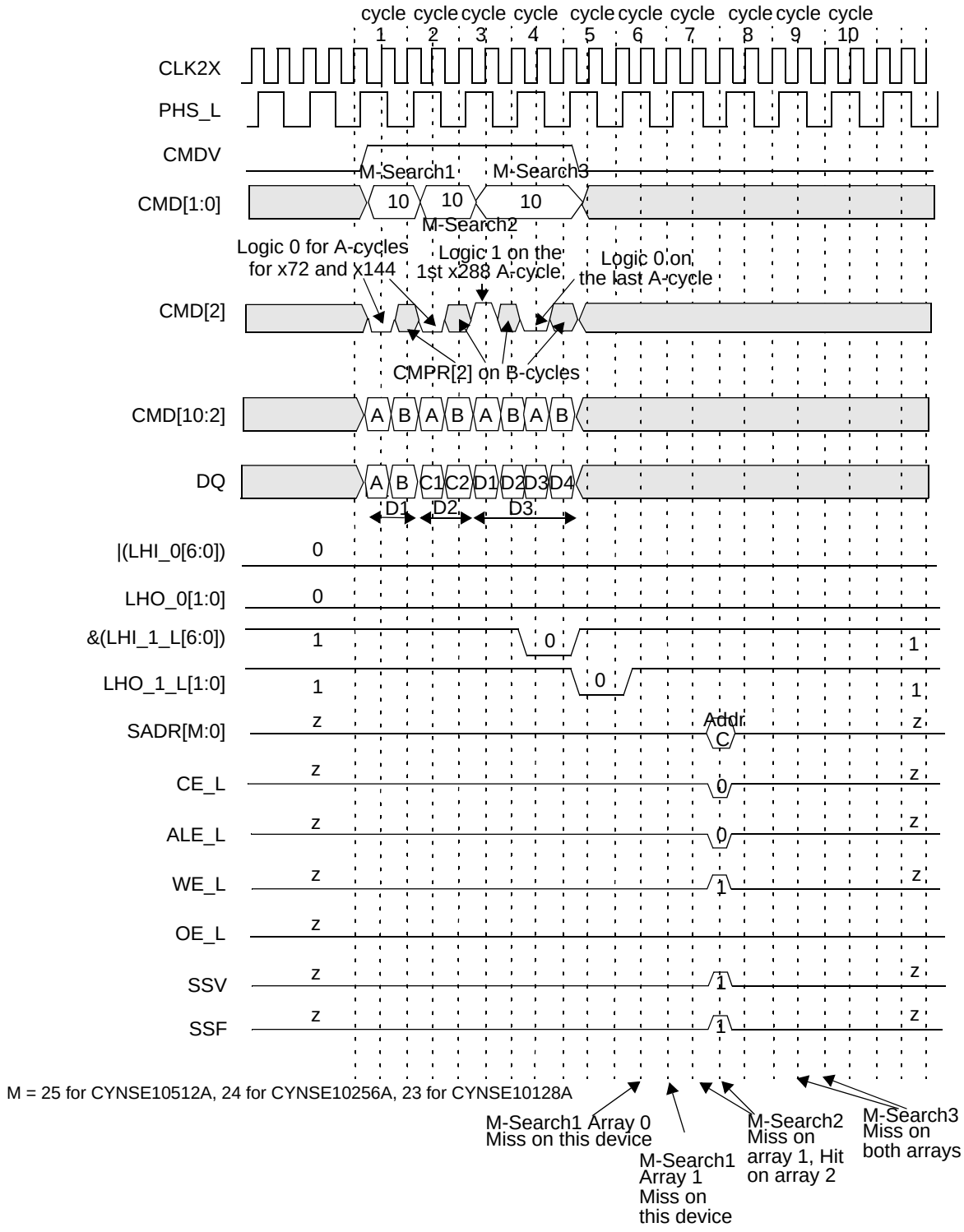



M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

NES = 00 (binary) in all blocks for Enhanced Mode, x72 search.

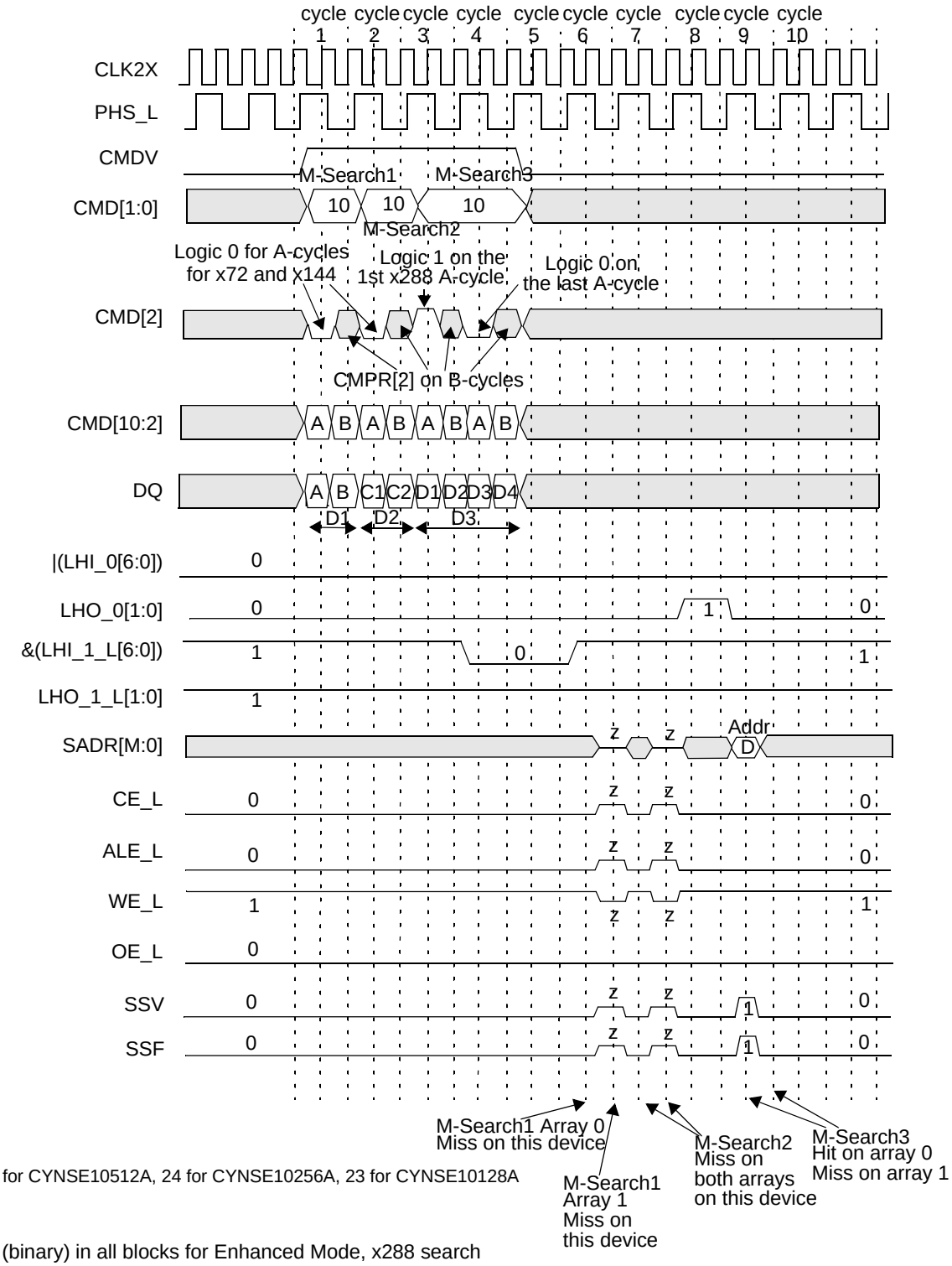
HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-46. Timing Diagram for Mixed MultiSearch (Eight Devices) for Device 1**




NES = 01 (binary) in all blocks for Enhanced Mode, x144 search.
HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-47. Timing Diagram for Mixed MultiSearch (Eight Devices) for Device 2**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

NES =10 (binary) in all blocks for Enhanced Mode, x288 search
HLAT = 000 (binary), TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary).

**Figure 6-48. Timing Diagram for Mixed MultiSearch (Eight Devices) for Device 7**

The MSE bit in the Command Register must be set high to enable the MultiSearch feature. The same with the Enhanced Mode (EMODE) bit. The following is the sequence of operation for a single mixed-width Search command (also refer to *Subsection 6.2, "Command Bus Parameters," on page 50*).

- **Cycle A**:
  - **Command Bus**: The host ASIC drives CMDV HIGH and applies Search command CMD[1:0] = "10" (binary). The CMD[2] and CMD[9] signals must be driven to logic 0 for the 72-bit search, but for 144-bit search, CMD[9] = 1 and CMD [2] = 0. For 288-bit search, CMD[9] is don't care, whereas CMD[2] = 1 for the first "A" cycle and 0 for the last "A" cycle. {CMD[10],CMD[5:3]} signals must be driven with the index to the GMR pair for use in this Search operation. CMD[7:6] signals must be driven with the same bits that will be driven on SADR[24:23] for CYNSE10512A, SADR[23:22] for CYNSE10256A, SADR[22:21] for CYNSE10128A by this device if it has a hit. CMD[8] must be set high for MultiSearch operation. Note, CMD[8] must be driven low for all Cycle A's of Single Search operations if MSE = 1 in CMD Register.
  - **DQ Bus**: At the same time in cycle A, DQ[71:0] must be driven with the 72-bit data to be compared.
- **Cycle B**:
  - **Command Bus**: The host ASIC continues to drive CMDV HIGH and to apply Search command CMD[1:0] = "10" (binary). CMD[5:2] must now be driven by the index of the comparand register pair for storing the search key presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 27 for a description of SSR[0:7]). CMD[10:9] are don't cares for this cycle.
  - **DQ Bus**: The DQ[71:0] continues to carry the search key to be compared.

**Notes**.

1. For 72-bit leading + 72-bit trailing Multisearches, the host ASIC can supply different 72-bit data on DQ[71:0] during both cycles A and B to be compared with the tables in array 0 and 1 of the data array. The even and odd pairs of GMRs selected for the comparison need not be programmed with the same value.
2. For all other Multisearch commands that contain a 72-bit trailing search, you must pay special attention to which part of the entire search key is used for the 72-bit trailing search. An example of this situation is illustrated in M-search 2 and M-search 3 in *Figure 6-7*. M-search 2 is a 144-bit leading search on Array 0 plus a 72-bit trailing search on Array 1. Notice that the Y2 portion of the entire key is used during the 72-bit search. A different behavior is observed for a leading search in Array 1 instead of Array 0. M-search 3 is a 288bit leading search on Array 1 plus a 72-bit trailing search on Array 0. In this example, Z3 is used as the 72-bit key for the trailing 72-bit search. The difference between M-search 2 and M-search 3 is the trailing 72-bit search (Array 0 and Array 1 respectively). This behavior is summarized as follow:
   - 72-bit trailing search on Array 0: Data on DQ during the last Cycle A of the entire Search command will be used as search key
   - 72-bit trailing search on Array 1: Data on DQ during the last Cycle B of the entire Search command will be used as search key
3. For all other Multisearches, the N-bit search key used for the N-bit trailing search is simply the last N-bits presented on the DQ bus when the Multisearch command is issued.
4. GMR and CPR selection also deserve special attention, please see *Section 5.1.2.4* for details.
5. A matching entry from each array that satisfies the Soft Priority and Mini-Key scheme will be the winning entries, and their location addresses La and Lb will be driven as part of the SRAM address on the SADR[N:0] lines (see Section 6.7, "SRAM PIO Access," on page 113), N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A.
6. Reading CMPR registers after Multisearches: You can only do this if your leading and trailing searches are of same width.
7. Learning from CMPR is only supported if your leading and trailing searches are of same width.

The latency of the MultiSearch from command to SRAM access cycle is 5 for a configuration of up to eight devices (TLSZ = 01 (binary)). SSV and SSF also shift further to the right for different values of HLAT, as specified in *Table 6-8*.

## 6.6 Learn Command

The device contains sixteen pairs of Comparand (CMPR) registers that store the search key as the device executes searches.

On a Search miss, signalled to the ASIC through the SSV and SSF signals (SSV = 1 (binary), SSF = 0 (binary)), the host ASIC can apply the Learn command to learn the entry from a CMPR register to the next-free location. However, it is recommended that the host ASIC first check the FULL signal, to determine if the device is full. If the device is not full, and the Search was a miss, a Learn can be applied. If the device is already full, and the Learn is issued, the operation will be suppressed. The Learn Command latency is calculated from the first cycle after the learn is issued. Irrespective of the width of the learn, the latency of the SADR bus is calculated to be 5+TLSZ after the first cycle. This calculation is shown in *Table 6-14*, which shows latency values for different learn widths after each of the commands are issued.

**Table 6-14. Latency of SADR for different learn widths**

| Learn-key widths | Latency of SADR field in CLK1X cycles |
|---|---|
| x72 | 5+TLSZ |
| x144 | 5+TLSZ |
| x288 | 4+TLSZ |
| x576 | 2+TLSZ |

The Learn command is a pipelined operation and lasts for two CLK cycles. *Figure 6-53*, *Figure 6-54* and *Figure 6-55* show the timing diagram of Learn operations with the address taken from the NFA or SRR register. *Figure 6-54* and *Figure 6-55* assume that the device performing the Learn operation is not the last device in the table and will therefore have its LRAM bit set to 0. The OE_L for the device with the LRAM bit set goes HIGH for two cycles for each Learn (one during the SRAM Write cycle and one during the cycle before). The SRAM Write cycle latency from the second cycle of the instruction is shown in *Table 6-15*. The Learn command also generates a Write cycle to the external SRAM (see Section 6.7, “SRAM PIO Access,” on page 113).

Note that mismatched entry-width Learn operation is not supported. For example, the result of a 72-bit Search miss stored in one of the SRR registers cannot be used for a 144-bit Learn operation.

### *6.6.1 Non-Enhanced Mode*

The Learn command in the Non-Enhanced mode supports x72 and x144 table widths. The operation uses the data stored in the user selected CMPR register for writing to an entry in the Data array. Non-Enhanced mode Learn operation ignores the DQ bus and cannot perform a write to the Mask array. The address for the target data entry is the INDEX field of the Next-free Address (NFA) register.

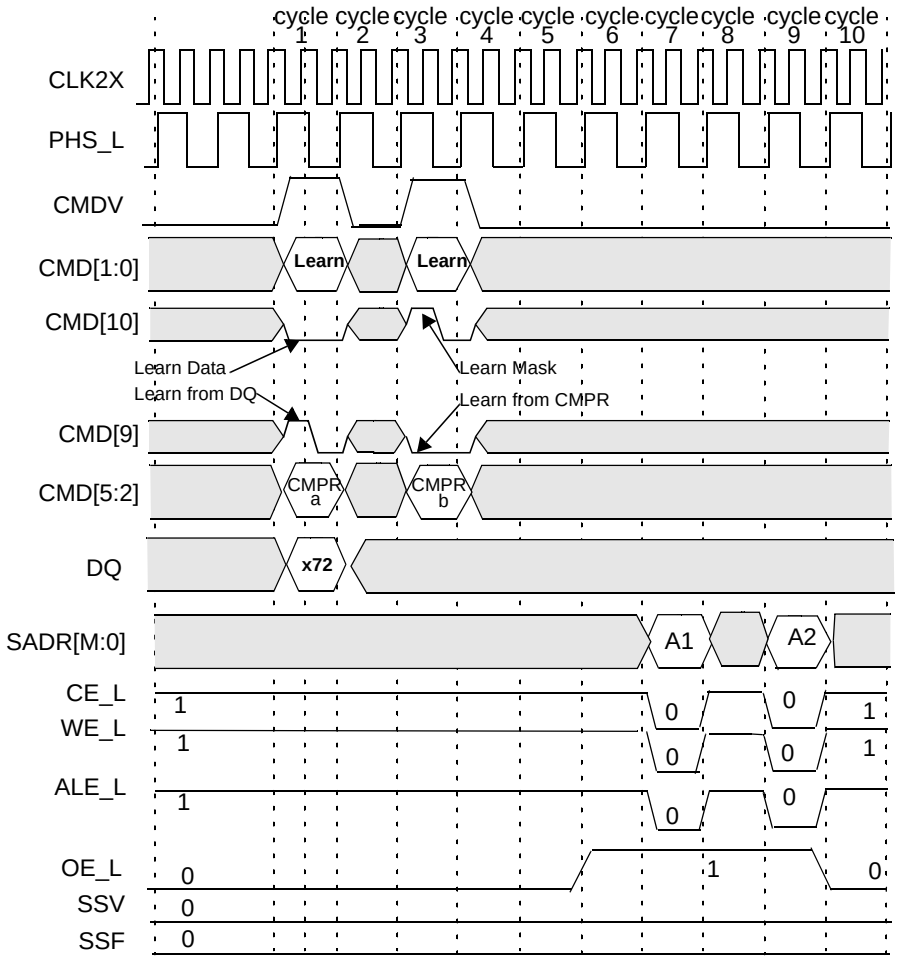
Once the operation is completed the NFA register’s INDEX field is updated with next highest priority free entry in the Data array. The LSB of each x72 entry is treated as a valid bit and used to indicate whether that entry is free (=0 (binary)) or not (=1 (binary)). For a 144-bit entry, bit [72] and bit[0] must be set to the same value.

Note that Learn command for x144 entry width in Non-Enhanced can only be issued when all the tables in the device is of x144 table width.

### *6.6.2 Enhanced Mode*

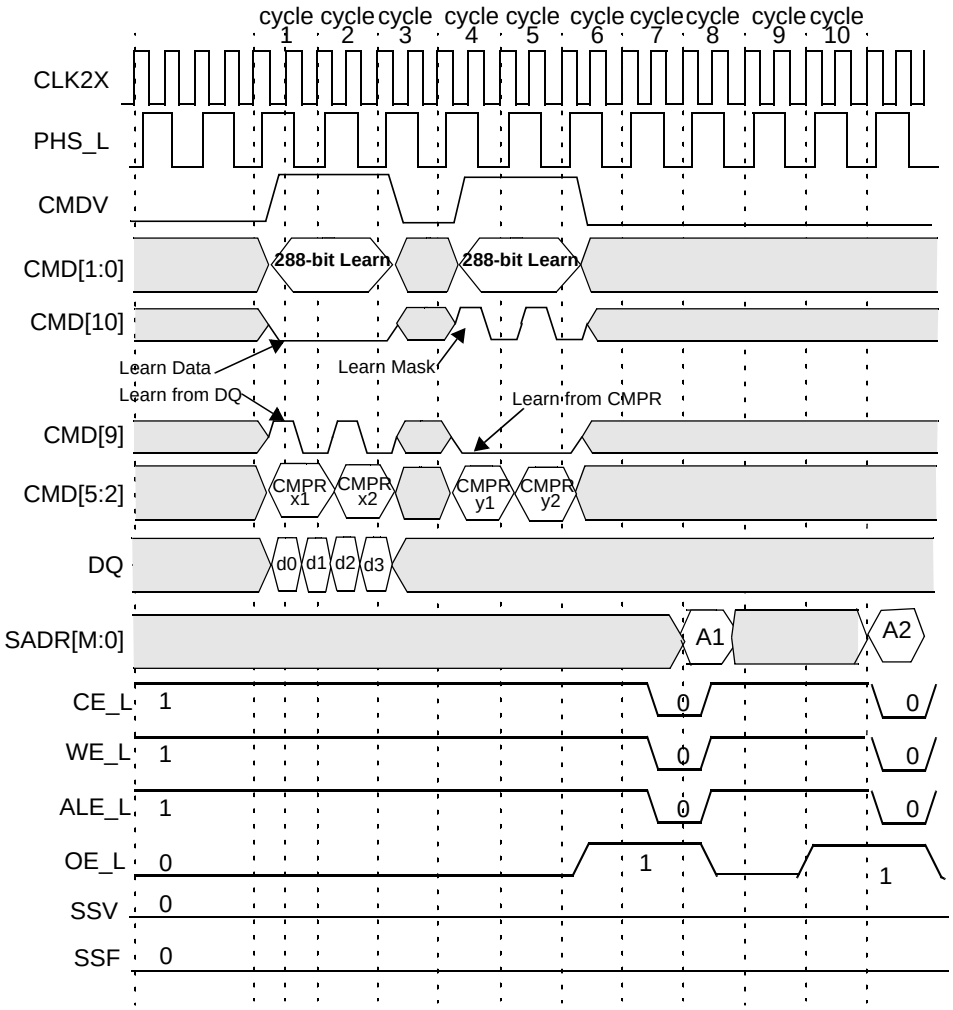
The Learn command in the Enhanced mode supports all table widths (x72, x144, x288 and x576). The user can select whether the data stored in the user selected CMPR register or the data presented in the DQ bus be used for the learn operation. The user can also select to write to an entry in either the Data or Mask array. The address for the target entry is the INDEX field of the user-selected Search Result Register (SRR). Each SRR is one-to-one associated to a Comparand (CMPR) register. So the selection of the SRR is accomplished by selecting the corresponding (CMPR) register.

The SRR register is updated after a Search operation. Only the LSB of each entry is used, regardless of width, to indicate whether that entry is free (=0 (binary)) or not (=1 (binary)).



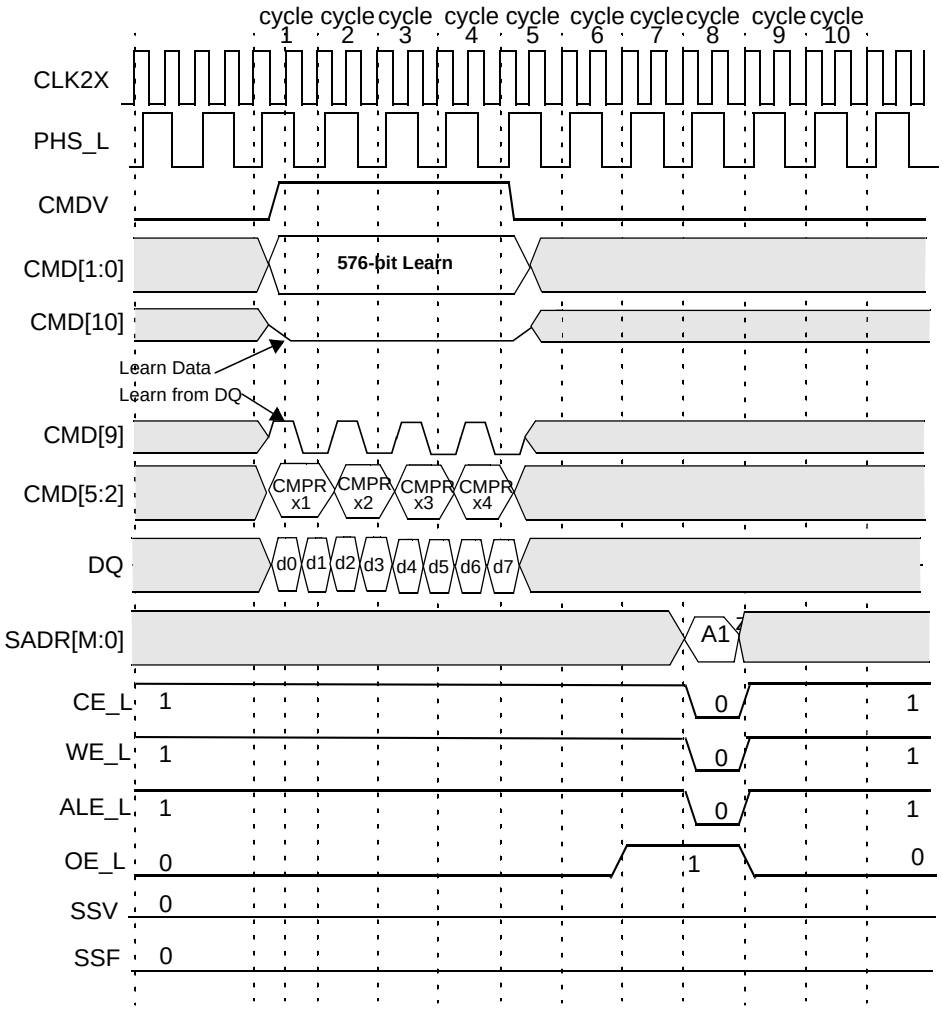

TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-49. Timing Diagram of 72-bit Learn from DQ Bus and CMPR Registers (One Device)**



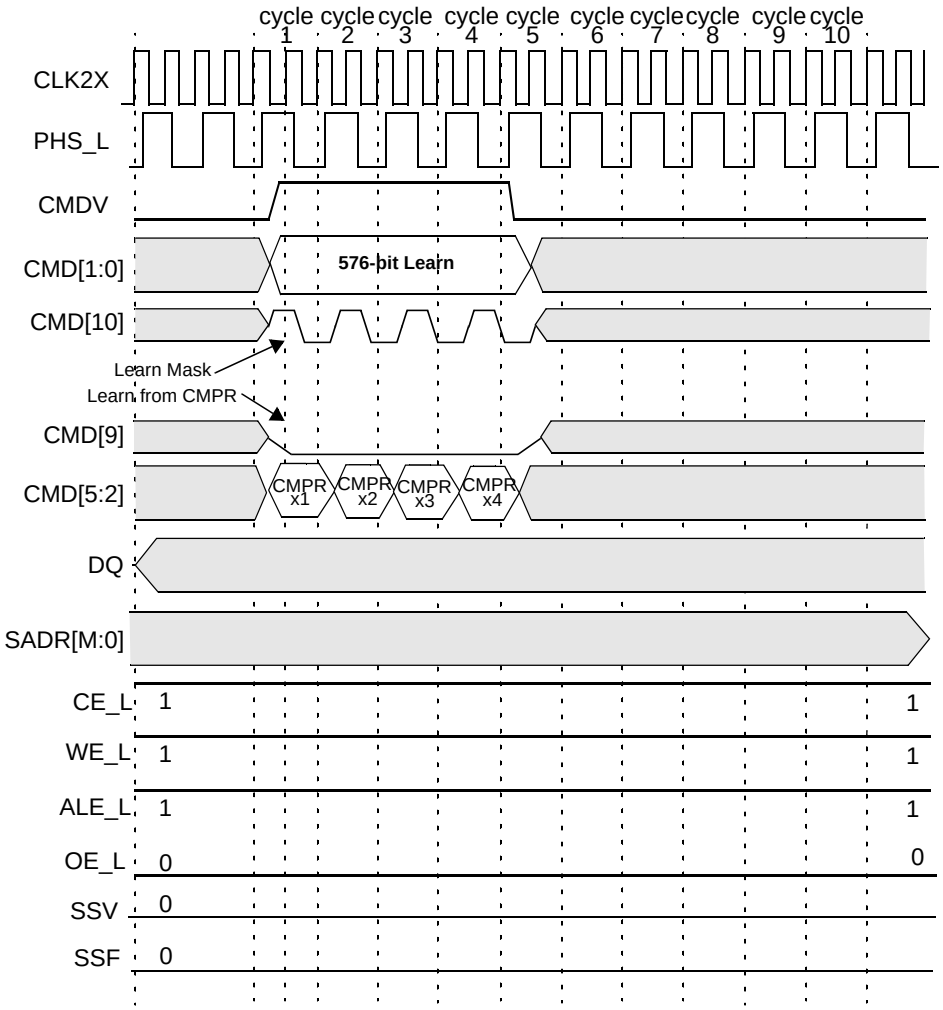

TLSZ = 10 (binary), LRAM = 1 (binary), LDEV = 1 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-50. Timing Diagram of 288-bit Learn from DQ Bus and CMPR Registers (One Device)**




TLSZ = 10 (binary), LRAM = 1 (binary), LDEV = 1 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-51. Timing Diagram of 576-bit Learn from DQ Bus (One Device)**




TLSZ = 10 (binary), LRAM = 1 (binary), LDEV = 1 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

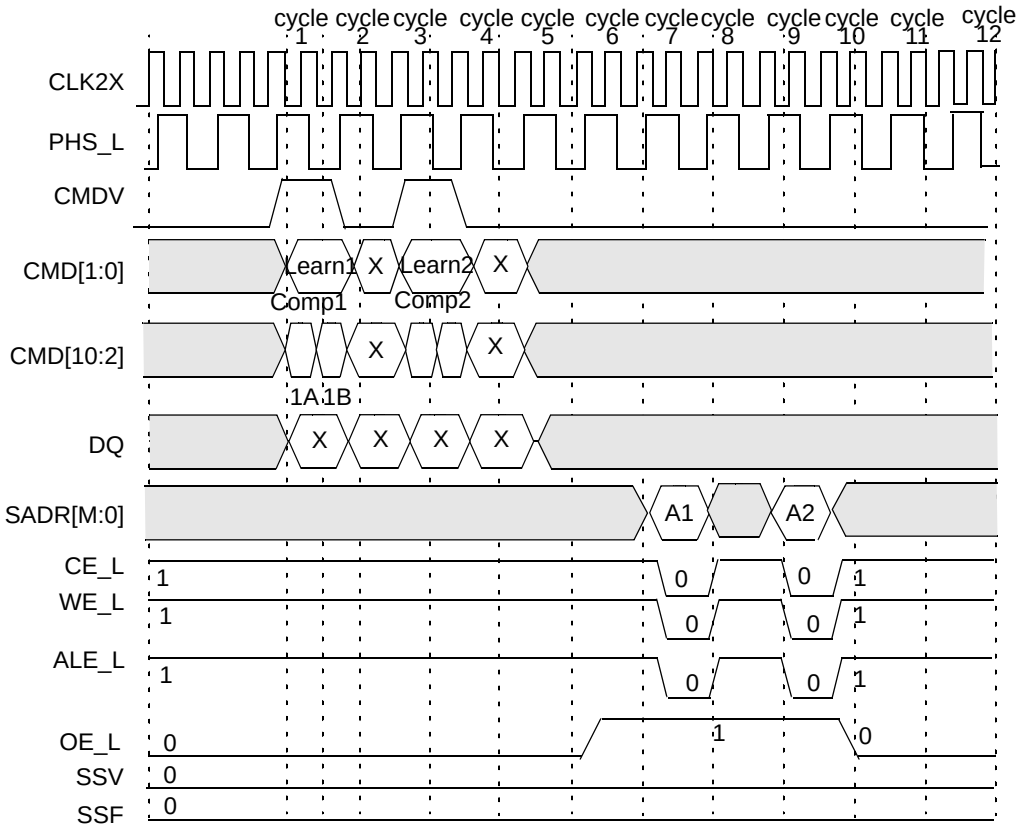
**Figure 6-52. Timing Diagram of 576-bit Learn from CMPR Register (One Device)**

### *6.6.3 Learn Operation on Depth-Cascaded Table*

When all entries in a device are occupied, the device asserts FULO to inform the downstream devices that it is full. The result of this communication between depth-cascaded devices determines the global FULL signal for the entire table. The FULL signal in the last device determines the fullness of the depth-cascaded table.

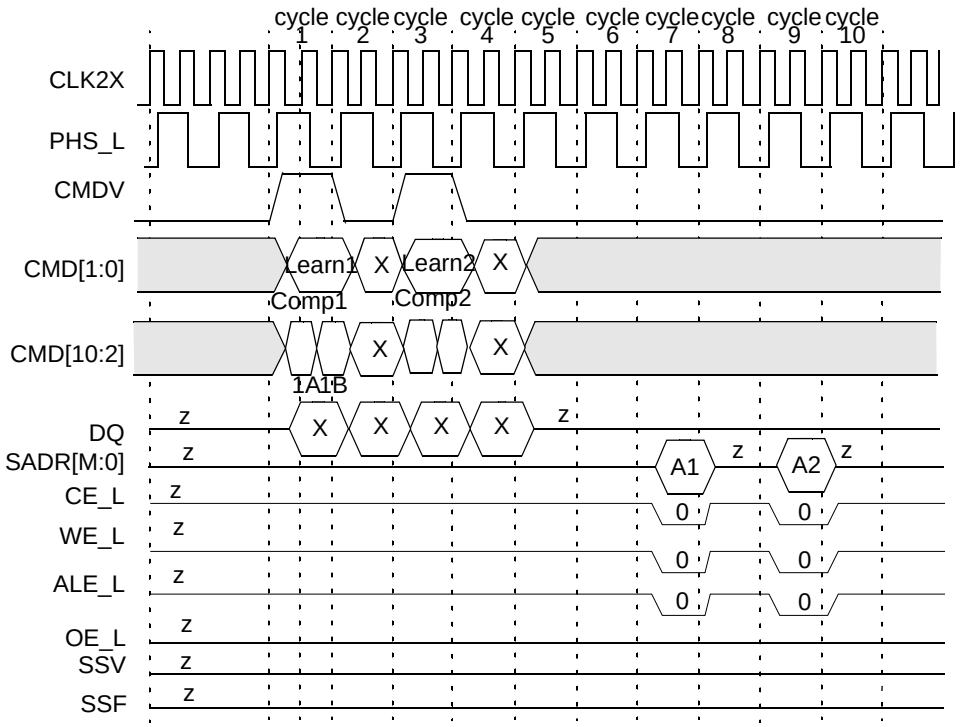
In a depth-cascaded table, only a single device will Learn the entry through the application of a Learn instruction. The determination as to which device will Learn is based on the FULI and FULO signals between the devices. The first non-full device learns the entry by storing the content of the selected CMPR register to the location pointed to by the NFA or SRR register.

The global FULL signal indicates to the table controller (the host ASIC) that all entries within a block are occupied and that no more entries can be learned. The Ayama 10000A device updates the signal after each Write or Learn command to a data array.



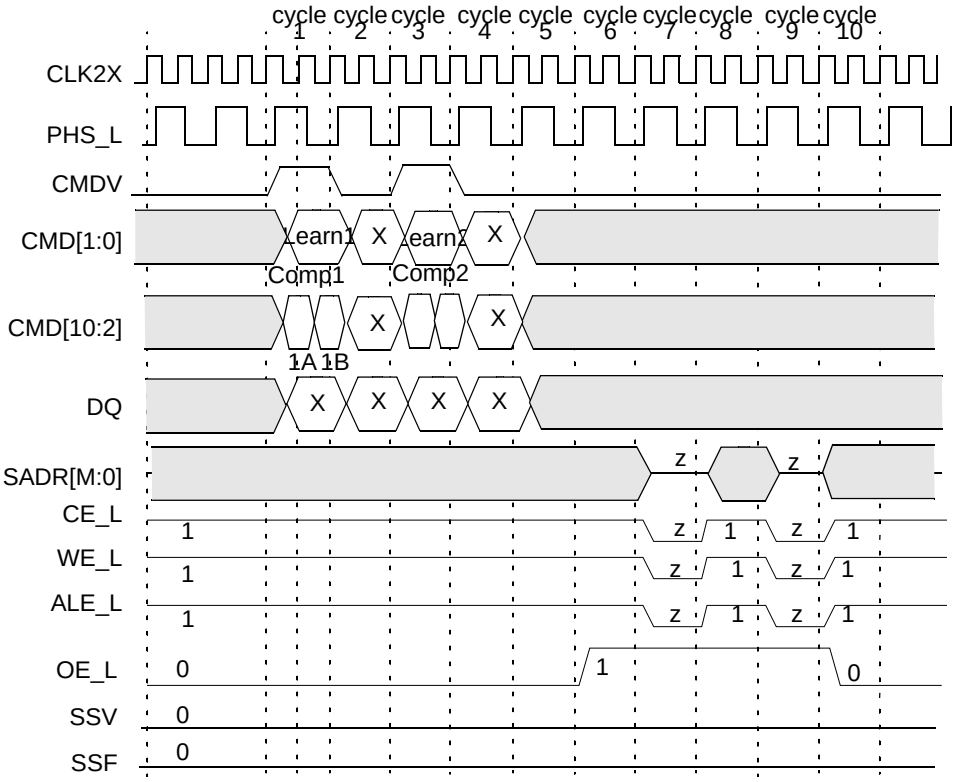

TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-53. Timing Diagram of Learn**




TLSZ = 01 (binary), LRAM = 0 (binary), LDEV = 0 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-54. Timing Diagram of Learn (Except on the Last Device [TLSZ = 01 (binary)])**




TLSZ = 01 (binary), LRAM = 1 (binary), LDEV = 1 (binary). M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-55. Timing Diagram of Learn on Device Number 7 (TLSZ = 01 (binary))**

**Table 6-15. SRAM Write Cycle Latency from Second Cycle of Learn Instruction**

| Number of Devices | Latency in CLK Cycles |
|---|---|
| 1–8 (TLSZ = 01 (binary)) | 5 |
| 1–31 (TLSZ = 10 (binary)) | 6 |

The Learn operation lasts two CLK cycles. The sequence of operation is as follows.

- **Cycle 1A**: The host ASIC applies the Learn instruction on CMD[1:0] using CMDV = 1 (binary). The CMD[5:2] field specifies the index of the comparand register pair that will be written in the data array in the 144-bit-configured table. For a Learn in a 72-bit-configured table, the even-numbered comparand specified by this index will be written. CMD[8:6] carries the bits that will be driven on SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A in the SRAM Write cycle.
- **Cycle 1B**: The host ASIC continues to drive CMDV to 1 (binary), CMD[1:0] to 11 (binary), and CMD[5:2] with the comparand pair index. CMD[6] must be set to 0 if the Learn is being performed on a 72-bit-configured table, and to 1 if the Learn is being performed on a 144-bit-configured table.
- **Cycle 2**: The host ASIC drives CMDV to 0.

At the end of cycle 2, a new instruction can begin. SRAM Write latency is the same as the Search to the SRAM Read cycle. It is measured from the second cycle of the Learn instruction.

## 6.7 SRAM PIO Access

SRAM Read enables read access to the off-chip SRAM containing associative data. The latency from the issuance of the Read instruction to the appearance of the address on the SRAM bus is the same as the Search instruction latency, and will depend on the value programmed for the TLSZ parameter in the device configuration register. The latency of the ACK from the Read instruction is the same as that from the Search instruction to the SRAM address latency, plus the HLAT programmed in the configuration register.

**Note**: SRAM Read is a blocking operation—no new instruction can begin until the ACK is returned by the selected device performing the access.

SRAM Write enables write access to the off-chip SRAM containing associative data. The latency from the second cycle of the Write instruction to the appearance of the address on the SRAM bus is the same as the Search instruction latency, and will depend on the TLSZ value parameter programmed in the device configuration register.

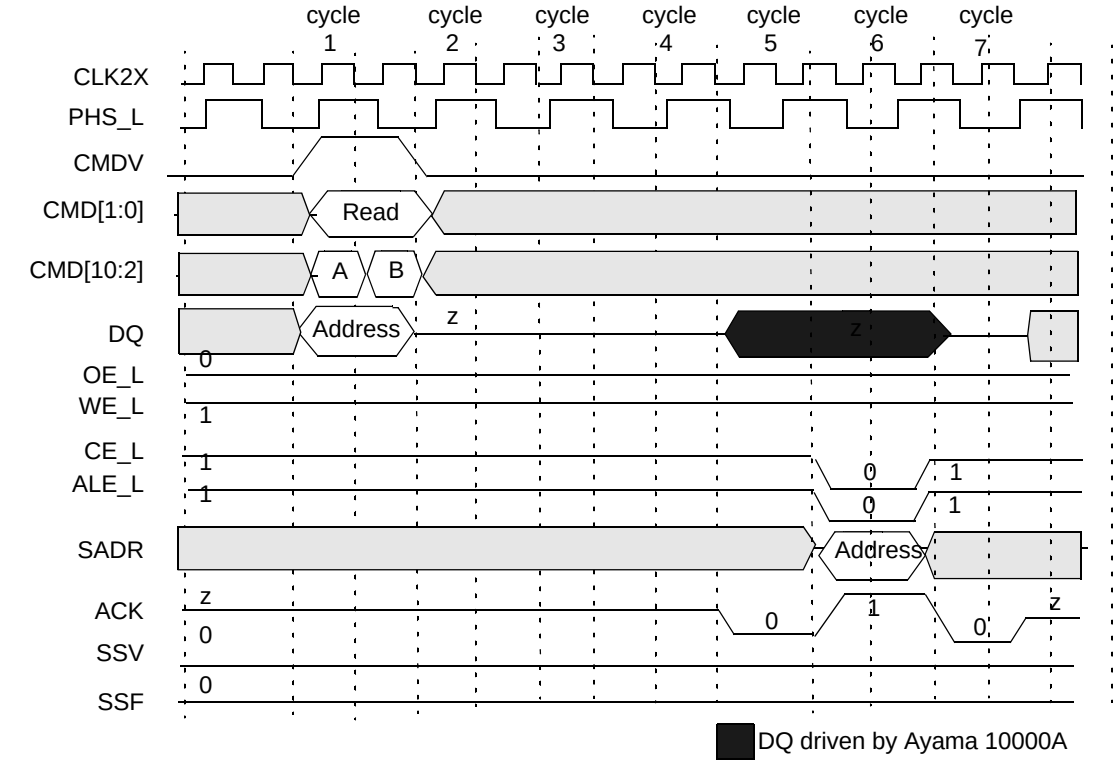
**Note**: SRAM Write is a pipelined operation—new instruction can begin right after the previous command has ended.

### *6.7.1 SRAM Read with a Table of One Device*

SRAM Read enables read access to the off-chip SRAM containing associative data. The latency from the issuance of the Read instruction to the appearance of the address on the SRAM bus is the same as Search instruction latency, and will depend on the TLSZ value parameter programmed into the device configuration register. ACK latency from the Read instruction is the same as that from the Search instruction to the SRAM address, plus the HLAT programmed in the configuration register. The following explains the SRAM Read operation in a table with only one device that has the following parameters: TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 1 (binary), and LDEV = 1 (binary). *Figure 6-56* shows the associated timing diagram. For the following description, the selected device refers to the only device in the table because it is the only device to be accessed.

- **Cycle 1A**: The host ASIC applies the Read instruction on CMD[1:0] using CMDV = 1 (binary). The DQ bus supplies the address, with DQ[20:19] set to 10 (binary), to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction on CMD[1:0] using CMDV = 1 (binary). The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[71:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[71:0] in a three-state condition.
- **Cycle 4**: The host ASIC keeps DQ[71:0] in a three-state condition.
- **Cycle 5**: The selected device starts to drive DQ[71:0] and drives ACK from High-Z to LOW.
- **Cycle 6**: The selected device drives the Read address on SADR[N:0] lines (N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A) and drives ACK HIGH, CE_L LOW, and ALE_L LOW.
- **Cycle 7**: The selected device drives CE_L HIGH, ALE_L HIGH, the SADR bus, the DQ bus in a three-state condition, and ACK LOW.

At the end of cycle 7, the selected device floats ACK in a three-state condition, and a new command can begin.




TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 1 (binary), LDEV = 1 (binary)

**Figure 6-56. SRAM Read Access**

### *6.7.2 SRAM Read with a Table of up to Eight Devices*

The following explains the SRAM Read operation completed through a table of up to eight devices using the following parameter: TLSZ = 01 (binary). *Figure 6-57* diagrams a block of eight devices. The following assumes that SRAM access is successfully achieved through Ayama 10000A device number 0. *Figure 6-58* and *Figure 6-59* show timing diagrams for device number 0 and device number 7, respectively.

- **Cycle 1A**: The host ASIC applies the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. During this cycle the host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction on CMD[1:0], using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[71:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[71:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[71:0].
- **Cycle 5**: The selected device continues to drive DQ[71:0] and drives ACK from High-Z to LOW.
- **Cycle 6**: The selected device drives the Read address on SADR[N:0] lines (N = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A) and drives ACK HIGH, CE_L LOW, WE_L HIGH, and ALE_L LOW.
- **Cycle 7**: The selected device drives CE_L, ALE_L, WE_L, and the DQ bus in a three-state condition. It continues to drive ACK LOW.

At the end of cycle 7, the selected device floats ACK in a three-state condition. A new command can begin.

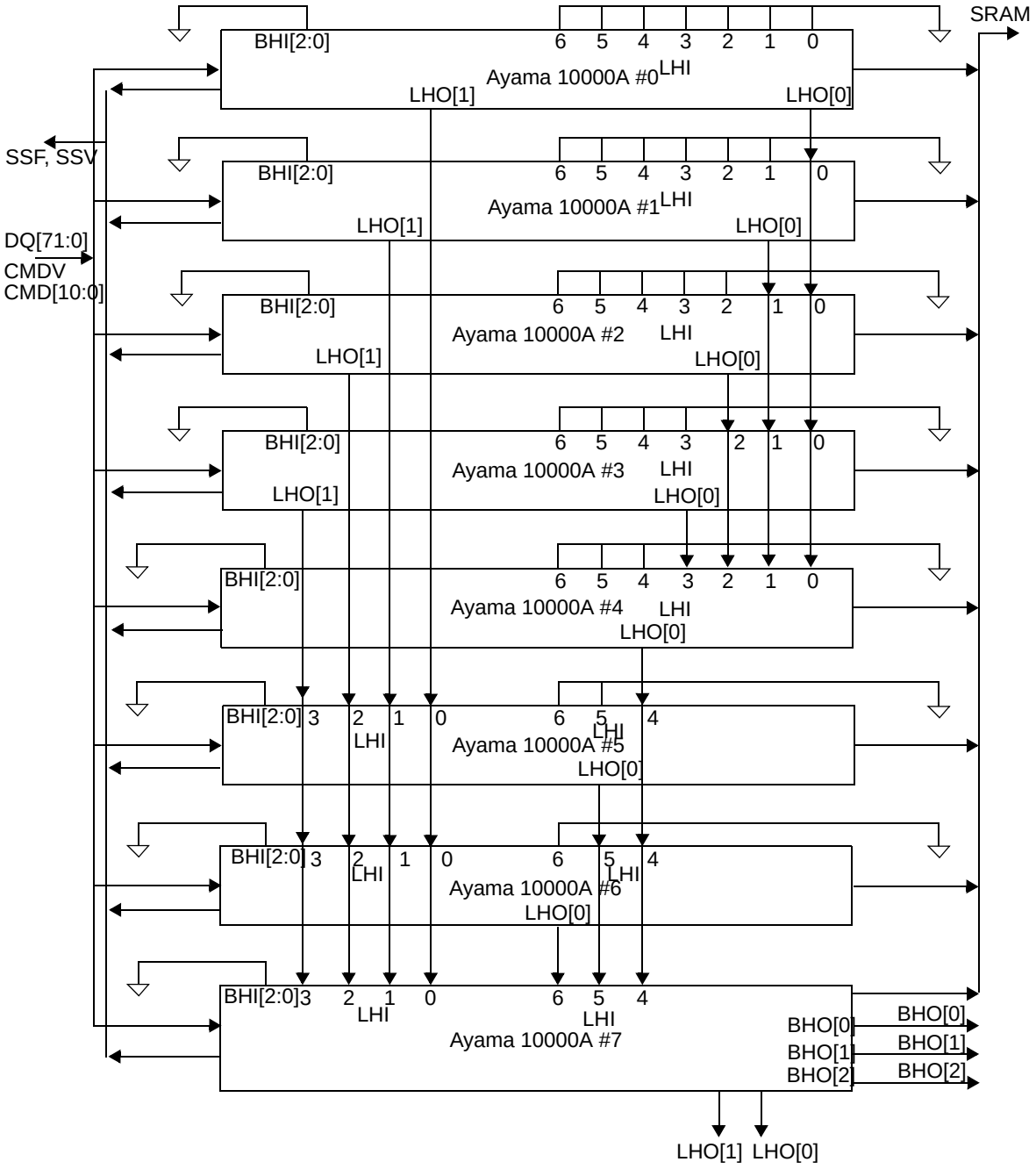
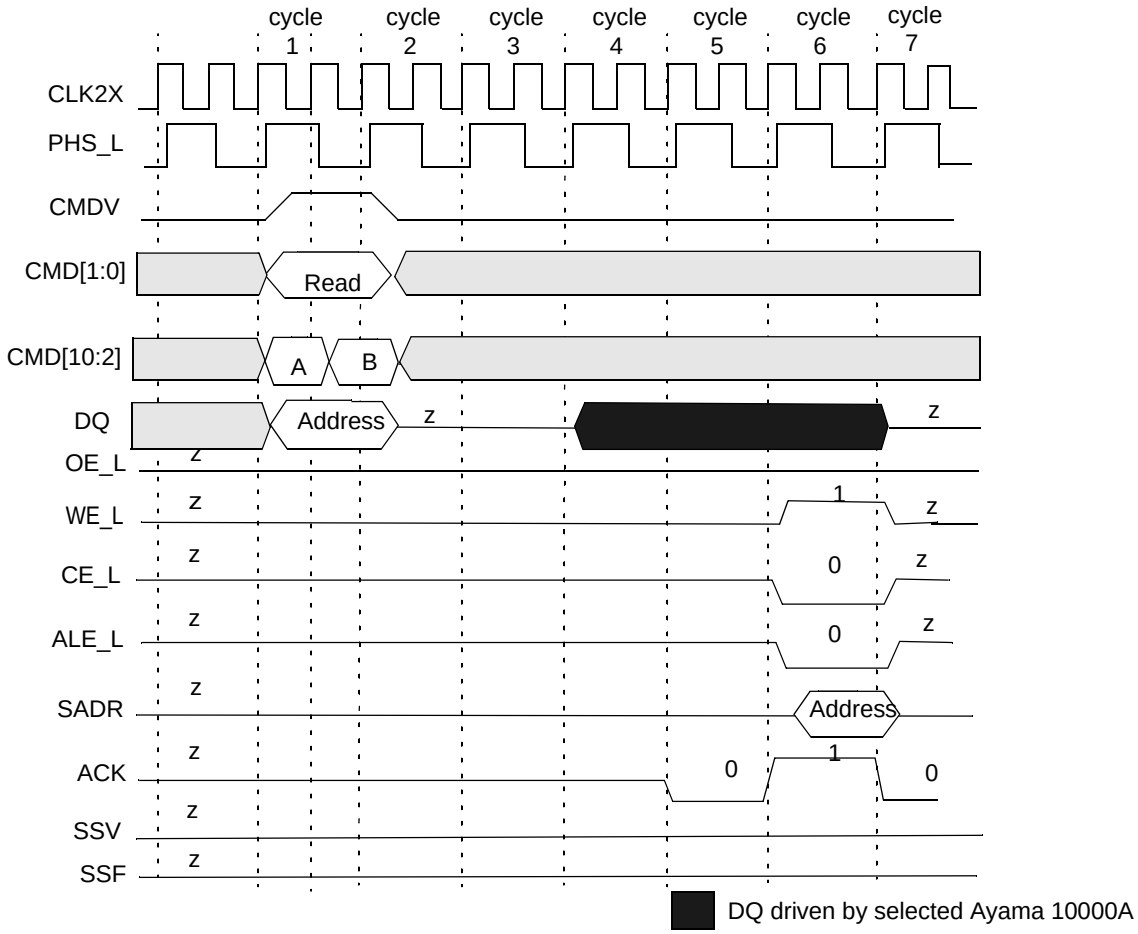
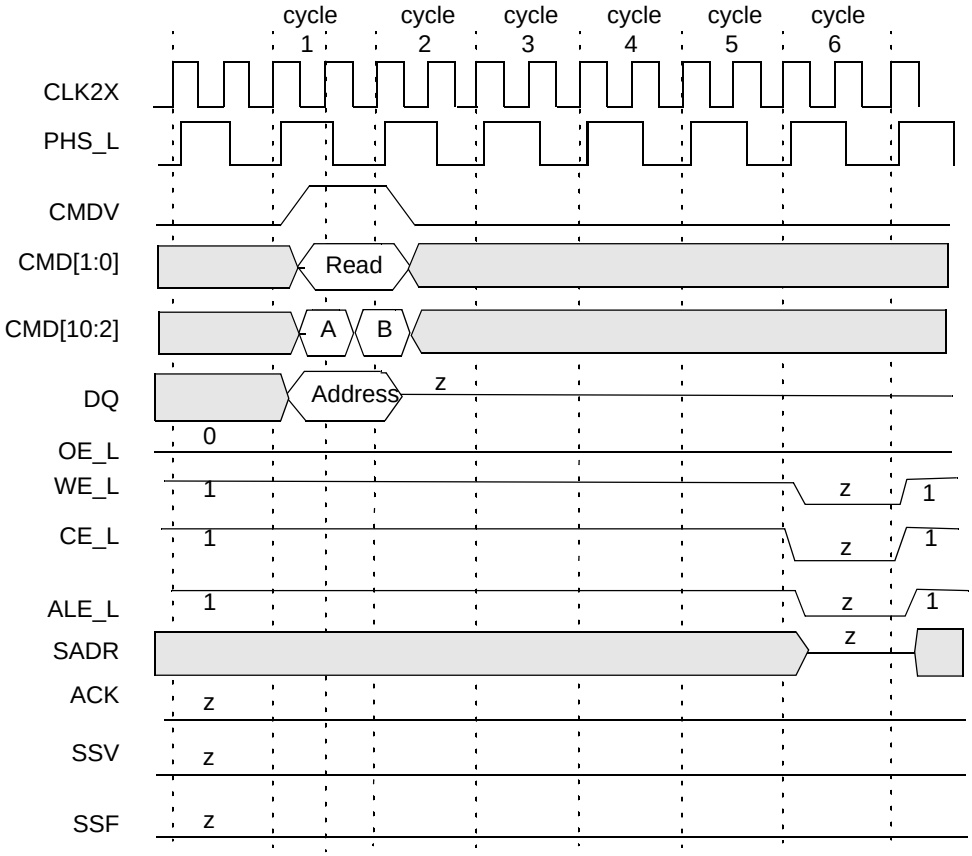



**Figure 6-57. Hardware Diagram of a Block of Eight Devices**




TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 0 (binary), LDEV = 0 (binary)

**Figure 6-58. SRAM Read of Device #0 in a Block of Eight Devices**




TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 1 (binary), LDEV = 1 (binary)

**Figure 6-59. SRAM Read Timing of Device #7 in a Block of Eight Devices**

### *6.7.3 SRAM Read with a Table of up to 31 Devices*

The following explains the SRAM Read operation accomplished through a table of up to 31 devices, using the following parameter: TLSZ = 10 (binary). The hardware diagram is shown in *Figure 6-60*. The following assumes that SRAM access is being accomplished through Ayama 10000A device number 0, and that device number 0 is the selected device. *Figure 6-61* and *Figure 6-62* show the timing diagrams for device number 0 and device number 30, respectively.

- **Cycle 1A**: The host ASIC applies the Read instruction to CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction to CMD[1:0], using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[71:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[71:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[71:0].
- **Cycles 5 to 6**: The selected device continues to drive DQ[71:0].
- **Cycle 7**: The selected device continues to drive DQ[71:0], and drives an SRAM Read cycle.
- **Cycle 8**: The selected device drives ACK from Z to LOW.
- **Cycle 9**: The selected device drives ACK to HIGH.
- **Cycle 10**: The selected device drives ACK from HIGH to LOW.

At the end of cycle 10, the selected device floats ACK to High-Z and a new command can begin.

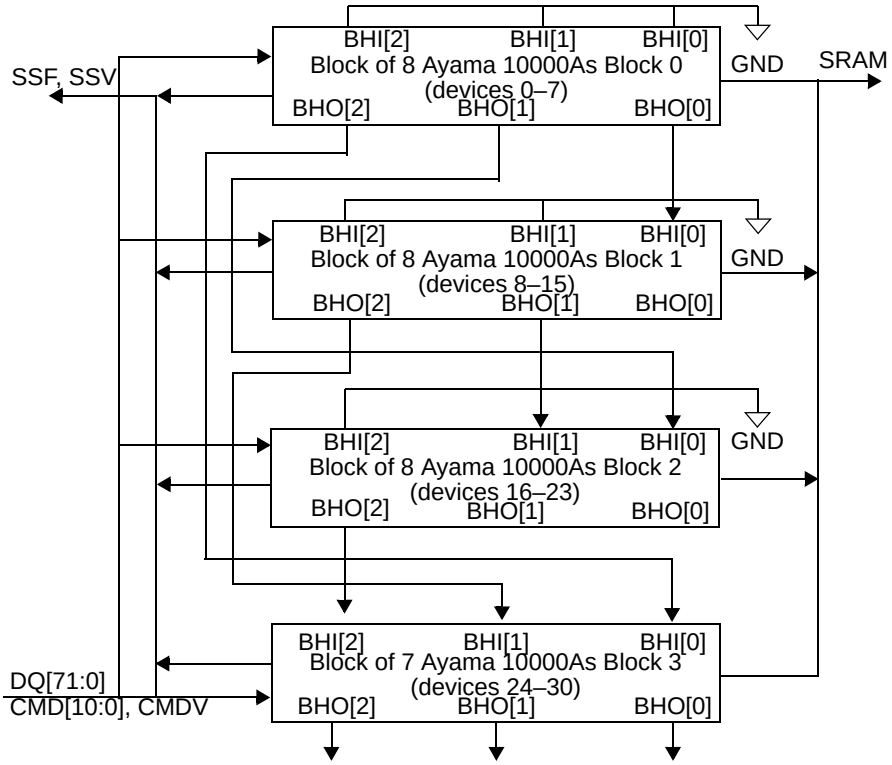
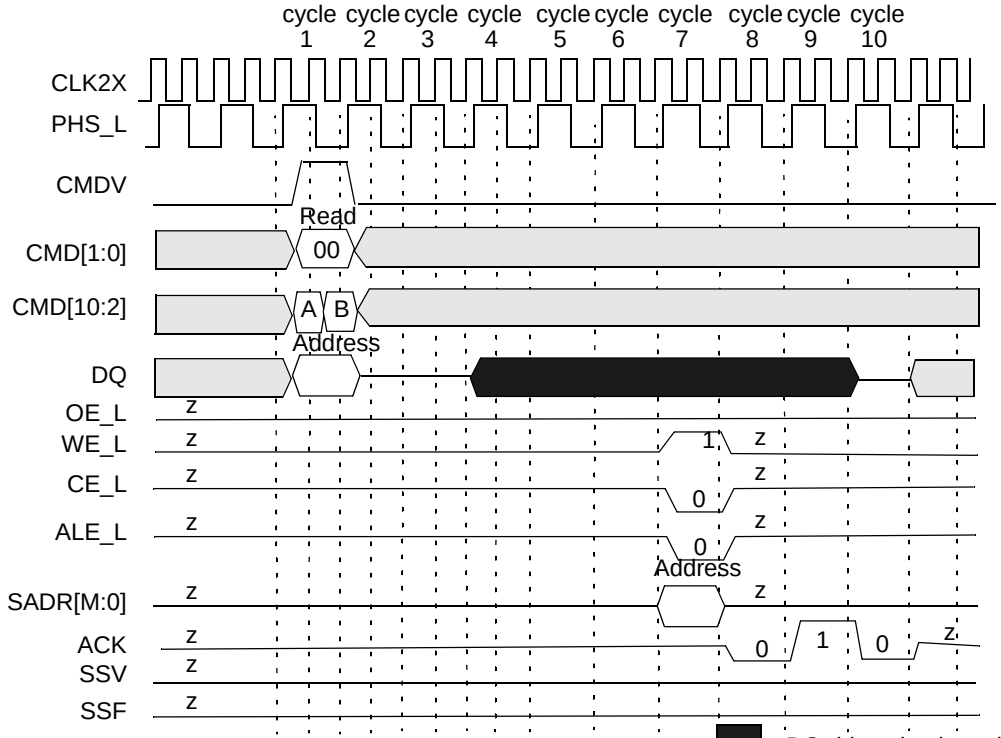



**Figure 6-60. Hardware Diagram of 31 Devices Using Four Blocks**




M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A
TLSZ = 10 (binary), HLAT = 010 (binary), LRAM = 0 (binary), LDEV = 0 (binary)

DQ driven by the selected Ayama 10000A

**Figure 6-61. SRAM Read of Device #0 in a Bank of 31 Devices**

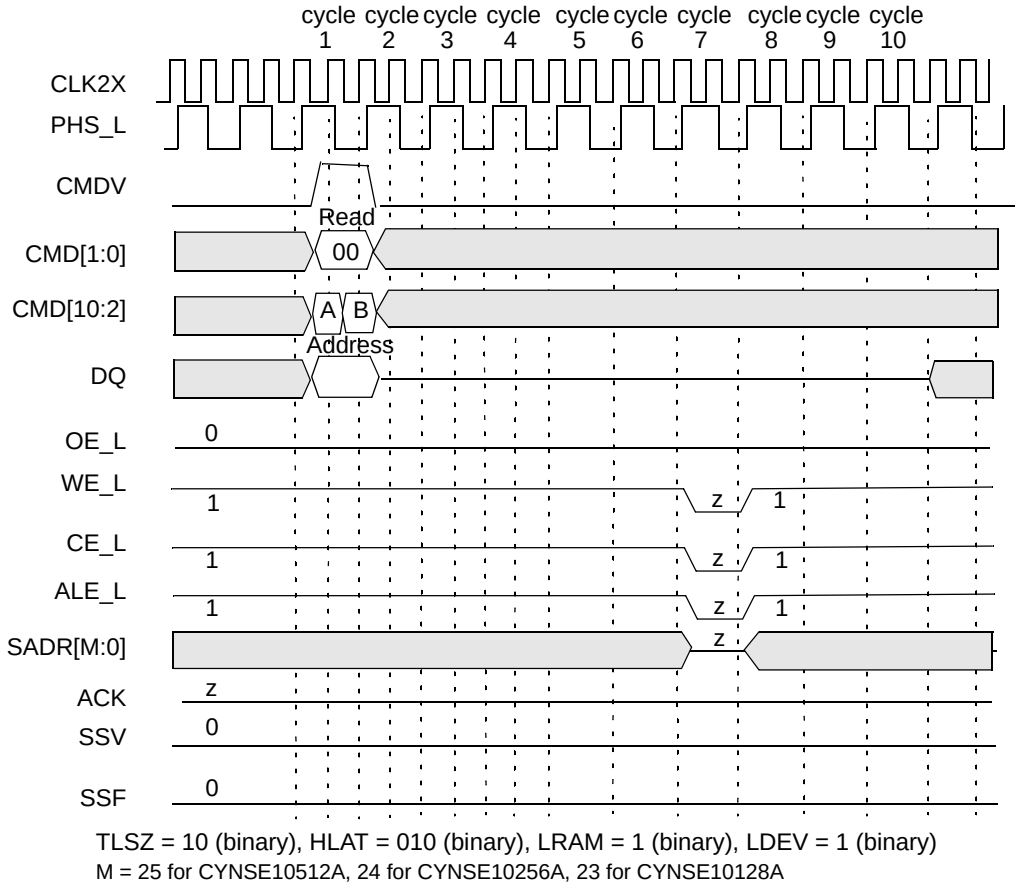


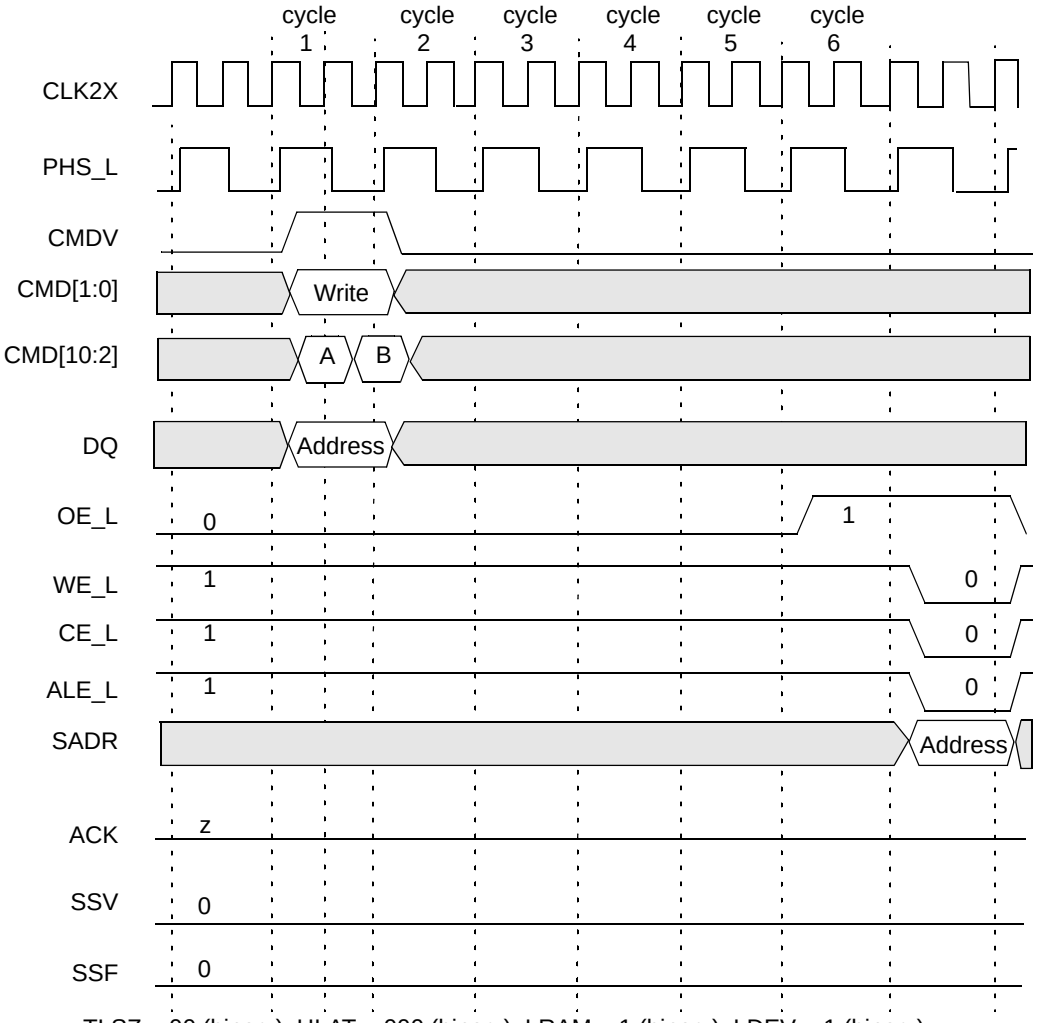

**Figure 6-62. SRAM Read of Device #0 in a Bank of 31 Devices**

### *6.7.4 SRAM Write with a Table of One Device*

SRAM Write enables Write access to the off-chip SRAM containing associative data. The latency from the second cycle of the Write instruction to the appearance of the address on the SRAM bus is the same as Search instruction latency, and will depend on the TLSZ value parameter programmed in the device configuration register. The following explains the SRAM Write operation accomplished through a table of only one device with the following parameters: TLSZ = 01 (binary), HLAT = 000 (binary), LRAM = 1 (binary), and LDEV = 1 (binary). *Figure 6-63* shows the timing diagram. For the following description, the selected device refers to the only device in the table because it is the only device that will be accessed.

- **Cycle 1A**: The host ASIC applies the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6] in this cycle.
- **Note**. CMD[2] must be set to 0 for SRAM Write because burst WRITEs into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address.
- **Note**. CMD[2] must be set to 0 for SRAM Write because burst WRITEs into the SRAM are not supported.
- **Cycle 2 and cycle 3**: wait states. Data not used by NSE.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation; the Write cycle appears at the SRAM bus, however, with the same latency as the Search instruction, as measured from the second cycle of the Write command.




TLSZ = 00 (binary), HLAT = 000 (binary), LRAM = 1 (binary), LDEV = 1 (binary)

**Figure 6-63. SRAM Write Access**

### 6.7.5 SRAM Write with a Table of up to Eight Devices

The following explains the SRAM Write operation accomplished through a table(s) of up to eight devices with the following parameters (TLSZ = 01 (binary)). The hardware diagram for this table is shown in *Figure 6-64*. The following assumes that SRAM access is achieved through Ayama 10000A device number 0. *Figure 6-65* and *Figure 6-66* show the timing diagram for device number 0 and device number 7, respectively.

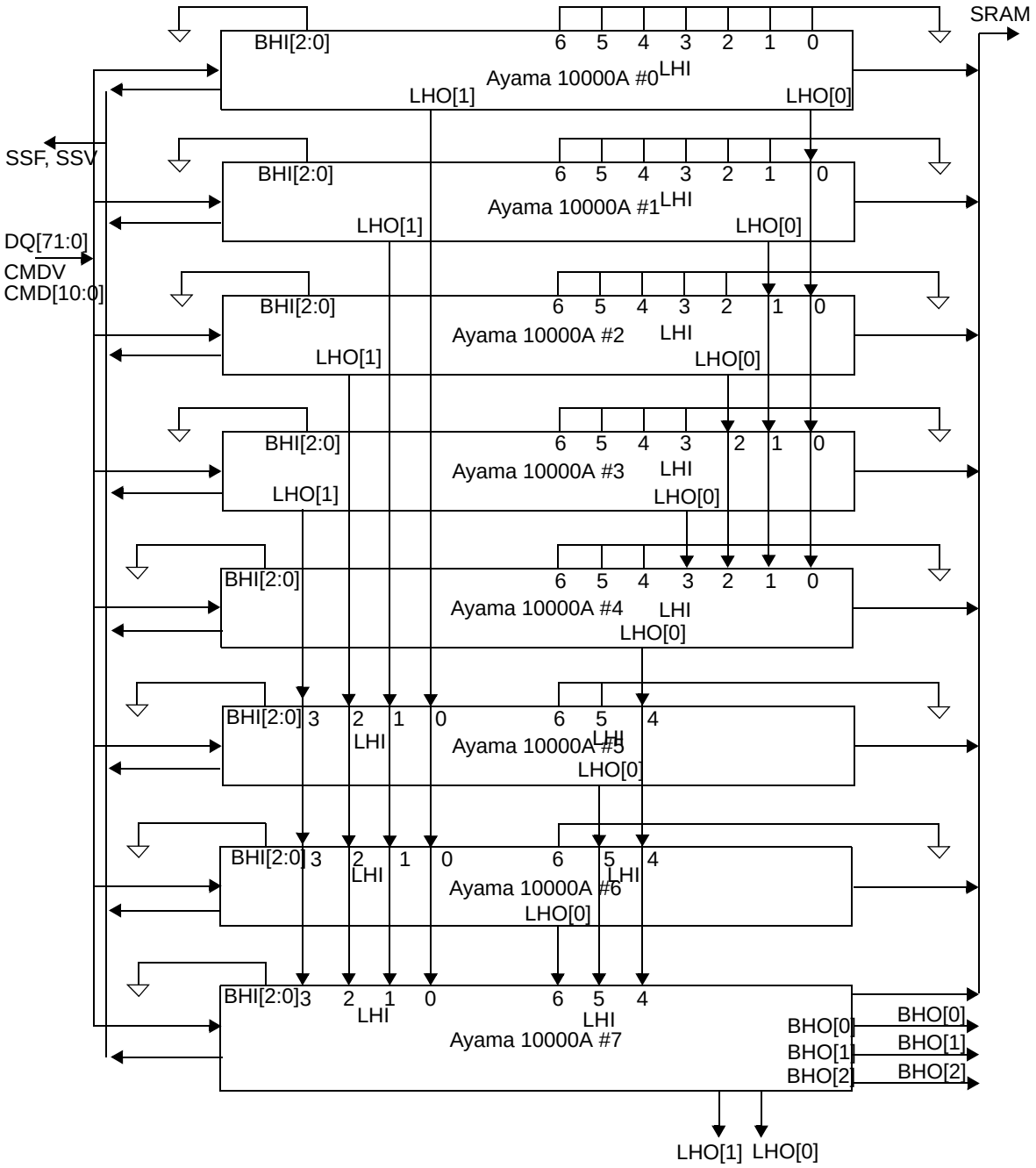



**Figure 6-64. Hardware Diagram of a Block of Eight Devices**

- **Cycle 1A**: The host ASIC applies the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6] in this cycle.

  **Note**. CMD[2] must be set to 0 for SRAM Write because burst WRITEs into the SRAM are not supported.

- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address.
  **Note**. CMD[2] must be set to 0 for SRAM Write because burst WRITEs into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the Ayama 10000A device.
- **Cycle 3**: The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the Ayama 10000A device.

At the end of cycle 3, a new command can begin. Write is a pipelined operation, but the Write cycle appears at the SRAM bus with the same latency as that of a Search instruction, as measured from the second cycle of the Write command.

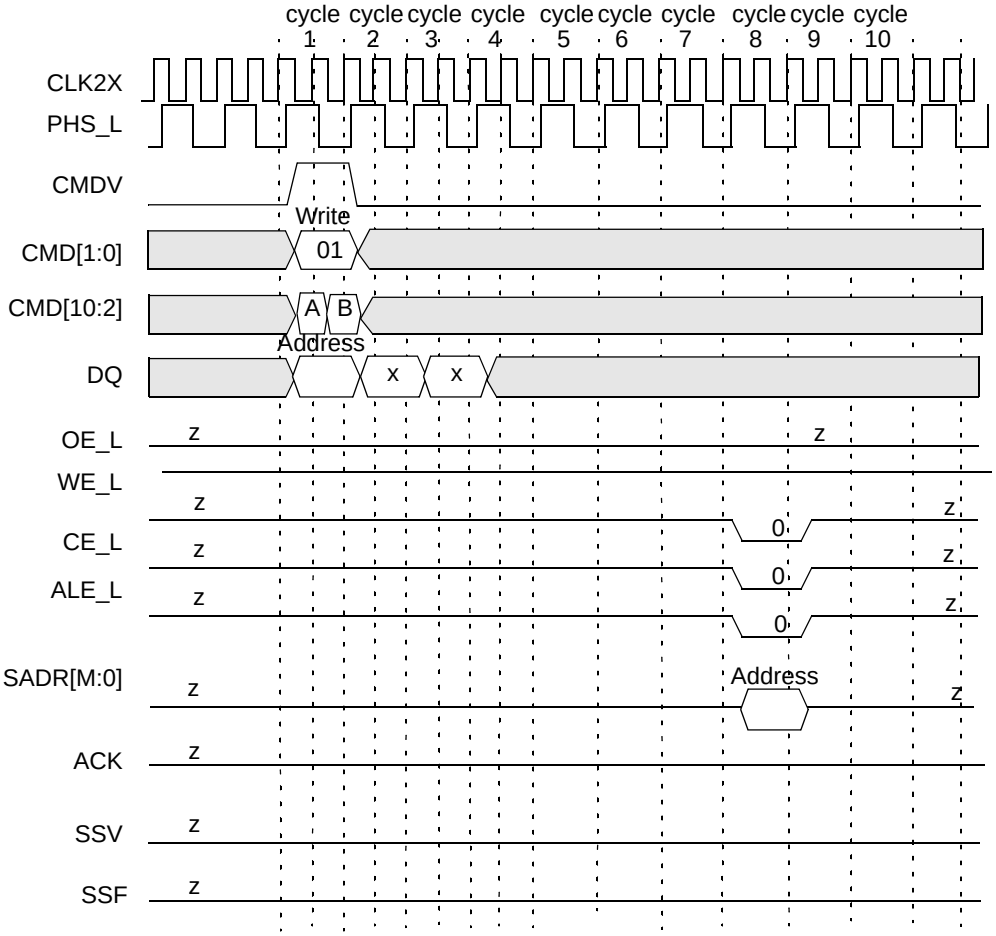



**Figure 6-65. SRAM Write of Device #0 in a Block of Eight Devices**

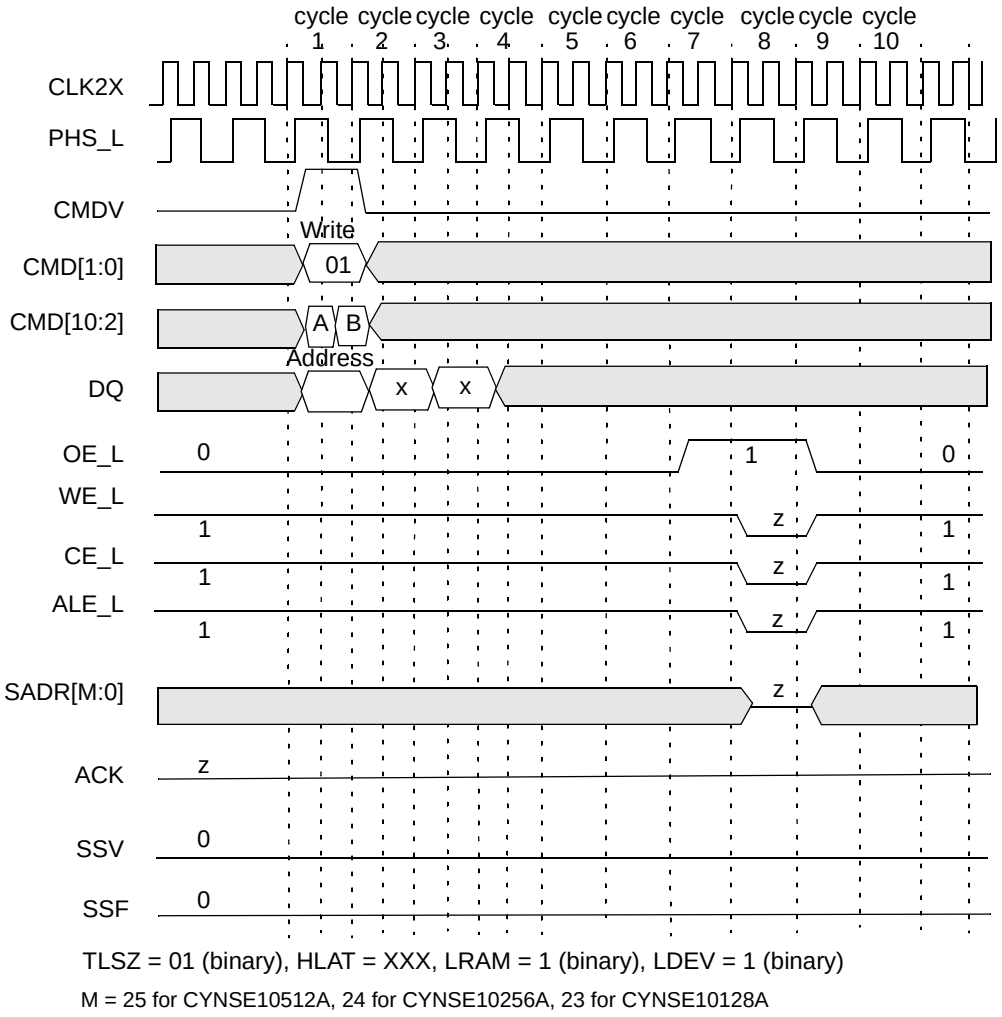



**Figure 6-66. SRAM Write Timing of Device #7 in Block of Eight Devices**

### *6.7.6 SRAM Write with Table(s) Consisting of up to 31 Devices*

The following explains the SRAM Write operation accomplished through a table of up to 31 devices with the following parameter: TLSZ = 10 (binary). The hardware diagram is shown in *Figure 6-67*. The following assumes that SRAM access is accomplished through Ayama 10000A device number 0—the selected device. *Figure 6-68* and *Figure 6-69* show timing diagrams for device number 0 and device number 30, respectively.

- **Cycle 1A**: The host ASIC applies the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, SADR[23:21] for CYNSE10128A on CMD[8:6] in this cycle.

  **Note**. CMD[2] must be set to 0 for SRAM Write because burst WRITEs into the SRAM are not supported.

- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address.

  **Note**. CMD[2] must be set to 0 for SRAM Write because burst WRITEs into the SRAM are not supported.

- **Cycle 2**: The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the Ayama 10000A device.
- **Cycle 3**: The host ASIC continues to drive DQ[71:0]. The data in this cycle is not used by the Ayama 10000A device.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation, but the Write cycle appears at the SRAM bus with the same latency as that of a Search instruction, as measured from the second cycle of the Write command.

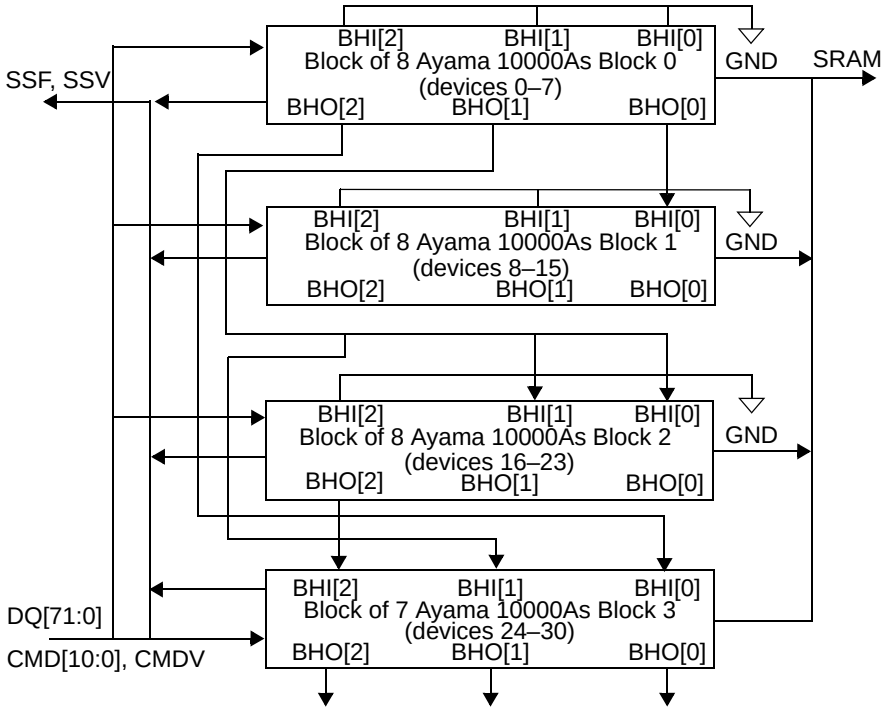
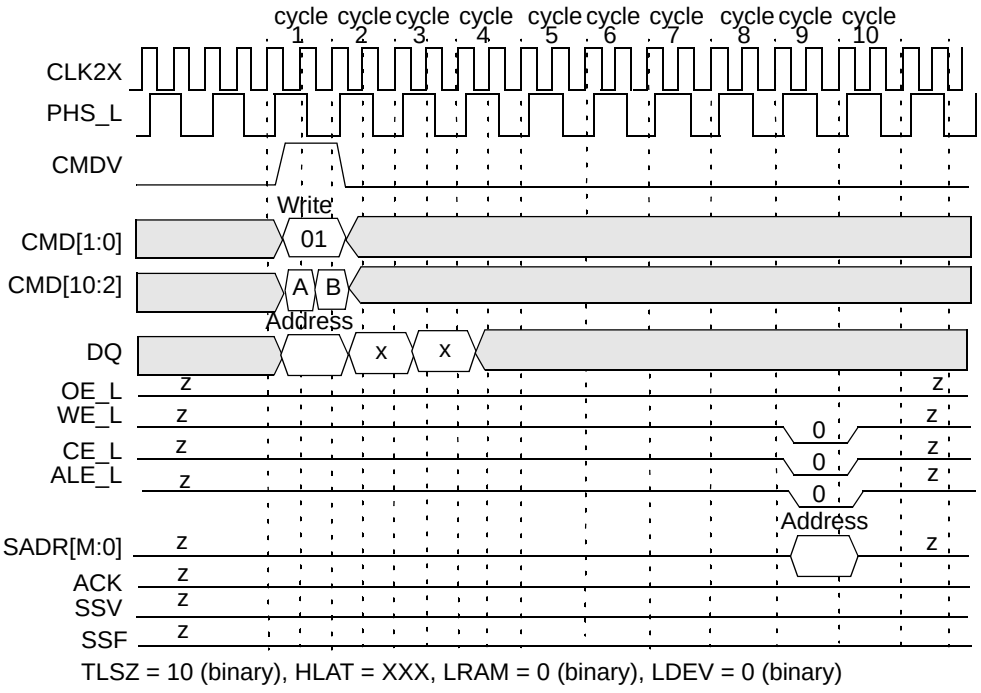


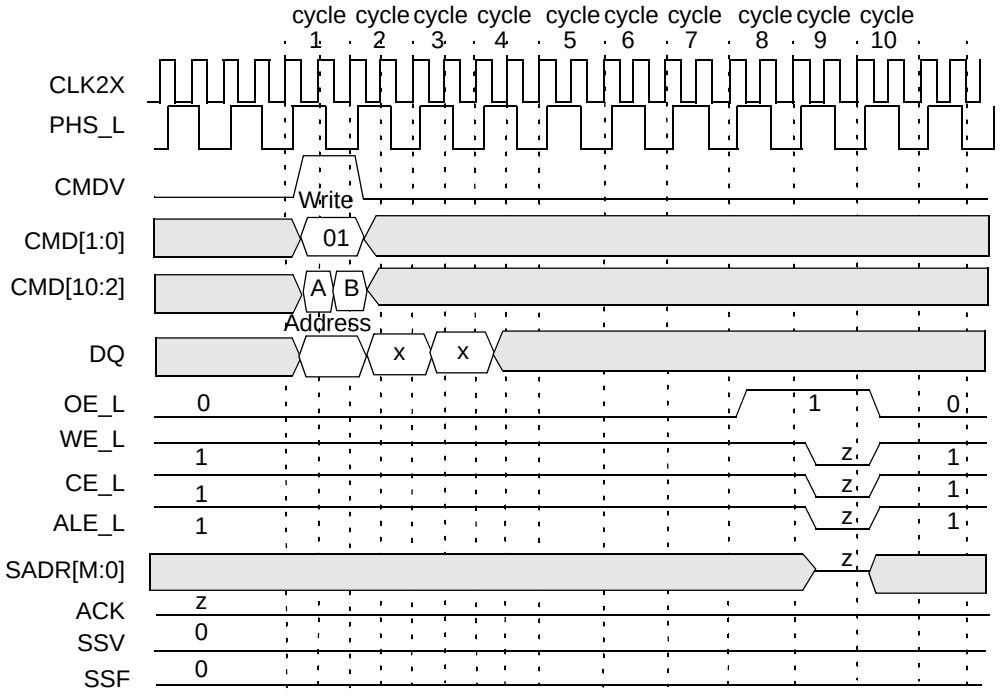

**Figure 6-67. Table of 31 Devices (Four Blocks)**




TLSZ = 10 (binary), HLAT = XXX, LRAM = 0 (binary), LDEV = 0 (binary)

M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-68. SRAM Write of Device #0 in Bank of 31 Devices**




TLSZ = 10 (binary), HLAT = XXX, LRAM = 1 (binary), LDEV = 1 (binary)
M = 25 for CYNSE10512A, 24 for CYNSE10256A, 23 for CYNSE10128A

**Figure 6-69. SRAM Write Through Device #30 in Bank of 31 Devices**

## 6.8 Timing Sequences for Back-to-Back Operations

*Table 6-16* shows the idle cycle requirements between operations. The operations in the second column represent operations already performed, and the operations in the first row are those we would like to perform next.

**Example calculations**:

1. Read after Write: The Write takes two cycles, and one idle cycle is required. Thus if the Write is issued in cycle 1, the Read cannot be issued until cycle 4. Note, all cycles after an SRAM Read or an NSE Read (blocking) operation are considered blocked until the ACK signal is returned.
2. Learn from SRR after Search x288, with TLSZ=10 (binary): The Search takes two cycles, and (2+TLSZ) idle cycles are required. Thus if the Search is issued in cycle 1, the Learn cannot be issued until cycle 7.

**Table 6-16. Required Idle Cycles Between Commands**

| # of Cycles | OPERATION | SEARCH | READ | WRITE | LEARN | SRAM |
|---|---|---|---|---|---|---|
| x72/x144 = 1 Cycle<br>x288 = 2 Cycles<br>x576 = 4 Cycles | SEARCH | No Wait | No Wait / 2+TLSZ[15] | No Wait | No Wait / 2+TLSZ[16,19] | TLSZ / 2+TLSZ[17] |
| 1 Cycle | READ | 5 | 5 | 5 | 5 | 5 |
| 2 Cycles | WRITE | 1 | 1 | 1 | 1 / 1+TLSZ[18] | 1 |
| x72/x144 = 1 Cycle<br>x288 = 2 Cycles<br>x576 = 4 Cycles | LEARN | 1 | 1 | 1 | 1 | 1 |
| 1 Cycle | SRAM READ | 5+TLSZ+HLAT | 5+TLSZ+HLAT | 5+TLSZ+HLAT | 5+TLSZ+HLAT | 5+TLSZ+HLAT |
| 2 Cycles | SRAM WRITE | 1 | 1 | 1 | 1 | 1 |

**Notes:**

15. When the register being read is SSR/SRR and it matches the target location of the previous search, a READ operation cannot be issued for 2+TLSZ idle cycles to avoid reading the old value. Otherwise there is no idle cycle requirement.
16. In Non-Enhanced Mode there is no idle cycle requirement. In Enhanced Mode, an SRR is updated on a SEARCH miss and is used as the address for the LEARN. Must wait for 2+TLSZ cycles after the last Search, before issuing a subsequent Learn that uses the same SRR as the last Search.
17. The SRAM operation needs to insert idle cycles to avoid SADR bus contention with previous SEARCH.
18. In non-Enhanced Mode, a WRITE operation updates the NFA register used for LEARN operation. Must wait for 1+TLSZ cycles before issuing LEARN to avoid learning with the old NFA value.
19. If the Learn is issued 2+TLSZ after the corresponding Search that updated the SRR, the Learn will be issued before the Search result or the updated FULL signal is returned. If the Search resulted in a hit, the Learn will be suppressed. If there was a miss, but the device is already full, the Learn will also be suppressed.

## 6.9 Full Signal Timing Diagram

FULL indicates when the array (Non-Enhanced Mode) or selected blocks (Enhanced Mode) is full.

In Non-Enhanced Mode, FULL is valid four CLK1X cycles after the command is issued, regardless of TLSZ and HLAT. At all other times, FULL maintains its value until another operation changes it.

In Enhanced Mode, FULL is valid when SSV is high. *Figure 6-70* is a timing diagram of the FULL signal in Enhanced (top) and non-Enhanced (bottom) Modes.

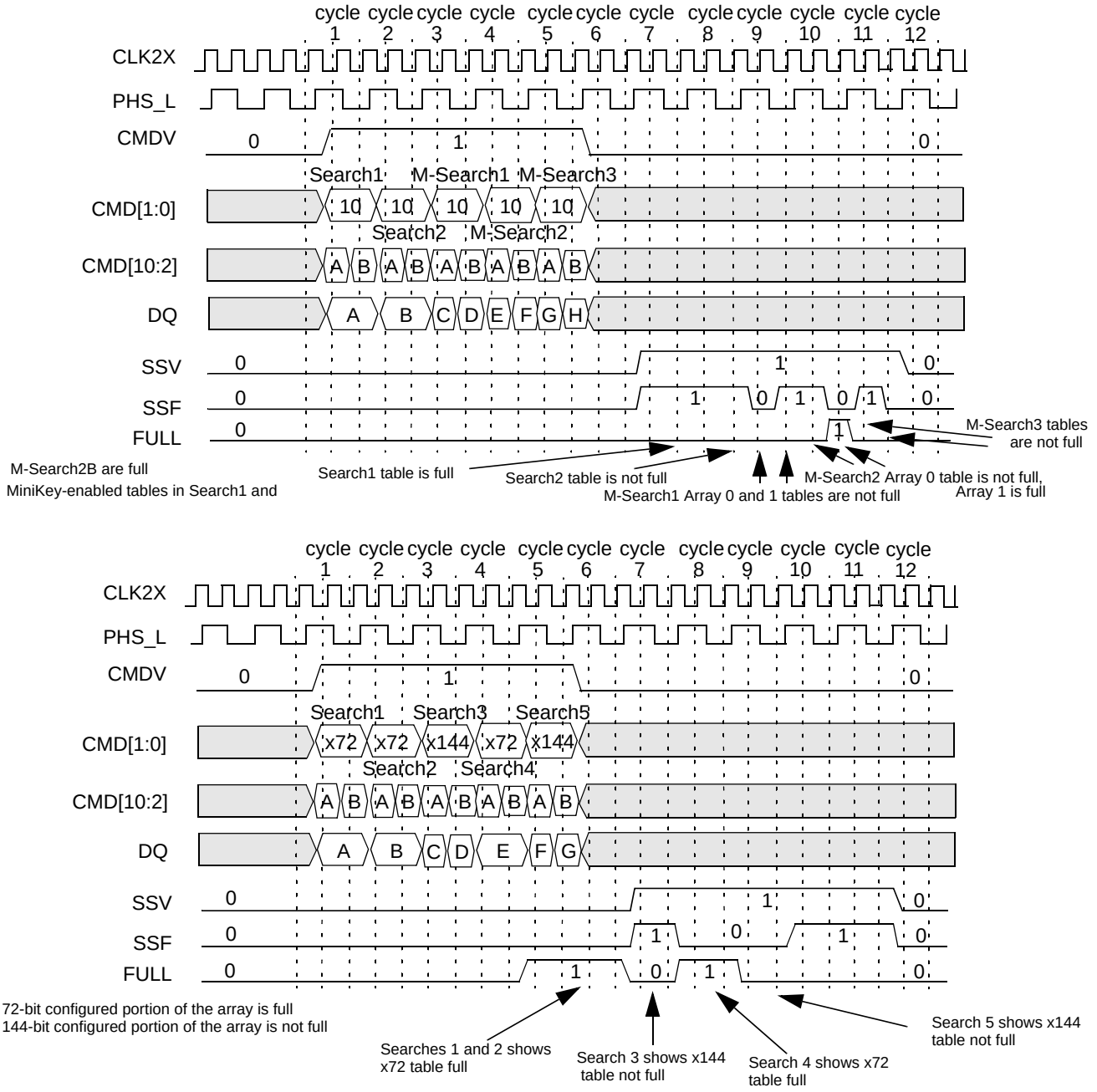



**Figure 6-70. Timing Diagram for Full Signal (TLSZ = 10)**

## 7.0 JTAG (IEEE 1149.1)

The Ayama 10000A device supports the Test Access Port and Boundary Scan Architecture as specified in IEEE JTAG Standard Number 1149.1. The pin interface to the chip consists of five signals with the standard definitions: TCK, TMS, TDI, TDO, and TRST_L. *Table 7-1* describes the operations that the test access port controller supports, and *Table 7-2* describes the TAP Device ID Register. JTAG can also be reset by driving TMS HIGH, and then holding it for three (3) TCK rising edges.

**Note**. To disable JTAG functionality, connect the TCK, TMS, and TDI pins to $V_{DDQ}$ through pull-resistors and hold TRST_L Low.

**Table 7-1. Supported Operations**

| Instruction | Type | Description |
|---|---|---|
| SAMPLE/PRELOAD | Mandatory | **Sample/Preload**. This operation loads the values of signals going to and from I/O pins into the boundary scan shift register to provide a snapshot of the normal functional operation. |
| EXTEST | Mandatory | **External Test**. This operation uses boundary scan values shifted in from the TAP to test connectivity external to the device. |
| BYPASS | Mandatory | **Bypass**. This operation bypasses the device in a JTAG chain by loading a single bit shift register between TDI and TDO and provides a minimum-length serial path when no test operation is required. |
| IDCODE | Optional | **Device JTAG ID Code**. This operation selects the JTAG Identification register and output the IDCODE field serially through TDO. |
| CLAMP | Optional | **Output Clamp**. This operation drives preset values onto the outputs of the device. |
| HIGHZ | Optional | **High-Z Output**. This operation sets the device output signals in high impedance state. |

**Table 7-2. TAP Device ID Register**

| Field | Range | Initial Value | Description |
|---|---|---|---|
| Revision | [31:28] | 0001 | **Revision Number**. This is the current device revision number. Numbers start from one and increment by one for each revision of the device. |
| Part Number | [27:12] | 0000 0000 0001 0100 | **Part Number**. This is the part number for CYNSE10128A. |
| | | 0000 0000 0001 0101 | This is the part number for CYNSE10256A. |
| | | 0000 0000 0001 0110 | This is the part number for CYNSE10512A. |
| MFID | [11:1] | 000_1101_1100 | **Manufacturer ID**. This field is the same as the manufacturer ID used in the TAP controller. |
| LSB | [0] | 1 | **Least Significant Bit**. |

## 8.0 Power Consumption

*Figure 8-1* depicts the power consumption of the Ayama 10512A device based on 50% I/O switching, 10-pF output load, 1.5V HSTLII VDDQ_ASIC/VDDQ_SRAM, and 1.2V VDD.

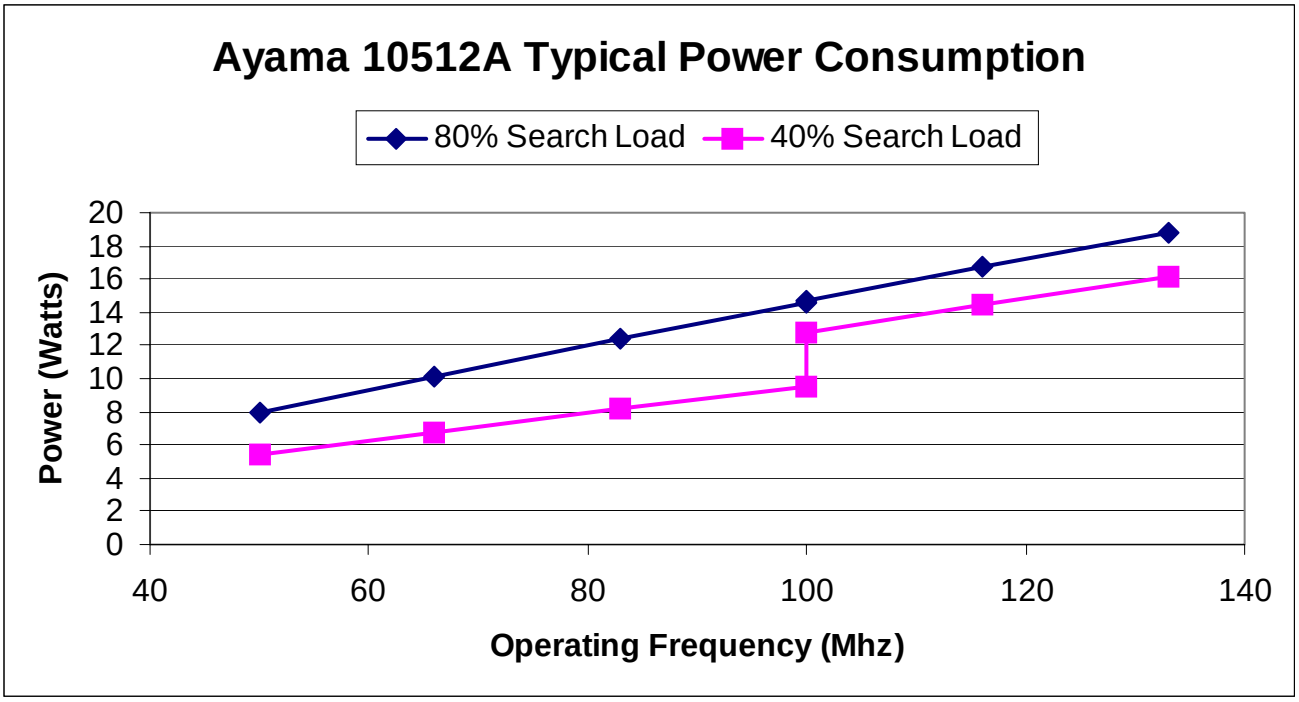



**Figure 8-1. Typical Power Consumption of Ayama 10512A**

**Note**: These values were determined through our power estimation model. Please contact Cypress to get an application specific power estimation.

*Table 8-1* indicates the power consumption values in Watts used in *Figure 8-1*. The Ayama 10512A demonstrates the worst case for power consumption as it contains the highest density value from Ayama 10128A/10256A/10512A. When CLK1x > 100 MHz, HIGHSPEED must be turned on by setting HIGHSPEED = '00', resulting in higher power consumption for low search loads at high frequencies. The power data described is when all the blocks in the device are active. A device that operates in Enhanced mode and utilizes Mini-Key may have lower power consumption depending on the configuration.

**Table 8-1. Power Consumption for Ayama 10512A (Watts)**

| Search Load | 50 MHz | 66 MHz | 83 MHz | 100 MHz | 116 MHz | 133 MHz |
|---|---|---|---|---|---|---|
| 80% High Speed Off | 8.01 | 10.18 | 12.41 | 14.61 | 16.62 | 18.74 |
| 80% High Speed On | 8.09 | 10.25 | 12.48 | 14.67 | 16.69 | 18.79 |
| 40% High Speed Off | 5.43 | 6.79 | 8.17 | 9.52 | 10.77 | 12.07 |
| 40% High Speed On | 7.13 | 8.97 | 10.86 | 12.72 | 14.43 | 16.20 |

## 9.0 Electrical Specifications

### 9.1 Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature: ..... –65°C to +150°C

Maximum Junction Temperature: .....125°C

Static Discharge Voltage (per JEDEC EIA./JESD22-A114A): ..... > 2000V

ESD HBM Model (EIA/JESD22-C101C): ..... > 500V

Latch-up Current: > ..... 300 mA

**Table 9-1. DC Electrical Characteristics for Ayama 10000A**

| Parameter | Description | Conditions | $V_{DDQ}$ = 1.5V | | $V_{DDQ}$ = 1.8V | | $V_{DDQ}$ = 2.5V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_{LI}$ | Input leakage current | $V_{DDQ} = V_{DDQ}$ Max., $V_{IN}$ = 0 to $V_{DDQ}$ Max. | –10 | 10 | –10 | 10 | –10 | 10 | µA |
| $I_{LO}$ | Output leakage current[25] | $V_{DDQ} = V_{DDQ}$ Max., $V_{IN}$ = 0 to $V_{DDQ}$ Max. | –10 | 10 | –10 | 10 | –10 | 10 | µA |
| $V_{IL}$ | Input LOW voltage[21] | | –0.3 | $V_{REF}$ – 0.1 | -0.3 | 0.35 $V_{DDQ}$ | –0.3 | 0.7 | V |
| $V_{IH}$ | Input HIGH voltage[20] | | $V_{REF}$ + 0.1 | $V_{DDQ}$ + 0.3 | 0.65 $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | 1.7 | $V_{DDQ}$ + 0.3 | V |
| $V_{OL}$ | Output LOW voltage | $V_{DDQ} = V_{DDQ}$ Min., $I_{OL}$ = 2 mA | | 0.4 | | 0.45 | | 0.7 | V |
| $V_{OH}$ | Output HIGH voltage | $V_{DDQ} = V_{DDQ}$ Min., $I_{OH}$ = 2 mA | $V_{DDQ}$ – 0.4 | | $V_{DDQ}$ – 0.45 | | 1.7 | | V |
| $I_{CC}$ | CYNSE10000A Operating Current | The operating current for NSE devices is highly application dependent, and can vary widely due to a number of system configurations. Please contact Cypress and provide system characteristics to receive application specific values. | | | | | | | |

**Table 9-2. Capacitance Characteristics**

| Parameter | Description | Max. | Unit |
|---|---|---|---|
| $C_{IN}$[22] | Input capacitance | 6 / 12[24] | pF |
| $C_{OUT}$[23] | Output capacitance | 6 | pF |

**Table 9-3. Operating Conditions for Ayama 10000A**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DDQ}$ = 2.5V | Operating voltage for I/O (2.5V LVCMOS) | 2.3 | 2.5 | 2.7 | V |
| $V_{DDQ}$ = 1.8V | Operating voltage for I/O (1.8V LVCMOS) | 1.65 | 1.8 | 1.95 | V |
| $V_{DDQ}$ = 1.5V | Operating voltage for I/O (HSTLI/II) | 1.4 | 1.5 | 1.6 | V |
| $V_{REF}$ | Reference voltage for I/O (HSTLI/II) | 0.68 | 0.75 | 0.9 | V |
| $V_{DD}$ | Operating supply voltage | 1.14 | 1.2 | 1.26 | V |
| $T_A$ | Ambient operating temperature (C) | 0 | | 70 | °C |
| | Ambient operating temperature (I) | –40 | | 85 | °C |
| $T_J$ | Maximum Operating Junction Temperature | | | 110 | °C |
| $\Theta_{JC}$ | Junction-to-Case thermal resistance | | 0.12 | | °C/W |
| $\Theta_{JA}$ | Junction-to-Ambient thermal resistance (Airflow = 0 LFM) | | 10.2 | | °C/W |
| $\Theta_{JA}$ | Junction-to-Ambient thermal resistance (Airflow = 200 LFM) | | 7.0 | | °C/W |

**Notes:**

20. Maximum allowable applies to overshoot only.
21. Minimum allowable applies to undershoot only.
22. f = 1 MHz, $V_{IN}$ = 0V.
23. f = 1 MHz, $V_{OUT}$ = 0V.
24. CMD bus signals has an input capacitance of 12 pF, $V_{REF}$ 30 pF, and all others 6 pF
25. Output leakage current does not cover cascade (LHO, BHO, FULO) signals because these are always driven and are not measurable

# 10.0 AC Timing Parameters, Waveforms and Test Conditions

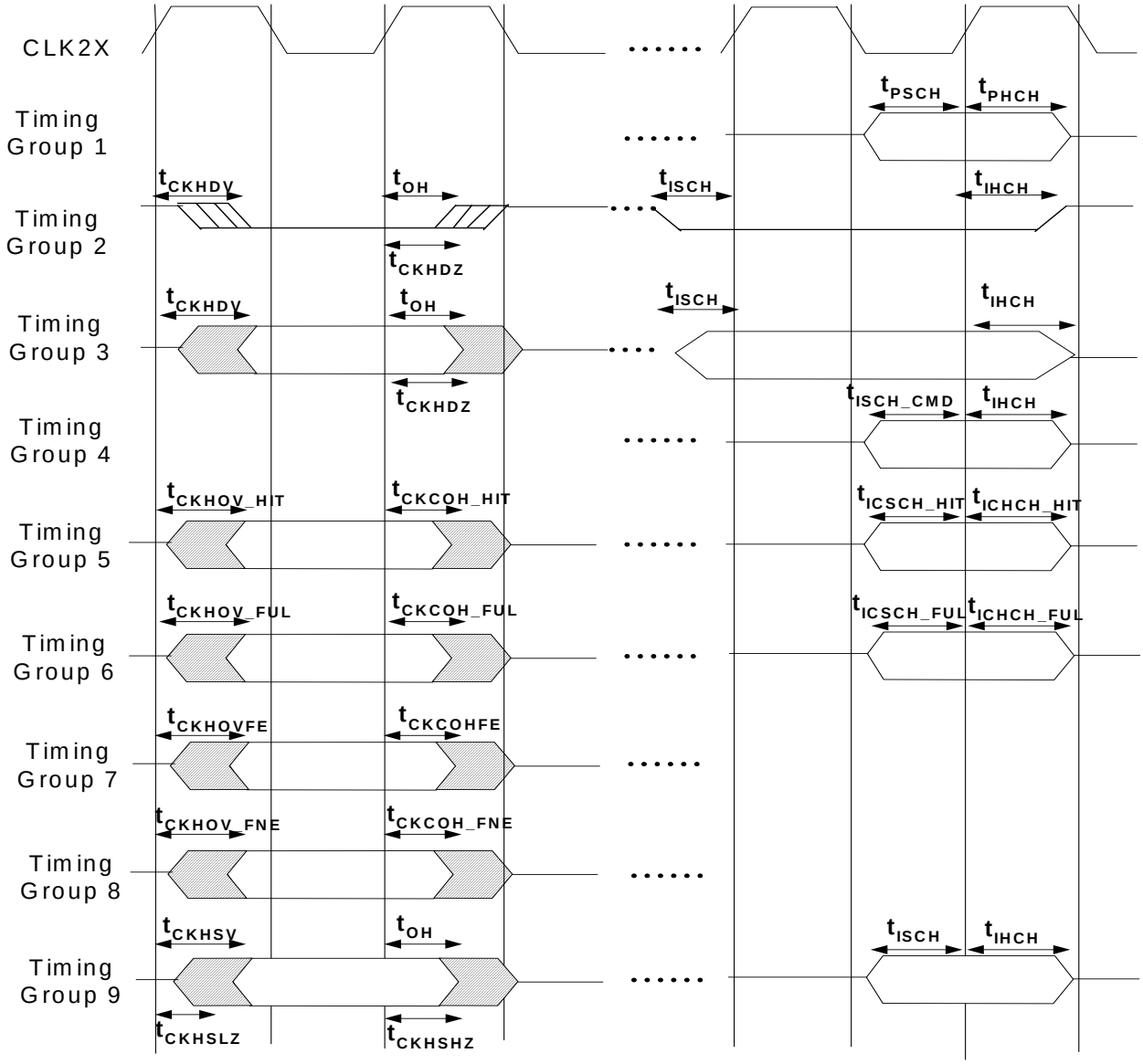
## 10.1 AC Timing Parameters and Waveforms with CLK2X

**Table 10-1. AC Timing Parameters with CLK2X**

| Parameter | Description | Ayama 10000A-083 | | Ayama 10000A-100 | | Ayama 10000A-133 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{CLOCK}$ | CLK2X frequency | 100 | 166 | 100 | 200 | 100 | 266 | MHz |
| $t_{LOCK}$ | PLL lock time | | 0.5 | | 0.5 | | 0.5 | ms |
| $t_{CKHI}$ | CLK2X HIGH pulse[26] | 2.4 | | 2.0 | | 1.5 | | ns |
| $t_{CKLO}$ | CLK2X LOW pulse[26] | 2.4 | | 2.0 | | 1.5 | | ns |
| $t_{PSCH}$ | PHS_L set-up time to CLK2X rising edge[26] | 1.8 | | 1.5 | | 1.4 | | |
| $t_{PHCH}$ | PHS_L hold-time to CLK2X rising edge [26] | 0.6 | | 0.6 | | 1.0 | | |
| $t_{ISCH}$ | Input set-up time to CLK2X rising edge[26] | 1.8 | | 1.5 | | 1.3 | | ns |
| $t_{IHCH}$ | Input hold time to CLK2X rising edge[26] | 0.6 | | 0.5 | | 0.3 | | ns |
| $t_{ISCH\_CMD}$ | CMD & CMDV Input set-up time to CLK2X rising edge[26] | 1.8 | | 1.5 | | 1.5 | | ns |
| $t_{ICSCH}$ | Cascaded input set-up time to CLK2X rising edge[27, 29] | | | | | | | |
| $t_{ICSCH\_HIT}$ | LHI, BHI signals | 4.5 | | 4 | | 3.5 | | ns |
| $t_{ICSCH\_FUL}$ | FULI signals | 1.8 | | 1.5 | | 1.4 | | ns |
| $t_{ICHCH}$ | Cascaded input hold time to CLK2X rising edge[27, 29] | | | | | | | |
| $t_{ICHCH\_HIT}$ | LHI, BHI signals | 0 | | 0 | | 0 | | ns |
| $t_{ICHCH\_FUL}$ | FULI signals | 0.8 | | 0.7 | | 0.5 | | ns |
| $t_{CKHOV}$ | Rising edge of CLK2X to cascade output valid[27, 28] | | | | | | | |
| $t_{CKHOV\_HIT}$ | LHO, BHO signals | | 3.9 | | 3.4 | | 2.6 | ns |
| $t_{CKHOV\_FUL}$ | FULO signals | | 7 | | 6.5 | | 5.8 | ns |
| $t_{CKCOH}$ | Rising edge of CLK2X to cascade output invalid (output hold)[30] | | | | | | | |
| $t_{CKCOH\_HIT}$ | LHO, BHO signals | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{CKCOH\_FUL}$ | FULO signals | 1.2 | | 1.2 | | 1.2 | | ns |
| $t_{CKHOVFE}$ | Rising edge of CLK2X to FULL signal valid (Enhanced mode) | | 3.5 | | 3.0 | | 2.6 | ns |
| $t_{CKHOV\_FNE}$ | Rising edge of CLK2X to FULL signal valid (Non-Enhanced mode) | | 7 | | 6.5 | | 5.8 | ns |
| $t_{CKCOHFE}$ | Rising edge of CLK2X to FULL invalid (Enhanced mode)[30] | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{CKCOH\_FNE}$ | Rising edge of CLK2X to FULL invalid (Non-Enhanced mode)[30] | 1.2 | | 1.2 | | 1.2 | | ns |
| $t_{CKHDV}$ | Rising edge of CLK2X to DQ valid[26] | | 3.5 | | 3.0 | | 2.6 | ns |
| $t_{CKHDZ}$ | Rising edge of CLK2X to DQ High-Z[26, 30] | 0.5 | 1.8 | 0.5 | 1.8 | 0.5 | 1.8 | ns |
| $t_{CKHSV}$ | Rising edge of CLK2X to SRAM bus valid[26] | | 3.5 | | 3.0 | | 2.8 | ns |
| $t_{CKHSHZ}$ | Rising edge of CLK2X to SRAM bus High-Z[26, 30] | 0.5 | 1.8 | 0.5 | 1.8 | 0.5 | 1.8 | ns |
| $t_{CKHSLZ}$ | Rising edge of CLK2X to SRAM bus Low-Z[26, 30] | 2.2 | | 1.9 | | 1.9 | | ns |
| $t_{OH}$ | Rising edge of CLK2X to DQ or SRAM bus invalid (output hold) | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{RSTL}$ | Minimum LOW pulse width for RST_L | 100 | | 100 | | 100 | | us |

**Notes:**

26. Values are based on 50% signal levels.
27. Values are based on 50% signal levels and a 50%/50% duty cycle of CLK1X/CLK2X
28. Based on an AC load of 6 pF.
29. Cascade signals only transition on CLK2X Cycle A rising edge
30. Based on an AC load of 30 pF. This parameter is guaranteed by design and is not production tested.




Timing Group 1: PHS_L

Timing Group 2: PARERR_L

Timing Group 3: DQ, PAR, ACK, EOT, MULTI_HIT

Timing Group 4: CMD[0:10], CMDV

Timing Group 5: LHI, BHI, LHO, BHO

Timing Group 6: FULI, FULO

Timing Group 7:FULL (ENHANCED)

Timing Group 8: FULL (NON-ENHANCED)

Timing Group 9: SADR, CE_L, OE_L, WE_L, ALE_L, SSF, SSV

**Figure 10-1. AC Timing Waveforms with CLK2X**

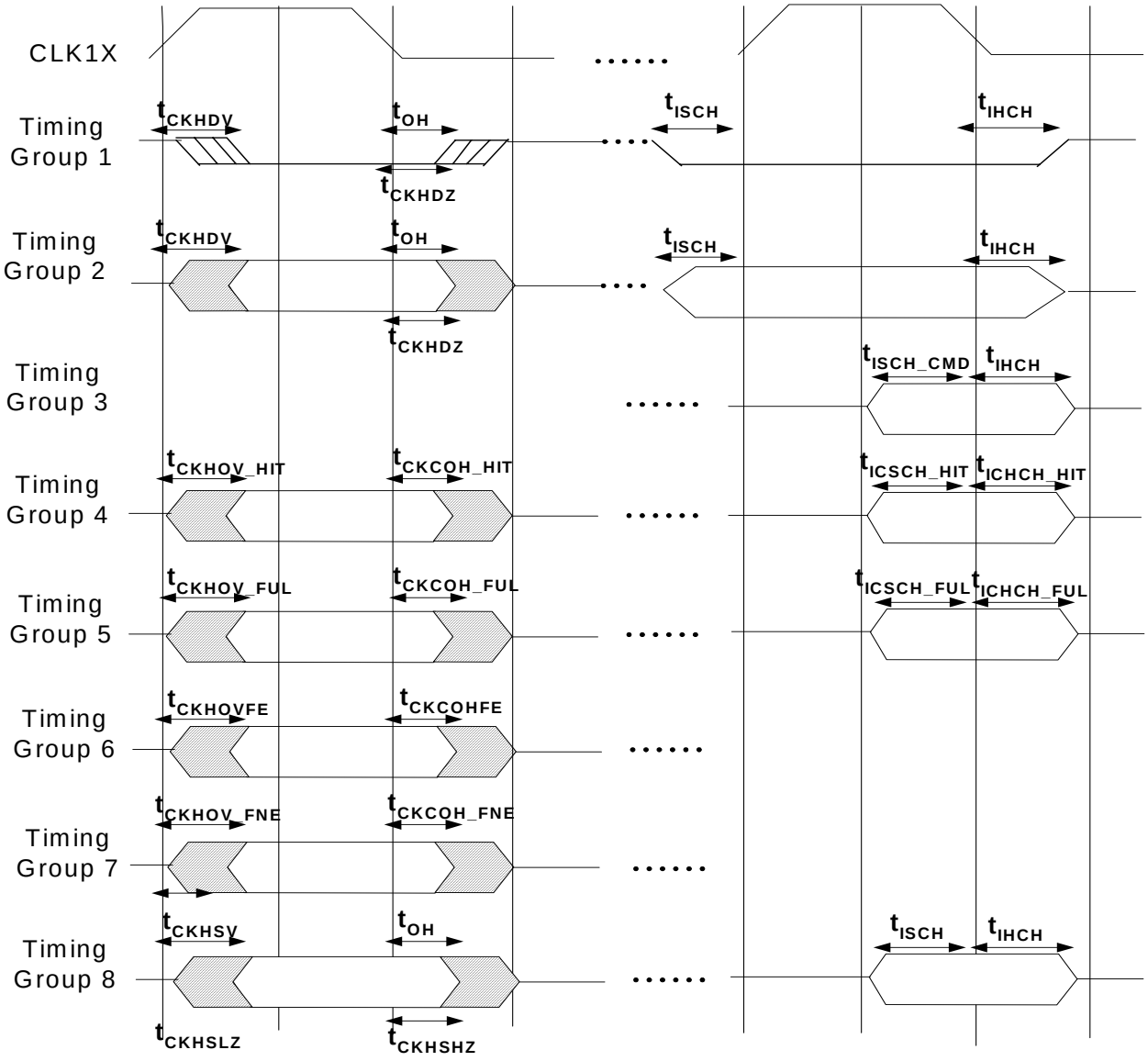
## 10.2 AC Timing Parameters and Waveforms with CLK1X

**Table 10-2. AC Timing Parameters with CLK1X**

| Parameter | Description | Ayama 10000A-083 | | Ayama 10000A-100 | | Ayama 10000A-133 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{CLOCK}$ | CLK1X frequency | 50 | 83 | 50 | 100 | 50 | 133 | MHz |
| $t_{LOCK}$ | PLL lock time | | 0.5 | | 0.5 | | 0.5 | ms |
| $t_{CKHI}$ | CLK1X HIGH pulse; worst-case duty cycle[26] | 5.4 | | 4.5 | | 3.4 | | ns |
| $t_{CKLO}$ | CLK1X LOW pulse; worst-case duty cycle[26] | 5.4 | | 4.5 | | 3.4 | | ns |
| $t_{ISCH}$ | Input set-up time to CLK1X edge[26] | 1.8 | | 1.5 | | 1.3 | | ns |
| $t_{IHCH}$ | Input hold time to CLK1X edge[26] | 0.6 | | 0.5 | | 0.3 | | ns |
| $t_{ISCH\_CMD}$ | CMD & CMDV Input set-up time to CLK1X edge[26] | 1.8 | | 1.5 | | 1.5 | | ns |
| $t_{ICSCH}$ | Cascaded input set-up time to CLK1X rising edge[27, 29] | | | | | | | |
| $t_{ICSCH\_HIT}$ | LHI, BHI signals | 4.5 | | 4 | | 3.5 | | ns |
| $t_{ICSCH\_FUL}$ | FULI signals | 1.8 | | 1.5 | | 1.4 | | ns |
| $t_{ICHCH}$ | Cascaded input hold time to CLK1X rising edge[27, 29] | | | | | | | |
| $t_{ICHCH\_HIT}$ | LHI, BHI signals | 0 | | 0 | | 0 | | ns |
| $t_{ICHCH\_FUL}$ | FULI signals | 0.8 | | 0.7 | | 0.5 | | ns |
| $t_{CKHOV}$ | Edge of CLK1X to cascade output valid[27, 28] | | | | | | | |
| $t_{CKHOV\_HIT}$ | LHO, BHO signals | | 3.9 | | 3.4 | | 2.6 | ns |
| $t_{CKHOV\_FUL}$ | FULO signals | | 7 | | 6.5 | | 5.8 | ns |
| $t_{CKCOH}$ | Edge of CLK1X to cascade output invalid (output hold)[30] | | | | | | | |
| $t_{CKCOH\_HIT}$ | LHO, BHO signals | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{CKCOH\_FUL}$ | FULO signals | 1.2 | | 1.2 | | 1.2 | | ns |
| $t_{CKHOVFE}$ | Edge of CLK1X to FULL signal valid (Enhanced mode) | | 3.5 | | 3.0 | | 2.6 | ns |
| $t_{CKHOV\_FNE}$ | Rising edge of CLK1X to FULL signal valid (Non-Enhanced mode) | | 7 | | 6.5 | | 5.8 | ns |
| $t_{CKCOHFE}$ | Edge of CLK1X to FULL invalid (Enhanced mode)[30] | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{CKCOH\_FNE}$ | Rising edge of CLK1X to FULL invalid (Non-Enhanced mode)[30] | 1.2 | | 1.2 | | 1 | | ns |
| $t_{CKHDV}$ | Rising edge of CLK1X to DQ valid[26] | | 3.5 | | 3.0 | | 2.6 | ns |
| $t_{CKHDZ}$ | Rising edge of CLK1X to DQ High-Z[26, 30] | 0.5 | 1.8 | 0.5 | 1.8 | 0.5 | 1.8 | ns |
| $t_{CKHSV}$ | Edge of CLK1X to SRAM bus valid.[26] | | 3.5 | | 3.0 | | 2.8 | ns |
| $t_{CKHSHZ}$ | Edge of CLK1X to SRAM bus High-Z.[26, 30] | 0.5 | 1.8 | 0.5 | 1.8 | 0.5 | 1.8 | ns |
| $t_{CKHSLZ}$ | Edge of CLK1X to SRAM bus Low-Z.[26, 30] | 1.9 | | 1.9 | | 1.9 | | ns |
| $t_{OH}$ | Rising edge of CLK1X to DQ or SRAM bus invalid (output hold) | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{RSTL}$ | Minimum LOW pulse width for RST_L | 100 | | 100 | | 100 | | us |

**Table 10-3. JTAG Timing Parameters**

| Parameter | Description | Ayama 10000A-083 | | Ayama 10000A-100 | | Ayama 10000A-133 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{JTAG}$ | Maximum JTAG TAP Controller Frequency | | 10 | | 10 | | 10 | MHz |
| $t_{TCYC}$ | TCK Clock Cycle Time | 100 | | 100 | | 100 | | ns |
| $t_{IH}$ | TCK Clock HIGH Time | 40 | | 40 | | 40 | | ns |
| $t_{TL}$ | TCK Clock LOW Time | 40 | | 40 | | 40 | | ns |
| $t_{TMSS}$ | TMS Set-up to TCK Clock Rise | 10 | | 10 | | 10 | | ns |
| $t_{TMSH}$ | TMS Hold After TCK Clock Rise | 10 | | 10 | | 10 | | ns |
| $t_{TDIS}$ | TDI Set-up to TCK Clock Rise | 10 | | 10 | | 10 | | ns |
| $t_{TDIH}$ | TDI Hold After TCK Clock Rise | 10 | | 10 | | 10 | | ns |
| $t_{TDOV}$ | TCK Clock LOW to TDO Valid | | 10 | | 10 | | 10 | ns |
| $t_{TDOX}$ | TCK Clock LOW to TDO Invalid | 0 | | 0 | | 0 | | ns |




Timing Group 1: PARERR_L

Timing Group 2: DQ, PAR, ACK, EOT, MULTI_HIT

Timing Group 3: CMD[0:10], CMDV

Timing Group 4: LHI, BHI, LHO, BHO

Timing Group 5: FULI, FULO

Timing Group 6:FULL (ENHANCED)

Timing Group 7: FULL (NON-ENHANCED)

Timing Group 8: SADR, CE_L, OE_L, WE_L, ALE_L, SSF, SSV

**Figure 10-2. AC Timing Waveforms with CLK1X**

## 10.3 AC Test Conditions and Output Loads

The following test conditions are the equivalent of the actual tester measurement condition. The effect of transmission line is removed from the results.

### *10.3.1 HSTL I/II*

**Table 10-4. 1.5V AC Table for HSTL Test Condition of Ayama 10000A**

| Conditions | Results |
|---|---|
| Input pulse levels | 0.25 to 1.25V |
| Input rise and fall times measured at 20% and 80% of input pulse | Faster than 1 V/ns (see *Figure 10-3*) |
| Input timing reference levels | 0.75V |
| Output reference levels | 0.75V |

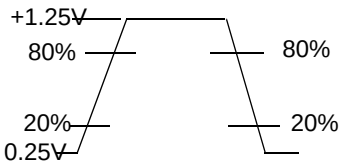



**Figure 10-3. HSTL I/II I/O Input Waveform**

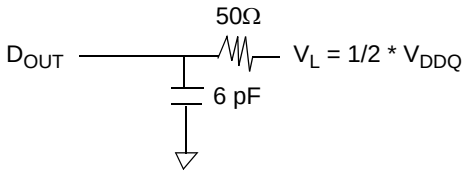



**Figure 10-4. Test Condition of HSTL I I/O Output Load Equivalent**

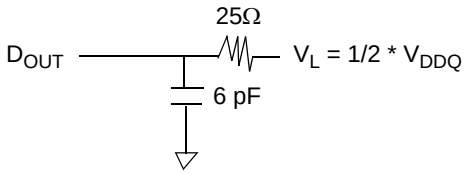



**Figure 10-5. Test Condition of HSTL II I/O Output Load Equivalent**

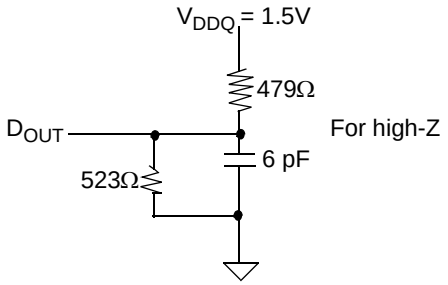



**Figure 10-6. Test Condition of HSTLI/II I/O High-Z Output Load Equivalent**

### *10.3.2 LVCMOS 2.5V/1.8V*

**Table 10-5. 2.5V / 1.8V AC Table for LVCMOS Test Condition of Ayama 10000A**

| Conditions | Results |
|---|---|
| Input pulse levels | GND to 2.5V/1.8V |
| Input rise and fall times measured for 2.5V LVCMOS at 0.25V and 2.25V | ≤ 1.2 ns (see *Figure 10-7*) |
| Input rise and fall times measured for 1.8V LVCMOS at 0.18V and 1.98V | ≤ 1.2 ns (see *Figure 10-7*) |
| Input timing reference levels (2.5V/1.8V) | 1.25V/0.9V |
| Output reference levels (2.5V/1.8V) | 1.25V/0.9V |

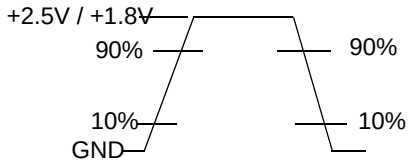



**Figure 10-7. LVCMOS I/O Input Waveform**

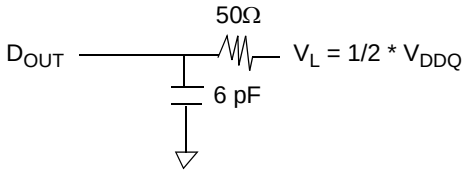



**Figure 10-8. Test Condition of 2.5V LVCMOS I/O Output Load Equivalent**

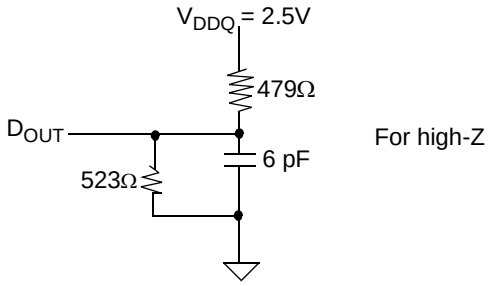



**Figure 10-9. Test Condition of 2.5V High-Z LVCMOS I/O Output Load Equivalent**

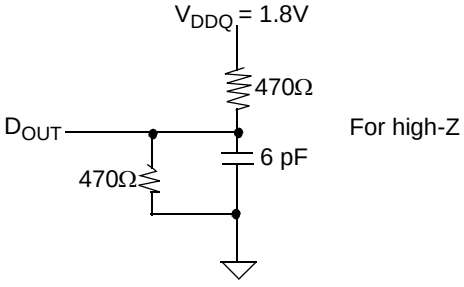



**Figure 10-10. Test Condition of 1.8V High-Z LVCMOS I/O Output Load Equivalent**

## 11.0 Pin Assignment and Pinout Diagram

*Figure 11-1* shows the pinout diagram and *Table 11-1* lists the pins assignment for Ayama 10000A.

| | AF | AE | AD | AC | AB | AA | Y | W | V | U | T | R | P | N | M | L | K | J | H | G | F | E | D | C | B | A | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | NC | GH_SPEED | RST_L | VSS | FULL | FULO[1] | FULI[6] | VDDQ_A | FULI[2] | FULI[0] | BHO[2] | VDDQ_A | BHO[0] | BHI[1] | VDDQ_A | LHO[0] | LHI[6] | LHI[2] | LHI[0] | ID[3] | ID[1] | ID[0] | TRST_L | TCK | TDI | NC | 1 |
| 2 | NC | VSS | VDDQ_A | EOT | ACK | ASICSEL | FULO[0] | FULI[5] | FULI[3] | VDDQ_A | VSS | BHO[1] | MULTI_HIT | BHI[2] | BHI[0] | LHO[1] | LHI[4] | LHI[3] | LHI[1] | ID[4] | ID[2] | VDDQ_J | TDO | TMS | VSS | DQ[71] | 2 |
| 3 | DQ[68] | DQ[70] | VDD | VDD | VDD | VDD | VDD | NC | FULI[4] | FULI[1] | VDD | VDD | VDD | VDD | VDD | VDD | LHI[5] | VDDQ_A | PARERR_L | VDD | VDD | VDD | VDD | VDD | DQ[69] | VDDQ_A | 3 |
| 4 | DQ[66] | VDDQ_A | VDD | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VDD | VDD | VDD | VDD | VDD | VDD | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VDD | DQ[65] | DQ[67] | 4 |
| 5 | DQ[62] | DQ[64] | VDD | VSS | | | | | | | | | | | | | | | | | | | VSS | VDD | DQ[61] | DQ[63] | 5 |
| 6 | VDDQ_A | DQ[60] | VDD | VSS | | | | | | | | | | | | | | | | | | | VSS | VDD | DQ[59] | VDDQ_A | 6 |
| 7 | DQ[56] | DQ[58] | VDD | VSS | | | | | | | | | | | | | | | | | | | VSS | VDD | DQ[55] | DQ[57] | 7 |
| 8 | DQ[52] | DQ[54] | HSVREF0 | VSS | | | | | | | | | | | | | | | | | | | VSS | HSVREF1 | VDDQ_A | DQ[53] | 8 |
| 9 | DQ[48] | DQ[50] | VDDQ_A | VSS | | | | | | | | | | | | | | | | | | | VSS | DQ[49] | DQ[47] | DQ[51] | 9 |
| 10 | VDDQ_A | DQ[44] | DQ[46] | VSS | | | | | | | | | | | | | | | | | | | VSS | VDDQ_A | DQ[45] | DQ[43] | 10 |
| 11 | DQ[40] | DQ[42] | VDD | VDD | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | VDD | VDD | DQ[39] | DQ[41] | 11 |
| 12 | DQ[36] | DQ[38] | VDD | VDD | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | VDD | VDD | VDDQ_A | DQ[37] | 12 |
| 13 | DQ[34] | VDDQ_A | VDD | VDD | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | VDD | VDD | DQ[33] | DQ[35] | 13 |
| 14 | DQ[30] | DQ[32] | VDD | VDD | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | VDD | VDD | DQ[29] | DQ[31] | 14 |
| 15 | VDDQ_A | DQ[28] | VDD | VDD | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | VDD | VDD | DQ[27] | VDDQ_A | 15 |
| 16 | DQ[24] | DQ[26] | VDD | VDD | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | VDD | VDD | DQ[23] | DQ[25] | 16 |
| 17 | DQ[22] | VDDQ_A | DQ[20] | VSS | | | | | | | | | | | | | | | | | | | VSS | DQ[19] | VDDQ_A | DQ[21] | 17 |
| 18 | DQ[14] | DQ[18] | DQ[16] | VSS | | | | | | | | | | | | | | | | | | | VSS | DQ[13] | DQ[15] | DQ[17] | 18 |
| 19 | VDDQ_A | DQ[12] | PAR[0] | VSS | | | | | | | | | | | | | | | | | | | VSS | PAR[1] | DQ[11] | VDDQ_A | 19 |
| 20 | DQ[8] | DQ[10] | VDD | VSS | | | | | | | | | | | | | | | | | | | VSS | VDD | DQ[7] | DQ[9] | 20 |
| 21 | DQ[4] | DQ[6] | VDD | VSS | | | | | | | | | | | | | | | | | | | HIGH_SPEED | VDD | VDDQ_A | DQ[5] | 21 |
| 22 | DQ[2] | VDDQ_A | VDD | VSS | | | | | | | | | | | | | | | | | | | VSS | VDD | DQ[1] | DQ[3] | 22 |
| 23 | SSV | DQ[0] | VDD | VSS | VSS | VSS | VSS | VSS | VSS | VSS_PLL | VDD | VDD | VDD | VDD | VDD | VDD | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VDD | VSS | VSS | 23 |
| 24 | SSF | VDDQ_A | VDD | VDD | VDD | VDD | VDD | SADR[24] | CE_L | OE_L | VDD_PLL | VDD | VDD | VDD | VDD | VDD | SADR[13] | SADR[11] | SADR[25] | VDD | VDD | VDD | VDD | VDD | CFG_L | SRAMSEL | 24 |
| 25 | CMD[10] | VSS | CMD[8] | CMD[6] | CMD[5] | CMD[3] | CMD[1] | CMDV | VDDQ_S | PHS_L | CLK_MODE | SADR[22] | SADR[21] | SADR[19] | VDDQ_S | SADR[15] | VDDQ_S | SADR[12] | VDDQ_S | SADR[8] | SADR[6] | SADR[5] | SADR[3] | SADR[1] | VSS | GH_SPEED | 25 |
| 26 | CMD[9] | NC | CMD[7] | VDDQ_A | CMD[4] | CMD[2] | CMD[0] | ALE_L | WE_L | K1X/ CLK2 | SADR[23] | VDDQ_S | SADR[20] | SADR[18] | SADR[17] | SADR[16] | SADR[14] | SADR[10] | SADR[9] | SADR[7] | VDDQ_S | SADR[4] | SADR[2] | VDDQ_S | SADR[0] | NC | 26 |
| | AF | AE | AD | AC | AB | AA | Y | W | V | U | T | R | P | N | M | L | K | J | H | G | F | E | D | C | B | A | |

**Figure 11-1. Pinout Diagram (Top View)**

**Table 11-1. Pin Assignment**

| Package Ball Number | Signal Name | Signal Type | Package Ball Number | Signal Name | Signal Type |
|---|---|---|---|---|---|
| A1 | NC | NO CONNECT | AA26 | CMD[2] | INPUT |
| A10 | DQ[43] | I/O | AA3 | $V_{DD}$ | 1.2V |
| A11 | DQ[41] | I/O | AA4 | $V_{SS}$ | GND |
| A12 | DQ[37] | I/O | AB1 | FULL | OUTPUT-T |
| A13 | DQ[35] | I/O | AB2 | ACK | OUTPUT-T |
| A14 | DQ[31] | I/O | AB23 | $V_{SS}$ | GND |
| A15 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | AB24 | $V_{DD}$ | 1.2V |
| A16 | DQ[25] | I/O | AB25 | CMD[5] | INPUT |
| A17 | DQ[21] | I/O | AB26 | CMD[4] | INPUT |
| A18 | DQ[17] | I/O | AB3 | $V_{DD}$ | 1.2V |
| A19 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | AB4 | $V_{SS}$ | GND |
| A2 | DQ[71] | I/O | AC1 | $V_{SS}$ | GND |
| A20 | DQ[09] | I/O | AC10 | $V_{SS}$ | GND |
| A21 | DQ[05] | I/O | AC11 | $V_{DD}$ | 1.2V |
| A22 | DQ[03] | I/O | AC12 | $V_{DD}$ | 1.2V |
| A23 | $V_{SS}$ | GND | AC13 | $V_{DD}$ | 1.2V |
| A24 | SRAMSEL | $V_{DDQ\_SRAM}/V_{SS}$ | AC14 | $V_{DD}$ | 1.2V |
| A25 | HIGH_SPEED1 | INPUT | AC15 | $V_{DD}$ | 1.2V |
| A26 | NC | NO CONNECT | AC16 | $V_{DD}$ | 1.2V |
| A3 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | AC17 | $V_{SS}$ | GND |
| A4 | DQ[67] | I/O | AC18 | $V_{SS}$ | GND |
| A5 | DQ[63] | I/O | AC19 | $V_{SS}$ | GND |
| A6 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | AC2 | EOT | OUTPUT-T |
| A7 | DQ[57] | I/O | AC20 | $V_{SS}$ | GND |
| A8 | DQ[53] | I/O | AC21 | $V_{SS}$ | GND |
| A9 | DQ[51] | I/O | AC22 | $V_{SS}$ | GND |
| AA1 | FULO[1][31] | OUTPUT-T | AC23 | $V_{SS}$ | GND |
| AA2 | ASICSEL | $V_{DDQ\_ASIC}/V_{SS}$ | AC24 | $V_{DD}$ | 1.2V |
| AA23 | $V_{SS}$ | GND | AC25 | CMD[6] | INPUT |
| AA24 | $V_{DD}$ | 1.2V | AC26 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| AA25 | CMD[3] | INPUT | AC3 | $V_{DD}$ | 1.2V |
| AC4 | $V_{SS}$ | GND | AE10 | DQ[44] | I/O |
| AC5 | $V_{SS}$ | GND | AE11 | DQ[42] | I/O |
| AC6 | $V_{SS}$ | GND | AE12 | DQ[38] | I/O |
| AC7 | $V_{SS}$ | GND | AE13 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| AC8 | $V_{SS}$ | GND | AE14 | DQ[32] | I/O |
| AC9 | $V_{SS}$ | GND | AE15 | DQ[28] | I/O |
| AD1 | RST_L | INPUT | AE16 | DQ[26] | I/O |
| AD10 | DQ[46] | I/O | AE17 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| AD11 | $V_{DD}$ | 1.2V | AE18 | DQ[18] | I/O |
| AD12 | $V_{DD}$ | 1.2V | AE19 | DQ[12] | I/O |
| AD13 | $V_{DD}$ | 1.2V | AE2 | $V_{SS}$ | GND |

**Note:**
31. When JTAG is not enabled, this pin always drives a 0 or 1.

**Table 11-1. Pin Assignment** (continued)

| Package Ball Number | Signal Name | Signal Type | Package Ball Number | Signal Name | Signal Type |
|---|---|---|---|---|---|
| AD14 | $V_{DD}$ | 1.2V | AE20 | DQ[10] | I/O |
| AD15 | $V_{DD}$ | 1.2V | AE21 | DQ[06] | I/O |
| AD16 | $V_{DD}$ | 1.2V | AE22 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| AD17 | DQ[20] | I/O | AE23 | DQ[00] | I/O |
| AD18 | DQ[16] | I/O | AE24 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| AD19 | PAR[0] | I/O | AE25 | $V_{SS}$ | GND |
| AD2 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | AE26 | NC | NO CONNECT |
| AD20 | $V_{DD}$ | 1.2V | AE3 | DQ[70] | I/O |
| AD21 | $V_{DD}$ | 1.2V | AE4 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| AD22 | $V_{DD}$ | 1.2V | AE5 | DQ[64] | I/O |
| AD23 | $V_{DD}$ | 1.2V | AE6 | DQ[60] | I/O |
| AD24 | $V_{DD}$ | 1.2V | AE7 | DQ[58] | I/O |
| AD25 | CMD[8] | INPUT | AE8 | DQ[54] | I/O |
| AD26 | CMD[7] | INPUT | AE9 | DQ[50] | I/O |
| AD3 | $V_{DD}$ | 1.2V | AF1 | NC | NO CONNECT |
| AD4 | $V_{DD}$ | 1.2V | AF10 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V2.5V |
| AD5 | $V_{DD}$ | 1.2V | AF11 | DQ[40] | I/O |
| AD6 | $V_{DD}$ | 1.2V | AF12 | DQ[36] | I/O |
| AD7 | $V_{DD}$ | 1.2V | AF13 | DQ[34] | I/O |
| AD8 | HSVREF0 | INPUT | AF14 | DQ[30] | I/O |
| AD9 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | AF15 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V2.5V |
| AE1 | HIGH_SPEEDI_L | INPUT | AF16 | DQ[24] | I/O |
| AF17 | DQ[22] | I/O | B23 | $V_{SS}$ | GND |
| AF18 | DQ[14] | I/O | B24 | CFG_L | INPUT |
| AF19 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | B25 | $V_{SS}$ | GND |
| AF2 | NC | NO CONNECT | B26 | SADR[0] | OUTPUT-T |
| AF20 | DQ[08] | I/O | B3 | DQ[69] | I/O |
| AF21 | DQ[04] | I/O | B4 | DQ[65] | I/O |
| AF22 | DQ[02] | I/O | B5 | DQ[61] | I/O |
| AF23 | SSV | OUTPUT-T | B6 | DQ[59] | I/O |
| AF24 | SSF | OUTPUT-T | B7 | DQ[55] | I/O |
| AF25 | CMD[10] | INPUT | B8 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V2.5V |
| AF26 | CMD[9] | INPUT | B9 | DQ[47] | I/O |
| AF3 | DQ[68] | I/O | C1 | TCK | INPUT |
| AF4 | DQ[66] | I/O | C10 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V2.5V |
| AF5 | DQ[62] | I/O | C11 | $V_{DD}$ | 1.2V |
| AF6 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | C12 | $V_{DD}$ | 1.2V |
| AF7 | DQ[56] | I/O | C13 | $V_{DD}$ | 1.2V |
| AF8 | DQ[52] | I/O | C14 | $V_{DD}$ | 1.2V |
| AF9 | DQ[48] | I/O | C15 | $V_{DD}$ | 1.2V |
| B1 | TDI[32] | INPUT | C16 | $V_{DD}$ | 1.2V |
| B10 | DQ[45] | I/O | C17 | DQ[19] | I/O |

**Note:**
32. This pin has an internal pull-up of approximately 5 KOhms.

**Table 11-1. Pin Assignment** (continued)

| Package Ball Number | Signal Name | Signal Type | Package Ball Number | Signal Name | Signal Type |
|---|---|---|---|---|---|
| B11 | DQ[39] | I/O | C18 | DQ[13] | I/O |
| B12 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | C19 | PAR[1] | I/O |
| B13 | DQ[33] | I/O | C2 | TMS[32] | INPUT |
| B14 | DQ[29] | I/O | C20 | $V_{DD}$ | 1.2V |
| B15 | DQ[27] | I/O | C21 | $V_{DD}$ | 1.2V |
| B16 | DQ[23] | I/O | C22 | $V_{DD}$ | 1.2V |
| B17 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | C23 | $V_{DD}$ | 1.2V |
| B18 | DQ[15] | I/O | C24 | $V_{DD}$ | 1.2V |
| B19 | DQ[11] | I/O | C25 | SADR[1] | OUTPUT-T |
| B2 | $V_{SS}$ | GND | C26 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V |
| B20 | DQ[7] | I/O | C3 | $V_{DD}$ | 1.2V |
| B21 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | C4 | $V_{DD}$ | 1.2V |
| B22 | DQ[1] | I/O | C5 | $V_{DD}$ | 1.2V |
| C6 | $V_{DD}$ | 1.2V | E24 | $V_{DD}$ | 1.2V |
| C7 | $V_{DD}$ | 1.2V | E25 | SADR[5] | OUTPUT-T |
| C8 | HSVREF1 | INPUT | E26 | SADR[4] | OUTPUT-T |
| C9 | DQ[49] | I/O | E3 | $V_{DD}$ | 1.2V |
| D1 | TRST_L[32] | INPUT | E4 | $V_{SS}$ | GND |
| D10 | $V_{SS}$ | GND | F1 | ID[1] | INPUT |
| D11 | $V_{DD}$ | 1.2V | F2 | ID[2] | INPUT |
| D12 | $V_{DD}$ | 1.2V | F23 | $V_{SS}$ | GND |
| D13 | $V_{DD}$ | 1.2V | F24 | $V_{DD}$ | 1.2V |
| D14 | $V_{DD}$ | 1.2V | F25 | SADR[6] | OUTPUT-T |
| D15 | $V_{DD}$ | 1.2V | F26 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V |
| D16 | $V_{DD}$ | 1.2V | F3 | $V_{DD}$ | 1.2V |
| D17 | $V_{SS}$ | GND | F4 | $V_{SS}$ | GND |
| D18 | $V_{SS}$ | GND | G1 | ID[3] | INPUT |
| D19 | $V_{SS}$ | GND | G2 | ID[4] | INPUT |
| D2 | TDO | OUTPUT-T | G23 | $V_{SS}$ | GND |
| D20 | $V_{SS}$ | GND | G24 | $V_{DD}$ | 1.2V |
| D21 | HIGH_SPEED2 | INPUT | G25 | SADR[8] | OUTPUT-T |
| D22 | $V_{SS}$ | GND | G26 | SADR[7] | OUTPUT-T |
| D23 | $V_{SS}$ | GND | G3 | $V_{DD}$ | 1.2V |
| D24 | $V_{DD}$ | 1.2V | G4 | $V_{SS}$ | GND |
| D25 | SADR[3] | OUTPUT-T | H1 | LHI[0] | INPUT |
| D26 | SADR[2] | OUTPUT-T | H2 | LHI[1] | INPUT |
| D3 | $V_{DD}$ | 1.2V | H23 | $V_{SS}$ | GND |
| D4 | $V_{SS}$ | GND | H24 | SADR[25][33] | OUTPUT-T |
| D5 | $V_{SS}$ | GND | H25 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V |
| D6 | $V_{SS}$ | GND | H26 | SADR[9] | OUTPUT-T |
| D7 | $V_{SS}$ | GND | H3 | PARERR_L | OUTPUT-Open Drain |

**Note:**
33. No-Connect in CYNSE10256A and CYNSE10128A.

**Table 11-1. Pin Assignment** (continued)

| Package Ball Number | Signal Name | Signal Type | Package Ball Number | Signal Name | Signal Type |
|---|---|---|---|---|---|
| D8 | $V_{SS}$ | GND | H4 | $V_{SS}$ | GND |
| D9 | $V_{SS}$ | GND | J1 | LHI[2] | INPUT |
| E1 | ID[0] | INPUT | J2 | LHI[3] | INPUT |
| E2 | $V_{DDQ\_JTAG}$ | 1.8V/2.5V | J23 | $V_{SS}$ | GND |
| E23 | $V_{SS}$ | GND | J24 | SADR[11] | OUTPUT-T |
| J25 | SADR[12] | OUTPUT-T | M2 | BHI[0] | INPUT |
| J26 | SADR[10] | OUTPUT-T | M23 | $V_{DD}$ | 1.2V |
| J3 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | M24 | $V_{DD}$ | 1.2V |
| J4 | $V_{SS}$ | GND | M25 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V |
| K1 | LHI[6] | INPUT | M26 | SADR[17] | OUTPUT-T |
| K2 | LHI[4] | INPUT | M3 | $V_{DD}$ | 1.2V |
| K23 | $V_{SS}$ | GND | M4 | $V_{DD}$ | 1.2V |
| K24 | SADR[13] | OUTPUT-T | N1 | BHI[1] | INPUT |
| K25 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V | N11 | $V_{SS}$ | GND |
| K26 | SADR[14] | OUTPUT-T | N12 | $V_{SS}$ | GND |
| K3 | LHI[5] | INPUT | N13 | $V_{SS}$ | GND |
| K4 | $V_{SS}$ | GND | N14 | $V_{SS}$ | GND |
| L1 | LHO[0][31] | OUTPUT-T | N15 | $V_{SS}$ | GND |
| L11 | $V_{SS}$ | GND | N16 | $V_{SS}$ | GND |
| L12 | $V_{SS}$ | GND | N2 | BHI[2] | INPUT |
| L13 | $V_{SS}$ | GND | N23 | $V_{DD}$ | 1.2V |
| L14 | $V_{SS}$ | GND | N24 | $V_{DD}$ | 1.2V |
| L15 | $V_{SS}$ | GND | N25 | SADR[19] | OUTPUT-T |
| L16 | $V_{SS}$ | GND | N26 | SADR[18] | OUTPUT-T |
| L2 | LHO[1][31] | OUTPUT-T | N3 | $V_{DD}$ | 1.2V |
| L23 | $V_{DD}$ | 1.2V | N4 | $V_{DD}$ | 1.2V |
| L24 | $V_{DD}$ | 1.2V | P1 | BHO[0][31] | OUTPUT-T |
| L25 | SADR[15] | OUTPUT-T | P11 | $V_{SS}$ | GND |
| L26 | SADR[16] | OUTPUT-T | P12 | $V_{SS}$ | GND |
| L3 | $V_{DD}$ | 1.2V | P13 | $V_{SS}$ | GND |
| L4 | $V_{DD}$ | 1.2V | P14 | $V_{SS}$ | GND |
| M1 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | P15 | $V_{SS}$ | GND |
| M11 | $V_{SS}$ | GND | P16 | $V_{SS}$ | GND |
| M12 | $V_{SS}$ | GND | P2 | MULTI_HIT[31] | OUTPUT-T |
| M13 | $V_{SS}$ | GND | P23 | $V_{DD}$ | 1.2V |
| M14 | $V_{SS}$ | GND | P24 | $V_{DD}$ | 1.2V |
| M15 | $V_{SS}$ | GND | P25 | SADR[21] | OUTPUT-T |
| M16 | $V_{SS}$ | GND | P26 | SADR[20] | OUTPUT-T |
| P3 | $V_{DD}$ | 1.2V | U24 | OE_L | OUTPUT-T |
| P4 | $V_{DD}$ | 1.2V | U25 | PHS_L | INPUT |
| R1 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | U26 | CLK1X/CLK2X | INPUT |
| R11 | $V_{SS}$ | GND | U3 | FULI[1] | INPUT |
| R12 | $V_{SS}$ | GND | U4 | $V_{SS}$ | GND |

**Table 11-1. Pin Assignment** (continued)

| Package Ball Number | Signal Name | Signal Type | Package Ball Number | Signal Name | Signal Type |
|---|---|---|---|---|---|
| R13 | $V_{SS}$ | GND | V1 | FULI[2] | INPUT |
| R14 | $V_{SS}$ | GND | V2 | FULI[3] | INPUT |
| R15 | $V_{SS}$ | GND | V23 | $V_{SS}$ | GND |
| R16 | $V_{SS}$ | GND | V24 | CE_L | OUTPUT-T |
| R2 | BHO[1][31] | OUTPUT-T | V25 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V |
| R23 | $V_{DD}$ | 1.2V | V26 | WE_L | OUTPUT-T |
| R24 | $V_{DD}$ | 1.2V | V3 | FULI[4] | INPUT |
| R25 | SADR[22] | OUTPUT-T | V4 | $V_{SS}$ | GND |
| R26 | $V_{DDQ\_SRAM}$ | 1.5V/1.8V/2.5V | W1 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V |
| R3 | $V_{DD}$ | 1.2V | W2 | FULI[5] | INPUT |
| R4 | $V_{DD}$ | 1.2V | W23 | $V_{SS}$ | GND |
| T1 | BHO[2][31] | OUTPUT-T | W24 | SADR[24][34] | OUTPUT-T |
| T11 | $V_{SS}$ | GND | W25 | CMDV | INPUT |
| T12 | $V_{SS}$ | GND | W26 | ALE_L | OUTPUT-T |
| T13 | $V_{SS}$ | GND | W3 | NC | NO CONNECT |
| T14 | $V_{SS}$ | GND | W4 | $V_{SS}$ | GND |
| T15 | $V_{SS}$ | GND | Y1 | FULI[6] | INPUT |
| T16 | $V_{SS}$ | GND | Y2 | FULO[0][31] | OUTPUT-T |
| T2 | $V_{SS}$ | GND | Y23 | $V_{SS}$ | GND |
| T23 | $V_{DD}$ | 1.2V | Y24 | $V_{DD}$ | 1.2V |
| T24 | $V_{DD\_PLL}$ | 1.2V | Y25 | CMD[1] | INPUT |
| T25 | CLK_MODE | INPUT | Y26 | CMD[0] | INPUT |
| T26 | SADR[23] | OUTPUT-T | Y3 | $V_{DD}$ | 1.2V |
| T3 | $V_{DD}$ | 1.2V | Y4 | $V_{SS}$ | GND |
| T4 | $V_{DD}$ | 1.2V | | | |
| U1 | FULI[0] | INPUT | | | |
| U2 | $V_{DDQ\_ASIC}$ | 1.5V/1.8V/2.5V | | | |
| U23 | $V_{SS\_PLL}$ | GND | | | |

**Note:**
34. No-Connect in CYNSE10128A.

## 12.0 Ordering Information

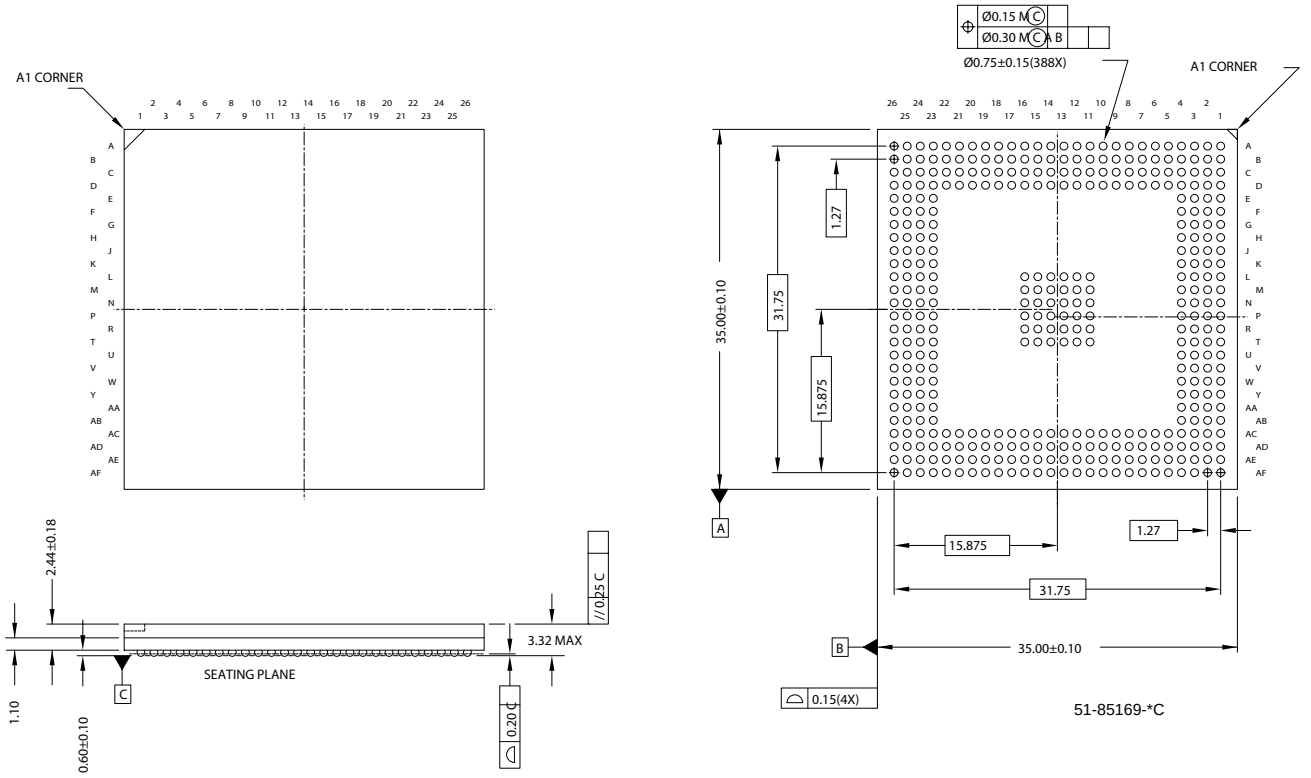
*Table 12-1* provides ordering information.

**Table 12-1. Ordering Information**

| Part Number | Description | I/O Voltage | Max. Freq. | Temp. Range |
|---|---|---|---|---|
| CYNSE10512A–83FGC | 83-MSPS 512K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 83 MHz | Comm |
| CYNSE10512A–100FGC | 100-MSPS 512K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 100 MHz | Comm |
| CYNSE10512A–133FGC | 133-MSPS 512K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 133 MHz | Comm |
| CYNSE10256A–83FGC | 83-MSPS 256K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 83 MHz | Comm |
| CYNSE10256A–100FGC | 100-MSPS 256K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 100 MHz | Comm |
| CYNSE10256A–133FGC | 133-MSPS 256K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 133 MHz | Comm |
| CYNSE10128A–083FGC | 83-MSPS 128K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 83 MHz | Comm |
| CYNSE10128A–100FGC | 100-MSPS 128K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 100 MHz | Comm |
| CYNSE10128A–133FGC | 133-MSPS 128K x 36-bit Entries NSE | 1.5V/1.8V/2.5V | 133 MHz | Comm |

## 13.0 Package Diagram

**388-Ball HFC-BGA FG388A**

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## Document History Page

| Document Title: CYNSE10512A/CYNSE10256A/CYNSE10128A Ayama 10000A Network Search Engine<br>Document Number: 38-02110 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 295472 | See ECN | CNG | New data sheet based on 38-02-069 with the following changes:<br>Added HIGH_SPEEDI_L to Signal Description List<br>Added note to clarify that FULL only comes on after a Missed search<br>Vddq_jtag can also be driven by 1.8V<br>Rewrote Section 5.1.2.4 to reflect multisearching behavior of new rev of silicon<br>Clarified usage of CMPRs for multisearching<br>Added new HIGHSPEED fields to the Hardware Register field description<br>Added Multi-width configuration field to the CPR description<br>Revised BPR description to reflect behavior of new rev of silicon<br>Modified figure 5-35 to illustrate eight CLK2x cycles of idle time is needed before device is functionally accessible<br>Revised 6.5.2 example that demonstrates Multisearching for single device<br>Removed section 6.5.4 in rev. *F; content already shown in section 6.5.7 in rev. *G<br>Removed section 6.5.7 in rev. *F; content already shown in section 6.5.7 in rev. *G<br>Changed Figure 6-69 to show that FULL signal should not comes on after a HIT<br>Added setup and hold time for PHS_L in *Table 10-1*. This is a new parameter. In older versions of this data sheet, this value is the same as $t_{ISCH}$ and $t_{IHCH}$<br>Changed parameters: $t_{ISCH}$, $t_{ICSCH\_FUL}$, $t_{CKHOV\_HIT}$, $t_{CKHOV\_FUL}$, $t_{CKCOH\_HIT}$, $t_{CKCOH\_FUL}$, $t_{CKHOVFE}$, $t_{CKHOV\_FNE}$, $t_{CKCOHFE}$, $t_{CKCOH\_FNE}$, $t_{CKHDV}$, $t_{CKHSV}$ and $t_{OH}$ from previous revision<br>Added footnotes 31, 32, 33, 34, 35<br>Added $t_{PSCH}$ and $t_{PHCH}$ in Figure 10-1<br>Changed parameters: $t_{ISCH}$, $t_{ICSCH\_FUL}$, $t_{CKHOV\_HIT}$, $t_{CKHOV\_FUL}$, $t_{CKCOH\_HIT}$, $t_{CKCOH\_FUL}$, $t_{CKHOVFE}$, $t_{CKHOV\_FNE}$, $t_{CKCOHFE}$, $t_{CKCOH\_FNE}$, $t_{CKHDV}$, $t_{CKHSV}$ and $t_{OH}$ from previous revision<br>Changed pin AE1 from VSS to HIGH_SPEEDI_L<br>Changed note 31 to note 36 and note 32 to note 37<br>Changed note 37 from “No-connect in 10256” to “No-connect in 10128” |
| *A | 393322 | See ECN | KMQ<br>CNG | Modified the HIGHSPEED field in the Hardware register description on Pg 33.<br>Changed $t_{CKHSV}$ for 133-MHz parts from 2.6ns to 2.8ns on Pg 128 and Pg 130.<br>Removed Industrial Temperature footnote 32 on page 128<br>Information Register (INFO) Initial Devise Revision number changed from 0001 to 0110 on page 30<br>Removed footnote 8 as it applied to legacy datasheet revision on page 48<br>Updated instances of Highspeed 1 and Highspeed 2 being pulled high based on CLK2X frequency to always being pulled high regardless of CLK2X frequency (Pages 15 and 28)<br>Added Hexadecimal addresses next to Decimal addresses to the Register Address Table on page 25<br>Updated signal type of Pin AA24 to 1.2V from 1.2 on Pin Assignment Table<br>Updated the fields in the BPRAs to 6 bits wide from 8 bits. Changes were made to Figure 5-26 and Tables 5-23, 5-24, 5-25, and 5-26<br>Updated parameters for: $t_{PSCH}$, $t_{ISCH}$ , $t_{ICSCH\_FUL}$, $t_{CKHSV}$ from previous revision in Table 10-1 and Table 10-2<br>Updated Power Consumption Figure 8-1 to reflect more accurate data<br>Added Table 8-1 to show how the Graph of Figure 8-1 is determined<br>Edited/Changed text in Section 8.0 in order to explain the use of HIGHSPEED when working with various levels in frequencies<br>Added a new section by inserting section 6.2.1 which explains EADR<br>Updated numerous tables, figures, and sectional paragraphs to more accurately reflect TLSZ<br>Changed the PARERR_L signal type to Output-Open Drain instead of Output<br>Added Operating $T_J$, $\Theta_{JC}$, and $\Theta_{JA}$ values to Table 9.3 (Operating Conditions for Ayama 10000A)<br>Created Table 9-2 by detaching capacitance component of Table 9-1 and making it a separate table<br>Updated Section 9.0 Maximum Ratings by including ESD HBM Model, removing ambient temperature with power applied, and changed storage from 125°C to 150°C<br>Changed entire layout of Figures 10-1 and 10-2 and modified groupings to increase accuracy and ease of use. |

## Document History Page (continued)

**Document Title: CYNSE10512A/CYNSE10256A/CYNSE10128A Ayama 10000A Network Search Engine**
**Document Number: 38-02110**

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| *A | 393322 | See ECN | KMQ CNG | Included PARERR_L into signal groupings with DQ in Figures 10-1 and 10-2.<br>Changed Figure 6-29 on page 83 to reflect 576 bits from bits 0 to 575 instead of 0 to 576.<br>Removed reference to blank “Figure” in section 6.3.3 Read Parity and replaced with paragraph to explain read parity.<br>Added fact of internal pull-up of approximately 5 kohms to JTAG pins in section 7.0 on page 125.<br>Changed ball AE1 in Figure 11-1 from VSS to HIGH_SPEEDI_L on page 135.<br>Changed REGSEL in Figure 5-31 to RSEL to remain consistent with Table 5-30<br>Changed description of Cycle 1 in sections 6.3.2 (Page 53) and 6.4.2 (Page 55), stating that the addresses is provided in the RBURREG and WBURREG register, respectively.<br>Modified Figure 6-2 and Figure 6-4 to reflect address not supplied on DQ bus.<br>Changed Figure 6-5 on page 57 to illustrate HLAT = 000, rather than HLAT = 001.<br>Included “note” to page 26 regarding block number specification for block registers.<br>Changed “INDEX” field to “ADDRESS” field in RBURREG and WBURREG.<br>Created new Figure 6-5 explaining search key format on DQ bus.<br>Removed footnotes 31-35 as restrictions are no longer valid<br>Performed various sectional formatting, re-phrasing, and order changes for better ease of flow<br>Corrected spelling and grammatical errors within document<br>Added description of GMR usage during Write commands in section 6.4 |
| *B | 421311 | See ECN | VSP/ TNT | Added the respective power to all the signals from Page 12 -14.<br>Added description to the CFG_L pin in Page 12<br>Added Note 14 in Page 51 with explanation of the CMPR and SSR field in CMD[10:0]<br>Corrected the sentence to “Each of the four A-cycles provide a GMR index to mask 144 bits of the data to be compared (each A-cycle provide a pair of GMR, which is 144 bits, four A-cycles will result in a total of 576 bits of GMR).” in Page 83.<br>Changed the title of Cascade interface to LVCMOS/HSTL I/II from LVCMOS/HSTL in Page 14<br>Added explanation for the behavior of the FULL signal during Write/Learn in Page 13 in Signal description<br>Corrected Figure 5-12 so that it has the same DEVID width for various devices<br>Added Table 6-14 in Page 106 and also explanation for calculation of latency during a learn command<br>Changed the GMR description in Page 27 to “When the device powers-up, the GMR registers are initialized to 0. Figure 5-9 below shows each portion (Even, Odd) of each GMR, and what address (in Decimal) is required to access that register.”<br>Corrected the EADR field in Page 50.This has been changed to SADR[25:23] for CYNSE10512A, SADR[24:22] for CYNSE10256A, and SADR[23:20] for CYNSE10128A from SADR[17:15],SADR[16:14],SADR[15:13] respectively<br>Removed the sentence “Learn operations with the address taken from the DQ bus... DQ bus contains the address instead of Don't Cares” in Page 104<br>Changed the Note in Page 21 to focus the discussion on x144 and x288 searches.<br>Added small description of HLAT field behavior in associative data mode<br>Added a small note for the CPR multi-width field which is a don’t care for a single search in Page 35<br>Corrected the description of SRR field in Page 36. There was a mention of SSR in the description which was a typo<br>Figure 6-6: Changed the HLAT and TLSZ values to 001 and 01 respectively in Page 58<br>Figure 6-8: Changed TLSZ to be 01 in Page 60<br>Figure 6-49: Changed the TLSZ value to 01 and added one other SADR address A2 in cycle 9 and corrected the OE_L, CE_L, ALE_L, values in Page 106<br>Figure 6-50: Changed the figure to suit the TLSZ value and the added changes to the CE_L, ALE_L, WE_L and OLE_L signals. Added other address A2 for the CMPR register in Page 107.<br>Figure 6-63: Changed the TLSZ value to 00 instead of 01 in Page 119 |