

## LOW SKEW, 1-TO-5, DIFFERENTIAL-TO-HSTL FANOUT BUFFER

ICS85214

# **General Description**



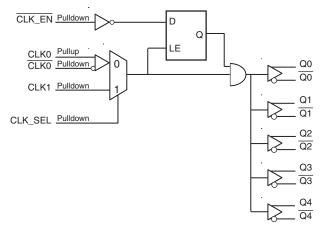
The ICS85214 is a low skew, high performance 1-to-5 Differential-to-HSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK0, CLK0 pair can accept most standard differential

input levels. The single ended CLK1 input accepts LVCMOS or LVTTL input levels. Guaranteed output and part-to-part skew characteristics make the ICS85214 ideal for those clock distribution applications demanding well defined performance and repeatability.

### **Features**

- Five differential HSTL compatible outputs
- Selectable differential CLK0, CLK0 or LVCMOS/LVTTL clock inputs
- CLK0, CLK0 pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- CLK1 can accept the following input levels: LVCMOS or LVTTL
- Output frequency up to: 700MHz
- Translates any single-ended input signal to HSTL levels with resistor bias on CLK0 input
- Output skew: 30ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.8ns (maximum)
- 3.3V core, 1.8V output operating supply
- 0°C to 85°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

# **Block Diagram**



# **Pin Assignment**

1 2 3 4 5	20 19 18 17 16 15	VDDO CLK_EN VDD nc CLK1 CLK0
4	17	□nc
5	16	□CLK1
6	15	□CLK0
7	14	□ CLK0
8	13	□nc
9	12	CLK_SEL
10	11	□GND
	3 4 5 6 7 8	2 19 3 18 4 17 5 16 6 15 7 14 8 13 9 12

ICS85214
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body
G Package
Top View

**Table 1. Pin Descriptions** 

Number	Name	Т	уре	Description
1, 2	Q0, Q0	Output		Differential output pair. HSTL interface levels.
3, 4	Q1, <u>Q1</u>	Output		Differential output pair. HSTL interface levels.
5, 6	Q2, <u>Q2</u>	Output		Differential output pair. HSTL interface levels.
7, 8	Q3, <del>Q3</del>	Output		Differential output pair. HSTL interface levels.
9, 10	Q4, <del>Q4</del>	Output		Differential output pair. HSTL interface levels.
11	GND	Power		Power supply ground.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects differential CLK1input. When LOW, selects CLK0, CLK0 inputs. LVCMOS/LVTTL interface levels.
13, 17	nc	Unused		No connect.
14	CLK0	Input	Pullup	Inverting differential clock input.
15	CLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
16	CLK1	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
18	$V_{DD}$	Power		Positive supply pin.
19	CLK_EN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Qx outputs are forced low, $\overline{Qx}$ outputs are forced high. LVTTL/LVCMOS interface levels.
20	$V_{DDO}$	Power		Output supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

## **Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## **Function Tables**

**Table 3A. Control Input Function Table** 

Inputs	Outputs			
CLK_EN	Q0:Q4	Q0:Q4		
0	Enabled	Enabled		
1	Disabled; LOW	Disabled; HIGH		

After  $\overline{\text{CLK\_EN}}$  switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK0,  $\overline{\text{CLK0}}$  inputs as described in Table 3B.

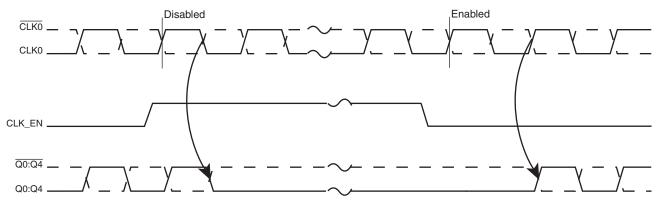


Figure 1. CLK\_EN Timing Diagram

**Table 3B. Clock Input Function Table** 

In	puts	Outputs			
CLK0 or CLK1	CLK0	Q[0:4]	Q[0:4]	Input to Output Mode	Polarity
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, Wiring the Differential Input to Accept Single-Ended Levels.

# **Absolute Maximum Ratings**

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V <sub>DD</sub>	4.6V
Inputs, V <sub>I</sub>	-0.5V to V <sub>DD</sub> + 0.5V
Outputs, V <sub>DDO</sub>	-0.5V to V <sub>DD</sub> + 0.5V
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, T <sub>STG</sub>	-65°C to 150°C

## **DC Electrical Characteristics**

Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0$ °C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
I <sub>DD</sub>	Power Supply Current				80	mA

Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0$ °C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage			2		$V_{DD} + 0.3$	V
V <sub>IL</sub>	Input Low Voltage			-0.3		0.8	٧
I <sub>IH</sub>	Input High Current	CLK1, CLK_EN, CLK_SEL	$V_{DD} = V_{IN} = 3.465V$			150	μΑ
I <sub>IL</sub>	Input Low Current	CLK1, CLK_EN, CLK_SEL	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0V	-5			μΑ

Table 4C. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0$ °C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$			5	μΑ
IH	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$			150	μΑ
	Input Low Current	CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			μΑ
I <sub>IL</sub>	Input Low Current	CLK	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0V	-5			μΑ
V <sub>PP</sub>	Peak-to-Peak Volta	ge; NOTE 1		0.15		1.3	V
V <sub>CMR</sub>	Common Mode Inp NOTE 1, 2	ut Voltage;		0.5		V <sub>DD</sub> – 0.85	V

NOTE 1: V<sub>IL</sub> should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

Table 4D. HSTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0$ °C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>OH</sub>	Output High Current; NOTE 1		1.0		1.4	V
V <sub>OL</sub>	Output Low Current; NOTE 1		0		0.4	V
V <sub>OX</sub>	Output Crossover Voltage		38% x (V <sub>OH</sub> – V <sub>OL</sub> ) + V <sub>OL</sub>		60% x (V <sub>OH</sub> – V <sub>OL</sub> ) + V <sub>OL</sub>	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs termination with  $50\Omega$  to ground.

## **AC Electrical Characteristics**

Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0$ °C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f	Output Frequency	CLK0, CLK0				700	MHz
f <sub>MAX</sub>	Output Frequency	CLK1				300	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1		<i>f</i> ≤ 700MHz	1.0		1.8	ns
tsk(o)	Output Skew; NOTE 2, 4					30	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4					250	ps
t <sub>R</sub> / t <sub>F</sub>	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK0, CLK0		46		54	%
ouc	Output Duty Cycle	CLK1		45		55	%

All parameters measured at <sub>fMAX</sub> unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from either the differential input crossing point or VDD/2 to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

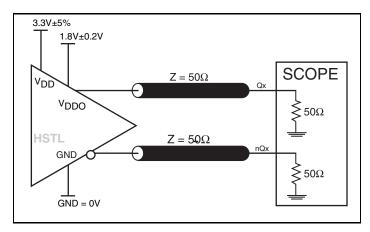
Measured at output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.

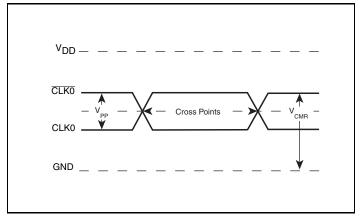
Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65. Parameter Measurement Information

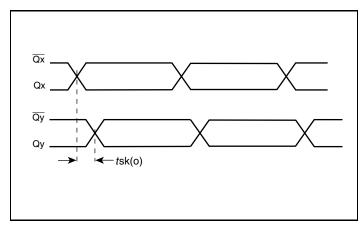
## **Parameter Measurement Information**



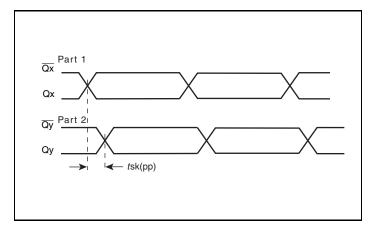
3.3V/1.8V Output Load AC Test Circuit



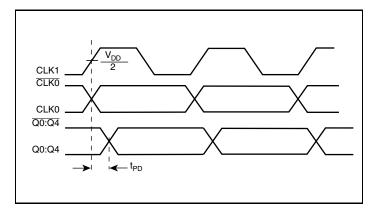
**Differential Input Level** 



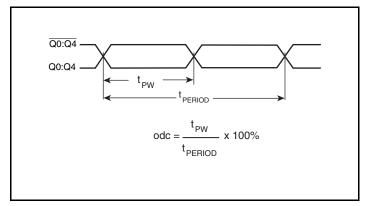
**Output Skew** 



**Part-to-Part Skew** 

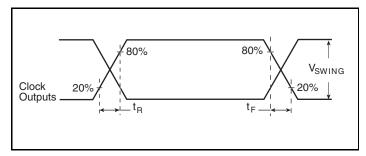


**Propagation Delay** 



**Output Duty Cycle/Pulse Width/Period** 

# **Parameter Measurement Information, continued**



**Output Rise/Fall Time** 

# **Application Information**

## Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V\_REF =  $V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V\_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ , V\_REF should be 1.25V and R2/R1 = 0.609.

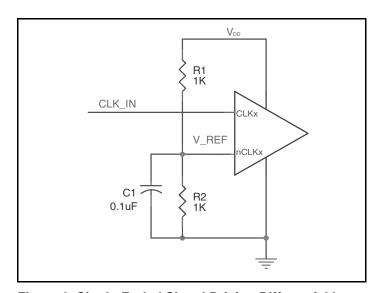


Figure 2. Single-Ended Signal Driving Differential Input

## **Differential Clock Input Interface**

The CLK/CLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/CLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

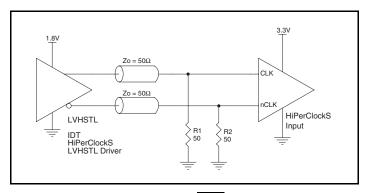


Figure 3A. HiPerClockS CLK/CLK Input
Driven by an IDT Open Emitter
HiPerClockS LVHSTL Driver

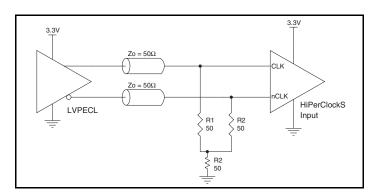


Figure 3B. HiPerClockS CLK/CLK Input
Driven by a 3.3V LVPECL Driver

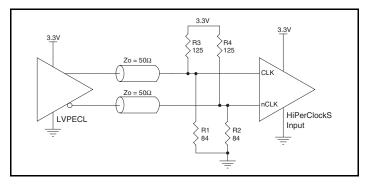


Figure 3C. HiPerClockS CLK/CLK Input
Driven by a 3.3V LVPECL Driver

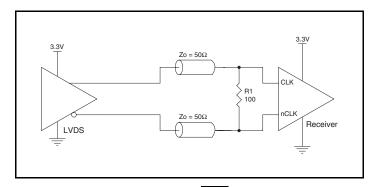


Figure 3D. HiPerClockS CLK/CLK Input Driven by a 3.3V LVDS Driver

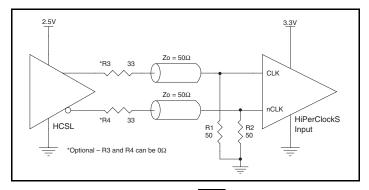


Figure 3E. HiPerClockS CLK/CLK Input Driven by a 3.3V HCSL Driver

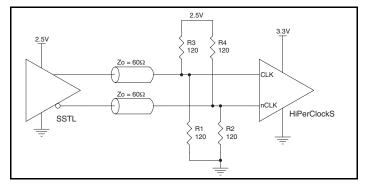


Figure 3F. HiPerClockS CLK/CLK Input
Driven by a 2.5V SSTL Driver

## **Recommendations for Unused Input and Output Pins**

## Inputs:

#### **LVCMOS Control Pins**

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1k\Omega$  resistor can be used.

#### **CLK/CLK** INPUTS

For applications not requiring the use of the differential input, both CLK and  $\overline{\text{CLK}}$  can be left floating. Though not required, but for additional protection, a  $1 k\Omega$  resistor can be tied from CLK0 to ground.

#### **CLK INPUT**

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a  $1 k\Omega$  resistor can be tied from the CLK input to ground.

# Schematic Example

Figure 4 shows a schematic example of the ICS85214. In this example, the input is driven by an IDT HiPerClockS HSTL driver. The decoupling capacitors should be physically located near the

## **Outputs:**

## **HSTL Outputs**

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

power pin. For ICS85214, the unused clock outputs can be left floating.

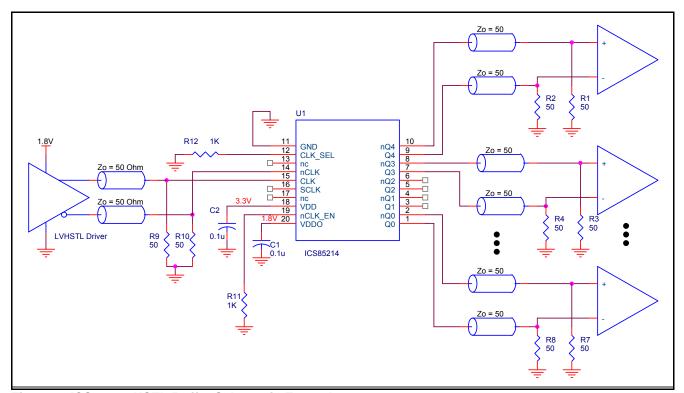


Figure 4. ICS85214 HSTL Buffer Schematic Example

### **Power Considerations**

This section provides information on power dissipation and junction temperature for the ICS85214. Equations and example calculations are also provided.

#### 1. Power Dissipation.

The total power dissipation for the ICS85214 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> = V<sub>DD\_MAX</sub> \* I<sub>DD\_MAX</sub> = 3.465V \* 850mA = 227.2mW
- Power (outputs)<sub>MAX</sub> = 32.8mW/Loaded Output pair
   If all outputs are loaded, the total power is 5 x 32.8mW = 164mW

Total Power\_MAX (3.465V, with all outputs switching) = 227.2mW + 144mW = 391.2mW

#### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj =  $\theta_{JA}$  \* Pd\_total + T<sub>A</sub>

Tj = Junction Temperature

 $\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd\_total = Total Device Power Dissipation (example calculation is in section 1 above)

 $T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

 $85^{\circ}\text{C} + 0.391\text{W} * 66.6^{\circ}\text{C/W} = 111^{\circ}\text{C}$ . This is well below the limit of  $125^{\circ}\text{C}$ .

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resitance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection

θ <sub>JA</sub> by Velocity						
Linear Feet per Minute	0	200	500			
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W			
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W			

#### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in Figure 6.

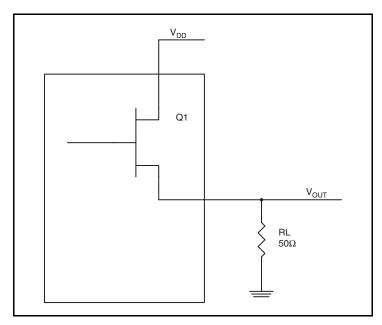


Figure 6. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load.

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd_{-}H = (V_{OH\_MAX}/R_{L}) * (V_{DDO\_MAX} - V_{OH\_MAX})$$

$$Pd_{-}L = (V_{OL\_MAX}/R_{L}) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd_H = (1.0V/50\Omega) * (2V - 1.0V) = 20mW$$
  
 $Pd_L = (0.4V/50\Omega) * (2V - 0.4V) = 12.8mW$ 

Total Power Dissipation per output pair = Pd\_H + Pd\_L = 32.8mW

# **Reliability Information**

Table 7.  $\theta_{\text{JA}}$  vs. Air Flow Table for a 20 Lead TSSOP

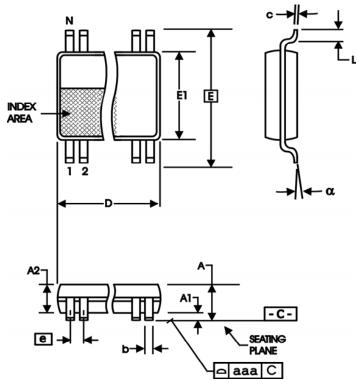
$\theta_{JA}$ by Velocity						
Linear Feet per Minute	0	200	500			
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W			
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W			

## **Transistor Count**

The transistor count for ICS85214 is: 674

# **Package Outline and Package Dimension**

Package Outline - G Suffix for 20 Lead TSSOP



**Table 8. Package Dimensions** 

All Dimensions in Millimeters					
Symbol	Minimum Maximum				
N	20				
Α		1.20			
A1	0.05	0.15			
A2	0.80	1.05			
b	0.19	0.30			
С	0.09	0.20			
D	6.40	6.60			
E	6.40 Basic				
E1	4.30	4.50			
е	0.65 Basic				
L	0.45	0.75			
α	0°	8°			
aaa		0.10			

Reference Document: JEDEC Publication 95, MO-153

# **Ordering Information**

### **Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85214AG	ICS85214AG	20 Lead TSSOP	Tube	0°C to 85°C
85214AGT	ICS85214AG	20 Lead TSSOP	2500 Tape & Reel	0°C to 85°C
85214AGLF	ICS85214AGLF	"Lead-Free" 20 Lead TSSOP	Tube	0°C to 85°C
85214AGLFT	ICS85214AGLF	"Lead-Free" 20 Lead TSSOP	2500 Tape & Reel	0°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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# **Revision History Sheet**

Rev	Table	Page	Description of Change	Date
А	T2	2	Changed LVHSTL to HSTL throughout the datasheet.  Pin Characteristics Table - changed C <sub>IN</sub> 4pF max. to 4pF typical	7/17/03
А	Т9	1 9 13	Features Section - added Lead-Free Bullet.  Added Recommendation of Unused Input and Output Pins.  Ordering Information Table - added Lead-Free part number, marking, and note.  Changed format throughout the datasheet.	3/13/07
В	ТЗВ	3 8	Clock Input Function Table - corrected CLK0 column from 0 (1st row) to 1 and 1 (2nd row) to 0.  Updated Differential Clock Input Interface section.	2/25/08

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