ICS87949I
Low Skew, ÷1, ÷2 Clock Generator

General Description

The ICS87949I is a low skew, ÷1, ÷2 Clock Generator. The ICS87949I has selectable single ended clock or LVPECL clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines.The effective fanout can be increased from 15 to 30 by utilizing the ability of the outputs to drive two series terminated lines.

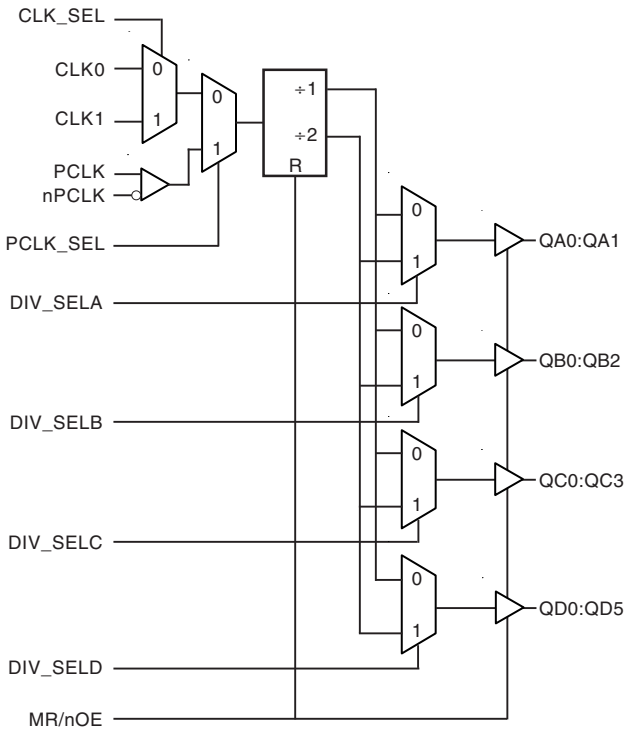
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87949I is characterized at 3.3V core/3.3V output. Guaranteed output and part-to-part skew characteristics make the ICS87949I ideal for those clock distribution applications demanding well defined performance and repeatability.

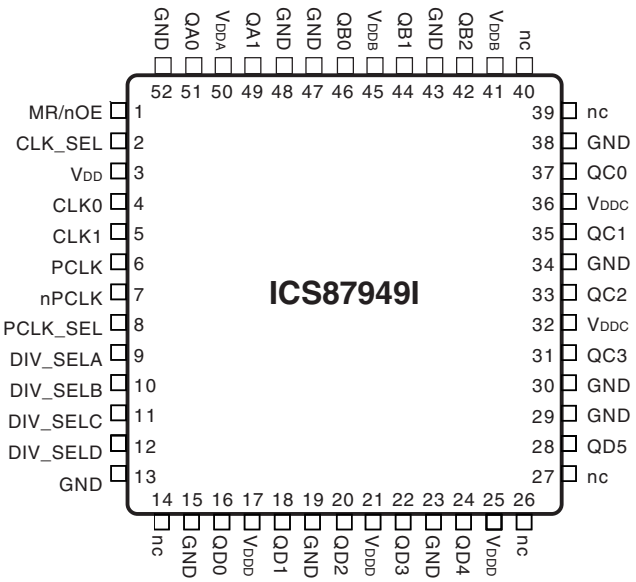
Features

- Fifteen single ended LVCMOS outputs, 7Ω typical output impedance
- Selectable LVCMOS or LVPECL clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 160MHz
- Output skew: 350ps (maximum)
- Part-to-part skew: 2.75ns (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

Block Diagram



Pin Assignment



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
3	V_{DD}	Power		Power supply pin.
4, 5	CLK0, CLK1	Input	Pullup	LVCMOS / LVTTL clock inputs.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8	PCLK_SEL	Input	Pulldown	PCLK select input. LVCMOS / LVTTL interface levels.
9	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
10	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
11	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels.
12	DIV_SELD	Input	Pulldown	Controls frequency division for Bank D outputs. LVCMOS / LVTTL interface levels.
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	GND	Power		Power supply ground.
14, 26, 27, 39, 40	nc	Unused		No connect.
16, 18, 20, 22, 24, 28	QD0, QD1, QD2, QD3, QD4, QD5	Output		Bank D outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
17, 21, 25	V_{DDD}	Power		Positive supply pins for Bank D outputs.
31, 33, 35, 37	QC3, QC2, QC1, QC0	Output		Bank C outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
32, 36	V_{DDC}	Power		Positive supply pins for Bank C outputs.
41, 45	V_{DDB}	Power		Positive supply pins for Bank B outputs.
42, 44, 46	QB2, QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
49, 51	QA1, QA0	Output		Bank A outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
50	V_{DDA}	Power		Positive supply pins for Bank A outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output);			25		pF
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3. FUNCTION TABLE

Inputs					Outputs			
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA0, QA1	QB0:QB2	QC0:QC3	QD0:QD5
1	X	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z
0	0	X	X	X	fIN/1	Active	Active	Active
0	1	X	X	X	fIN/2	Active	Active	Active
0	X	0	X	X	Active	fIN/1	Active	Active
0	X	1	X	X	Active	fIN/2	Active	Active
0	X	X	0	X	Active	Active	fIN/1	Active
0	X	X	1	X	Active	Active	fIN/2	Active
0	X	X	X	0	Active	Active	Active	fIN/1
0	X	X	X	1	Active	Active	Active	fIN/2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_{DD}	-0.5V to V_{DD} + 0.5 V
Outputs, V_{DDx}	-0.5V to V_{DDx} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
V_{DDx}	Output Supply Voltage; NOTE 1		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				85	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.

TABLE 4B. DC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{PP}	Peak-to-Peak Input Voltage		0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		V_{DD} - 2.0V		V_{DD} - 0.6V	V
I_{IN}	Input Current				±120	µA
V_{OH}	Output High Voltage	I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20mA			0.4	V

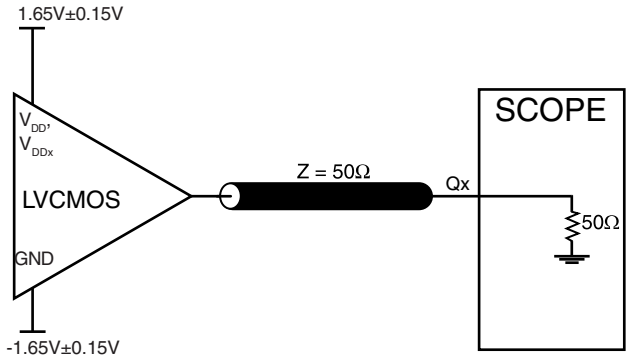
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, $T_A =$ -40°C TO 85°C

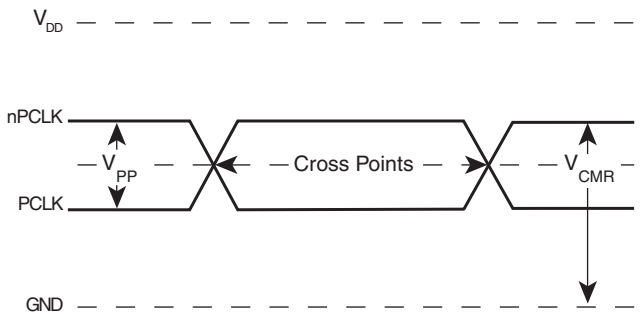
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency			160			MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	PCLK, nPCLK		1.9		9.0	ns
		CLK0, CLK1		1.7		10.6	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	PCLK, nPCLK		1.8		8.6	ns
		CLK0, CLK1		1.6		10.5	ns
*t*sk(o)	Output Skew; NOTE 2, 5		Measured on rising edge at $V_{DDx}/2$			350	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge at $V_{DDx}/2$			2.75	ns
		CLK0, CLK1				4	ns
t_R	Output Rise Time; NOTE 4		0.8 to 2.0V	0.1		1.0	ns
t_F	Output Fall Time; NOTE 4		0.8 to 2.0V	0.1		1.0	ns
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 4					11	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 4					11	ns

NOTE 1: Measured from the $V_{DD}/2$ or crosspoint of the input to $V_{DDx}/2$ of the output.
NOTE 2: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

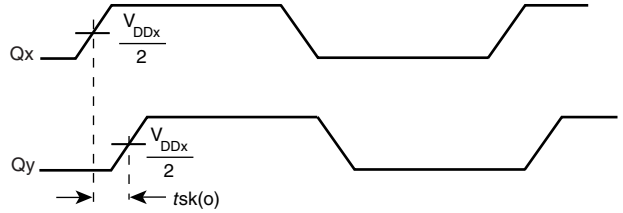
PARAMETER MEASUREMENT INFORMATION



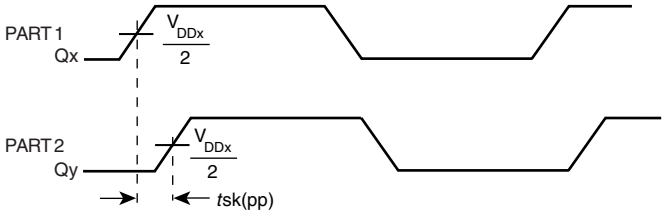
3.3V OUTPUT LOAD AC TEST CIRCUIT



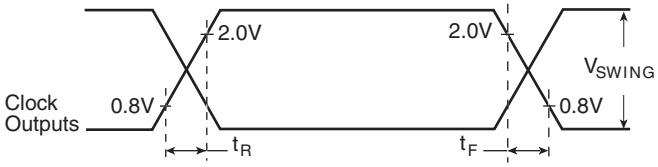
DIFFERENTIAL INPUT LEVEL



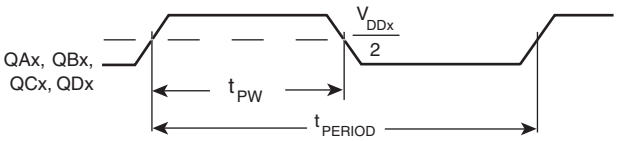
OUTPUT SKEW



PART-TO-PART SKEW

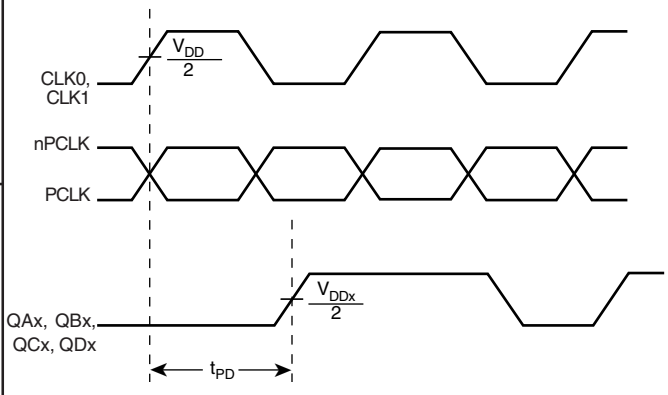


OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1F* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

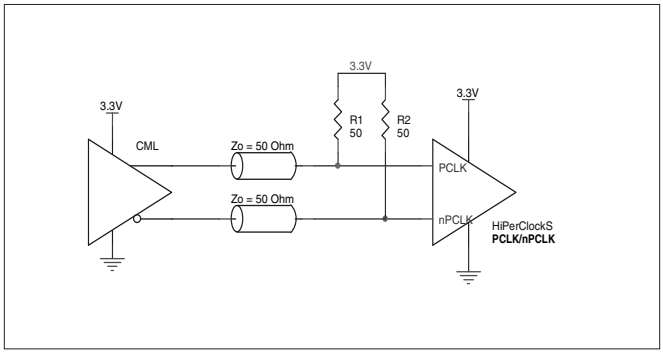


FIGURE 1A. PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

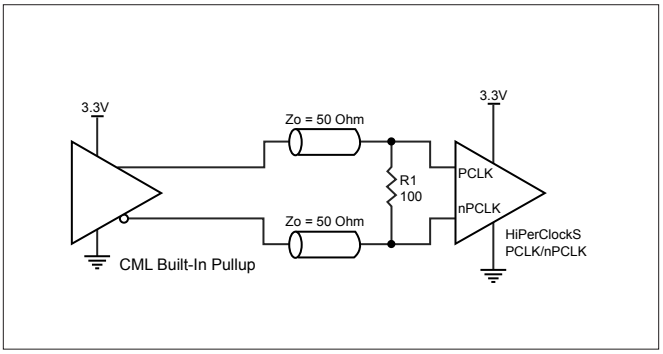


FIGURE 1B. PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

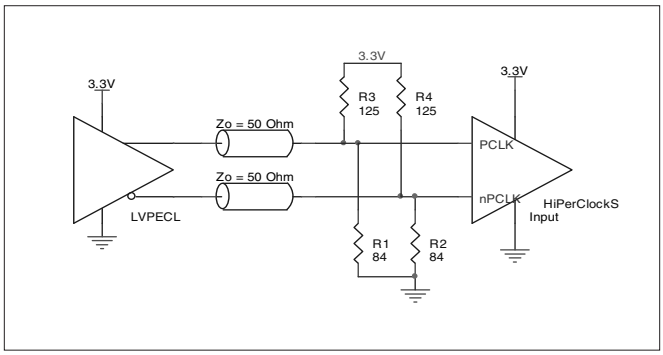


FIGURE 1C. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

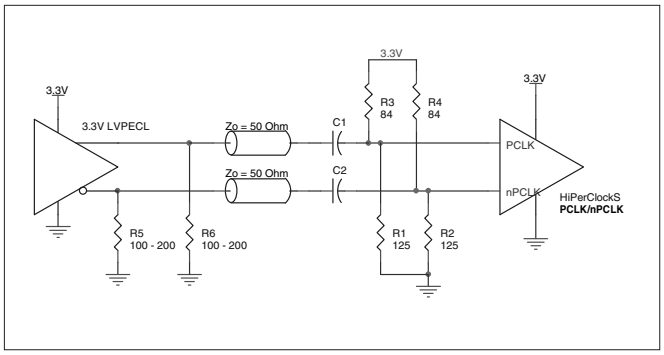


FIGURE 1D. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

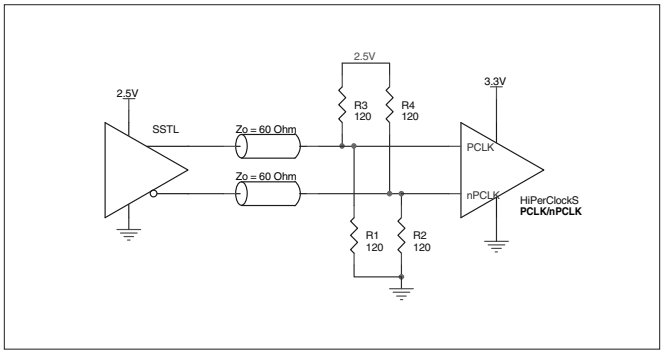


FIGURE 1E. PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

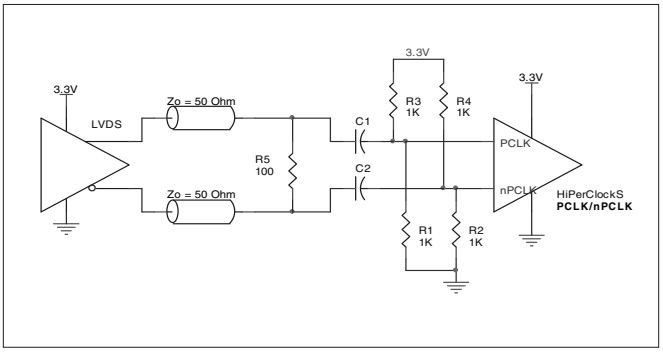


FIGURE 1F. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT
The transistor count for ICS87949I is: 1545

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

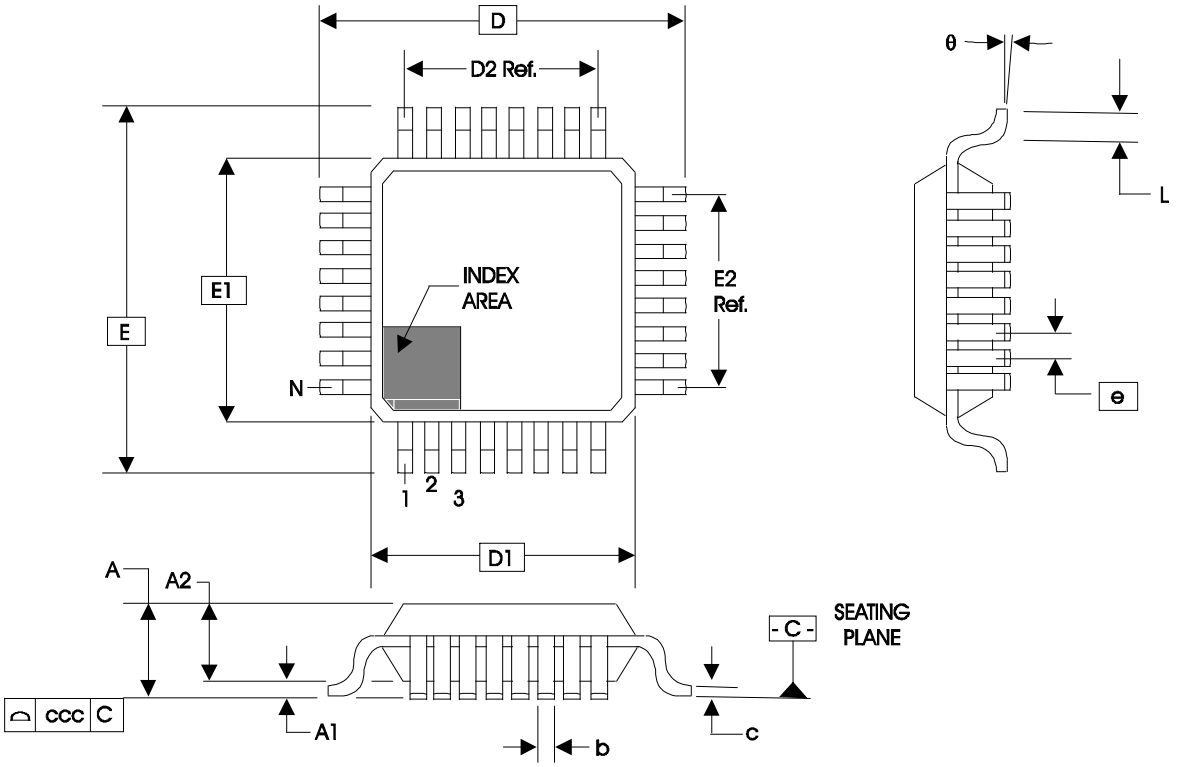


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87949AYI	ICS87949AYI	52 Lead LQFP	Tube	-40°C to 85°C
87949AYIT	ICS87949AYI	52 Lead LQFP on Tape and Reel	500 Tape & Reel	-40°C to 85°C
87949AYILF	ICS87949AYILF	52 Lead LQFP	Tube	-40°C to 85°C
87949AYILFT	ICS87949AYILF	52 Lead LQFP on Tape and Reel	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	1 2 7	In Features section revised bullet to read "Maximum output frequency..." instead of "Maximum input frequency...". In Pin Description Table revised MR/nOE description. Revised Output Rise & Fall Time Diagram.	08/14/02
A	T5	5	AC Characteristics table - corrected Output Enable/Disable Time symbols.	10/18/02
B	T4B T5	4 5	DC Characteristics table - changed V_{CMR} from GND + 1.5V min./V_{DD} max. to V_{DD} - 2.0V min./V_{DD} - 0.6V max. AC Characteristics table - changed (PCLK, nPCLK) tp_{LH} from 4.7ns max. to 9.0ns max.,deleted typical value. (CLK0, CLK1)) tp_{LH} from 5.7ns max. to 10.6ns max., deleted typical value. (PCLK, nPCLK) tp_{HL} from 4.6ns max. to 8.6ns max., deleted typical value. (CLK0, CLK1)) tp_{HL} from 5.6ns max. to 10.5ns max., deleted typical value.	10/22/02
B		8	Modified Package Outline to correspond with the Package Dimensions table.	11/21/02
C	T1 T2 T8	1 2 3 7 8 11	Feature section - added lead-free bullet. Pin Description Table - updated MR/nOE pin description. Pin Chararcteristics Table - changed C_{IN} from 4pF max. to 4pF typical and added 5Ω min. / 12Ω max. to R_{OUT}. Added *Recommendations for Unused Input and Output Pins.* Added *LVPECL Clock Input Interface.* Ordering Information Table - added lead-free part number, marking, and note.	11/22/05
C	T8	11 13	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/5/10

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www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775

Tech Support
netcom@idt.com