LOW SKEW, 1-TO-6, CRYSTAL/LVCMOS/DIFFERENTIAL-TO-3.3V, 2.5V LVPECL FANOUT BUFFER

ICS8536-01

General Description

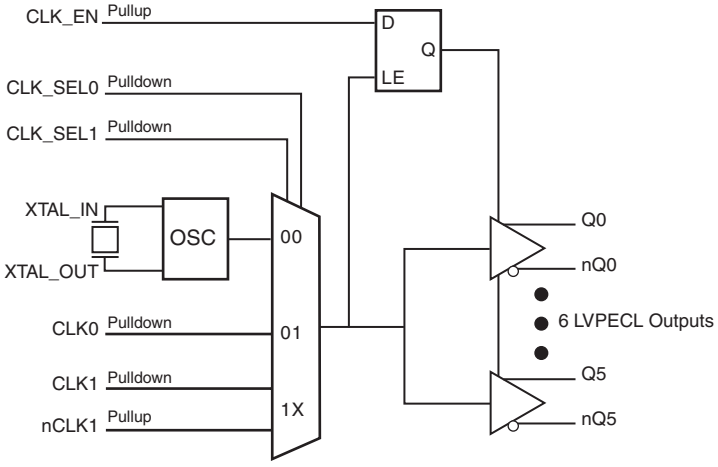
The ICS8536-01 is a low skew, high performance 1-to-6 Selectable Crystal, Single-Ended, or Differential Input-to-3.3V, 2.5V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8536-01 has selectable crystal, single ended or differential clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to LVPECL levels. The CLK1, nCLK1 pair can accept most standard differential input levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8536-01 ideal for those applications demanding well defined performance and repeatability.

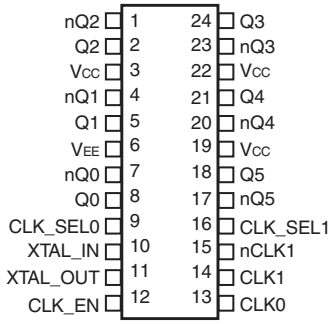
Features

- Six 3.3V, 2.5V LVPECL outputs
- Selectable crystal oscillator, differential CLK1/nCLK1 pair or LVCMOS/LVTTL clock input
- CLK1/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Crystal frequency range: 12MHz - 40MHz
- Output skew: 55ps (maximum) CLK1/nCLK1 @ 3.3V
- Part-to-part skew: 450ps (maximum)
- Additive phase jitter, RMS: 0.19ps (typical)
- Full 3.3V or 2.5V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8536-01
24-Lead TSSOP
4.40mm x 7.8mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
3, 19, 22	V_{CC}	Power		Power supply pins.
4, 5	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
6	V_{EE}	Power		Negative supply pin.
7, 8	nQ0, Q0	Ouput		Differential output pair. LVPECL interface levels.
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels. See Table 3B.
10, 11	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3A.
13	CLK0	Input	Pulldown	LVCMOS/LVTTL clock input.
14	CLK1	Input	Pulldown	Non-inverting differential clock input.
15	nCLK1	Input	Pullup	Inverting differential clock input.
17, 18	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pulup Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs	
CLK_EN	**CLK_SEL1**	**CLK_SEL0**	**Selected Source**	**Q0:Q5**	**nQ0:nQ5**
0	0	0	XTAL	Disabled	Disabled
0	0	1	CLK0	Disabled	Disabled
0	1	X	CLK1/nCLK1	Disabled	Disabled
1	0	0	XTAL	Enabled	Enabled
1	0	1	CLK0	Enabled	Enabled
1	1	X	CLK1/nCLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in *Figure 1.*
In the active mode, the state of the outputs are a function of the selected clock input as described in Table 3B.

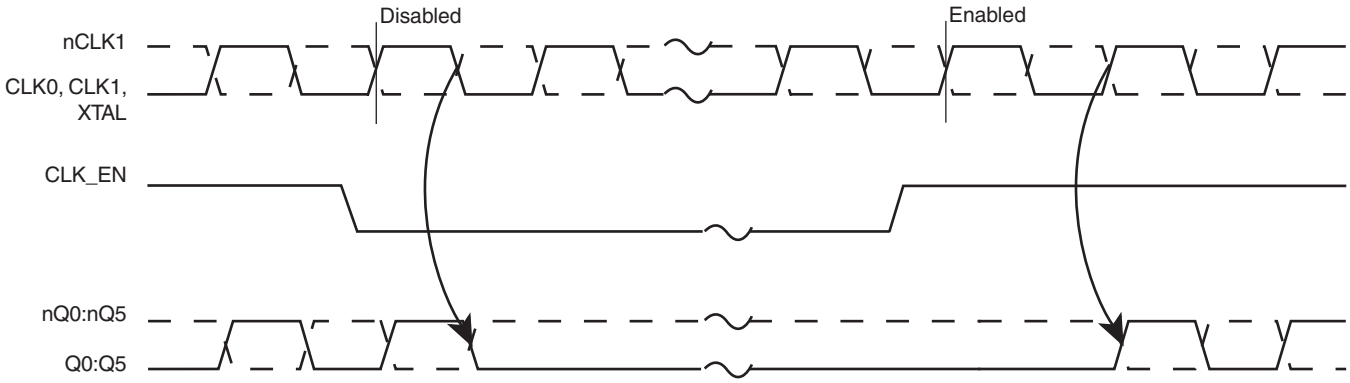


FIGURE 1. CLK_EN TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	84.6°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				85	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				85	mA

Table 4C. LVCMOS / LVTTL DC Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK_SEL0:1	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		CLK_EN	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK_SEL0:1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		CLK_EN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

TABLE 4D. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			5	µA
		CLK1	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	CLK1/nCLK1				700	MHz
		CLK0				300	MHz
t_{PD}	Propagation Delay, NOTE1A, 1B	CLK1/nCLK1		1.7		2.5	ns
		CLK0		1.35		2.0	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2		CLK1/nCLK1, 155.52MHz, Integration Range: 12kHz - 20MHz		0.19		ps
*t*sk(o)	Output Skew; NOTE 3, 5					55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5					450	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK1/nCLK1		48		52	%
		CLK0		44		56	%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 6A	*f* = 150MHz		-76		dB
		NOTE 6B	*f* = 250MHz		-75		dB

All parameters measured at f_{MAX} unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
NOTE 1B: Measured from V_{CC}/2 input crossing point to the differential output crossing point.
NOTE 2: Driving only one input clock.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6A: CLK0 (150MHz) sensitivity is measured with CLK_SEL[1:0] = 00.
NOTE 6B: CLK0 (250MHz) sensitivity is measured with CLK_SEL[1:0] = 1X.

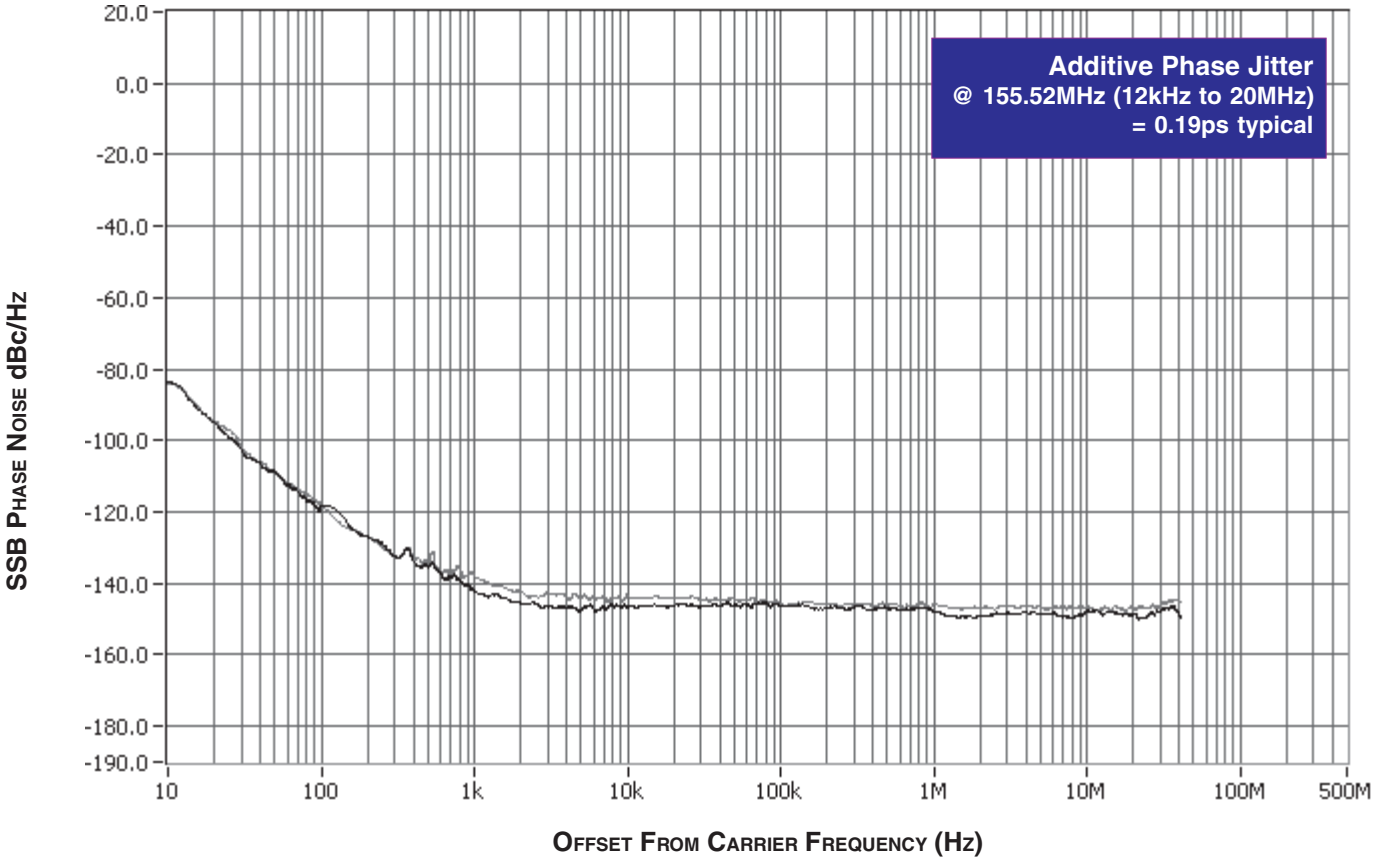
TABLE 6B. AC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	CLK1/nCLK1				700	MHz
		CLK0				300	MHz
t_{PD}	Propagation Delay, NOTE1A, 1B	CLK1/nCLK1		1.7		2.0	ns
		CLK0		1.4		2.05	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2		CLK1/nCLK1, 155.52MHz, Integration Range: 12kHz - 20MHz		0.19		ps
*t*sk(o)	Output Skew; NOTE 3, 5					55	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5					450	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK1/nCLK1		48		52	%
		CLK0		46		54	%
$MUX_{\_ISOLATION}$	MUX Isolation	NOTE 6A	*f* = 150MHz		-76		dB
		NOTE 6B	*f* = 250MHz		-75		dB

For notes, see Table 6A above.

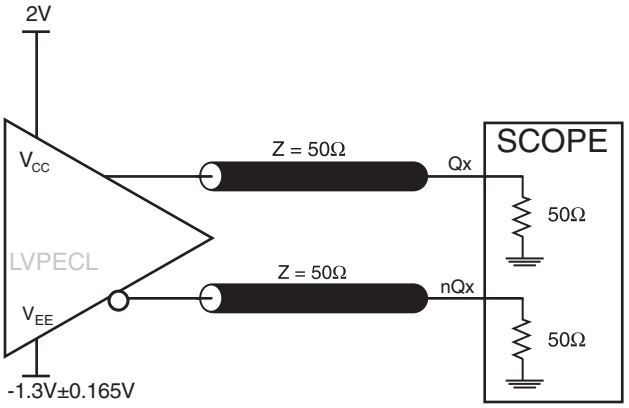
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

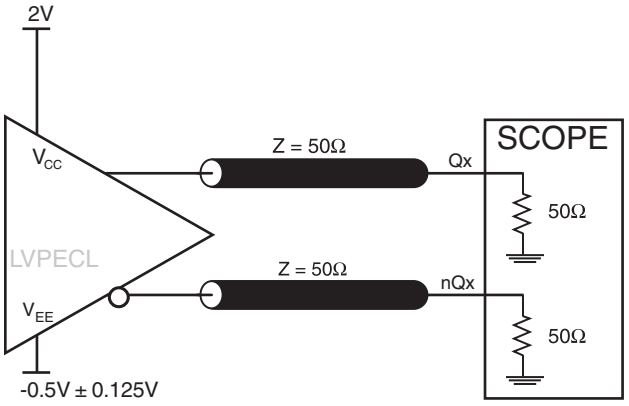


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

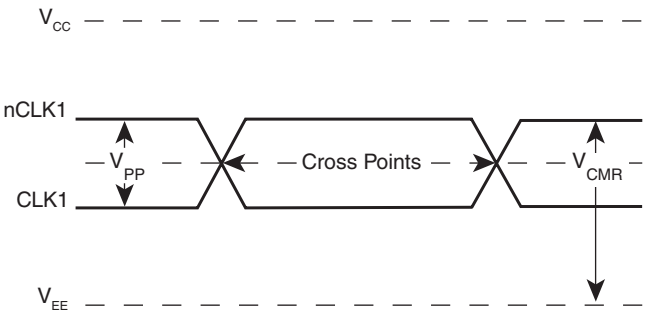
Parameter Measurement Information



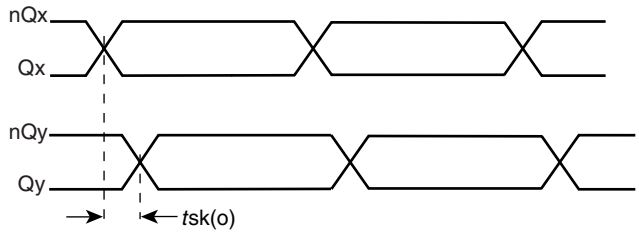
3.3V LVPECL Output Load AC Test Circuit



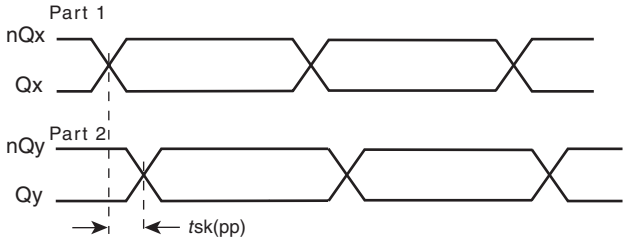
2.5V LVPECL Output Load AC Test Circuit



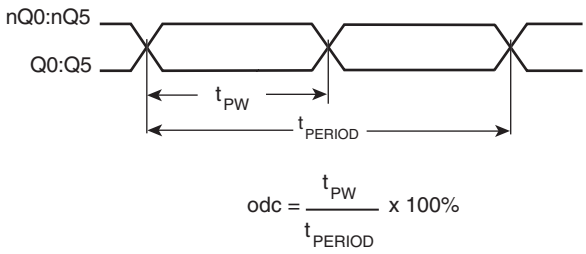
Differential Input Levels



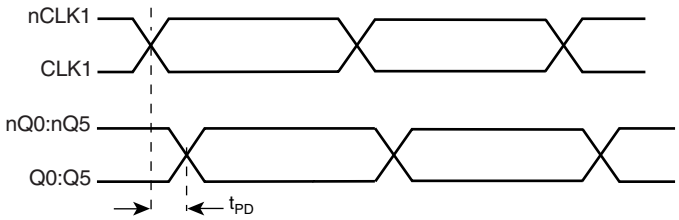
Output Skew



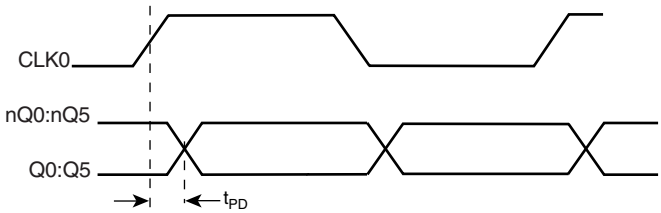
Part-to-Part Skew



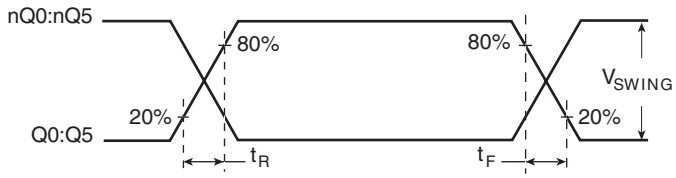
Output Duty Cycle/Pulse Width/Period



PROPAGATION DELAY (DIFFERENTIAL INPUT)



PROPAGATION DELAY (LVCMOS INPUT)



OUTPUT RISE/FALL TIME

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{cc}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{cc} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

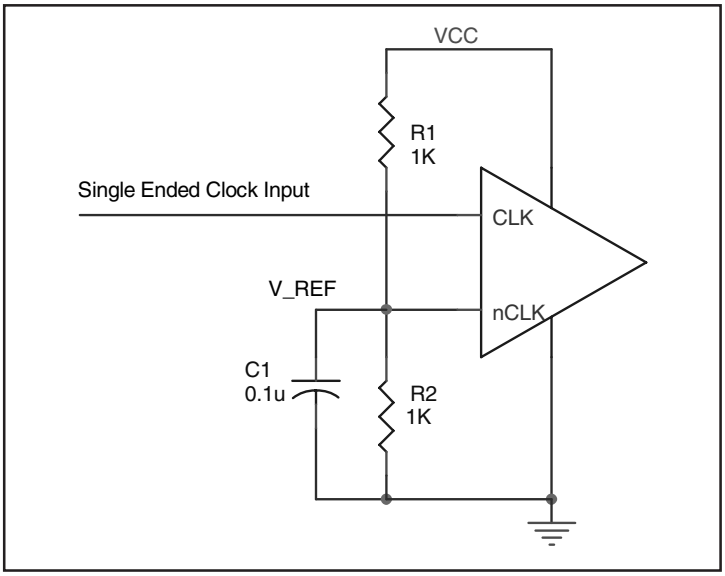


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK Inputsa

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS8536-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

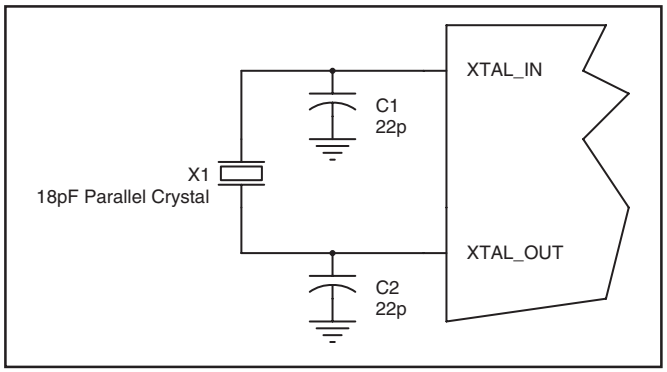


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

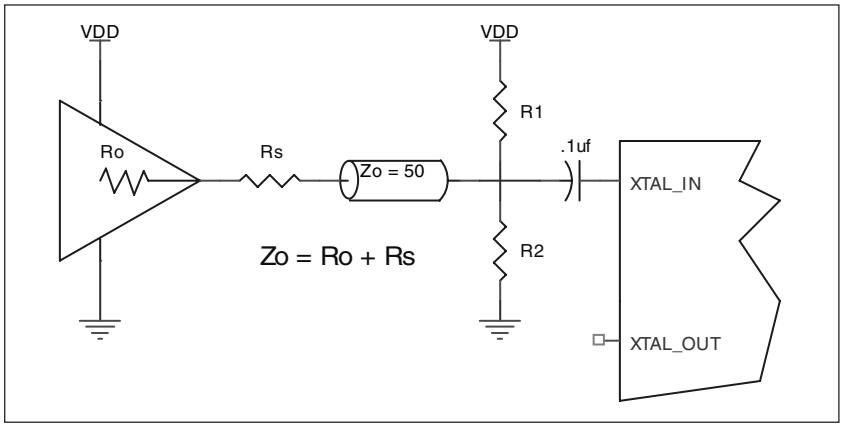


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 4A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

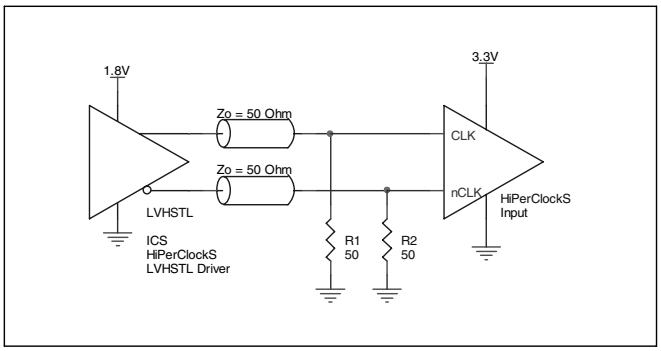


Figure 4A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

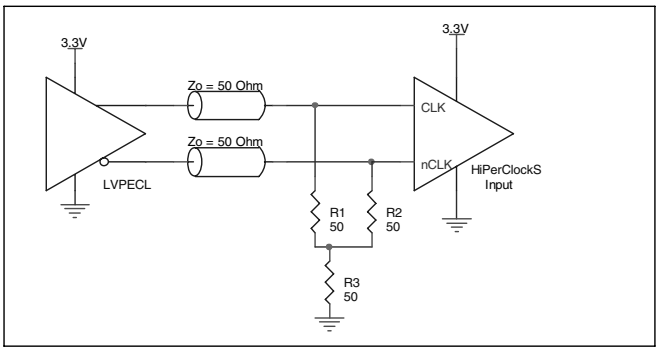


Figure 4B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

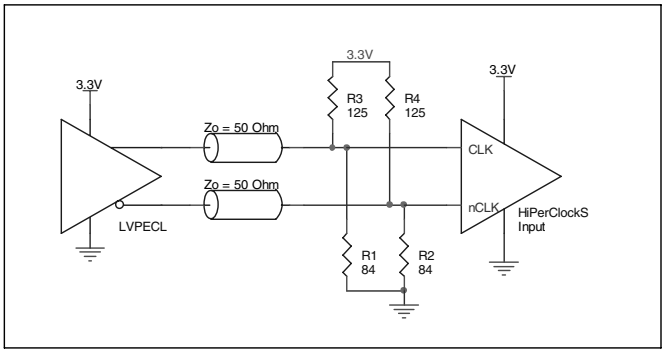


Figure 4C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

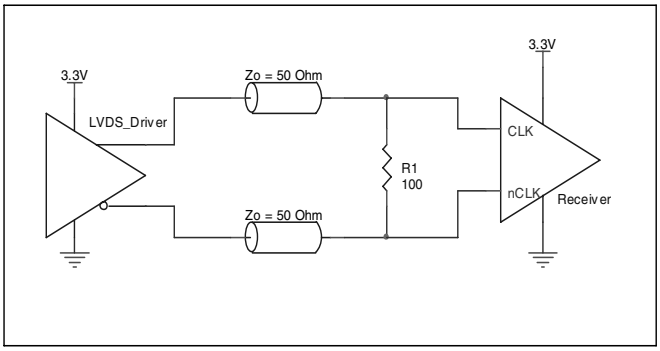


Figure 4D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

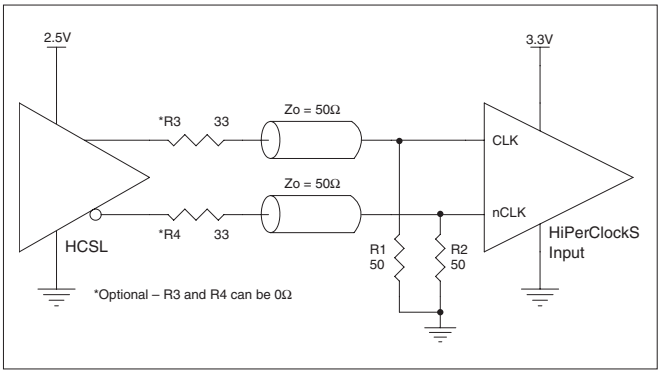


Figure 4E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

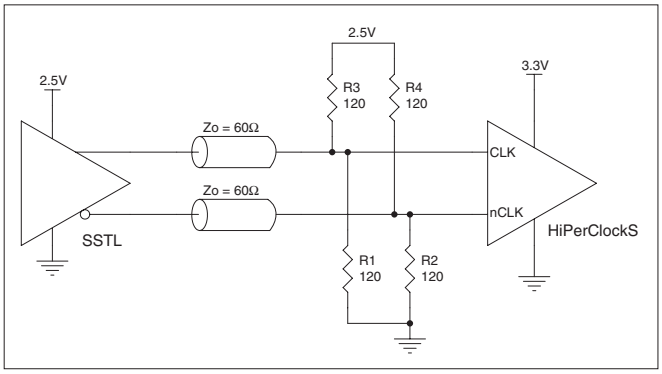


Figure 4F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

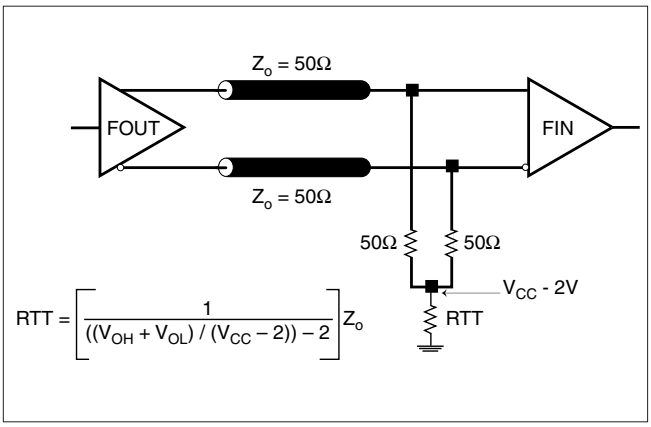


FIGURE 5A. LVPECL OUTPUT TERMINATION

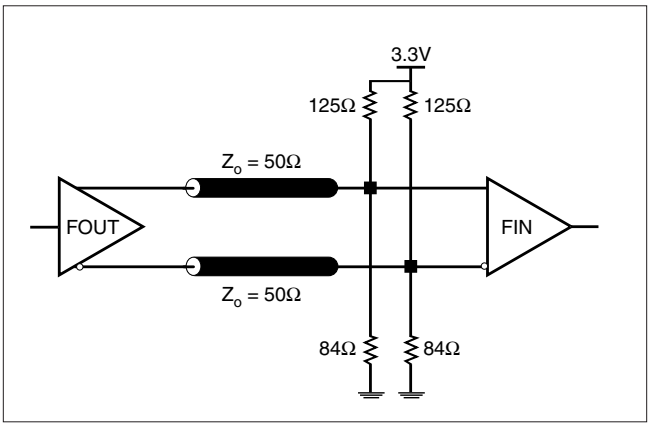


FIGURE 5B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

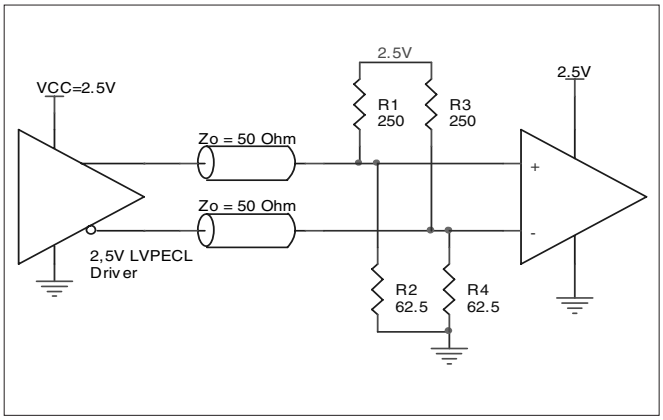


FIGURE 6A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

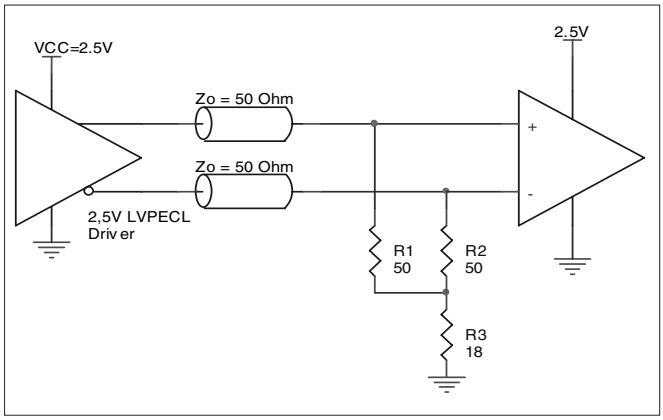


FIGURE 6B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

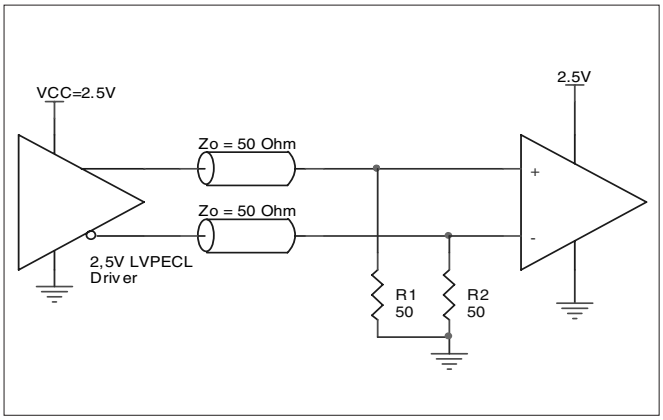


FIGURE 6C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8536-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8536-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 85mA = 294.525**mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30mW = **180mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 294.525mW + 180mW **= 474.525mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 84.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.475W * 84.6°C/W = 110.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	84.6°C/W	80.3°C/W	78.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

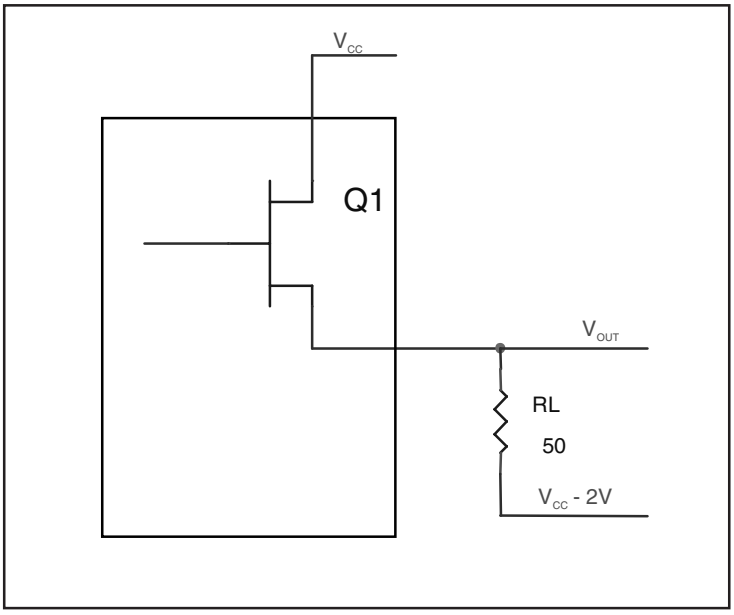


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	84.6°C/W	80.3°C/W	78.1°C/W

Transistor Count

The transistor count for ICS8536-01 is: 513

Package Outline - G Suffix for 24 Lead TSSOP

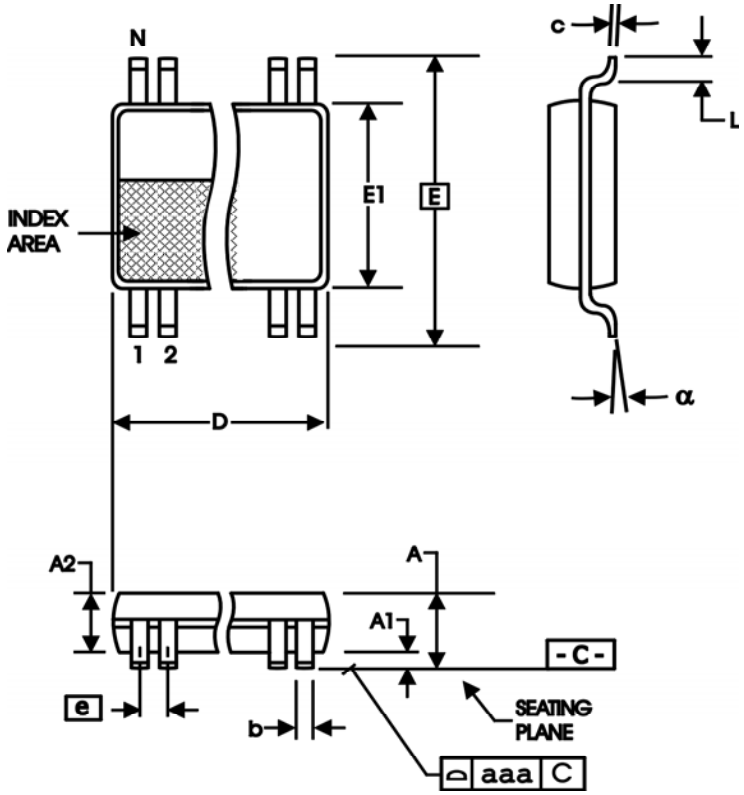


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8536AG-01	ICS8536AG-01	24 Lead TSSOP	tube	0°C to 70°C
8536AG-01T	ICS8536AG-01	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
8536AG-01LF	ICS8536AG-01L	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
8536AG-01LFT	ICS8536AG-01L	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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