Nonvolatile Memory, Dual 1024-Position Programmable Resistors

ADN2850*

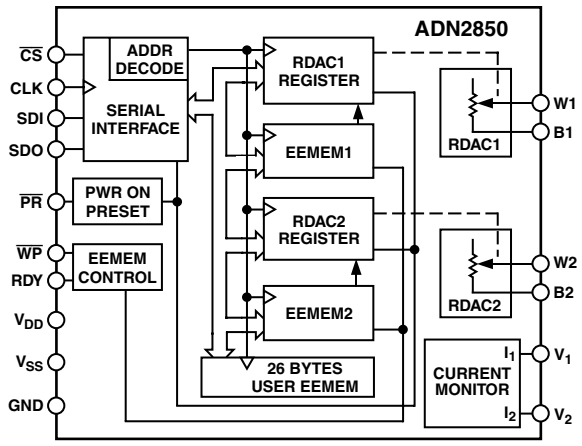
FEATURES

Dual, 1024-Position Resolution
25 kΩ, 250 kΩ Full-Scale Resistance
Low Temperature Coefficient: 35 ppm/°C
Nonvolatile Memory[1] Preset Maintains Wiper Settings
Permanent Memory Write-Protection
Wiper Settings Read Back
Actual Tolerance Stored in EEMEM[1]
Linear Increment/Decrement
Log Taper Increment/Decrement
SPI Compatible Serial Interface
3 V to 5 V Single Supply or ±2.5 V Dual Supply
26 Bytes User Nonvolatile Memory for Constant Storage
Current Monitoring Configurable Function
100-Year Typical Data Retention T_A = 55°C

APPLICATIONS

SONET, SDH, ATM, Gigabit Ethernet, DWDM Laser Diode Driver Optical Supervisory Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADN2850 provides dual-channel, digitally controlled programmable resistors[2] with resolution of 1024 positions. These devices perform the same electronic adjustment function as a mechanical rheostat with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance. The ADN2850's versatile programming via a standard serial interface allows 16 modes of operation and adjustment, including scratch pad programming, memory storing and retrieving, increment/decrement, log taper adjustment, wiper setting readback, and extra user defined EEMEM[1].

Another key feature of the ADN2850 is that the actual tolerance is stored in the EEMEM. The actual full-scale resistance can therefore be known, which is valuable for tolerance matching and calibration.

In the scratch pad programming mode, a specific setting can be programmed directly to the RDAC[2] register, which sets the resistance between terminals W and B. The RDAC register can also be loaded with a value previously stored in the EEMEM register. The value in the EEMEM can be changed or protected. When changes are made to the RDAC register, the value of the new setting can be saved into the EEMEM. Thereafter, such value will be transferred automatically to the RDAC register during system power ON, which is enabled by the internal preset strobe. EEMEM can also be retrieved through direct programming and external preset pin control.

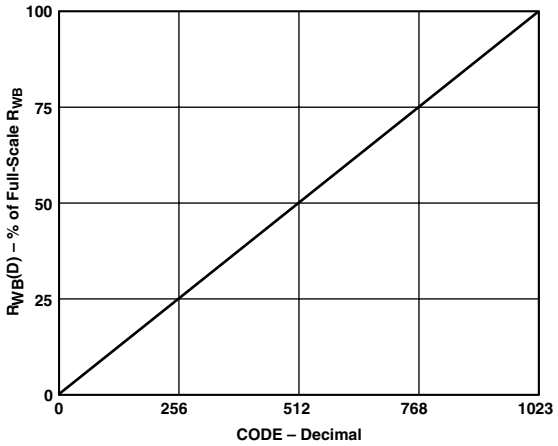


Figure 1. $R_{WB}(D)$ vs. Decimal Code

The linear step increment and decrement commands enable the setting in the RDAC register to be moved UP or DOWN, one step at a time. For logarithmic changes in wiper setting, a left/right bit shift command adjusts the level in ±6 dB steps.

The ADN2850 is available in the 5 mm × 5 mm 16-lead frame chip scale LFCSP and thin 16-lead TSSOP packages. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

*Patent pending

NOTES
[1]The term nonvolatile memory and EEMEM are used interchangeably.
[2]The term programmable resistor and RDAC are used interchangeably.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADN2850–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 25 kΩ, 250 kΩ VERSIONS

(V_{DD} = 3 V to 5.5 V and –40°C < T_A < +85°C, unless otherwise noted.)[1]

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE (Specifications apply to all RDACs)						
Resistor Differential Nonlinearity[3]	R-DNL	R_{WB}	–2		+2	LSB
Resistor Integral Nonlinearity[3]	R-INL	R_{WB}	–4		+4	LSB
Resistance Temperature Coefficient	$\Delta R_{WB}/\Delta_T$			35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V, I_W = 100 μA, Code = Half-scale		50	100	Ω
		V_{DD} = 3 V, I_W = 100 μA, Code = Half-scale		200		Ω
Channel Resistance Matching	$\Delta R_{WB}/R_{WB}$	Ch 1 and 2 R_{WB}, Dx = $3FF_H$		0.1		%
Nominal Resistor Tolerance	ΔR_{WB}		–30		+30	%
RESISTOR TERMINALS						
Terminal Voltage Range[4]	$V_{W, B}$		V_{SS}		V_{DD}	V
Capacitance[5] Bx	C_B	f = 1 MHz, measured to GND, Code = Half-scale		11		pF
Capacitance[5] Wx	C_W	f = 1 MHz, measured to GND, Code = Half-scale		80		pF
Common-Mode Leakage Current[6]	I_{CM}	$V_W = V_B = V_{DD}/2$		0.01	±2	μA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V	2.0			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±2.25	μA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	3.0		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND, T_A = 25°C		2	4.5	μA
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		3.5	6.0	μA
Programming Mode Current	$I_{DD(PG)}$	$V_{IH} = V_{DD}$ or V_{IL} = GND		35		mA
Read Mode Current[7]	$I_{DD(XFR)}$	$V_{IH} = V_{DD}$ or V_{IL} = GND	0.3	3	9	mA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V		3.5	6.0	μA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		18	50	μW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%
CURRENT MONITOR TERMINALS						
Current Sink at V_1[9]	I_1		0.0001		10	mA
Current Sink at V_2	I_2				10	mA
DYNAMIC CHARACTERISTICS[5, 10]						
Resistor Noise Spectral Density	e_{N_WB}	R_{WB_FS} = 25 kΩ/250 kΩ, f = 1 kHz		20/64		nV/√Hz
Analog Crosstalk (C_{W1}/C_{W2})	C_T	$V_{B1} = V_{B2}$ = 0 V, Measured V_{W1} with V_{W2} = 100 mV p-p @ f = 100 kHz, Code 1 = Code 2 = 200_H		–65		dB

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Unit
INTERFACE TIMING CHARACTERISTICS (apply to all parts)[5, 11]						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulsewidth	t_4, t_5	Clock Level High or Low	10			ns
Data Setup Time	t_6	From Positive CLK Transition	5			ns
Data Hold Time	t_7	From Positive CLK Transition	5			ns
$\overline{CS}$ to SDO – SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO – SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[12]	t_{10}	R_P = 2.2 kΩ, C_L < 20 pF			50	ns
$\overline{CS}$ High Pulsewidth[13]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[13]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.15	0.3	ms
Read/Store to Nonvolatile EEMEM[14]	t_{16}	Applies to Command 2_H, 3_H, 9_H		35		ms
$\overline{CS}$ Rise to Clock Edge Setup	t_{17}		10			ns
Preset Pulsewidth (Asynchronous)	t_{PRW}	Not Shown in Timing Diagram	50			ns
Preset Response Time to Wiper Setting	t_{PRESP}	$\overline{PR}$ Pulsed Low to Refresh Wiper Positions		140		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[15]			100			K Cycles
Data Retention[16]				100		Years

NOTES

[1] Parts can be operated at 2.7 V single supply, except from 08C to –408C, where minimum 3 V is needed.

[2] Typicals represent average readings at 258C and V_{DD} = 5 V.

[3] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W ~ 50 µA for V_{DD} = 2.7 V and I_W ~ 400 µA for V_{DD} = 5 V.

[4] Resistor terminals W and B have no limitations on polarity with respect to each other.

[5] Guaranteed by design and not subject to production test.

[6] Common-mode leakage current is a measure of the dc leakage from any terminal B and W to a common-mode bias level of $V_{DD}/2$.

[7] Transfer (XFR) mode current is not continuous. Current consumed while EEMEM locations are read and transferred to the RDAC register. See TPC 9.

[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).

[9] Applies to photodiode of optical receiver.

[10] All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = –2.5 V.

[11] See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and 5 V.

[12] Propagation delay depends on value of V_{DD}, R_{PULL_UP}, and C_L. See Applications section.

[13] Valid for commands that do not activate the RDY pin.

[14] RDY pin low only for commands 2, 3, 8, 9, 10, and PR hardware pulse: CMD_8 ~ 1 ms; CMD_9, 10 ~ 0.1 ms; CMD_2, 3 ~ 20 ms. Device operation at T_A = –40°C and V_{DD} < 3 V extends the save time to 35 ms.

[15] Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, and +85°C; typical endurance at +25°C is 700,000 cycles.

[16] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 V will derate with junction temperature.

Specifications subject to change without notice.

The ADN2850 contains 16,000 transistors. Die size: 93 mil × 103 mil, 10,197 sq mil.

TIMING DIAGRAMS

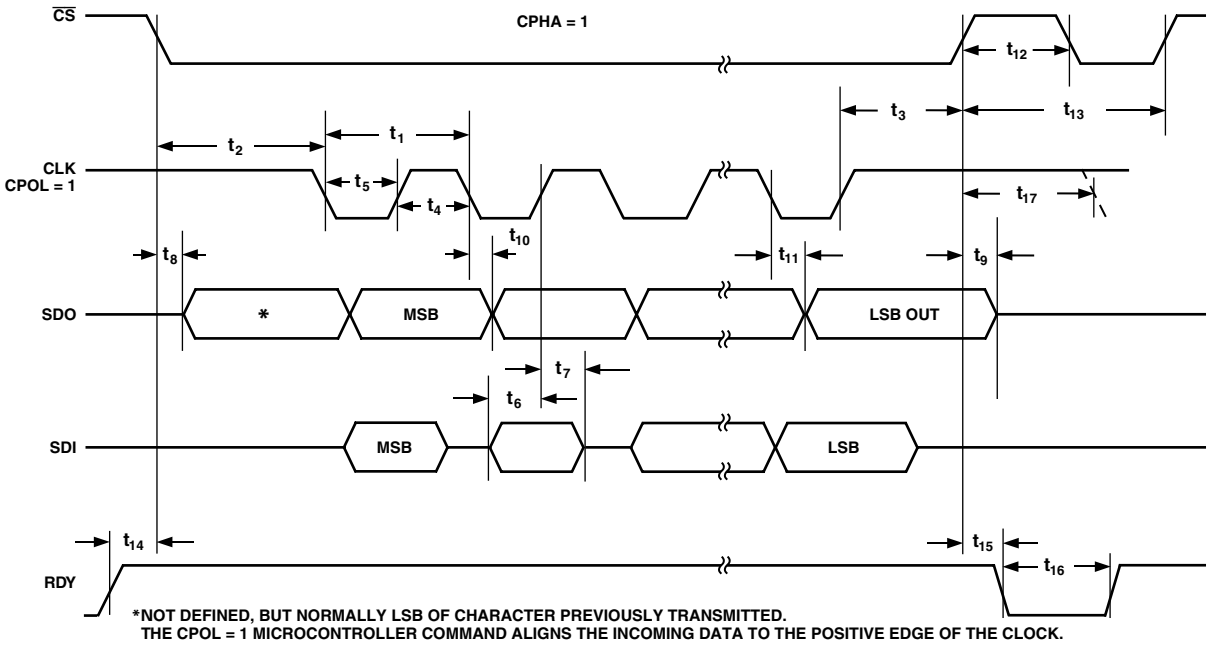


Figure 2a. CPHA = 1 Timing Diagram

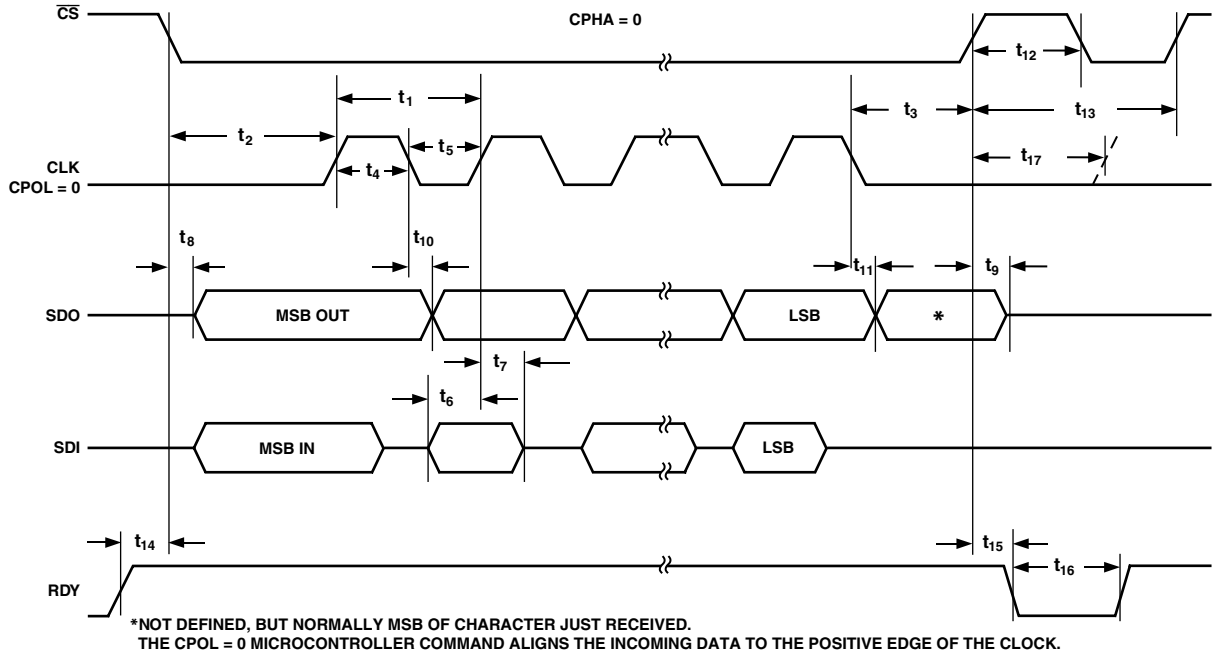


Figure 2b. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND ..... –0.3 V, +7 V
V_{SS} to GND ..... +0.3 V, –7 V
V_{DD} to V_{SS} ..... 7 V
V_B, V_W to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
I_B, I_W
  Intermittent[2] .....±20 mA
  Continuous ..... ±2 mA
Digital Inputs and Output Voltage
  to GND ..... –0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[3] ..... –40°C to +85°C
Maximum Junction Temperature ($T_{J\,MAX}$) ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature, Soldering[4]
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C

Thermal Resistance Junction-to-Ambient θ_{JA},
  LFCSP-16 ..... 35°C/W
  TSSOP-16 ..... 150°C/W
Thermal Resistance Junction-to-Case θ_{JC},
  TSSOP-16 ..... 28°C/W
Package Power Dissipation = $(T_{J\,MAX} - T_A)/\theta_{JA}$

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the B and W terminals at a given resistance.

[3]Includes programming of nonvolatile memory.

[4]Applicable to TSSOP-16 only. For LFCSP-16, please consult factory for details.

ORDERING GUIDE

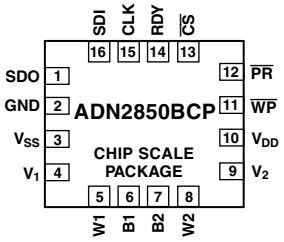
Model	R_{WB_FS} (kΩ)	RDNL (LSB)	RINL (LSB)	Temperature Range (°C)	Package Description	Package Option	Ordering Quantity	Top Mark*
ADN2850BCP25	25	±2	±4	–40 to +85	LFCSP-16	CP-16	96	BCP25
ADN2850BCP25-RL7	25	±2	±4	–40 to +85	LFCSP-16 7" Reel	CP-16	1,000	BCP25
ADN2850BCP250	250	±2	±4	–40 to +85	LFCSP-16	CP-16	96	BCP250
ADN2850BCP250-RL7	250	±2	±4	–40 to +85	LFCSP-16 7" Reel	CP-16	1,000	BCP250
ADN2850BRU25	25	±2	±4	–40 to +85	TSSOP-16	RU-16	96	2850B25
ADN2850BRU25-RL7	25	±2	±4	–40 to +85	TSSOP-16 7" Reel	RU-16	1,000	2850B25

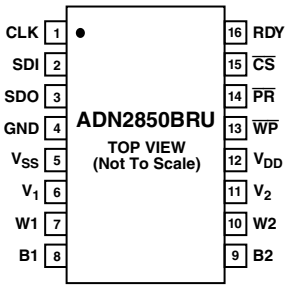
*Line 1 contains product number, ADN2850, line 2 Top Mark branding contains differentiating detail by part type, line 3 contains lot number, line 4 contains product date code YYWW.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2850 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS





ADN2850BCP PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SDO	Serial Data Output Pin. Open-Drain output requires external pull-up resistor. CMD_9 and CMD_10 activate the SDO output. See Instruction Operation Truth Table (Table II). Other commands shift out the previously loaded SDI bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages.
2	GND	Ground Pin, logic ground reference
3	V_{SS}	Negative Supply. Connect to zero volts for single-supply applications.
4	V_1	Log Output Voltage 1 generated from internal diode configured transistor
5	W1	Wiper terminal of RDAC1 ADDR (RDAC1) = 0_H.
6	B1	B terminal of RDAC1
7	B2	B terminal of RDAC2
8	W2	Wiper terminal of RDAC2. ADDR (RDAC2) = 1_H.
9	V_2	Log Output Voltage 2 generated from internal diode configured transistor
10	V_{DD}	Positive Power Supply Pin
11	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present register contents, except $\overline{PR}$ and CMD_1 and CMD_8 will refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high.
12	$\overline{PR}$	Hardware Override Preset Pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
13	$\overline{CS}$	Serial Register chip select active low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
14	RDY	Ready. Active high open-drain output. Identifies completion of commands 2, 3, 8, 9, 10, and $\overline{PR}$.
15	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
16	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.

ADN2850BRU PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
3	SDO	Serial Data Output Pin. Open-drain out put requires external pull-up resistor. CMD_9 and CMD_10 activate the SDO output. See Instruction Operation Truth Table (Table II). Other commands shift out the previously loaded SDI bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages.
4	GND	Ground Pin, logic ground reference
5	V_{SS}	Negative Supply. Connect to zero volts for single-supply applications.
6	V_1	Log Output Voltage 1 generated from internal diode configured transistor
7	W1	Wiper terminal of RDAC1. ADDR (RDAC1) = 0_H.
8	B1	B terminal of RDAC1
9	B2	B terminal of RDAC2
10	W2	Wiper terminal of RDAC2. ADDR (RDAC2) = 1_H.
11	V_2	Log Output Voltage 2 generated from internal diode configured transistor
12	V_{DD}	Positive Power Supply Pin
13	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents except $\overline{PR}$ and CMD_1 and CMD_8 will refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high.
14	$\overline{PR}$	Hardware Override Preset Pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
15	$\overline{CS}$	Serial Register chip select active low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active high open-drain output. Identifies completion of commands 2, 3, 8, 9, 10, and $\overline{PR}$.

Table I. 24-Bit Serial Data-Word

	MSB			Instruction Byte 0					Data Byte 1								Data Byte 0							LSB
RDAC	C3	C2	C1	C0	0	0	0	A0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Command bits are C0 to C3. Address bits are A3–A0. Data bits D0 to D9 are applicable to RDAC wiper register whereas D0 to D15 are applicable to EEMEM Register. Command instruction codes are defined in Table II.

Table II. Instruction Operation Truth Table[1, 2, 3]

Inst Number	Instruction Byte 0 B23 • • • • • • • • • • • • • • • • B16								Data Byte 1 B15 • • • • • • B8	Data Byte 0 B7 • • • • • B0	Operation
	C3	C2	C1	C0	A3	A2	A1	A0	X • • • • D9 D8	D7 • • • • • D0	
0	0	0	0	0	X	X	X	X	X • • • • X X	X • • • • • • X	NOP: Do nothing. See Table XI for Programming example.
1	0	0	0	1	0	0	0	A0	X • • • • X X	X • • • • • • X	Retrieve contents of EEMEM(A0) to RDAC(A0) Register. This command leaves device in the Read Program power state. To return part to the idle state, perform NOP instruction 0. See Table XI.
2	0	0	1	0	0	0	0	A0	X • • • • X X	X • • • • • • X	SAVE WIPER SETTING: Write contents of RDAC(A0) to EEMEM(A0). See Table X.
3[4]	0	0	1	1	A3	A2	A1	A0	D15 • • • • D8	D7 • • • • • D0	Write contents of Serial Register Data Bytes 0 and 1 (total 16-bit) to EEMEM(ADDR). See Table XIII.
4[5]	0	1	0	0	0	0	0	A0	X • • • • X X	X • • • • • • X	Decrement 6 dB: Right shift contents of RDAC(A0) Register, stops at all "Zeros."
5[5]	0	1	0	1	X	X	X	X	X • • • • X X	X • • • • • • X	Decrement All 6 dB: Right shift contents of all RDAC Registers, stops at all "Zeros."
6[5]	0	1	1	0	0	0	0	A0	X • • • • X X	X • • • • • • X	Decrement contents of RDAC(A0) by "One," stops at all "Zeros."
7[5]	0	1	1	1	X	X	X	X	X • • • • X X	X • • • • • • X	Decrement contents of all RDAC Registers by "One," stops at all "Zeros."
8	1	0	0	0	X	X	X	X	X • • • • X X	X • • • • • • X	RESET: Load all RDACs with their corresponding EEMEM previously saved values.
9	1	0	0	1	A3	A2	A1	A0	X • • • • X X	X • • • • • • X	Transfer contents of EEMEM (ADDR) to Serial Register Data Bytes 0 and 1, and previously stored data can be read out from the SDO pin. See Table XIV.
10	1	0	1	0	0	0	0	A0	X • • • • X X	X • • • • • • X	Transfer contents of RDAC (A0) to Serial Register Data Bytes 0 and 1, and wiper setting can be read from the SDO pin. See Table XV.
11	1	0	1	1	0	0	0	A0	X • • • • D9 D8	D7 • • • • • D0	Write contents of Serial Register Data Bytes 0 and 1 (total 11-bit) to RDAC(A0). See Table IX.
12[5]	1	1	0	0	0	0	0	A0	X • • • • X X	X • • • • • • X	Increment 6 dB: Left shift contents of RDAC(A0), stops at all "Ones." See Table XII.
13[5]	1	1	0	1	X	X	X	X	X • • • • X X	X • • • • • • X	Increment All 6 dB: Left shift contents of all RDAC Registers, stops at all "Ones."
14[5]	1	1	1	0	0	0	0	A0	X • • • • X X	X • • • • • • X	Increment contents of RDAC(A0) by "One," stops at all "Ones." See Table X.
15[5]	1	1	1	1	X	X	X	X	X • • • • X X	X • • • • • • X	Increment contents of all RDAC Registers by "One," stops at all "Ones."

NOTES

[1]The SDO output shifts out the last 24 bits of data clocked into the serial register for daisy-chain operation. Exception: for any instruction following Instruction 9 or 10, the selected internal register data will be present in data byte 0 and 1. The instructions following 9 and 10 must also be a full 24-bit data-word to completely clock out the contents of the serial register.

[2]The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding nonvolatile EEMEM register.

[3]Execution of the above operations takes place when the $\overline{CS}$ strobe returns to logic high.

[4]Instruction 3 writes 2 data bytes (total 16-bit) to EEMEM. But in the cases of addresses 0 and 1, only the last 10 bits are valid for wiper position setting.

[5]The increment, decrement, and shift commands ignore the contents of the shift register data bytes 0 and 1.

OPERATIONAL OVERVIEW

The ADN2850 programmable resistor is designed to operate as a true variable resistor. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratch pad register which allows unlimited changes of resistance settings. The scratch pad register can be programmed with any position setting using the standard SPI serial interface by loading the 24-bit data-word. The format of the data-word is that the first 4 bits are instructions, the following 4 bits are addresses, and the last 16 bits are data. Once a specific value is set, this value can be saved into a corresponding EEMEM register. During subsequent power-ups, the wiper setting will automatically be loaded at that value. Saving data to the EEMEM takes about 25 ms and consumes approximately 20 mA. During this time the shift register is locked, preventing any changes from taking place. The RDY pin indicates the completion of this EEMEM saving process. There are also 13 two-bytes addresses, of user defined data that can be stored in EEMEM.

OPERATION DETAIL

There are 16 instructions that facilitate users' programming needs. Referring to Table II, the instructions are:

0. Do Nothing
1. Restore EEMEM setting to RDAC
2. Save RDAC setting to EEMEM
3. Save user data or RDAC setting to EEMEM
4. Decrement 6 dB
5. Decrement all 6 dB
6. Decrement one step
7. Decrement all one step
8. Reset all EEMEM settings to RDAC
9. Read EEMEM to SDO
10. Read Wiper Setting to SDO
11. Write data to RDAC
12. Increment 6 dB
13. Increment all 6 dB
14. Increment one step
15. Increment all one step

Tables VIII to XIV provide a few programming examples by using some of these instructions.

Scratch Pad and EEMEM Programming

The basic mode of setting the programmable resistor wiper position (programming the scratch pad register) is done by loading the serial data input register with the instruction 11, the corresponding address, and the data. Since the scratch pad register is a standard logic register, there is no restriction on the number of changes allowed. When the desired wiper position is determined, the user can load the serial data input register with the instruction 2, which stores the setting into the corresponding EEMEM register. The EEMEM value can be changed at any time or permanently protected by activating the $\overline{WP}$ command. Table III provides a programming example listing the sequence of serial data input (SDI) words and the corresponding serial data output (SDO) in hexadecimal format.

Table III. Set and Save RDAC with Independent Data to EEMEM Registers

SDI	SDO	Action
$B00100_H$	$XXXXXX_H$	Loads data 100_H into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
$20xxxx_H$	$B00100_H$	Saves copy of RDAC1 register content into corresponding EEMEM1 register.
$B10200_H$	$20xxxx_H$	Loads 200_H data into RDAC2 register, Wiper W2 moves to 1/2 full-scale position.
$21xxxx_H$	$B10200_H$	Saves copy of RDAC2 register contents into corresponding EEMEM2 register.

At system power ON, the scratch pad register is automatically refreshed with the value previously saved in the corresponding EEMEM register. The factory preset EEMEM value is midscale. During operations, the scratch pad register can also be refreshed with the current contents of the EEMEM registers in three different ways. First, executing instruction 1 retrieves the corresponding EEMEM value. Second, executing instruction 8 resets the EEMEM values of both channels. Finally, pulsing the $\overline{PR}$ pin also refreshes both EEMEM settings. Operating the hardware control $\overline{PR}$ function, however, requires a complete pulse signal. When $\overline{PR}$ goes low, the internal logic sets the wiper at midscale. The EEMEM value will not be loaded until PR returns to high.

EEMEM Protection

The write-protect ($\overline{WP}$) disables any changes of the scratch pad register contents regardless of the software commands, except that the EEMEM setting can be refreshed and can overwrite the $\overline{WP}$ by using commands 1, 8, and $\overline{PR}$ pulse. To disable $\overline{WP}$, it is recommended to execute a NOP command before returning $\overline{WP}$ to logic high.

Linear Increment and Decrement Commands

The increment and decrement commands (14, 15, 6, 7) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to just send an increment or decrement command to the device. The adjustment can be individually or gang controlled. For increment command, executing instruction 14 will automatically move the wiper to the next resistance segment position. The master increment instruction 15 will move all resistor wipers up by one position.

Logarithmic Taper Mode Adjustment (±6 dB/step)

There are four programming instructions which provide the logarithmic taper increment and decrement wiper position control by either individual or gang control. 6 dB increment is activated by instructions 12 and 13 and 6 dB decrement is activated by instructions 4 and 5. For example, starting at zero scale, executing 11 times the increment instruction 12 will move the wiper in 6 dB per step from the 0% of the full-scale R_{WB} to the full-scale R_{WB}. The 6 dB increment instruction doubles the value of the RDAC register contents each time the command is executed. When the wiper position is near the maximum setting, the last 6 dB increment instruction will cause the wiper to go to the full-scale 1023-code position. Further 6 dB per increment instruction will no longer change the wiper position beyond its full-scale, Table IV.

6 dB step increment and decrement are achieved by shifting the bit internally to the left and right, respectively. The following information explains the nonideal ±6 dB step adjustment at certain

conditions. Table IV illustrates the operation of the shifting function on the individual RDAC register data bits. Each line going down the table represents a successive shift operation. Note that the left shift 12 and 13 commands were modified such that if the data in the RDAC register is equal to zero, and the data is left shifted, the RDAC register is then set to code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale, and the data is left shifted, then the data in the RDAC register is automatically set to full scale. This makes the left shift function as ideal a logarithmic adjustment as possible.

The right shift 4 and 5 commands will be ideal only if the LSB is zero (i.e., ideal logarithmic—no error). If the LSB is a one, then the right shift function generates a linear half LSB error, which translates to a number of bits-dependent logarithmic error as shown in Figure 3. The plot shows the error of the odd numbers of bits for ADN2850.

Table IV. Detail Left and Right Shift Functions for 6 dB Step Increment and Decrement

	Left Shift	Right Shift	
	00 0000 0000	11 1111 1111	
	00 0000 0001	01 1111 1111	
	00 0000 0010	00 1111 1111	
	00 0000 0100	00 0111 1111	
	00 0000 1000	00 0011 1111	
Left Shift	00 0001 0000	00 0001 1111	Right Shift
+6 dB/step	00 0010 0000	00 0000 1111	−6 dB/step
	00 0100 0000	00 0000 0111	
	00 1000 0000	00 0000 0011	
	01 0000 0000	00 0000 0001	
	10 0000 0000	00 0000 0000	
	11 1111 1111	00 0000 0000	
	11 1111 1111	00 0000 0000	

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each right shift 4 and 5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 3 shows plots of Log_Error [i.e., $20 \times \log_{10}$ (error/code)] ADN2850. For example, code 3 Log_Error = $20 \times \log_{10}$ (0.5/3) = –15.56 dB, which is the worst case. The plot of Log_Error is more significant at the lower codes.

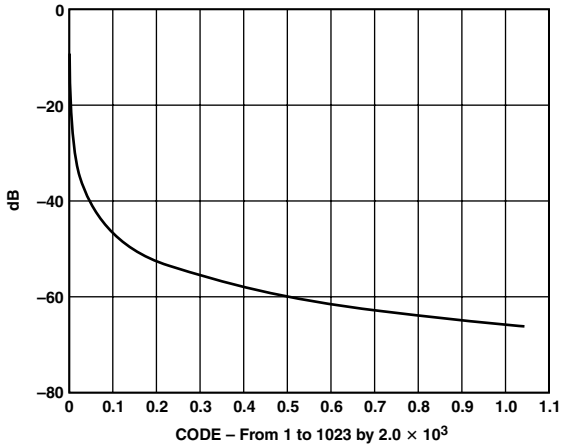


Figure 3. Plot of Log_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits Are Ideal)

Using Additional Internal Nonvolatile EEMEM

The ADN2850 contains additional internal user storage registers (EEMEM) for saving constants and other 16-bit data. Table V provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and and 26 bytes (13 addresses × 2 bytes each) of USER EEMEM.

Table V. EEMEM Address Map

EEMEM Number	Address	EEMEM Content For
1	0000	RDAC1[1, 2]
2	0001	RDAC2
3	0010	USER1[3]
4	0011	USER2
:	:	:
15	1110	USER13
16	1111	% Tolerance[4]

NOTES
[1]RDAC data stored in EEMEM locations are transferred to their corresponding RDAC REGISTER at power-on, or when instructions 1, 8, and $\overline{PR}$ are executed.
[2]Execution of instruction 1 leaves the device in the read mode power consumption state. After the last instruction 1 is executed, the user should perform a NOP, instruction 0 to return the device to the low power idling state.
[3]USER <data> are internal nonvolatile EEMEM registers available to store and retrieve constants and other 16-bit information using instructions 3 and 9 respectively.
[4]Read only.

Calculating Actual Full-Scale Resistance

The actual tolerance of the rated full-scale resistance R_{WB1} is stored in EEMEM register 15 during factory testing. The actual full-scale resistance can therefore be calculated, which will be valuable for tolerance matching or calibration. Notice this value is read only, and the full-scale resistance of R_{WB2_FS} matches R_{WB1_FS}, of typically 0.1%.

The tolerance in % is stored in the last 16 bits of data in EEMEM register 15. The format is sign magnitude binary format with the MSB designates for sign (0 = positive and 1 = negative), the next 7 MSB designate for the integer number, and the 8 LSB designate for the decimal number. See Table VI.

Table VI. Tolerance in % from Rated Full-Scale Resistance

Bit	D15	D14	D13	D12	D11	D10	D9	D8	·	D7	D6	D5	D4	D3	D2	D1	D0
sign mag	sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	Sign	7 Bits for Integer Number							Decimal Point	8 Bits for Decimal Number							

For example, if $R_{WB\_FS\_RATED}$ = 250 kΩ and the data is 0001 1100 0000 1111, $R_{WB\_FS\_ACTUAL}$ can be calculated as follows:

MSB: 0 = Positive
Next 7 MSB: 001 1100 = 28
8 LSB: 0000 1111 = $15 \times 2^{-8} = 0.06$
% Tolerance = +28.06%

Thus, $R_{WB\_FS\_ACTUAL}$ = 320.15 kΩ

Daisy-Chain Operation

The serial data output pin (SDO) serves two purposes. It can be used to read out the contents of the wiper settings or EEMEM values using instructions 10 and 9 respectively. If these instructions are not used, SDO can be used for daisy-chaining multiple devices in simultaneous operations (see Figure 4). The SDO pin contains an open-drain N-Ch FET and requires a pull-up resistor if SDO function is used. Users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may induce time delay to the subsequent devices (see Figure 4). If two ADN2850s are daisy-chained, a total 48 bits of data is required. The first 24 bits (formatted 4-bit instruction, 4-bit address, and 16-bit data) go to U2 and the second 24 bits with the same format go to U1. The $\overline{CS}$ should be kept low until all 48 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.

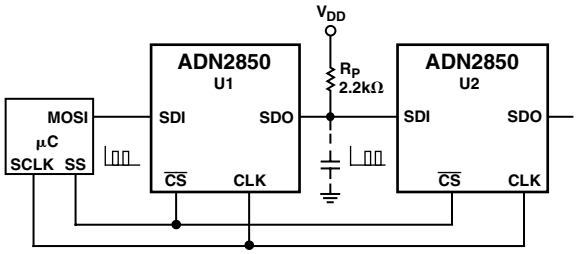


Figure 4. Daisy-Chain Configuration

DIGITAL INPUT/OUTPUT CONFIGURATION

All digital inputs are ESD protected. Digital inputs are high impedance and can be driven directly from most digital sources. Active at logic low, $\overline{PR}$ and $\overline{WP}$ should be biased to V_{DD} if they are not used. There are no internal pull-up resistors present on any digital input pins. To avoid floating digital pins that may cause false triggering in a noisy environment, pull-up resistors should be added to these pins. However, this only applies to the case where the device will be detached from the driving source once it is programmed.

The SDO and RDY pins are open-drain digital outputs. Similarly, pull-up resistors are needed if these functions are used. To optimize the speed and power trade-off, use 2.2 kΩ pull-up resistors.

The equivalent serial data input and output logic is shown in Figure 5. The open-drain output SDO is disabled whenever chip select $\overline{CS}$ is logic high. ESD protection of the digital inputs is shown in Figures 6a and 6b.

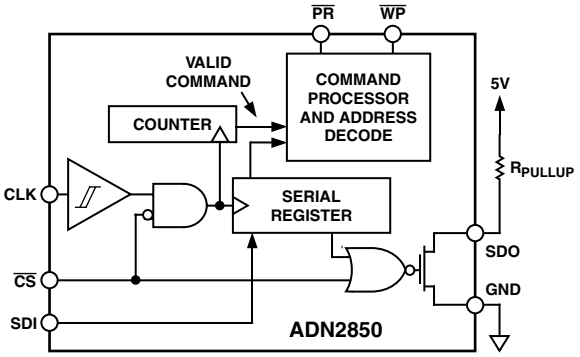


Figure 5. Equivalent Digital Input-Output Logic

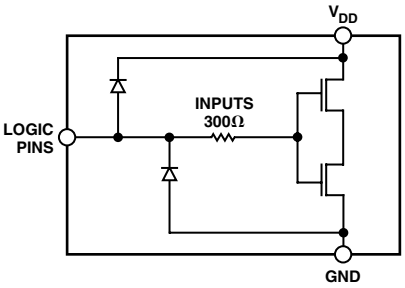


Figure 6a. Equivalent ESD Digital Input Protection

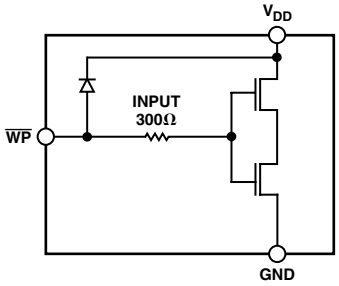


Figure 6b. Equivalent $\overline{WP}$ Input Protection

SERIAL DATA INTERFACE

The ADN2850 contains a 4-wire, SPI compatible, digital interface (SDI, SDO, $\overline{CS}$, and CLK). The 24-bit serial word must be loaded with MSB first, and the format of the word is shown in Table I. The Command Bits (C0 to C3) control the operation of the programmable resistor according to the instruction shown in Table II. A0 to A3 are assigned for address bits. A0 is used to address RDAC1 or RDAC2. Addresses 2 to 14 are accessible by users. Address 15 is reserved for the factory. Table V provides an address map of the EEMEM locations. The data bits (D0 to D9) are the values that are loaded into the RDAC registers at instruction 11. The data bits (D0 to D15) are the values that are loaded into the EEMEM registers at instruction 3.

The last instruction prior to a period of no programming activity should be applied with the No Operation (NOP), instruction 0. It is recommended to do so to ensure minimum power consumption in the internal logic circuitry

The SPI interface can be used in two slave modes, CPHA = 1, CPOL = 1 and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits that dictate SPI timing in these microconverters and microprocessors: ADuC812/ADuC824, M68HC11, and MC68HC16R1/916R1.

TERMINAL VOLTAGE OPERATING RANGE

The ADN2850 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper two-terminal programmable resistance operation. Supply signals present on terminals W and B that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 7).

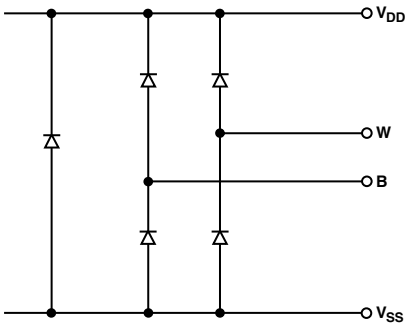


Figure 7. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the ADN2850 device is primarily used as a digital ground reference that needs to be tied to the PCB's common ground. The digital input control signals to the ADN2850 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the Specifications table of this data sheet. An internal level shift circuit ensures that the common-mode voltage range of the two terminals extends from V_{SS} to V_{DD} regardless of the digital input level. In addition, there is no polarity constraint on voltage across terminals W and B. The magnitude of $|V_{WB}|$ is bounded by $V_{DD} - V_{SS}$.

Power-Up Sequence

Since diodes limit the voltage compliance at terminals B and W (see Figure 7) it is important to power V_{DD}/V_{SS} first before applying any voltage to terminals B and W. Otherwise, the diode will be forward biased such that V_{DD}/V_{SS} will be powered unintentionally. For example, applying 5 V across V_{DD} will cause the V_{DD} terminal to exhibit 4.3 V. Although it is not destructive to the device, it may affect the rest of the user's system. As a result, the ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, Digital Inputs, and $V_{B/W}$. The order of powering V_B, V_W, and Digital Inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on reset remains effective, which retrieves EEMEM saved values to the RDAC registers (see TPC 7).

Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum of conductor length. Ground paths should have low resistance and low inductance. To minimize the digital ground bounce, the digital signal ground reference can be joined remotely to the analog ground terminal of the ADN2850.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramics capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance (see Figure 8).

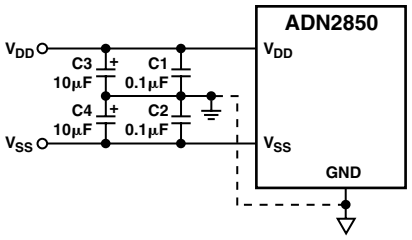


Figure 8. Power Supply Bypassing

RDAC STRUCTURE

The patent-pending RDAC contains a string of equal resistor segments, with an array of analog switches, that act as the wiper connection. The number of positions is the resolution of the device. The ADN2850 has 1024 connection points, allowing it to provide better than 0.1% setability resolution. Figure 9 shows an equivalent structure of the connections between the two terminals that make up one channel of the RDAC. The S_{WB} will always be ON, while one of the switches SW(0) to SW($2^N - 1$) will be ON one at a time depending on the resistance position decoded from the data bits. Since the switch is not ideal, there is a 50 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics if accurate prediction of the output resistance is needed.

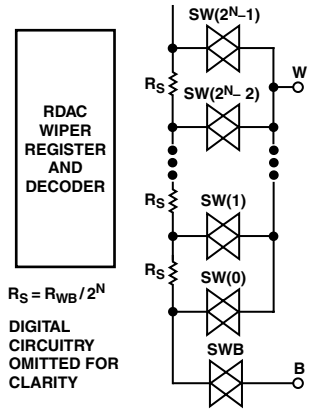


Figure 9. Equivalent RDAC Structure

Table VII. Nominal Individual Segment Resistor Values

Device Resolution	25 kΩ	250 kΩ
1024-Step	24.4	244

CALCULATING THE PROGRAMMABLE RESISTANCE

The nominal full-scale resistance of the RDAC between terminals W and B, R_{WB_FS}, is available with 25 kΩ and 250 kΩ with 1024 positions (10-bit resolution). The final digits of the part number determine the nominal resistance value, e.g., 25 kΩ = 25 and 250 kΩ = 250.

The 10-bit data-word in the RDAC latch is decoded to select one of the 1024 possible settings. The following discussion describes the calculation of resistance $R_{WB}(D)$ at different codes of a 25 kΩ part. The wiper's first connection starts at the B terminal for data 000_H. $R_{WB}(0)$ is 50 Ω because of the wiper resistance and it is independent of the full-scale resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 24.4 Ω + 50 = 74.4 Ω

for data 001_H. The third connection is the next tap point representing $R_{WB}(2) = 48.8 + 50 = 98.8\ \Omega$ for data 002_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(1023) = 25026\ \Omega$. See Figure 9 for a simplified diagram of the equivalent RDAC circuit.

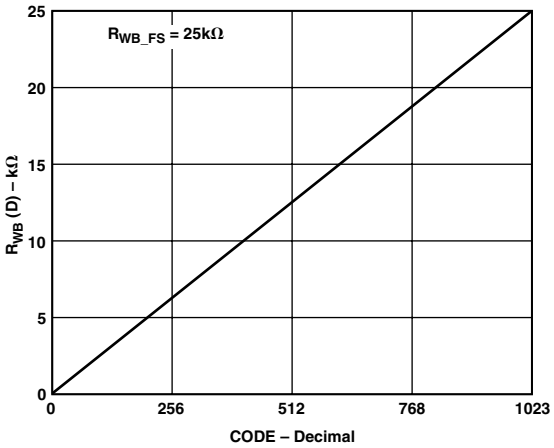


Figure 10. $R_{WB}(D)$ vs. Code

The general equation that determines the programmed output resistance between Wx and Bx is:

$$R_{WB}(D) = \frac{D}{1024} \times R_{WB\_FS} + R_W \quad (1)$$

where D is the decimal equivalent of the data contained in the RDAC register, R_{WB_FS} is the full-scale resistance between terminals W and B, and R_W is the wiper resistance.

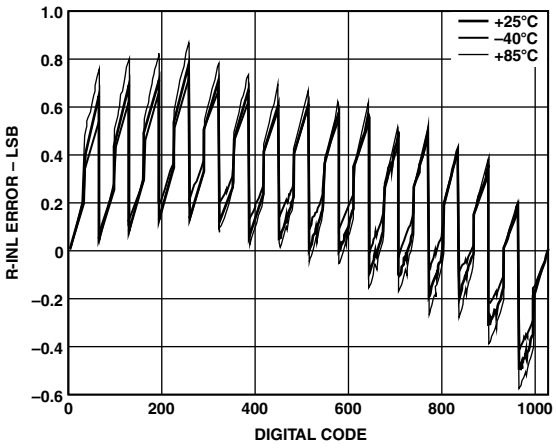
For example, the following output resistance values will be set for the following RDAC latch codes with $V_{DD} = 5$ V (applies to $R_{WB\_FS} = 25$ kΩ programmable resistors):

Table VIII. R_{WB} at Selected Codes (R_{WB_FS} = 25 kΩ)

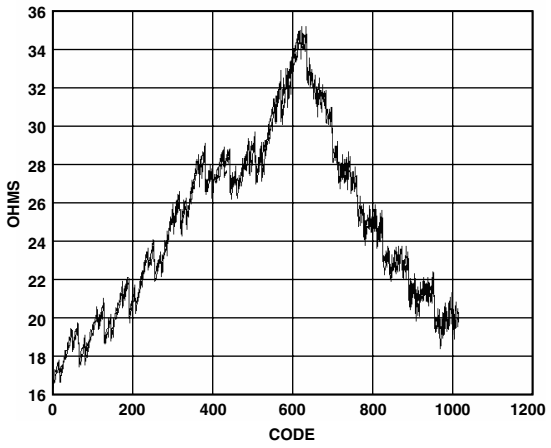
D (DEC)	$R_{WB}(D)$ (Ω)	Output State
1023	25026	Full-Scale
512	12550	Mid Scale
1	74.4	1 LSB
0	50	Zero-Scale (Wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 50 Ω is present. In this state, care should be taken to limit the current flow between W and B to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

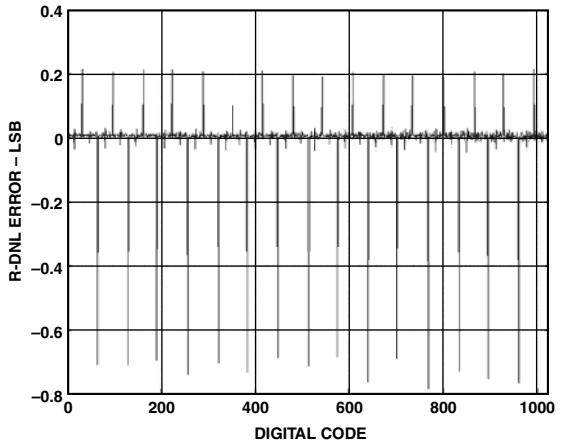
Channel-to-channel R_{WB} matching is well within 1% at full-scale. The change in R_{WB} with temperature has a 35 ppm/°C temperature coefficient.



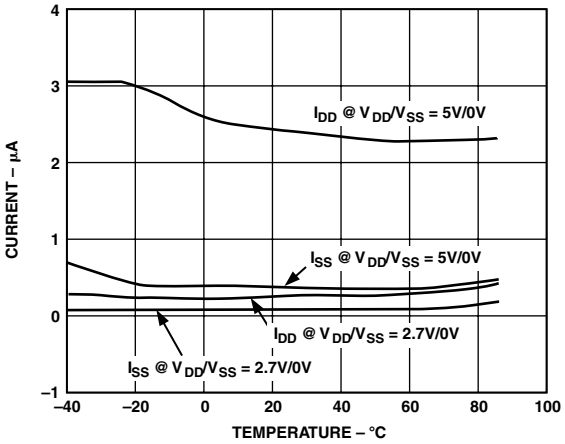
TPC 1. R-INL vs. Code, T_A = −40°C, +25°C, +85°C Overlay, R_{AB} = 25 kΩ



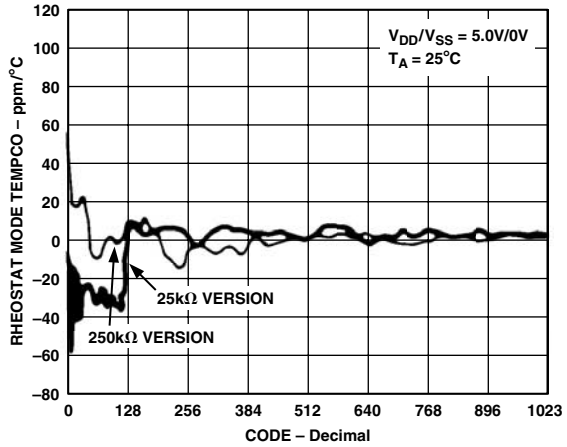
TPC 4. Wiper On-Resistance vs. Code



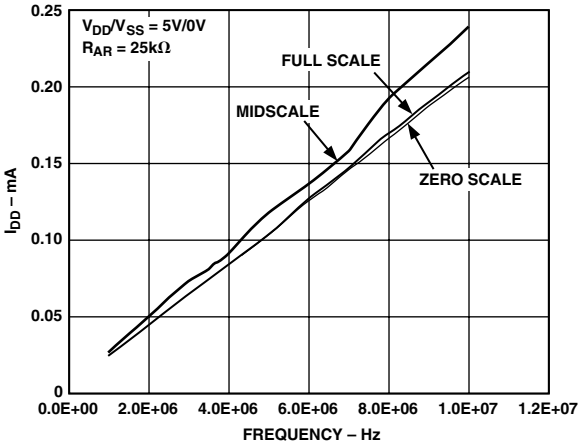
TPC 2. R-DNL vs. Code, T_A = −40°C, +25°C, +85°C Overlay, R_{AB} = 25 kΩ



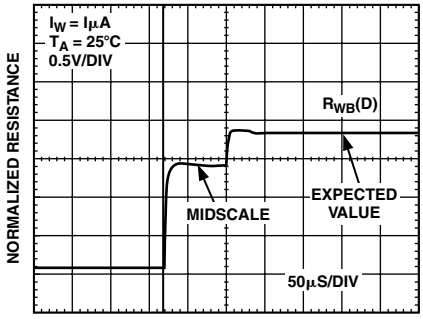
TPC 5. I_{DD} vs. Temperature, R_{AB} = 25 kΩ



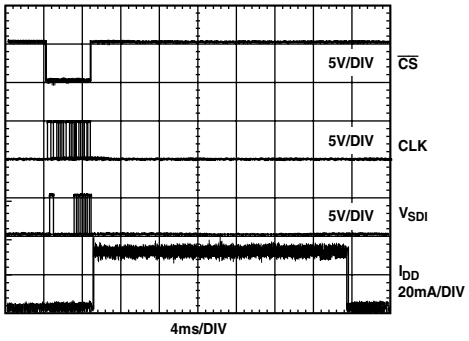
TPC 3. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco



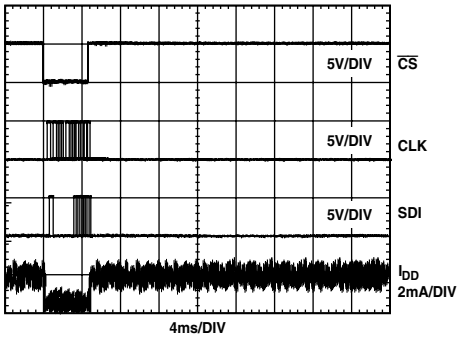
TPC 6. I_{DD} vs. Clock Frequency, R_{AB} = 25 kΩ



TPC 7. Memory Restore During Power-On Reset

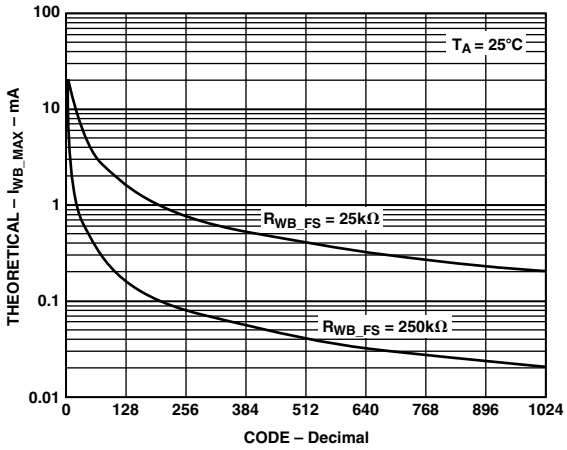


TPC 8. I_{DD} vs. Time (Save) Program Mode



SUPPLY CURRENT RETURNS TO MINIMUM POWER CONSUMPTION IF INSTRUCTION 0 (NOP) IS EXECUTED IMMEDIATELY AFTER INSTRUCTION 1 (READ EEMEM)

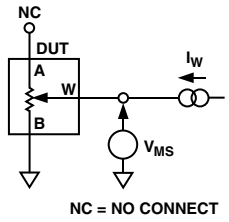
TPC 9. I_{DD} vs. Time (Read) Program Mode



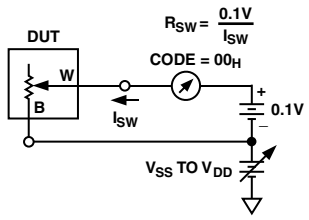
TPC 10. I_{WB_MAX} vs. Code

TEST CIRCUITS

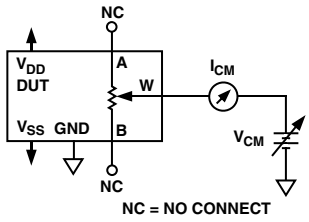
Test Circuits 1 to 3 show some of the test conditions used in the Specifications table.



Test Circuit 1. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)



Test Circuit 2. Incremental ON Resistance



Test Circuit 3. Common-Mode Leakage Current

PROGRAMMING EXAMPLES

The following programming examples illustrate the typical sequence of events for various features of the ADN2850. Users should refer to Table II for the instructions and data-word format. The instruction numbers, addresses, and data appearing at SDI and SDO pins are displayed in hexadecimal format in the following examples.

Table IX. Scratch Pad Programming

SDI	SDO	Action
$B00100_H$	$XXXXXX_H$	Loads data 100_H into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
$B10200_H$	$B00100_H$	Loads data 200_H into RDAC2 register, Wiper 2 moves to 1/2 full-scale position.

Table X. Incrementing RDAC Followed by Storing the Wiper Setting to EEMEM

SDI	SDO	Action
$B00100_H$	$XXXXXX_H$	Loads data 100_H into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
$E0XXXX_H$	$B00100_H$	Increments RDAC1 register by one to 101_H.
$E0XXXX_H$	$E0XXXX_H$	Increments RDAC1 register by one to 102_H. **Repeat the increment command – ($E0XXXX_H$) until desired wiper position is reached**
$20XXXX_H$	$XXXXXX_H$	Saves RDAC1 data into EEMEM1 Optionally tie $\overline{WP}$ to GND to protect EEMEM values

Table XI. Restoring EEMEM Values to RDAC Registers

EEMEM values for RDACs can be restored by: Power-On, Strobing $\overline{PR}$ pin or Programming shown below.

SDI	SDO	Action
$10XXXX_H$	$XXXXXX_H$	Restores EEMEM1 value to RDAC1 register.
$00XXXX_H$	100100_H	NOP. Recommended step to minimize power consumption.
$8XXXXX_H$	$00XXXX_H$	Reset EEMEM1 and EEMEM2 values to RDAC1 and RDAC2 registers respectively.

Table XII. Using Left Shift by One to Increment 6 dB Steps

SDI	SDO	Action
$C0XXXX_H$	$XXXXXX_H$	Moves wiper 1 to double the present data contained in RDAC1 register.
$C1XXXX_H$	$C0XXXX_H$	Moves wiper 2 to double the present data contained in RDAC2 register.

Table XIII. Storing Additional User Data in EEMEM

SDI	SDO	Action
$32AAAA_H$	$XXXXXX_H$	Stores data $AAAA_H$ into spare EEMEM location USER1. (Allowable to address in 13 locations with maximum 16 bits of data).
335555_H	$32AAAA_H$	Stores data 5555_H into spare EEMEM location USER2. (Allowable to address in 13 locations with maximum 16 bits of data).

Table XIV. Reading Back Data From Various Memory Locations

SDI	SDO	Action
$92XXXX_H$	$XXXXXX_H$	Prepares data read from USER1 location.
$00XXXX_H$	$92AAAA_H$	NOP instruction 0 sends 24-bit word out of SDO where the last 16 bits contain the contents of USER1 location. NOP command ensures device returns to idle power dissipation state.

Table XV. Reading Back Wiper Setting

SDI	SDO	Action
$B00200_H$	$XXXXXX_H$	Sets RDAC1 to midscale.
$C0XXXX_H$	$B00200_H$	Doubles RDAC1 from midscale to full-scale.
$A0XXXX_H$	$C0XXXX_H$	Prepares reading wiper setting from RDAC1 register.
$XXXXXX_H$	$A003FF_H$	Readback full-scale value from RDAC1 register.

Analog Devices offers a user-friendly ADN2850EVAL evaluation kit that can be controlled by a personal computer through the printer port. The driving program is self-contained, so no programming languages or skills are needed.

APPLICATIONS

Optical Transmitter Calibration with ADN2841

Together with the multirate 2.7 Gbps Laser Diode Driver ADN2841, the ADN2850 forms an optical supervisory system where the dual programmable resistors are used to set the laser average optical power and extinction ratio (see Figure 11). The ADN2850 is particularly ideal for the optical parameter settings because of its high resolution, compact footprint, and superior temperature coefficient characteristics.

The ADN2841 is a 2.7 Gbps laser diode driver that uses a unique control algorithm to manage both the laser average power and extinction ratio after the laser initial factory calibration. It stabilizes the laser data transmission by continuously monitoring its optical power, and correcting the variations caused by temperature and the laser degradation over time. In the ADN2841, the I_{MPD} monitors the laser diode current. Through its dual-loop power and extinction ratio control, calibrated by the ADN2850, the internal driver controls the bias current I_{BIAS} and consequently the average power. It also regulates the modulation current I_{MODP} by changing the modulation current linearly with slope efficiency. Any changes in the laser threshold current or slope efficiency are therefore compensated. As a result, this optical supervisory system minimizes the laser characterization efforts and enables designers to apply comparable lasers from multiple sources.

Incoming Optical Power Monitoring

The ADN2850 comes with a pair of matched diode connected PNPs, Q_1 and Q_2, that can be used to configure an incoming optical power monitoring function. With a reference current source, an instrumentation amplifier, and a logarithmic amplifier, this feature can be used to monitor the optical power by knowing the dc average photodiode current from the following relationships:

$$V_1 = V_{BE1} = V_T In \frac{I_{C1}}{I_{S1}} \quad (2)$$

$$V_2 = V_{BE2} = V_T In \frac{I_{C2}}{I_{S2}} \quad (3)$$

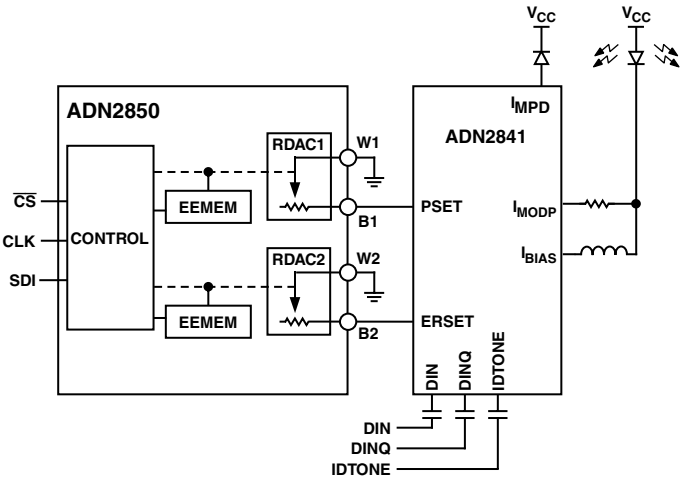


Figure 11. Optical Supervisory System

Knowing $I_{C1} = a_1 \times I_{PD}$, $I_{C2} = a_2 \times I_{REF}$, and $Q_1 - Q_2$ are matched, therefore a and I_S are matched. Combining Equations 2 and 3 theoretically yields:

$$V_2 - V_1 = V_T In \left(\frac{I_{REF}}{I_{PD}} \right) \quad (4)$$

Where I_{S1} and I_{S2} are saturation current
V_1, V_2 are V_{BE}, base-emitted voltages of the diode connector transistors
V_T is the thermal voltage, which is equal to k × T/q.
V_T = 26 mV at 25°C
k = Boltzmann's constant = 1.38E–23 Joules/Kelvin
q = electron charge = 1.6E–19 coulomb
T = temperature in Kelvin
I_{PD} = photodiode current
I_{REF} = reference current

Figure 12 shows such a conceptual circuit.

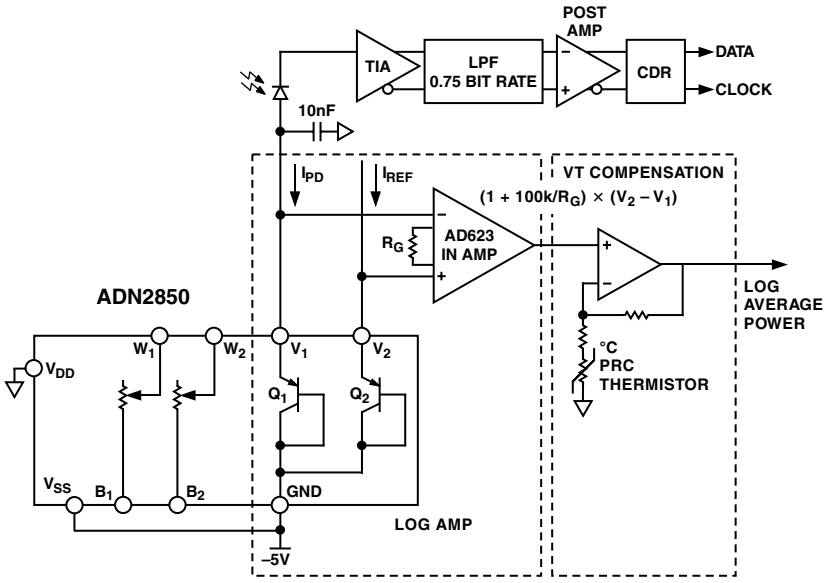


Figure 12. Conceptual Incoming Optical Power Monitoring Circuit

The output voltage represents the average incoming optical power. The output voltage of the log stage does not have to be accurate from device to device, as the responsivity of the photodiode will change between devices. An op amp stage is shown after the log amp stage, which compensates for V_T variation over temperature.

Equation 4 is ideal. If the reference current is 1 mA at room temperature, characterization shows that there is an additional 30 mV offset between V_2 and V_1. A curve fit approximation yields

$$V_2 - V_1 = 0.026 \times In\left(\frac{0.001}{I_{PD}}\right) + 0.03 \quad (5)$$

Such offset is believed to be caused by the transistors self-heating and the thermal gradient effect. As seen in Figure 13, the error between an approximation and the actual performance ranges is less than 0% to –4% from 0.1 mA to 0.1 μA.

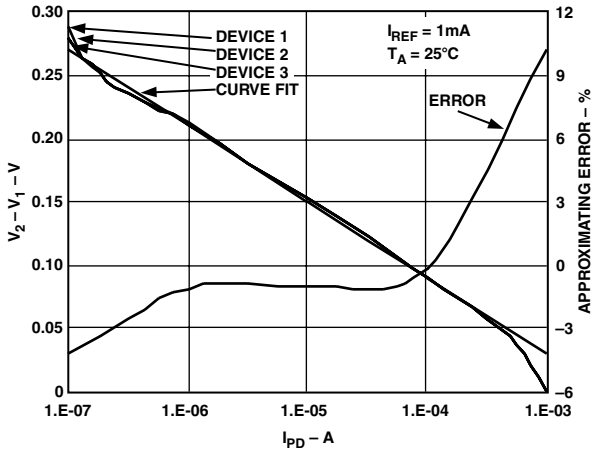


Figure 13. Typical $V_2 - V_1$ vs. I_{PD} at I_{REF} = 1 mA and T_A = 25°C

Resistance Scaling

The ADN2850 offers either 25 kΩ or 250 kΩ full-scale resistance. Users who need lower resistance and still maintain the numbers of step adjustment can parallel two or more devices. Figure 14 shows a simple scheme of paralleling both channels of the programmable resistors. In order to adjust half of the resistance linearly per step, users need to program both devices coherently with the same settings. Note that since the devices will be programmed one after another, an intermediate state will occur, and this method may not be suitable for certain applications.

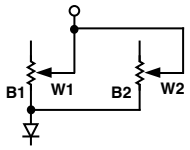


Figure 14. Reduce Resistance by Half with Linear Adjustment Characteristics

Much lower resistance can also be achieved by paralleling a discrete resistor as shown in Figure 15.

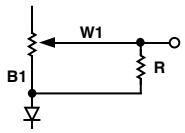


Figure 15. Resistor Scaling with Pseudo-Log Taper Adjustment Characteristics

The equivalent resistance at a given setting is approximated as:

$$R_{eq} = \frac{D \times R_{WB\_FS} + 51200}{D \times R_{WB\_FS} + 51200 + 1024 \times R} \quad (6)$$

In this approach, the adjustment is not linear but pseudo-logarithmic. Users should be aware of the need for tolerance matching as well as temperature coefficient matching of the components.

BASIC RDAC SPICE MODEL

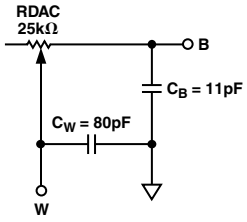


Figure 16. RDAC Circuit Simulation Model (RDAC = 25 kΩ)

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RADCs. A general parasitic simulation model is shown in Figure 16.

Listing I provides a macro model net list for the 25 kΩ RDAC:

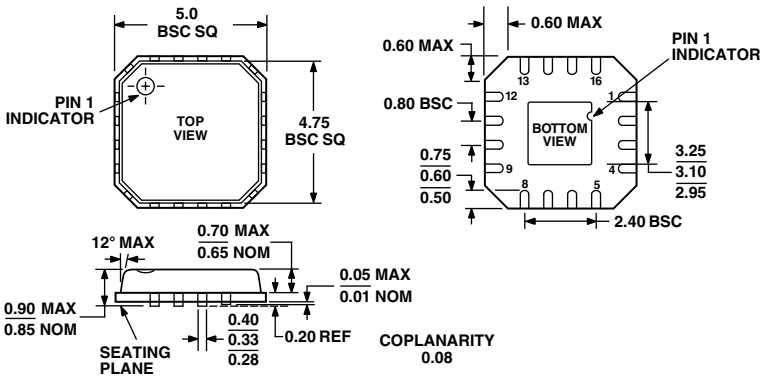
Listing I. Macro Model Net List for RDAC

```
.PARAM D = 1024, RDAC = 25E3
*
.SUBCKT RDAC (W, B)
*
RWB W B {D/1024 × RDAC + 50}
CW W 0 80E-12
CB B 0 11E-12
*
.ENDS RDAC
```

OUTLINE DIMENSIONS

16-Lead Frame Chip Scale Package [LFCSP]
5 x 5 mm Body
(CP-16 5x5)

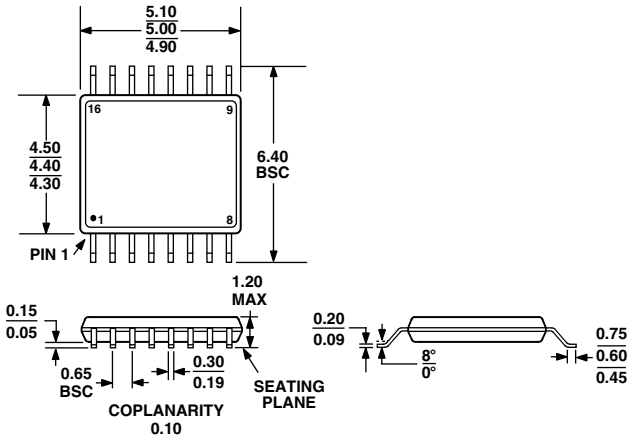
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220VHHB

16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB

Revision History

Location	Page

9/02—Data sheet changed from REV. A to REV. B.

Changes to GENERAL DESCRIPTION 1
Changes to ELECTRICAL CHARACTERISTICS 2
Changes to Calculating Actual Full-Scale Resistance section 9
Changes to Table VI 9
Updated OUTLINE DIMENSIONS 18

C02660–0–9/02(B)

PRINTED IN U.S.A.