Carmine Evaluation Board

FUJITSU

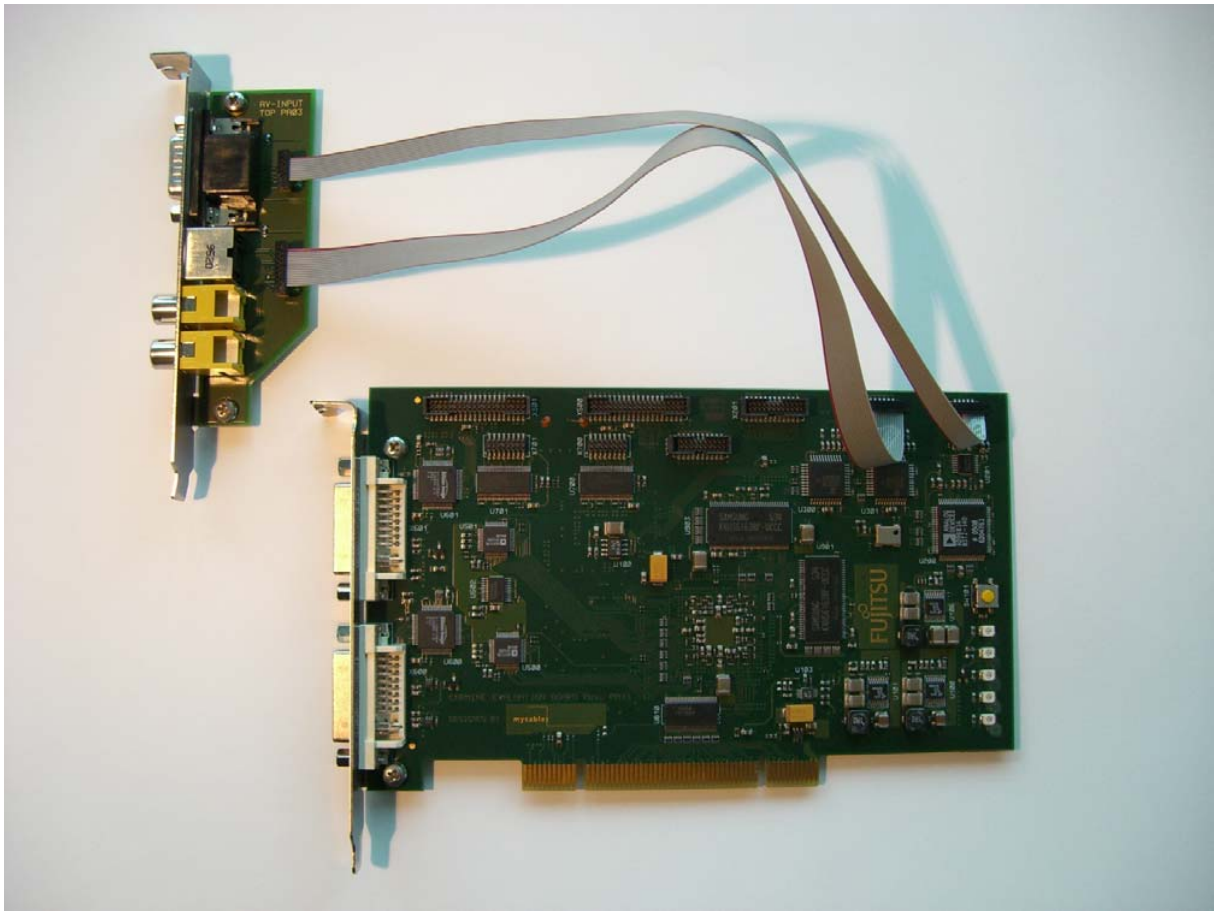
MB86297-EB01

Rev. 1.3

Feb 2007

1.3

Carmine Evaluation Board Manual



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Document Revision History

Revision Number	Date	Description of changes
1.0	15/07/05	Preliminary Version
1.1	08/11/05	First Version for Board Revision PA10
1.2	03/01/06	Adopted to board revision PA11
1.3	19/02/07	Typo corrections, new (corrected) block diagram, contact addresses

Evaluation Board Revision History

Revision Number	Date	Description of changes
PA10	8/11/05	First Version PA10
PA11	03/01/06	Revised version - 0 Ohm resistor at U103 (permanent Reset) removed - Vref termination: 4x 0 Ohm replaced with 1.5KOhm (DDR read problem) - metal plate added - distance between DVI connectors increased - jumper labeled auf Bauteil von 0-7 - pin 1 marking for X400 (FPGA programming) - pin 1 marking for X100/X101 (AV Board) - R602 and R612 not assembled, enabling I2C-access to DVI-Encoder - R307 und R318 not assembled, pin 25 U300 connected GND, (defining I2C address to SAA)

CONTENTS

1 Overview

This PCI evaluation board is designed to evaluate and test the functionality of the Fujitsu MB86297 “Carmine” Graphic Display Controller (GDC).

The evaluation board can be used in any 5V or 3.3V PCI system (PCI V2.1 compliant) at 33 MHz / 66 MHz bus frequency. The example software and drivers included in this system were developed for the Windows NT™, Windows 2000™ and Windows XP™ operating systems.

2 Hardware Installation

In order to install the MB86297-EB01 evaluation board in your system, follow these instructions:

1. Make sure all jumpers are set to their default positions (refer to “Jumper Settings”).
2. Power down your target system (PC or other PCI environment) and insert the card. Note that either 3.3V or 5V systems can be used. Level-converters allow the operation of the evaluation board in a 5V environment, but the Carmine GDC itself only has a 3.3V PCI interface.
3. Restart your target system
4. Install the software driver and example software **(refer to the software installation instructions on the CD ROM)**
5. Connect at least one DVI or VGA monitor to the output connector(s) to see the examples provided

3 System Components

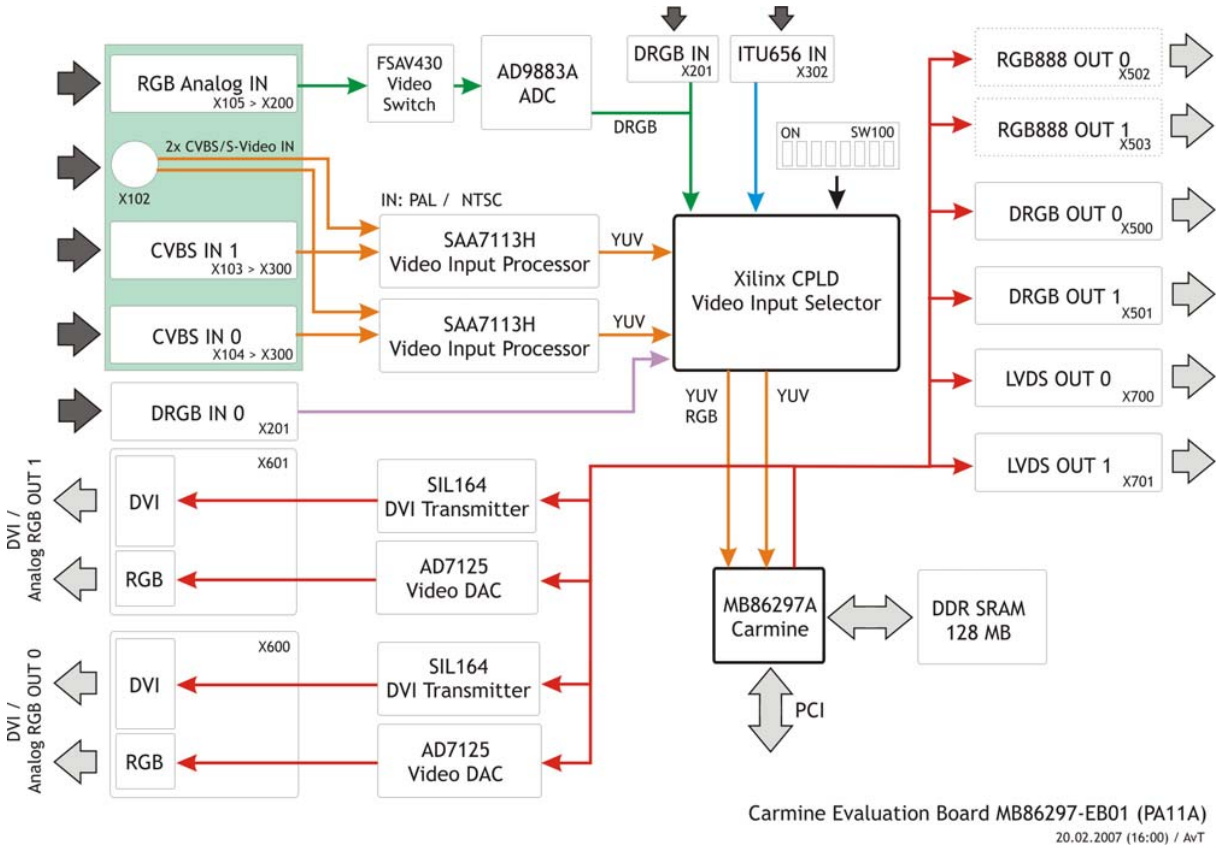


Figure 1 Block Diagram

The main components and interfaces of the MB86297-EB01 evaluation board:
"Carmine" Graphic Controller

- 128Mbyte DDR SDRAM memory

Video outputs

- 2x DVI
- 2x Analog RGB
- 2x RGB digital
- 2x LVDS

Video input:

- 1x Digital RGB666
- 1x Analog RGB
- 2x CVBS/FBAS (PAL or NTSC)

Others

- Test LEDs
- Configuration switches

4 Main Board External Appearance

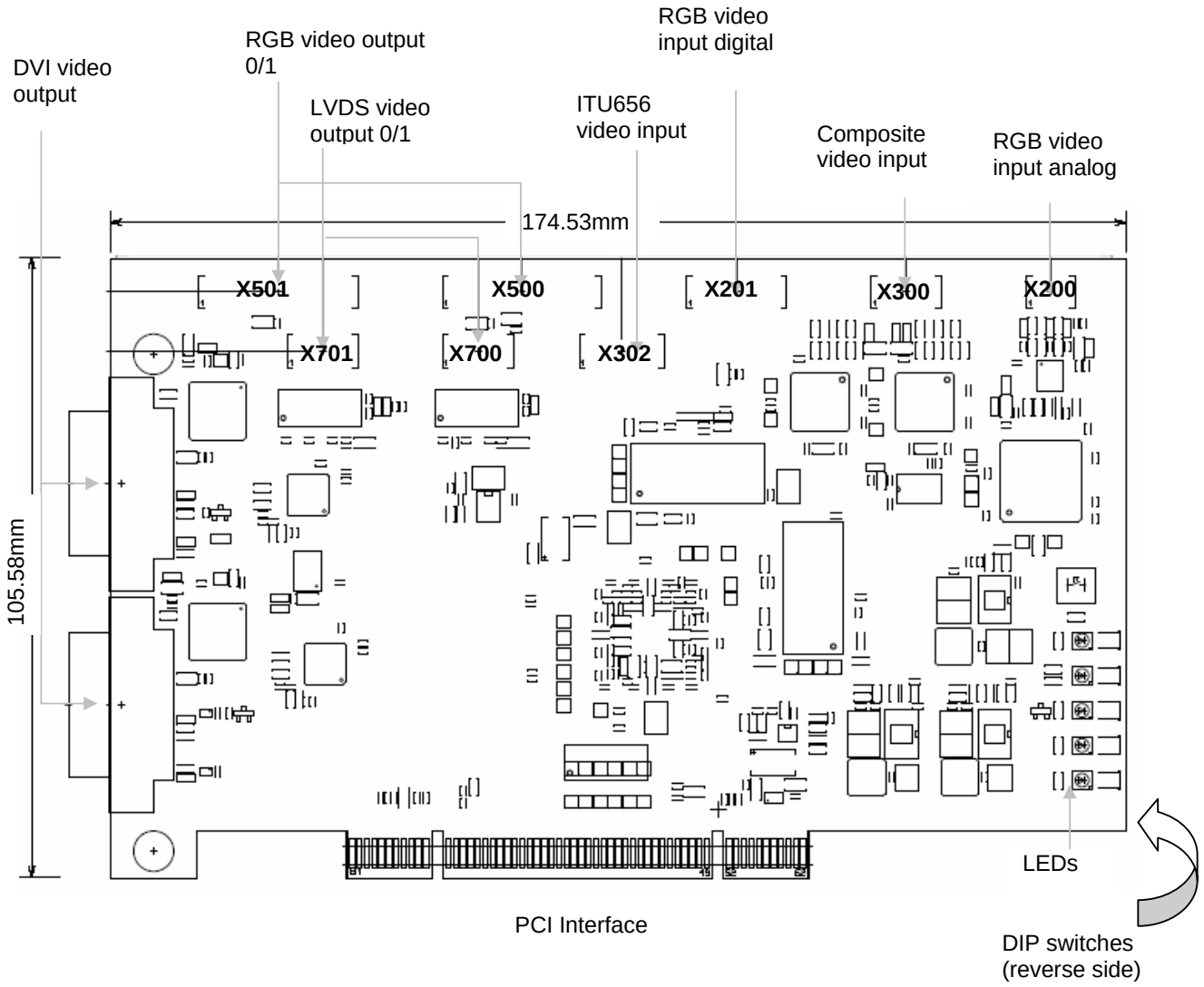


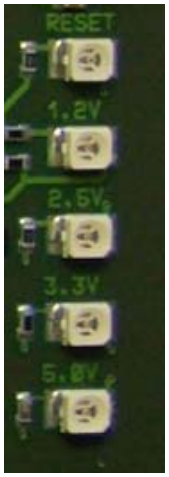
Figure 2 Interfaces of the evaluation board (top side)

5 LEDs

LEDs are connected to the power nets. An illuminated LED indicates the availability of the respective power supply (net). The LEDs are located at the lower right corner on the top side of board (Figure 2)

LED	Function	Description
D100	Reset	(Red) Reset level active
D101	1.2V supply	(Green) Availability of 1.2V power supply
D102	2.5V supply	(Green) Availability of 2.5V power supply
D103	3.3V supply	(Green) Availability of 3.3V power supply
D104	5.0V supply	(Green) Availability of 5.0V power supply

Table 1 LEDs connected to the Power Nets



6 Configuration

This table gives an overview of the DIP switch SW100 on the lower side of the Carmine evaluation board. Be sure to set all switches according to the function you want to use. Before inserting the evaluation board for the first time, make sure all jumpers are correctly set to their default positions (***default jumper positions are marked in bold italic***).

Dip switch	Function	Set	Description
0	JTAG	***ON***	***JTAG TRST# Disable***
		OFF	JTAG TRST# Enable
1	Carmine MODE0	ON	DDR SDRAM without termination
		OFF	***DDR SDRAM with termination***
2	Carmine MODE1	ON	DDR SDRAM without termination
		OFF	***DDR SDRAM with termination***
3	Carmine CLKSEL0	ON	(other clock inputs : see table in manual)
		OFF	***14.32 MHz Clock input***
4	Carmine CLKSEL1	***ON***	***14.32 MHz Clock input***
		OFF	(other clock inputs : see table in manual)
5	Video Mode 0	ON	(see table below)
		OFF	***RGB Input***
6	Video Mode 1	ON	(see table below)
		OFF	***RGB Input***
7	Video Out#0 RGB select	***ON***	***Switch RGB#0 Output Mode ON***
		OFF	OFF

Table 2 DIP Switch Settings

Video In Mode 1	Video In Mode 0	Function
OFF (0)	OFF (0)	RGB input
OFF (0)	ON (1)	YUV input 1
ON (1)	OFF (0)	YUV input 2
ON (1)	ON (1)	No input

Table 3 Video Input Mode

7 Interfaces and Connectors

7.1 Connectors for video output

The board provides several interfaces for video inputs and outputs. Because of size limits it was not possible to place all input and output connectors for all video interfaces on one board slot. The main board itself has 2 DVI connectors for DVI and analog RGB video outputs. Use the provided DVI > VGA adaptor to connect an older VGA monitor.

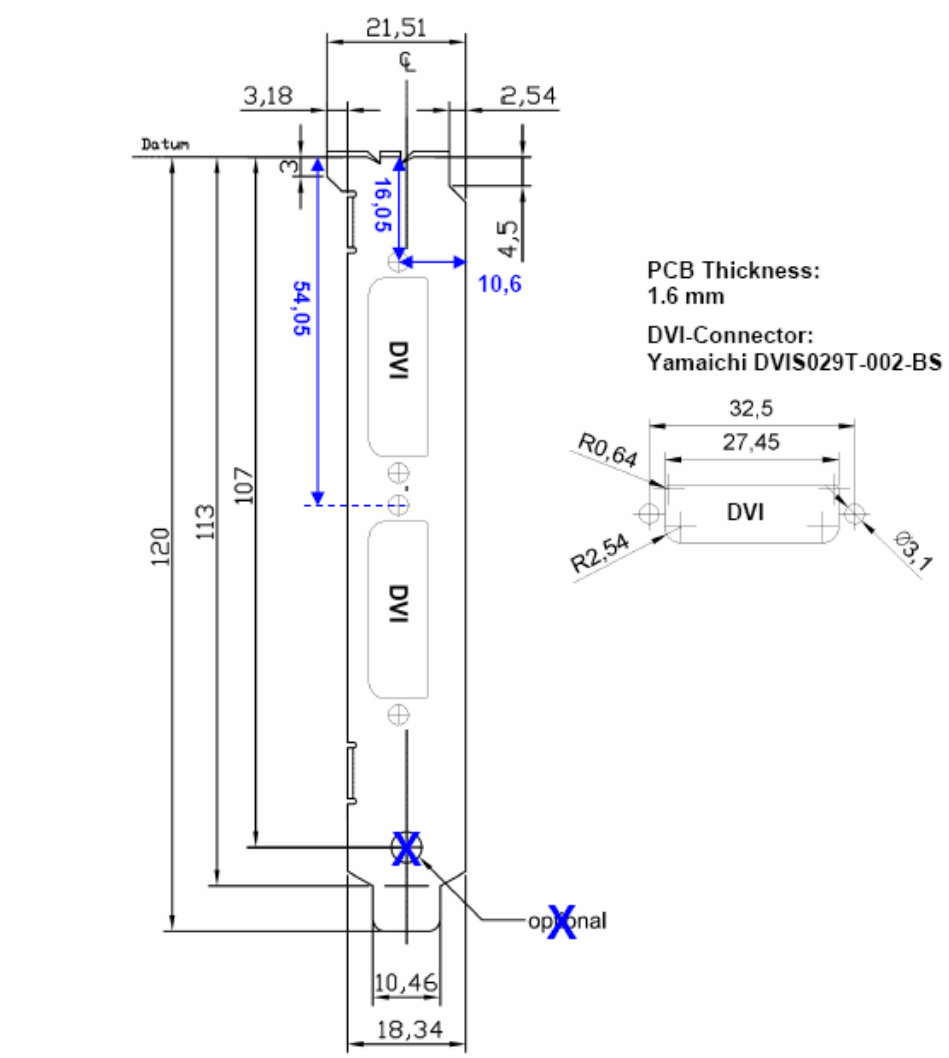


Figure 3 Video Output Connectors

7.2 The AV Video Input Board

Connectors for the video input (composite video, analog RGB) are located on an additional board ("AV-Input board") which can be connected to the main evaluation board via the flat cables that are provided.

Make sure to connect the analog video inputs from the AV-Input board from connector X100 to the X300 port on the main board. The RGB analog input port must be connected from the X101 to the X200 port on the main board.
Take special care about the correct polarity (red marking) when connecting the flat cables !

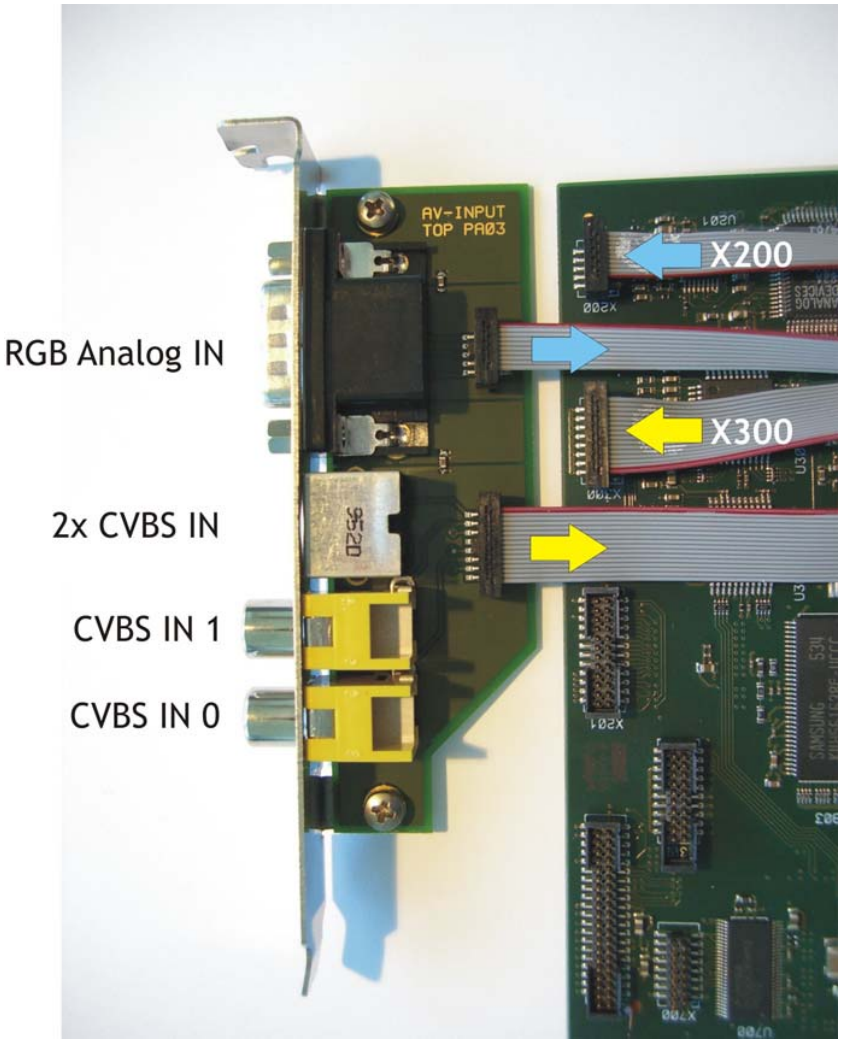


Figure 4 Video Input Connectors

7.3 Interfaces for Digital RGB and LVDS Output

The signals of digital RGB outputs and LVDS outputs are available on pin headers X500, X501, X700 and X701. Note that cables for the external connection of these interfaces are not provided with the evaluation board.

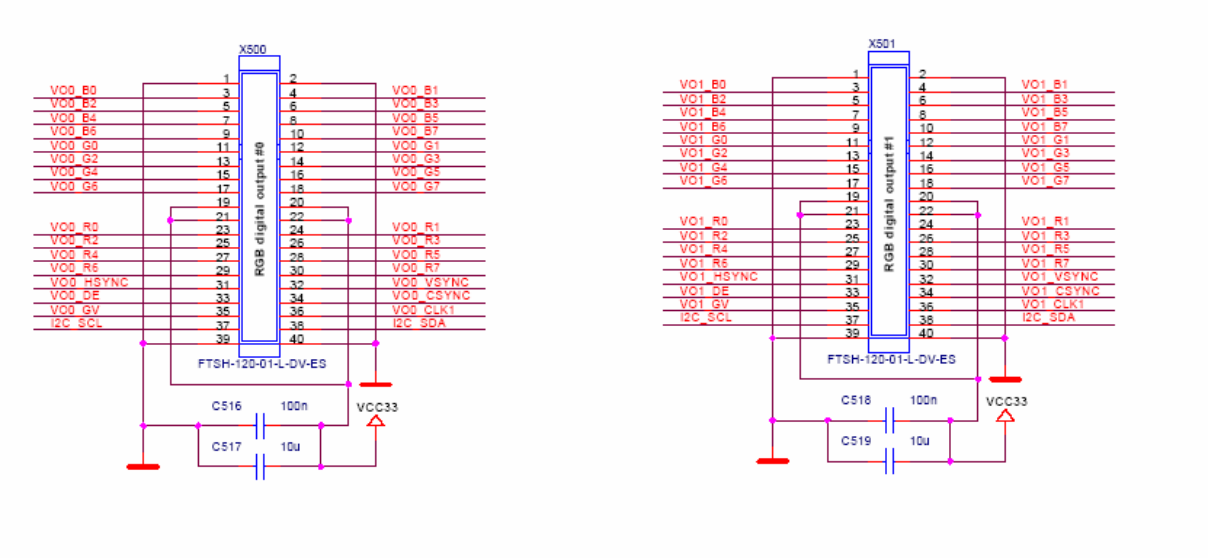


Figure 5 Digital RGB Output

7.4 LVDS Interface

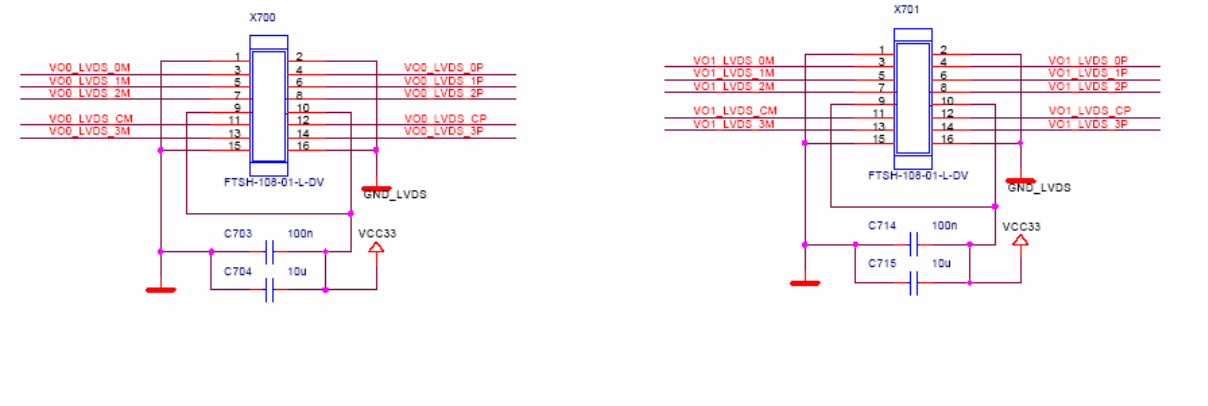


Figure 6 LVDS Interface

8 CPLD Functions

The Carmine Evaluation board incorporates a Xilinx CPLD CoolRunner ll (XC2C128-7TQ144, U400) which is normally pre-programmed. If necessary, the device can be re-programmed using the JTAG interface (X400) on the reverse side of the board. Use the Xilinx programming tools (ISE) for reprogramming (www.xilinx.com).

The CPLD provides the following functions:

The on-board DIP switches (SW100) and the I2C interface of the Carmine graphics processor are used to select the video input source for the ITU RBT-656 (RGB666) video capture interfaces of the Carmine device. After a reset, the input source will be selected according to switch 7 and switch 6 of SW100.

If bit 2 of the CONFIG register in the CPLD is set to logical '1', the input source will be selected from bit 1 and bit 0 of the CONFIG register. The CONFIG register is programmed via the I2C interface of the Carmine graphic processor.

Switch 7 is equivalent to bit 1 of the CONFIG register and switch 6 is equivalent to bit 0. The following table shows the selectable combinations:

Bit 1 (DIP7)	Bit 0 (DIP6)	Input Source
0	0	RGB input
0	1	YUV input 1
1	0	YUV input 2
1	1	No input

Bit 3 of the CONFIG register sets the output enable signal of the switch FSAV430 (U201). If bit 3 is set to logical '0' (default after reset) the selected connection with switch 8 of SW100 is connected else the connection is open.

Bit 5 and bit 4 of the CONFIG register set the switch FSAV433 (U502) and NC7SB3257 (U602). Bit 5 is equivalent to VO_CTRL1. Bit 4 is equivalent to VO_CTRL0. The CONFIG register of the CPLD can be programmed via the I2C interface of the Carmine graphic processor.

The following table shows the registers and the addresses of the I2C functions in the CPLD:

I2C	Address Function
0x60	Write config register
0x61	Read config register
0x62	No function
0x63	Read version code
0x64	No function
0x65	Read status register
0x66	No function
0x67	Read status register

The following table shows the configuration of the CONFIG register:

Bit	Function
7	Not used
6	Not used
5	VO_CTRL1, set video out
4	VO_CTRL0, set video out
3	CONFIG7
2	0: SW100 1: CONFIG(6..5), set video in
1	CONFIG6, set video in
0	CONFIG5, set video in

The following table shows the configuration of the VERSION register:

Version	Details
0xa1	First version

The following table shows the configuration of the STATUS register:

Bit	Function
7	1
6	1
5	1
4	1
3	1
2	1
1	1
0	0: RGB input cable not connected, 1: RGB input cable connected

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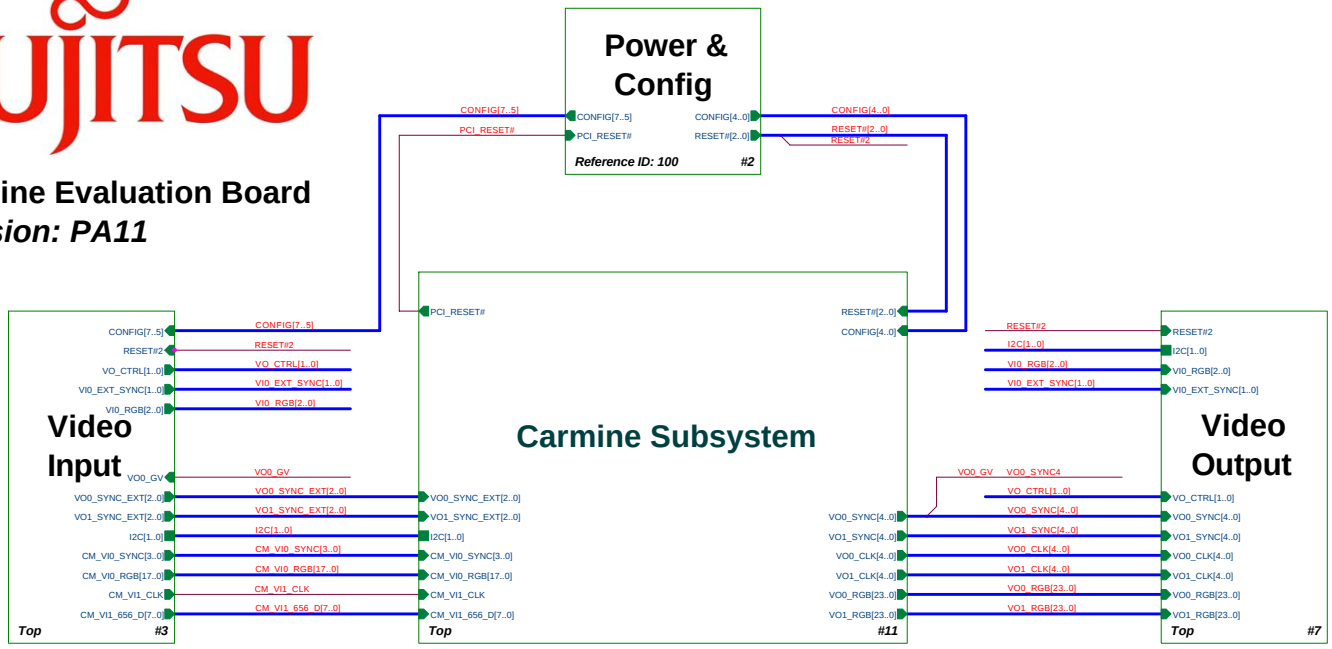

Carmine Evaluation Board

Hierarchy	Part References
+---#1 Carmine Eval Top	
|	
+---#2 Power	1xx
+---#3 Video Input	
+---#4 RGB Input	2xx
+---#5 YUV Input	3xx
+---#6 Vin Selector	4xx
+---#7 Video Output	
+---#8 RGB Output	5xx
+---#9 DVI Output	6xx
+---#10 LVDS Output	7xx
+---#11 Carmine Subsystem	
+---#12 Carmine	8xx
+---#13 Carmine Power	8xx
+---#14 PCI	8xx
+---#15 DRAM	9xx

I2C Address Map

Device	Function	Write	Read
U200 AD9883	RGB input ADC	0x98	0x99
U300 SAA7113	composite video in #0	0x48	0x49
U301 SAA7113	composite video in #1	0x4a	0x4b
U400 XC2C128*	video input selector	0x60	0x61
U600 SIL164	DVI transmitter #0	0x70	0x71
U601 SIL164	DVI transmitter #1	0x72	0x73

* I2C address of video input selector depends on CPLD implementation

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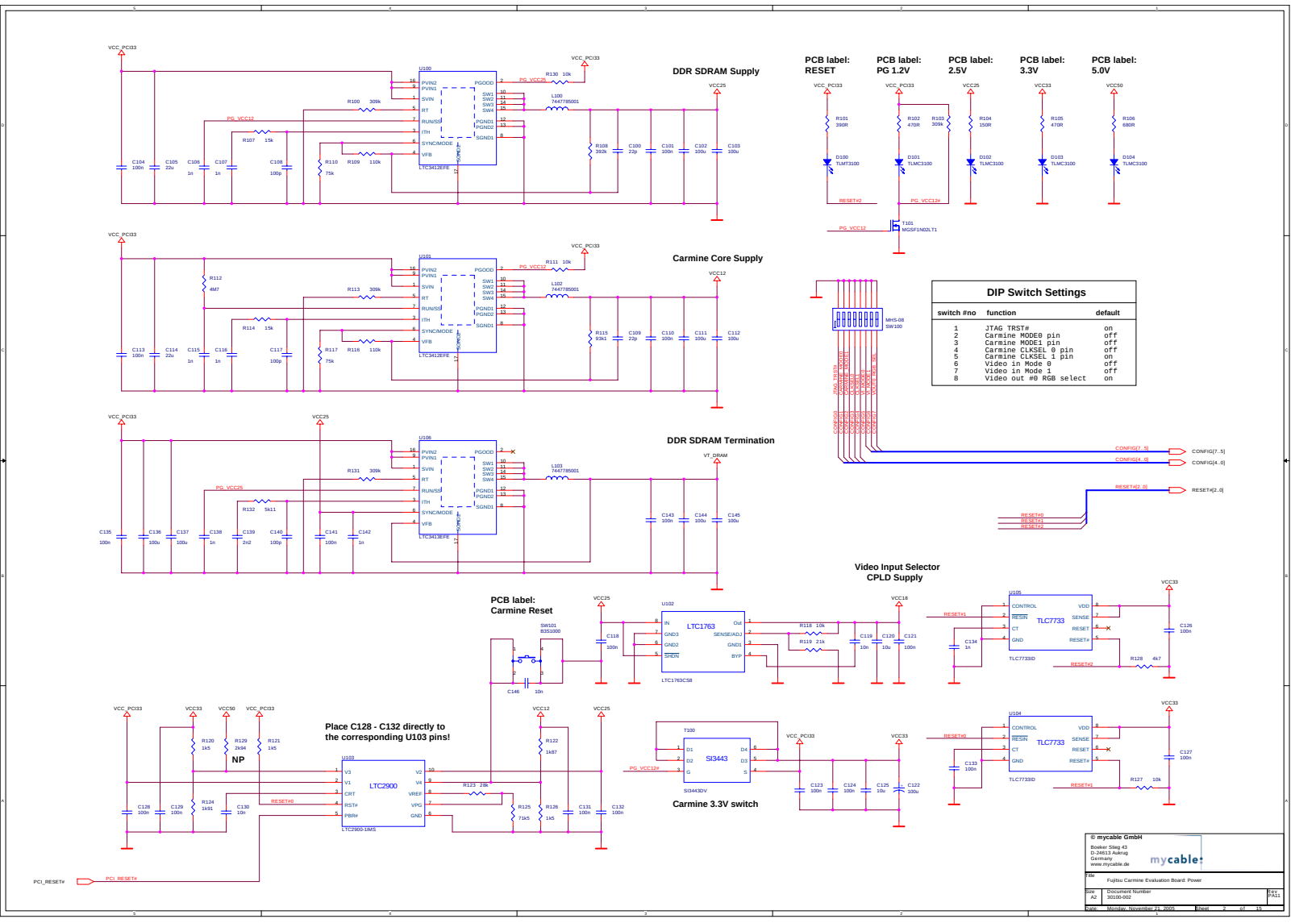

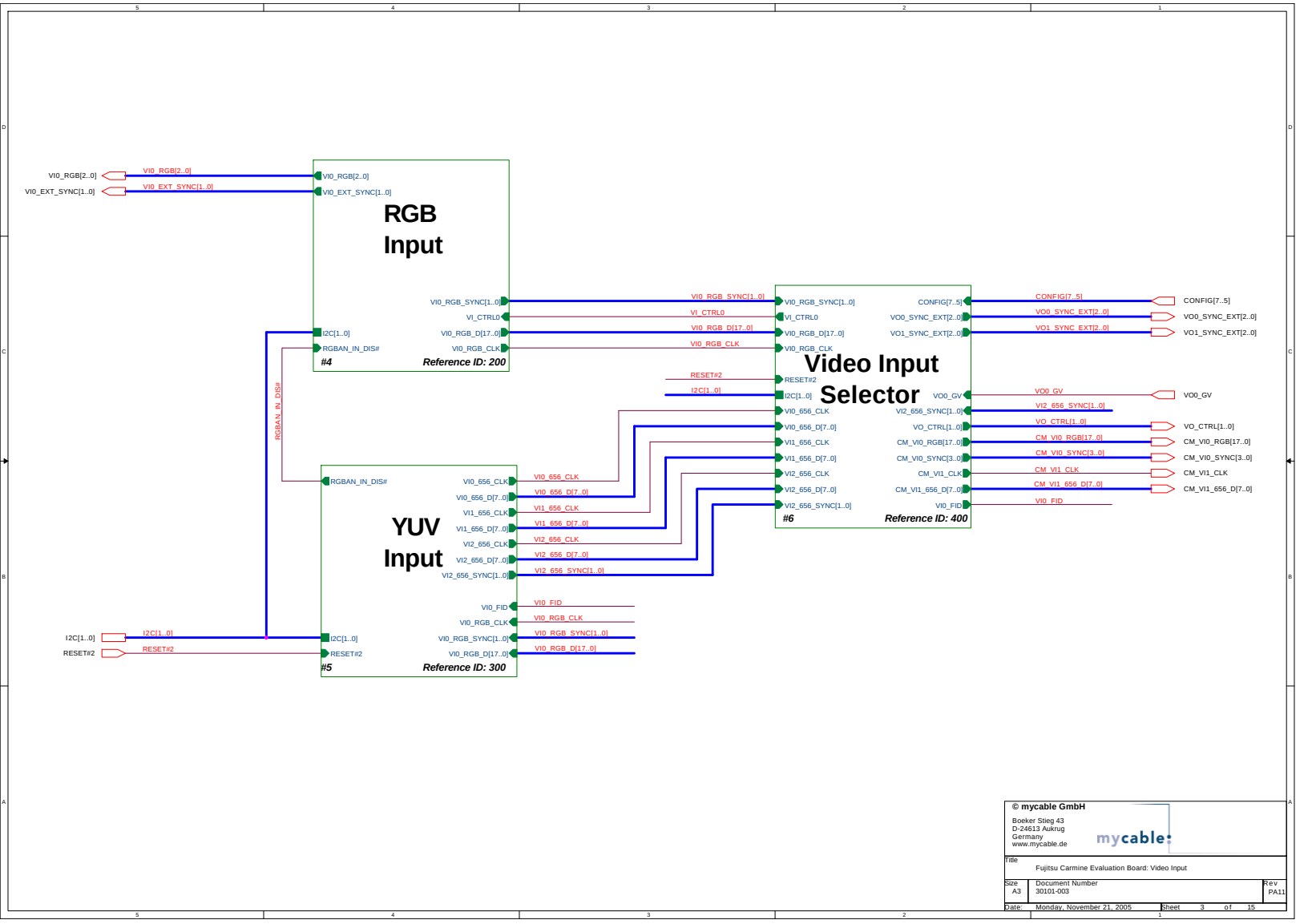

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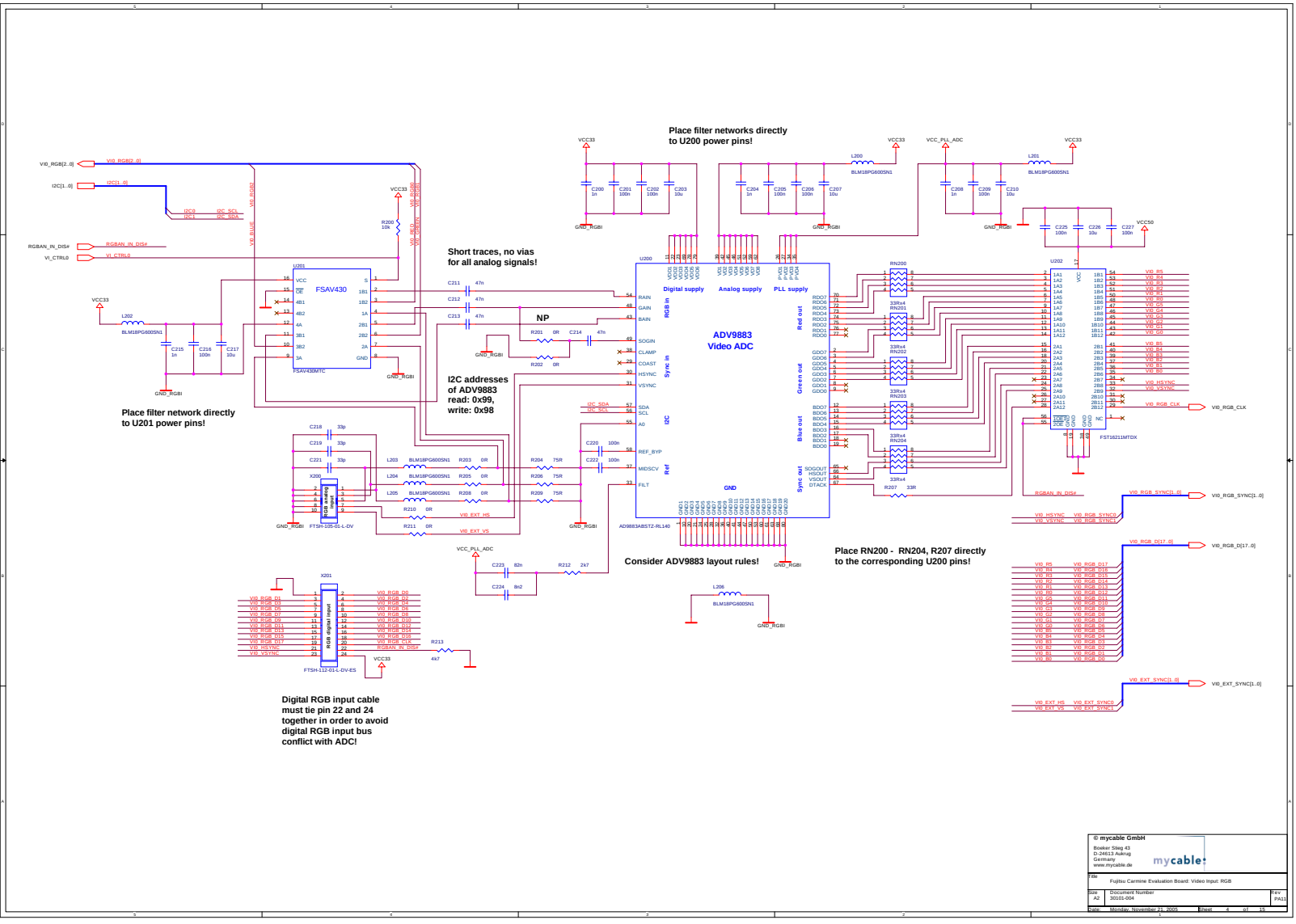

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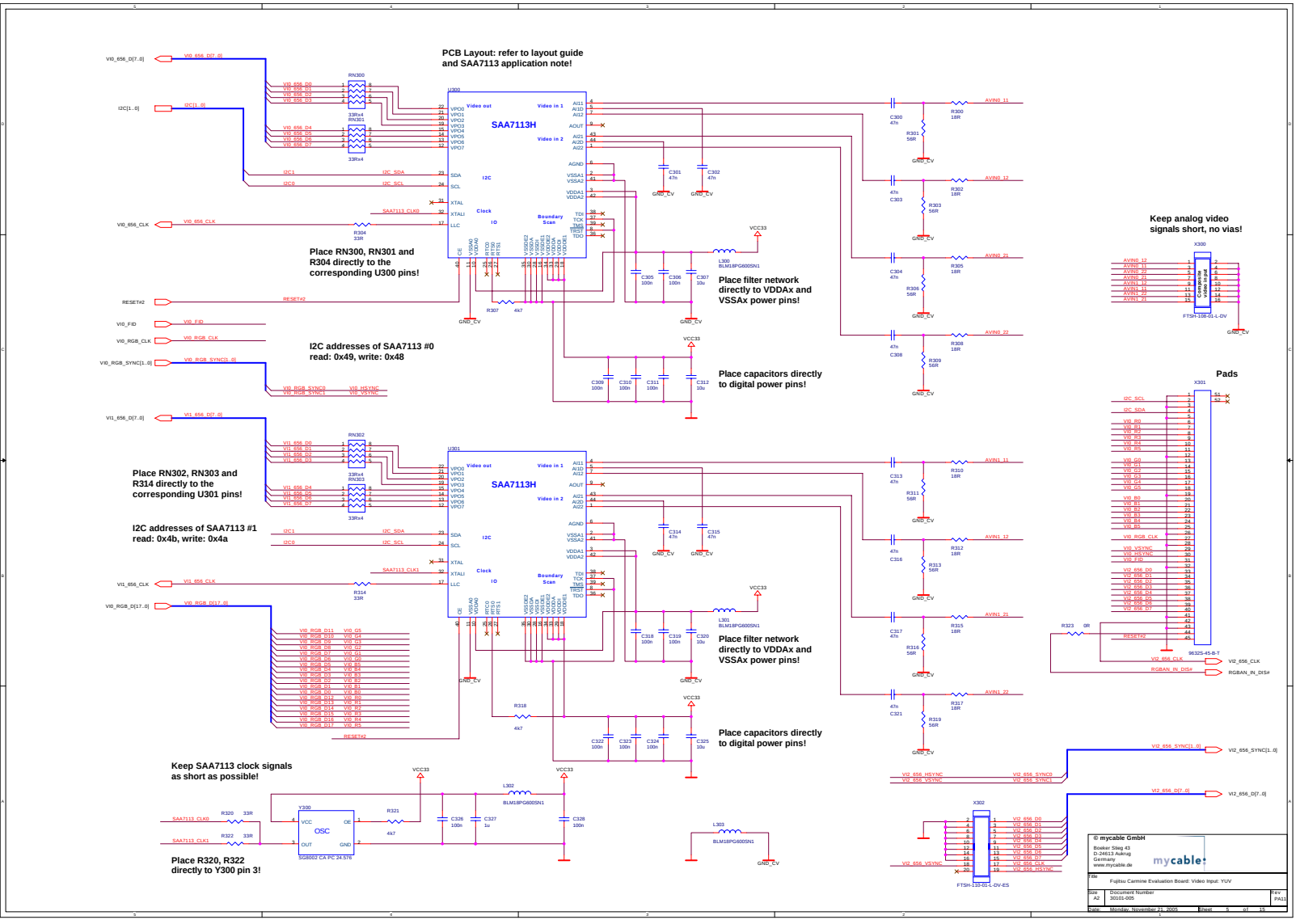

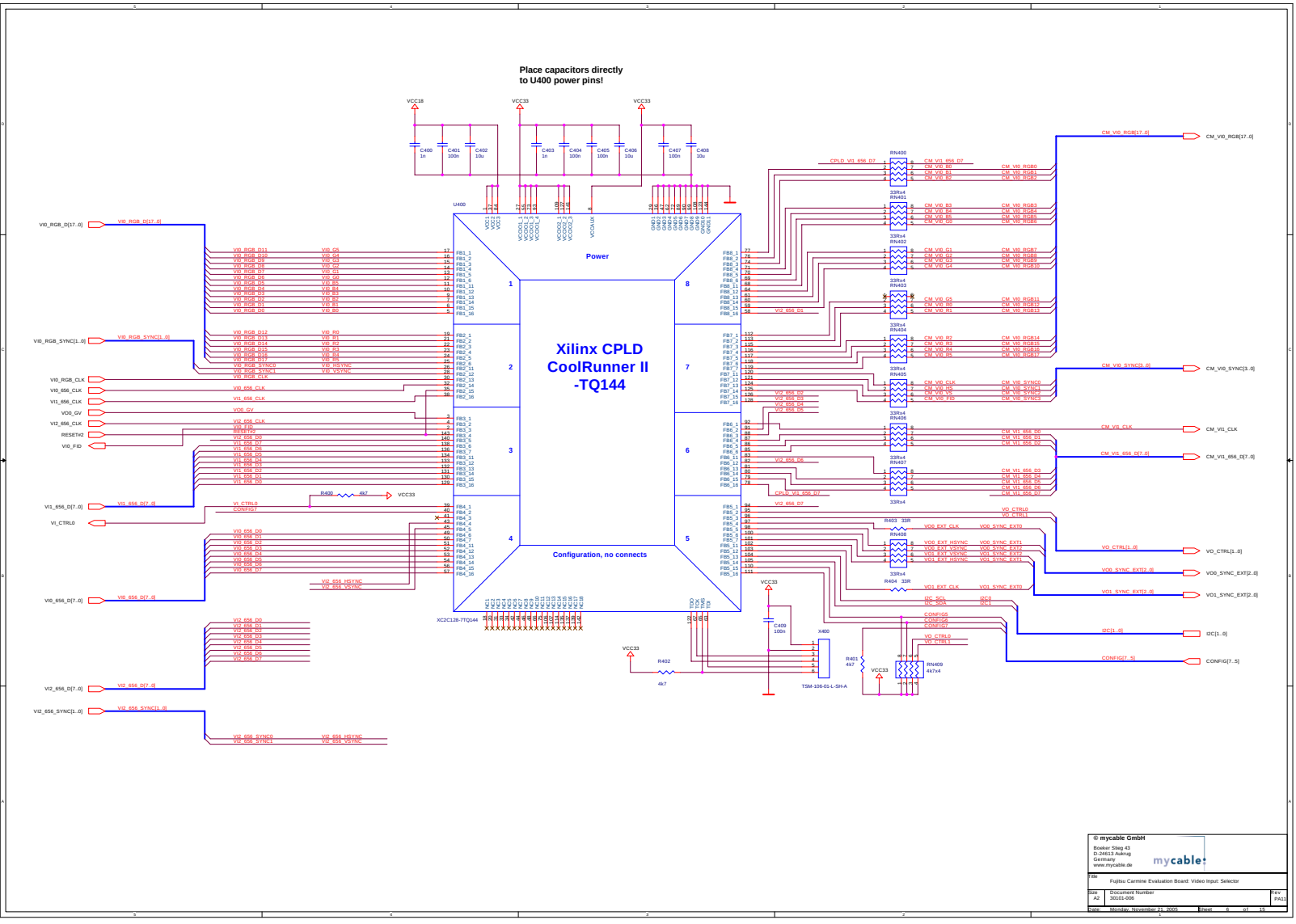

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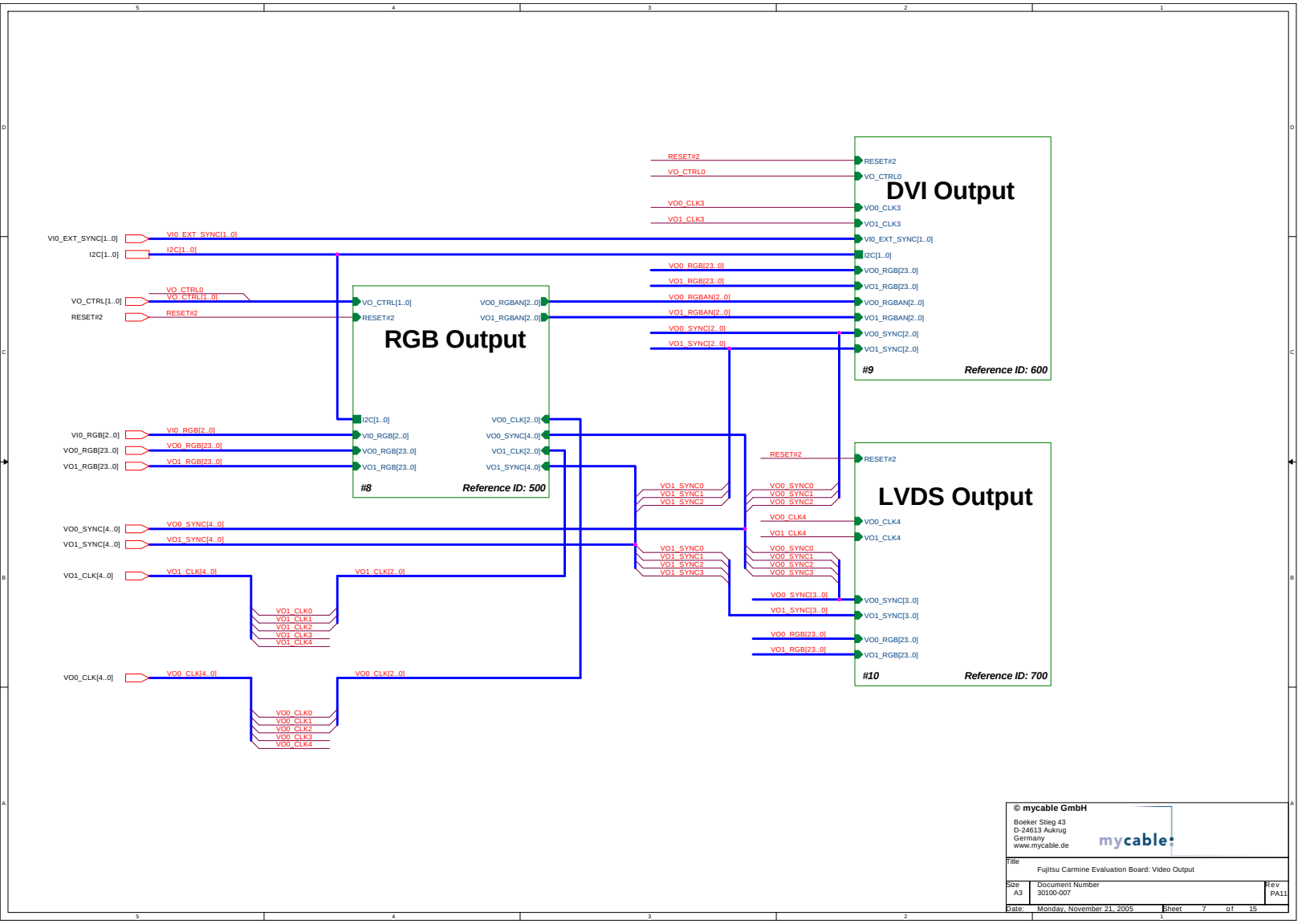

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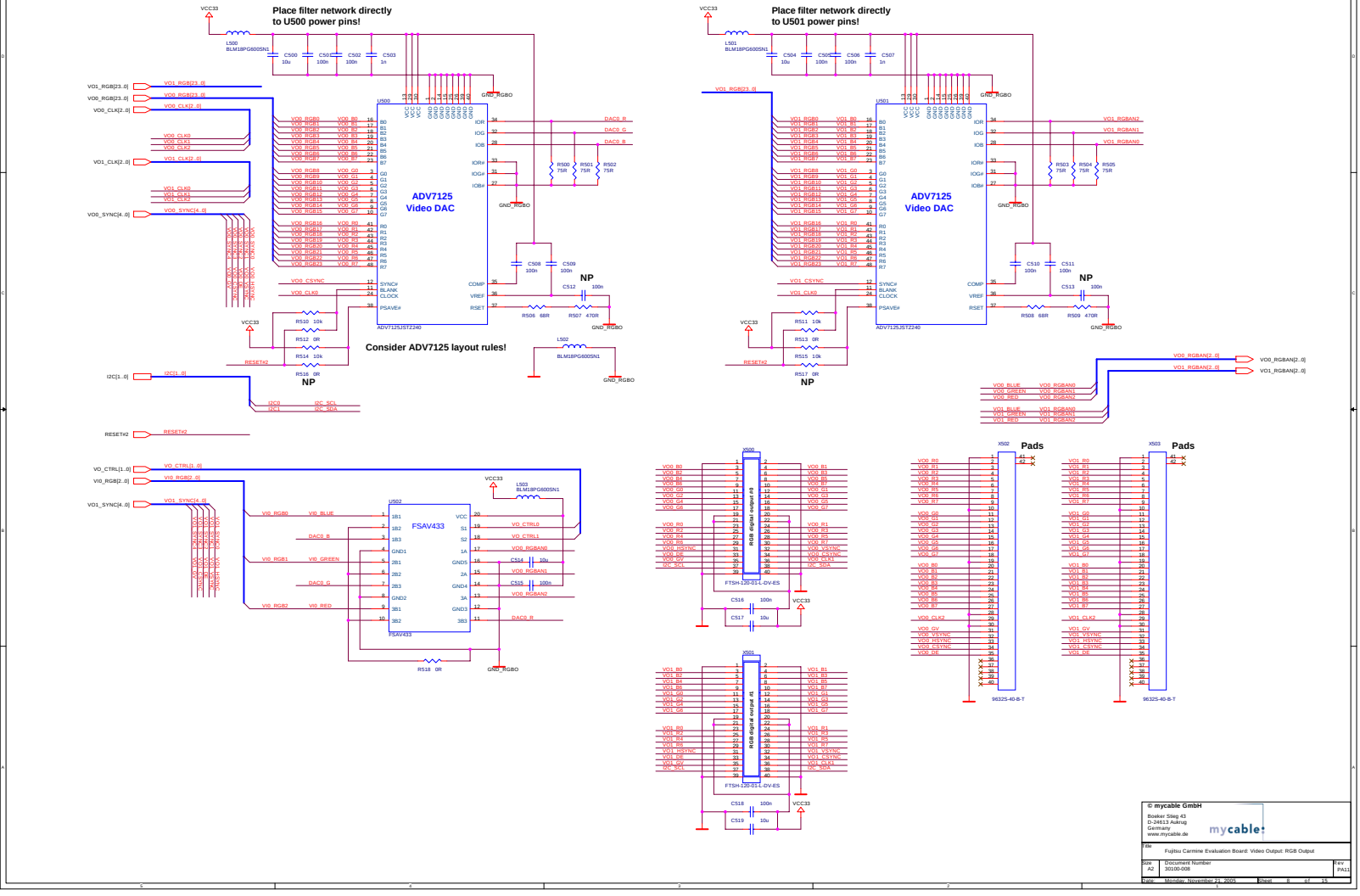

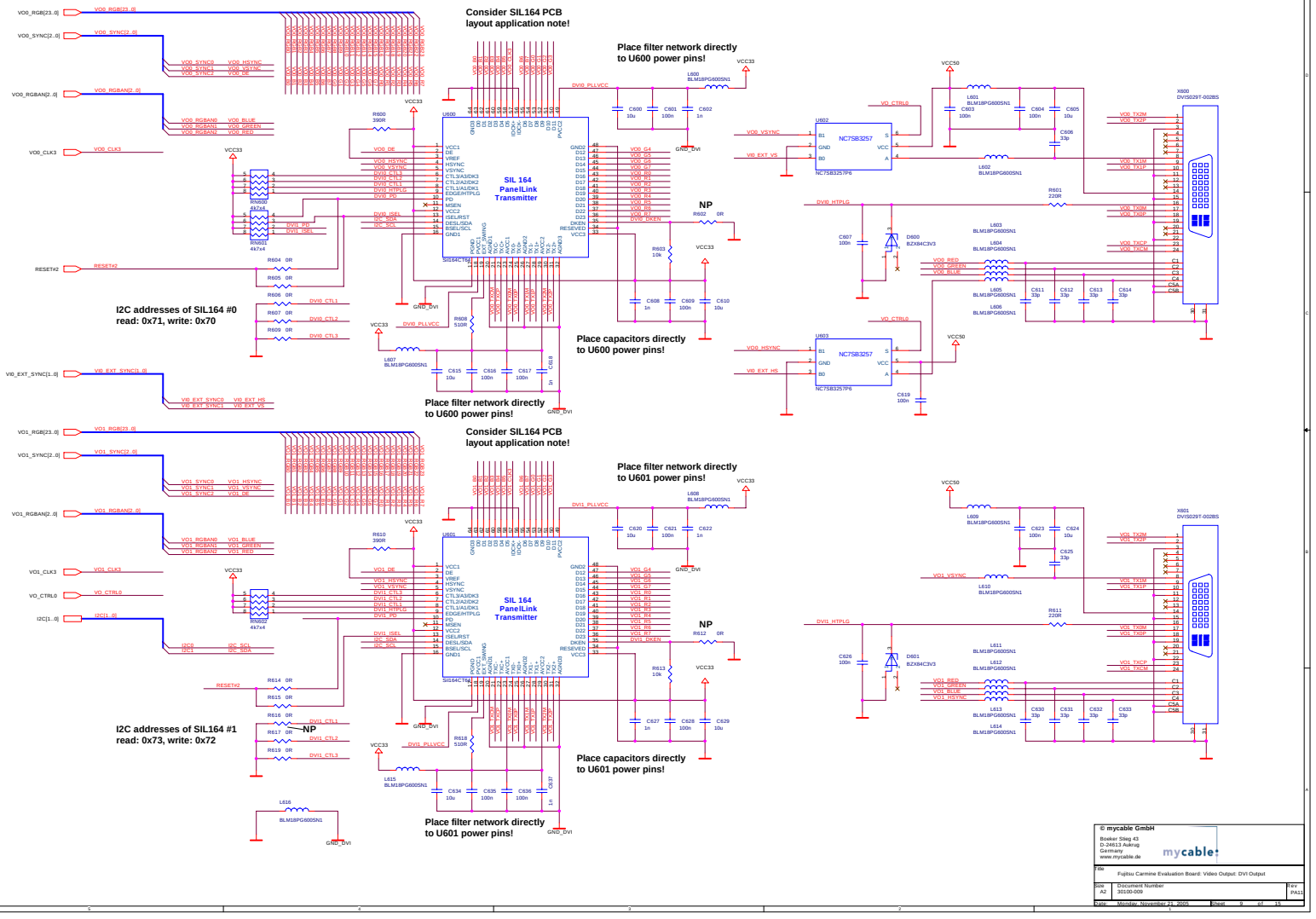

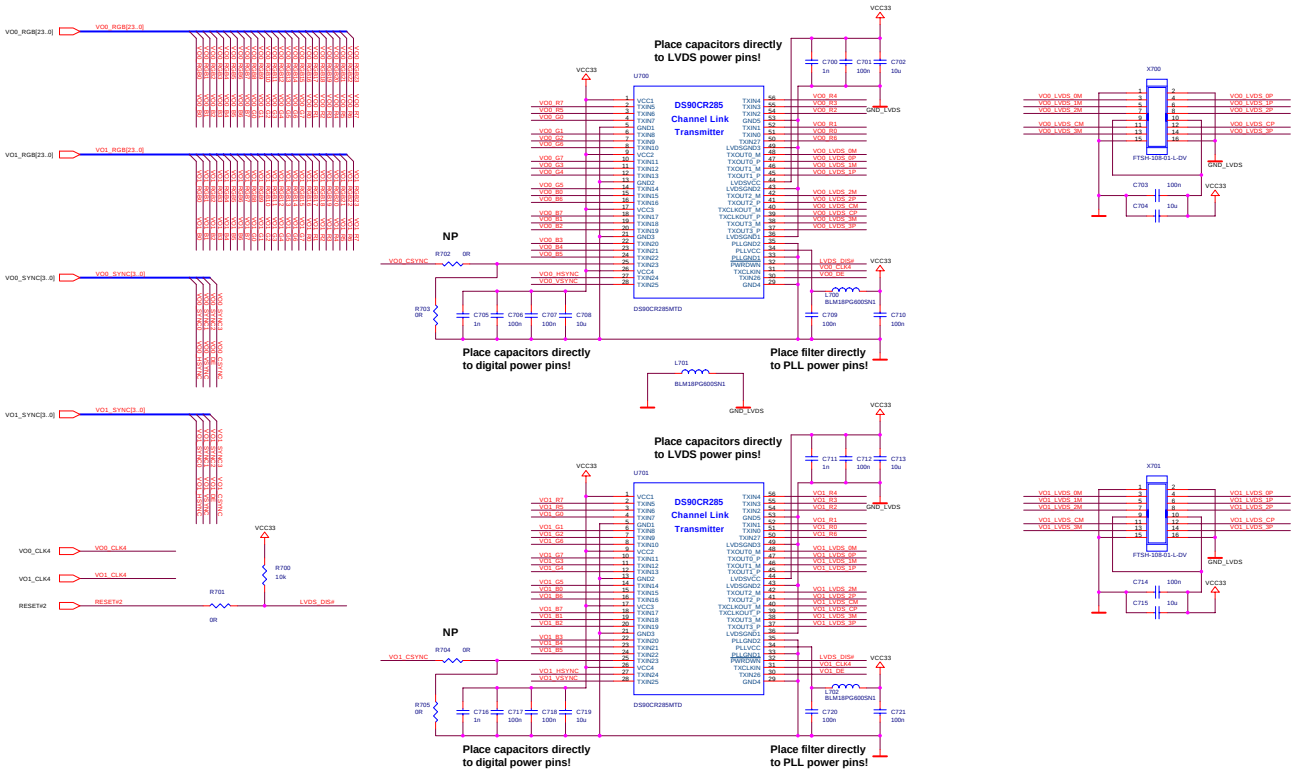

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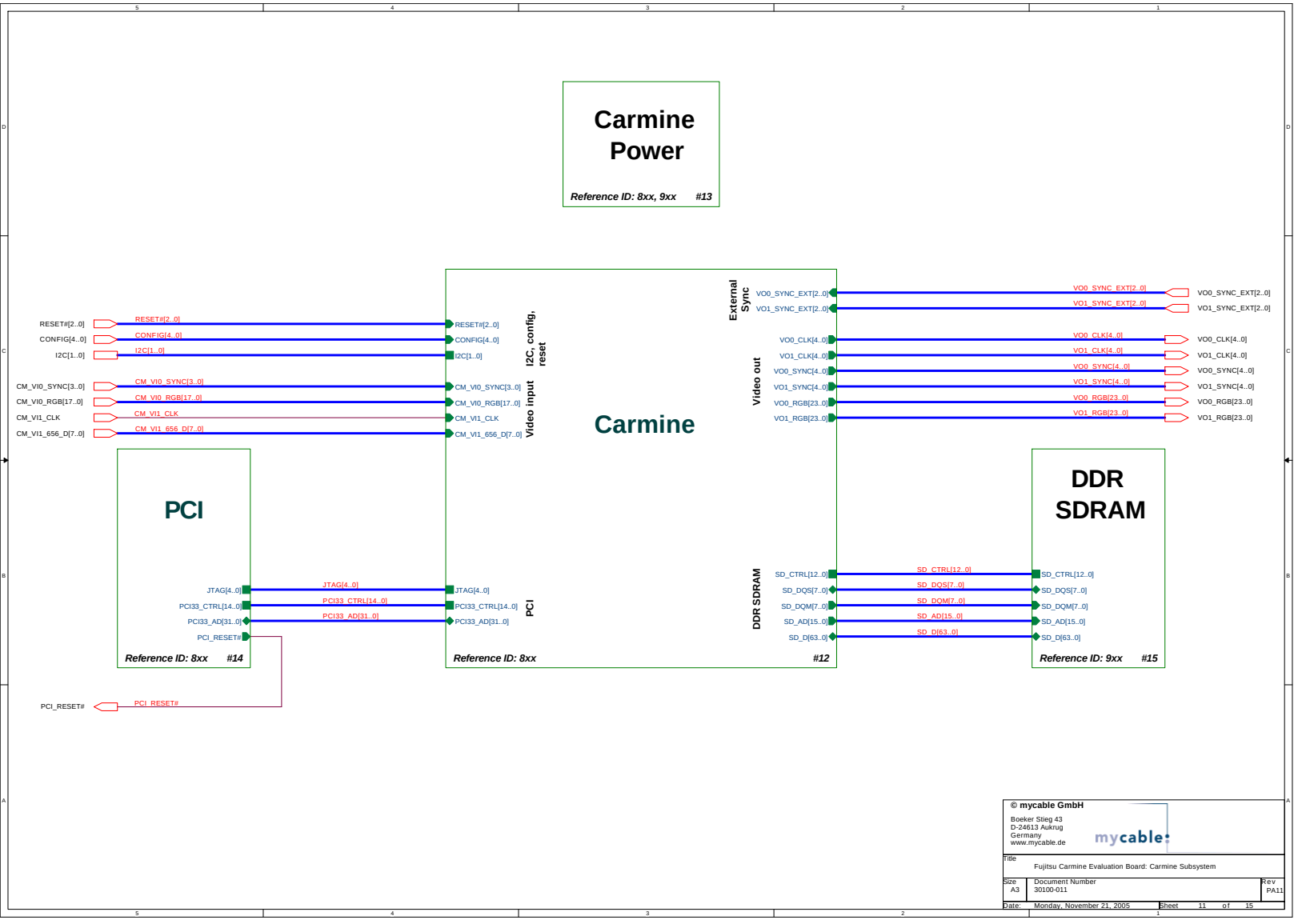

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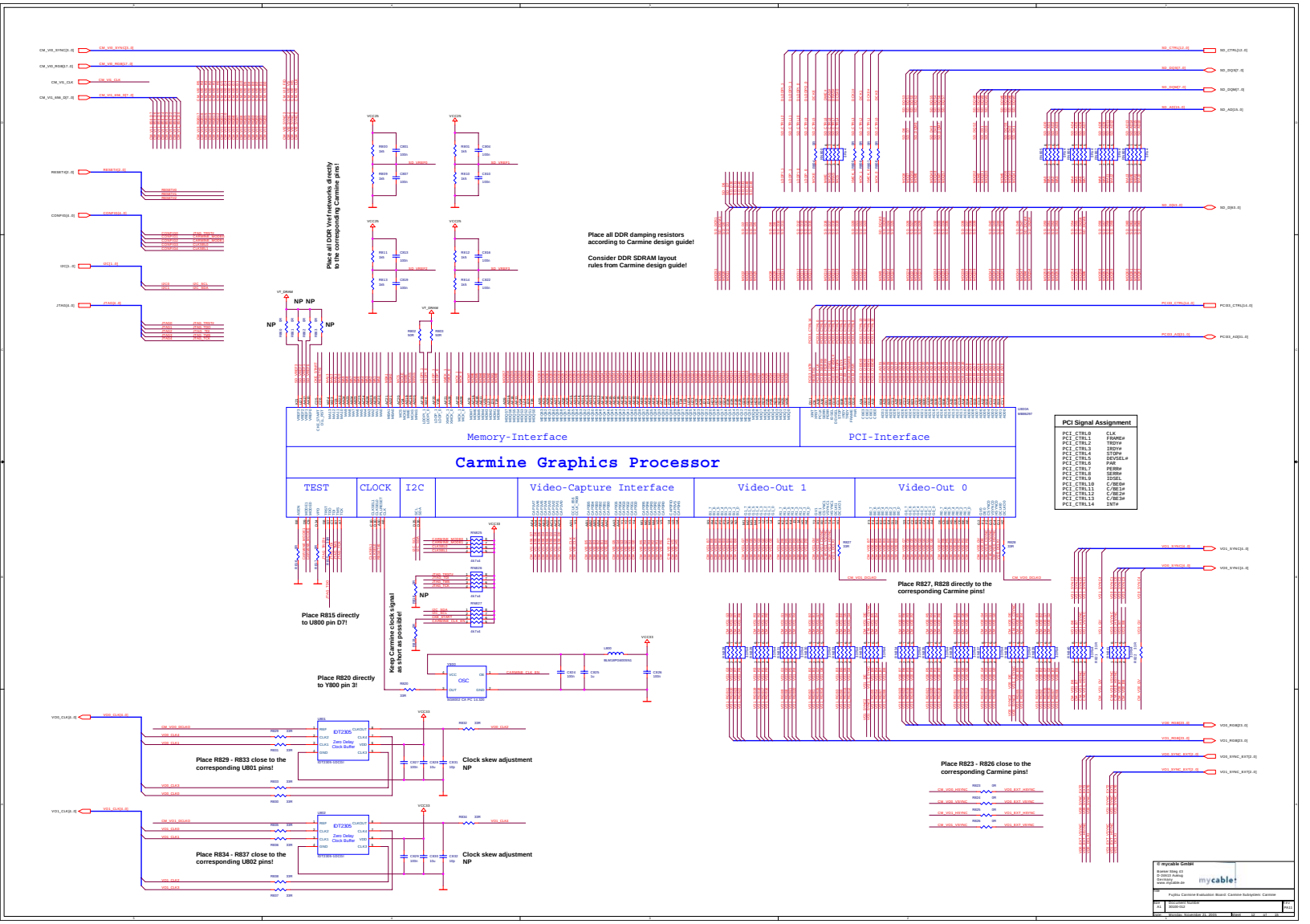

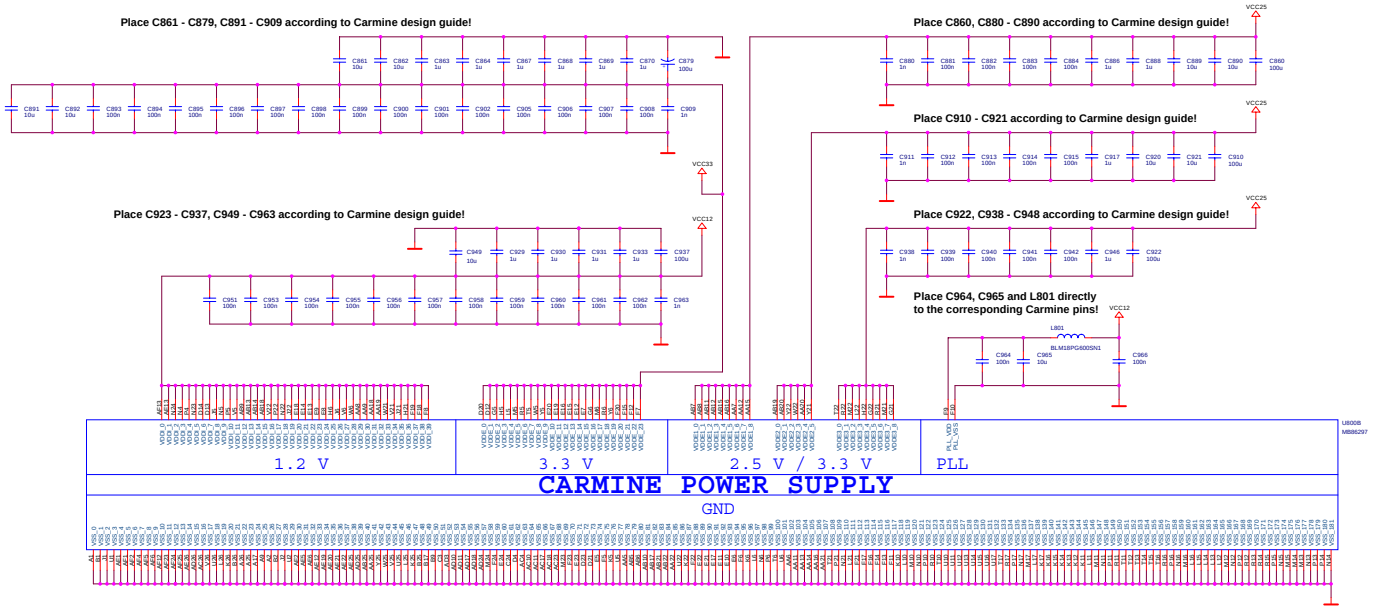

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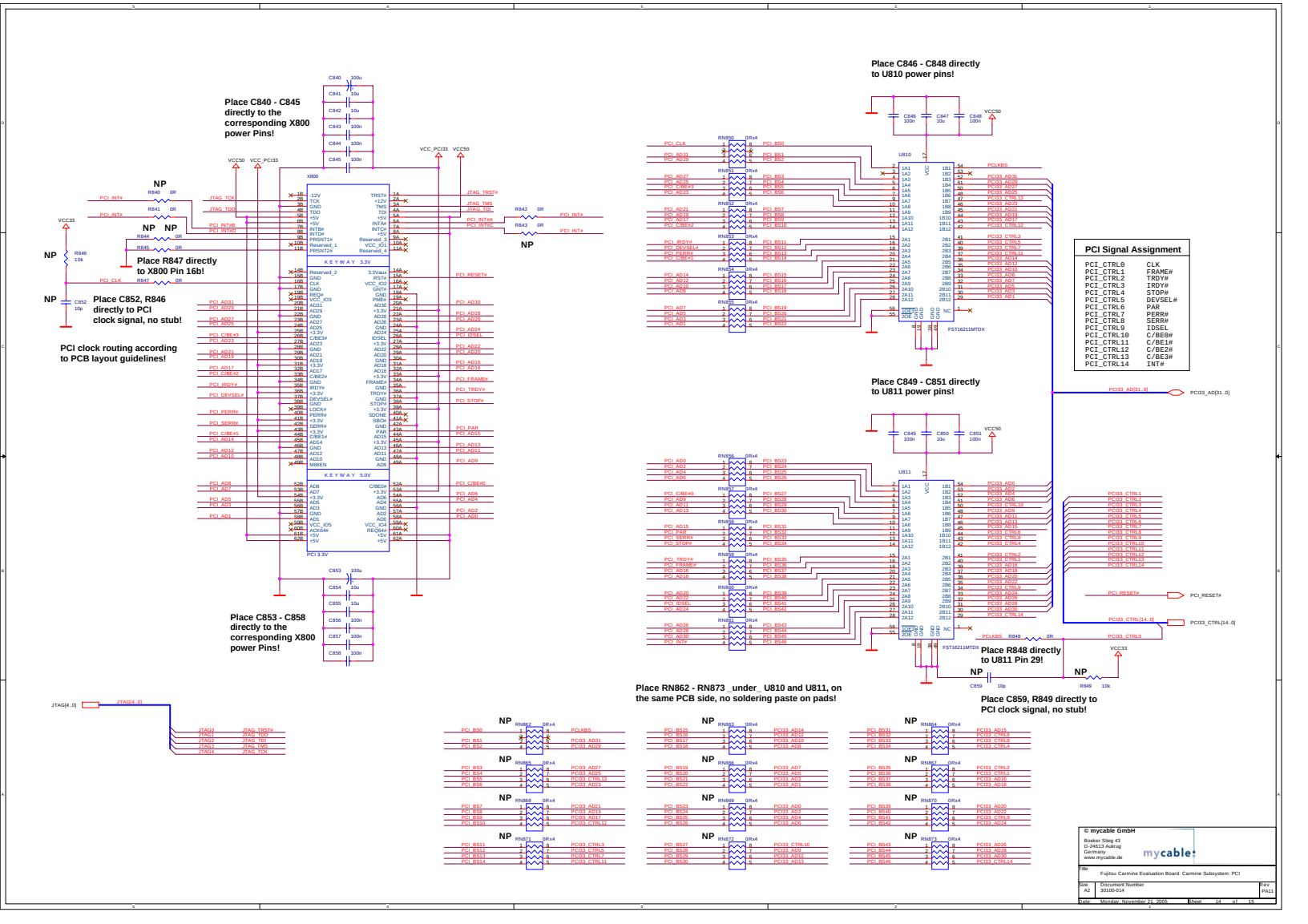
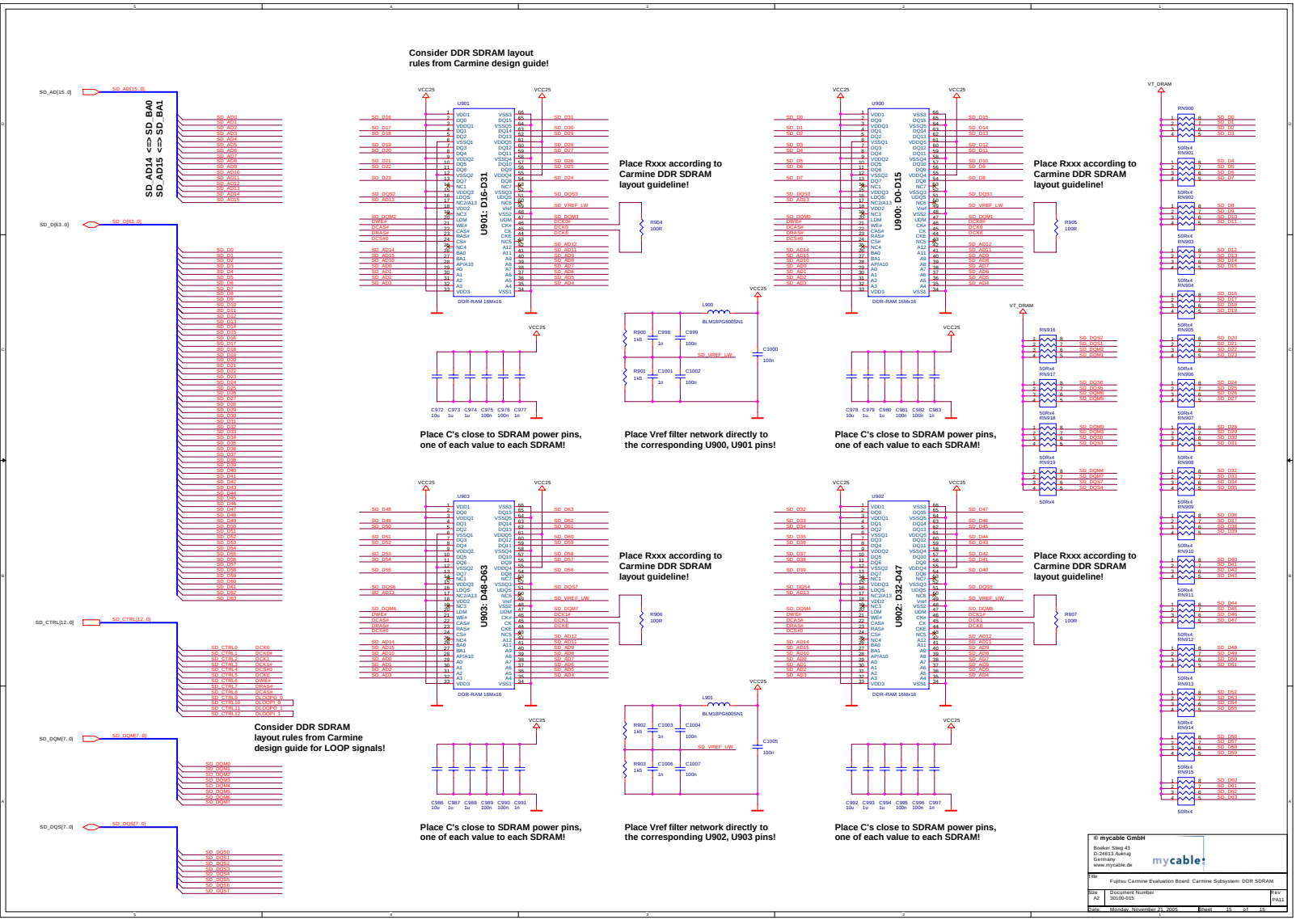
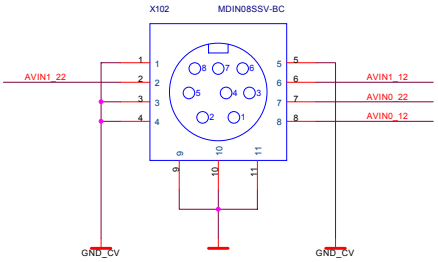
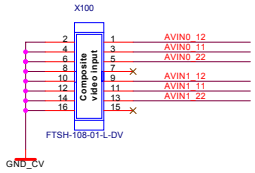


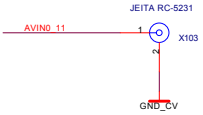


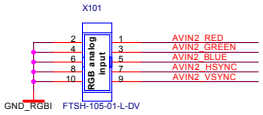
Carmine Evaluation Board
Analog Video Input Slot

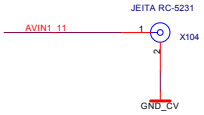
Revision: PA2

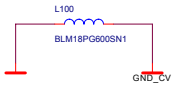


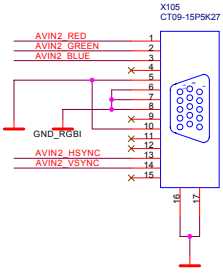


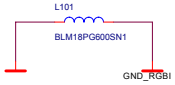












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Title	Fujitsu Carmine Evaluation Board: Analog Video Input Slot	
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