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Stratix III FPGA Development Kit

from *Altera Corporation*

The Stratix® III FPGA Development Kit delivers a complete environment for the development and testing of designs requiring high-performance and high-density devices.

Altera® Stratix III FPGAs combine the world's highest performance and highest density with the lowest possible power consumption. You'll find Stratix III FPGAs provide the high-performance and high-integration capabilities needed for next-generation basestations, network infrastructure, and advanced imaging equipment.

- Ordering Information
- HSMC Interface
- Available Documentation
- Development Kit Contents

Stratix III FPGA Development Kit Ordering Information

Table 1. Stratix III FPGA Development Kit Ordering Code and Pricing Information

Ordering Code	Price	Ordering Information
DK-DEV-3SL150N	$2,495	Contact your local Altera distributor to place your order.

HSMC Interface

Altera developed the specification for the high-speed mezzanine connector (HSMC) interface, which is based on the Samtec mechanical connector, to define and standardize the interface between optional daughtercards and host boards. This specification outlines both the electrical and mechanical properties of the interface between daughtercard and host. You can also create your own HSMC interface compatible daughtercards.

- Request a copy of the HSMC specification

Available Documentation

The installer package for this board containing all of the documentation and software examples is available at ftp://ftp.altera.com/outgoing/devkit/StratixIII_Dev_Kit-v7.2.0.exe.

Stratix III FPGA Development Kit Contents

The Stratix III FPGA Development Kit is RoHS compliant and includes:

- Stratix III development board
  - Stratix III EP3SL150F1152 high-performance FPGA
    - 142,500 equivalent logic elements (LEs)
    - 744 user I/O pins
    - 384 18 x 18 multipliers
  - Clocking
    - 125.000-MHz oscillator
    - 50.000-MHz oscillator
    - SMA input
    - SMA output
  - Configuration
    - MAX® II flash passive serial configuration circuit
      - MAX II EPM2210GF256C3N CPLD
        - 2,210 LEs
        - 272 user I/O pins
        - 8 Kbytes of user flash memory
    - On-board USB-Blaster™ using Quartus® II development software programming
    - JTAG download port
  - General user input/output
    - Power consumption display
      - Displays each power rail individually
    - System reset pushbutton
    - Board-specific DIP switch
    - JTAG bypass DIP switch
    - User reset pushbutton
    - User pushbuttons (x4)
    - User DIP switch (x8)
    - User LEDs (x8)
    - User quad 7-segment display
    - 128 x 64 dot pixels graphics display
    - LCD (16 character x 2 line)
  - Memory devices
    - 128-Mbyte DDR2 SDRAM DIMM
    - 16-Mbyte DDR2 SDRAM devices (individually addressable)
    - 36-Mbit QDRII SRAM device
    - 4-Mbyte PSRAM
    - 64-Mbyte flash memory
  - Components and interfaces
    - USB 2.0
    - 10/100/1000 Ethernet
    - Two HSMC interfaces
- Quartus II Development Kit Edition software, including a one-year license
- Cable and accessories
  - External AC adapter power supply
  - Power cord (including support for UK, Europe)

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