

## 32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

### Features

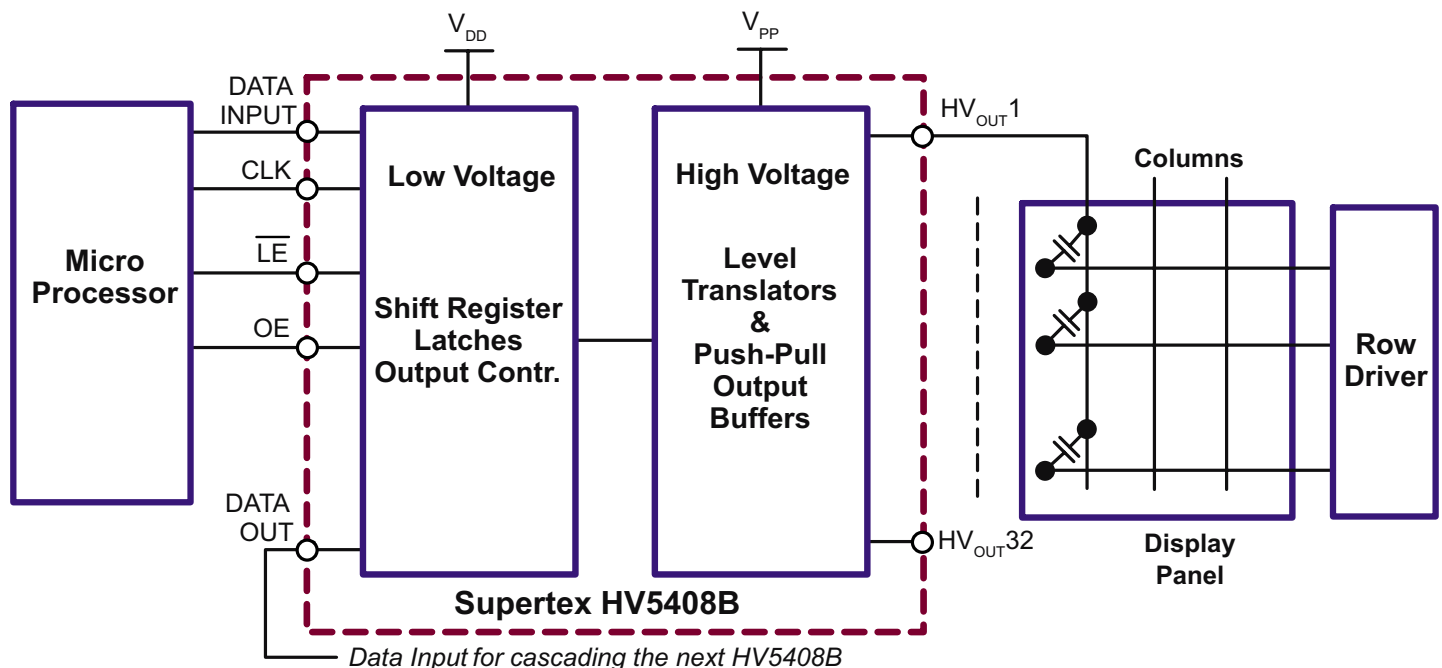
- ▶ Processed with HVCMOS® technology
- ▶ Low power level shifting
- ▶ SOURCE/SINK current minimum 20mA
- ▶ Shift register speed 8.0MHz
- ▶ Latched data outputs
- ▶ CMOS compatible inputs
- ▶ Forward and reverse shifting options
- ▶ Diode to VPP allows efficient power recovery

### General Description

The HV5408B is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities, such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

The HV5408B consists of a 32-bit shift register, 32 latches, and control logic to enable outputs. Q1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. When viewed from the top of the package, the HV5408B shifts in the counter-clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the  $\overline{LE}$  (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the  $\overline{LE}$  input is high. The data in the latch is retained when  $\overline{LE}$  is low.

### Typical Application Circuit



## Ordering Information

Device	Package Options		
	44-Lead Quad Cerpac .650x.650in body .190in height (max) .050in pitch	44-Lead PQFP 10.00x10.00mm body 2.35mm height (max) 0.80mm pitch	44-Lead PLCC .653x.653in body .180in height (max) .050in pitch
HV5408B	HV5408DJ-B*	HV5408PG-B-G	HV5408PJ-B-G



-G indicates package is RoHS compliant ("Green").

\* Hi-Rel process flow available.

## Absolute Maximum Ratings

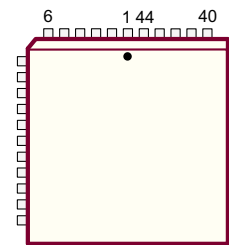
Parameter	Value
Supply voltage, $V_{DD}$	-0.5V to +16V
Supply voltage, $V_{PP}$	-0.5V to +90V
Logic input levels	-0.5V to $V_{DD} + 0.5V$
Ground current <sup>1</sup>	1.5A
Continuous total power dissipation <sup>2</sup>	
Plastic	1200mW
Ceramic	1500mW
Operating temperature range	
Plastic	-40°C to +85°C
Ceramic	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature <sup>3</sup>	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

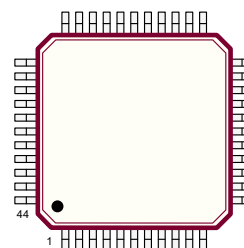
### Notes:

- Duty cycle is limited by the total power dissipated in the package.
- For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.
- 1.6mm (1/16 inch) from case for 10 seconds

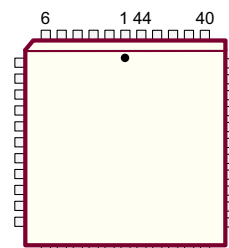
## Pin Configurations



44-Lead Quad Cerpac (DJ)  
(top view)



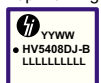
44-Lead PQFP (PG)  
(top view)



44-Lead PLCC (PJ)  
(top view)

## Product Marking

Top Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
C = Country of Origin\*  
A = Assembler ID\*

Bottom Marking



\*May be part of top marking

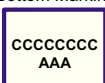
44-Lead Quad Cerpac  
(DJ)

Top Marking



YY = Year Sealed  
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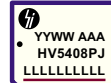
Bottom Marking



\*May be part of top marking

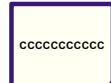
44-Lead PQFP  
(PG)

Top Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
A = Assembler ID  
C = Country of Origin\*

Bottom Marking



\*May be part of top marking

44-Lead PLCC  
(PJ)

Packages may or may not include the following marks: Si or

## Recommended Operating Conditions (over -40°C to 85°C for plastic and -55°C to 125°C for ceramic)

Sym	Parameter	Min	Max	Units
V <sub>DD</sub>	Logic voltage supply	10.8	13.2	V
V <sub>PP</sub>	High voltage supply	8.0	80	V
V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> - 2.0	V <sub>DD</sub>	V
V <sub>IL</sub>	Input low voltage	0	2.0	V
f <sub>CLK</sub>	Clock frequency	0	8.0	MHz

## Power-Up Sequence

Power-up sequence should be the following:

1. Connect ground
2. Apply V<sub>DD</sub>
3. Set all inputs (Data, CLK,  $\overline{LE}$ , etc.) to a known state
4. Apply V<sub>PP</sub>
5. The V<sub>PP</sub> should not fall below V<sub>DD</sub> or float during operation.

Power-down sequence should be the reverse of the above.

## Electrical Characteristics (V<sub>PP</sub> = 60V, V<sub>DD</sub> = 12V, T<sub>A</sub> = 25°C)

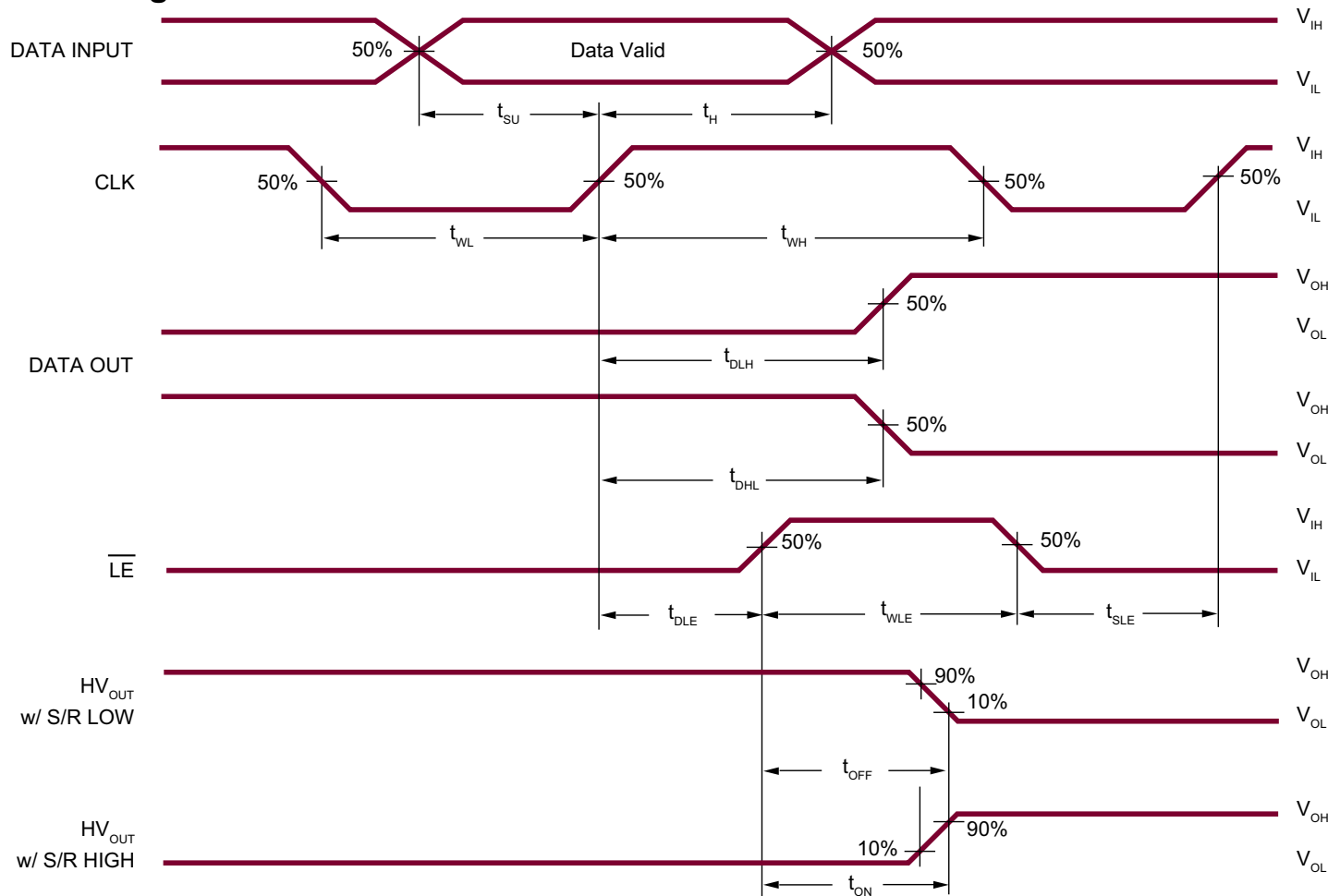
### DC Characteristics

Sym	Parameter	Min	Max	Units	Conditions
I <sub>PP</sub>	V <sub>PP</sub> supply current	-	0.5	mA	HV <sub>OUTPUTS</sub> high to low
I <sub>DDQ</sub>	I <sub>DD</sub> supply current (quiescent)	-	100	μA	All inputs = V <sub>DD</sub> or GND
I <sub>DD</sub>	I <sub>DD</sub> supply current (operating)	-	15	mA	V <sub>DD</sub> = V <sub>DD</sub> max, f <sub>CLK</sub> = 8.0MHz
V <sub>OH</sub> (data)	Shift register output voltage	10.5	-	V	I <sub>O</sub> = -100μA
V <sub>OL</sub> (data)	Shift register output voltage	-	1.0	V	I <sub>O</sub> = 100μA
I <sub>IH</sub>	Current leakage, any input	-	1.0	μA	V <sub>IN</sub> = V <sub>DD</sub>
I <sub>IL</sub>	Current leakage, any input	-	-1.0	μA	V <sub>IN</sub> = 0
V <sub>OC</sub>	HV output clamp diode voltage	-	-1.5	V	I <sub>OL</sub> = -100mA
V <sub>OH</sub>	HV output when sourcing	52	-	V	I <sub>OH</sub> = -20mA, -40 to 85°C
V <sub>OL</sub>	HV output when sinking	-	8.0	V	I <sub>OL</sub> = 20mA, -40 to 85°C
V <sub>OH</sub>	HV output when sourcing	52	-	V	I <sub>OH</sub> = -15mA, -55 to 125°C
V <sub>OL</sub>	HV output when sinking	-	8.0	V	I <sub>OL</sub> = 15mA, -55 to 125°C

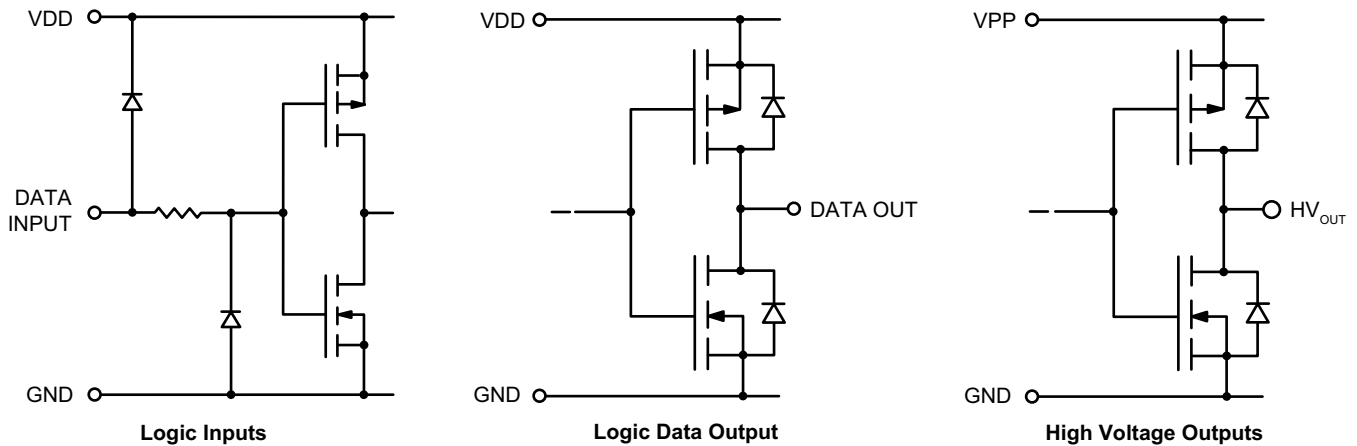
AC Characteristics

Sym	Parameter	Min	Max	Units	Conditions
$f_{CLK}$	Clock frequency	-	8.0	MHz	---
$t_{WL}$ or $t_{WH}$	Clock width, HIGH or LOW	62	-	ns	---
$t_{SU}$	Setup time before CLK rises	25	-	ns	---
$t_H$	Hold time after CLK rises	10	-	ns	---
$t_{DLH}$ (Data)	Data output delay after L to H CLK	-	110	ns	$C_L = 15pF$
$t_{DHL}$ (Data)	Data output delay after H to L CLK	-	110	ns	$C_L = 15pF$
$t_{DLE}$	$\overline{LE}$ delay after L to H CLK	50	-	ns	---
$t_{WLE}$	Width of $\overline{LE}$ pulse	50	-	ns	---
$t_{SLE}$	$\overline{LE}$ setup time before L to H CLK	50	-	ns	---
$t_{ON}$	Delay from $\overline{LE}$ to $HV_{OUT}$ L to H	-	500	ns	---
$t_{OFF}$	Delay from $\overline{LE}$ to $HV_{OUT}$ H to L	-	500	ns	---

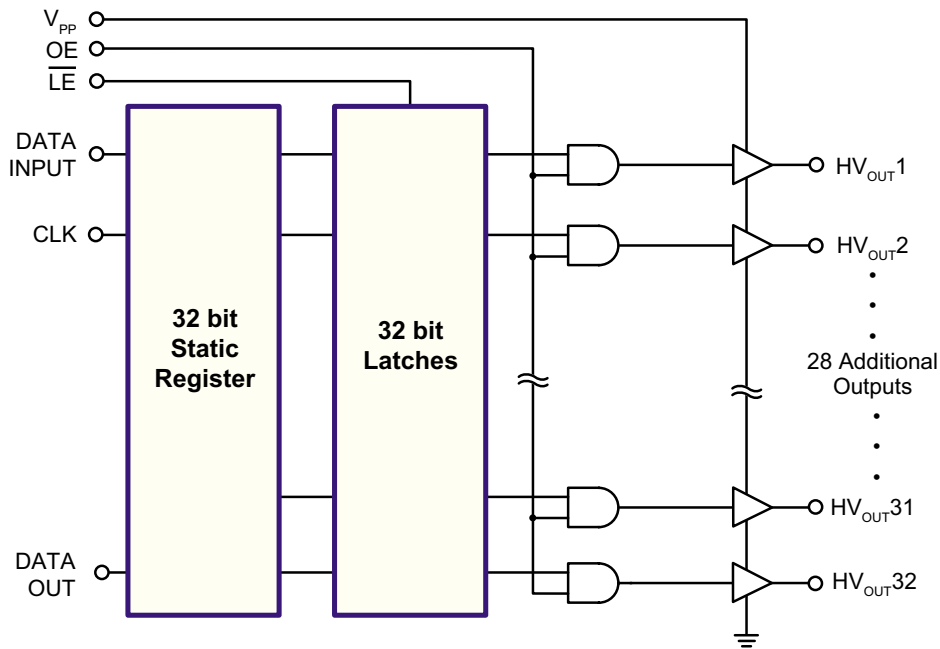
Switching Waveforms



### Input and Output Equivalent Circuits



### Functional Block Diagram



### Function Tables

DATA INPUT	CLK*	DATA OUT
H		H
L		L
X	No	No change

Note:

\* = LOW - to - HIGH transition

H = High  
L = Low  
X = Don't Care

DATA INPUT	LE	OE	HV OUT
X	X	L	All HV <sub>OUT</sub> = LOW
X	L	H	Previous latched data
H	H	H	H
L	H	H	L

## 44-Lead PQFP Pin Assignment (PG)

Pin	Function	Description
1	HV <sub>OUT</sub> 11	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V <sub>PP</sub> rail levels.
2	HV <sub>OUT</sub> 12	
3	HV <sub>OUT</sub> 13	
4	HV <sub>OUT</sub> 14	
5	HV <sub>OUT</sub> 15	
6	HV <sub>OUT</sub> 16	
7	HV <sub>OUT</sub> 17	
8	HV <sub>OUT</sub> 18	
9	HV <sub>OUT</sub> 19	
10	HV <sub>OUT</sub> 20	
11	HV <sub>OUT</sub> 21	
12	HV <sub>OUT</sub> 22	
13	HV <sub>OUT</sub> 23	
14	HV <sub>OUT</sub> 24	
15	HV <sub>OUT</sub> 25	
16	HV <sub>OUT</sub> 26	
17	HV <sub>OUT</sub> 27	
18	HV <sub>OUT</sub> 28	
19	HV <sub>OUT</sub> 29	
20	HV <sub>OUT</sub> 30	
21	HV <sub>OUT</sub> 31	
22	HV <sub>OUT</sub> 32	
23	DATA OUT	Serial data output. Data output for cascading to the data input of the next device.
24	N/C	No connect.
25		
26		
27	CLK	Data shift register clock Input are shifted into the shift register on the positive edge of the clock.
28	GND	Logic and high voltage ground.
29	VPP	High voltage power rail.
30	VDD	Low voltage logic power rail.

## 44-Lead PQFP Pin Assignment (PG)

Pin	Function	Description
31	$\overline{\text{LE}}$	Latch enable input. When $\overline{\text{LE}}$ is HIGH, shift register data is transferred into a data latch. When $\overline{\text{LE}}$ is LOW, data is latched, and new data can be clocked into the shift register.
32	DATA INPUT	Serial data input. Data needs to be present before each rising edge of the clock.
33	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
34	N/C	No connect.
35	HV <sub>OUT1</sub>	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V <sub>PP</sub> rail levels.
36	HV <sub>OUT2</sub>	
37	HV <sub>OUT3</sub>	
38	HV <sub>OUT4</sub>	
39	HV <sub>OUT5</sub>	
40	HV <sub>OUT6</sub>	
41	HV <sub>OUT7</sub>	
42	HV <sub>OUT8</sub>	
43	HV <sub>OUT9</sub>	
44	HV <sub>OUT10</sub>	

## 44-Lead Quad Cerpac/PLCC Pin Assignment (DJ/PJ)

Pin	Function	Description
1	HV <sub>OUT</sub> 16	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V <sub>PP</sub> rail levels.
2	HV <sub>OUT</sub> 17	
3	HV <sub>OUT</sub> 18	
4	HV <sub>OUT</sub> 19	
5	HV <sub>OUT</sub> 20	
6	HV <sub>OUT</sub> 21	
7	HV <sub>OUT</sub> 22	
8	HV <sub>OUT</sub> 23	
9	HV <sub>OUT</sub> 24	
10	HV <sub>OUT</sub> 25	
11	HV <sub>OUT</sub> 26	
12	HV <sub>OUT</sub> 27	
13	HV <sub>OUT</sub> 28	
14	HV <sub>OUT</sub> 29	
15	HV <sub>OUT</sub> 30	
16	HV <sub>OUT</sub> 31	
17	HV <sub>OUT</sub> 32	
18	DATA OUT	Serial data output. Data output for cascading to the data input of the next device.
19	N/C	No connect.
20		
21		
22	CLK	Data shift register clock Input are shifted into the shift register on the positive edge of the clock.
23	GND	Logic and high voltage ground.
24	VPP	High voltage power rail.
25	VDD	Low voltage logic power rail.
26	$\overline{LE}$	Latch enable input. When $\overline{LE}$ is HIGH, shift register data is transferred into a data latch. When $\overline{LE}$ is LOW, data is latched, and new data can be clocked into the shift register.
27	DATA INPUT	Serial data input. Data needs to be present before each rising edge of the clock.

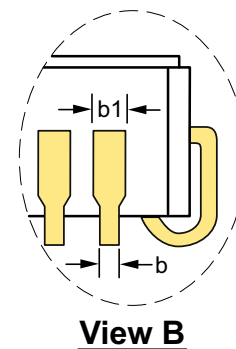
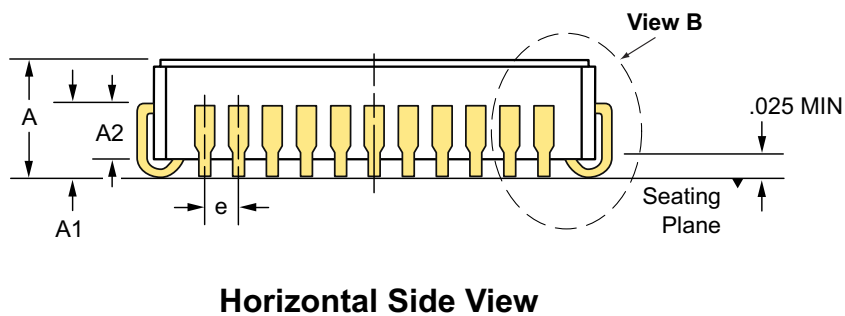
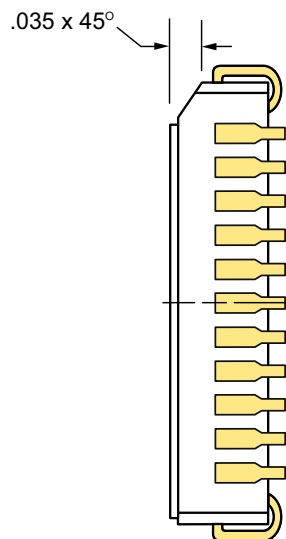
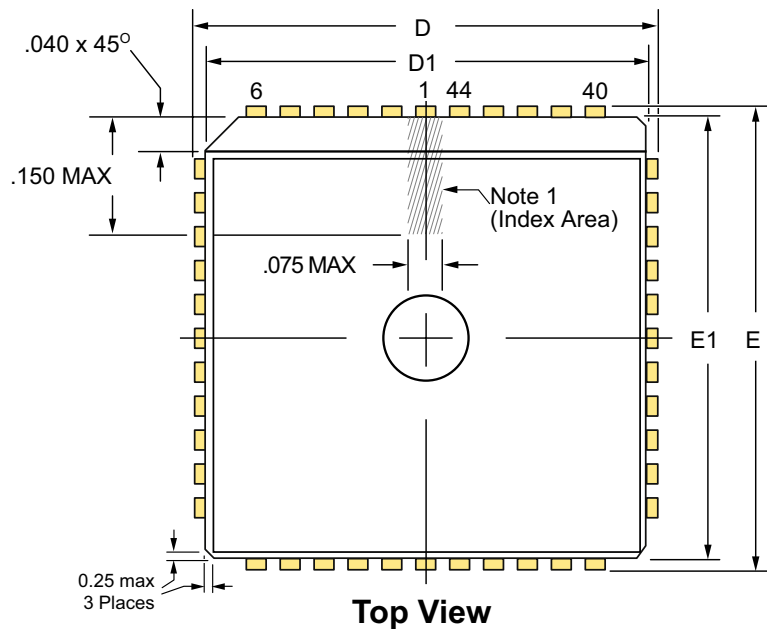


## 44-Lead Quad Cerpac/PLCC Pin Assignment (DJ/PJ)

Pin	Function	Description
28	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
29	N/C	No connect.
30	HV <sub>OUT</sub> 1	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to V <sub>PP</sub> rail levels.
31	HV <sub>OUT</sub> 2	
32	HV <sub>OUT</sub> 3	
33	HV <sub>OUT</sub> 4	
34	HV <sub>OUT</sub> 5	
35	HV <sub>OUT</sub> 6	
36	HV <sub>OUT</sub> 7	
37	HV <sub>OUT</sub> 8	
38	HV <sub>OUT</sub> 9	
39	HV <sub>OUT</sub> 10	
40	HV <sub>OUT</sub> 11	
41	HV <sub>OUT</sub> 12	
42	HV <sub>OUT</sub> 13	
43	HV <sub>OUT</sub> 14	
44	HV <sub>OUT</sub> 15	

# 44-Lead Quad Cerpac Package Outline (DJ)

.650x.650in body, .190in height (max), .050in pitch



**Note:**  
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	
Dimension (inches)	MIN	.155	.090	.060 REF	.017	.026	.685	.630	.685	.630	.050 BSC
	NOM	.172	.100		.019	.029	.690	.650	.690	.650	
	MAX	.190	.120		.021	.032	.695	.665	.695	.665	

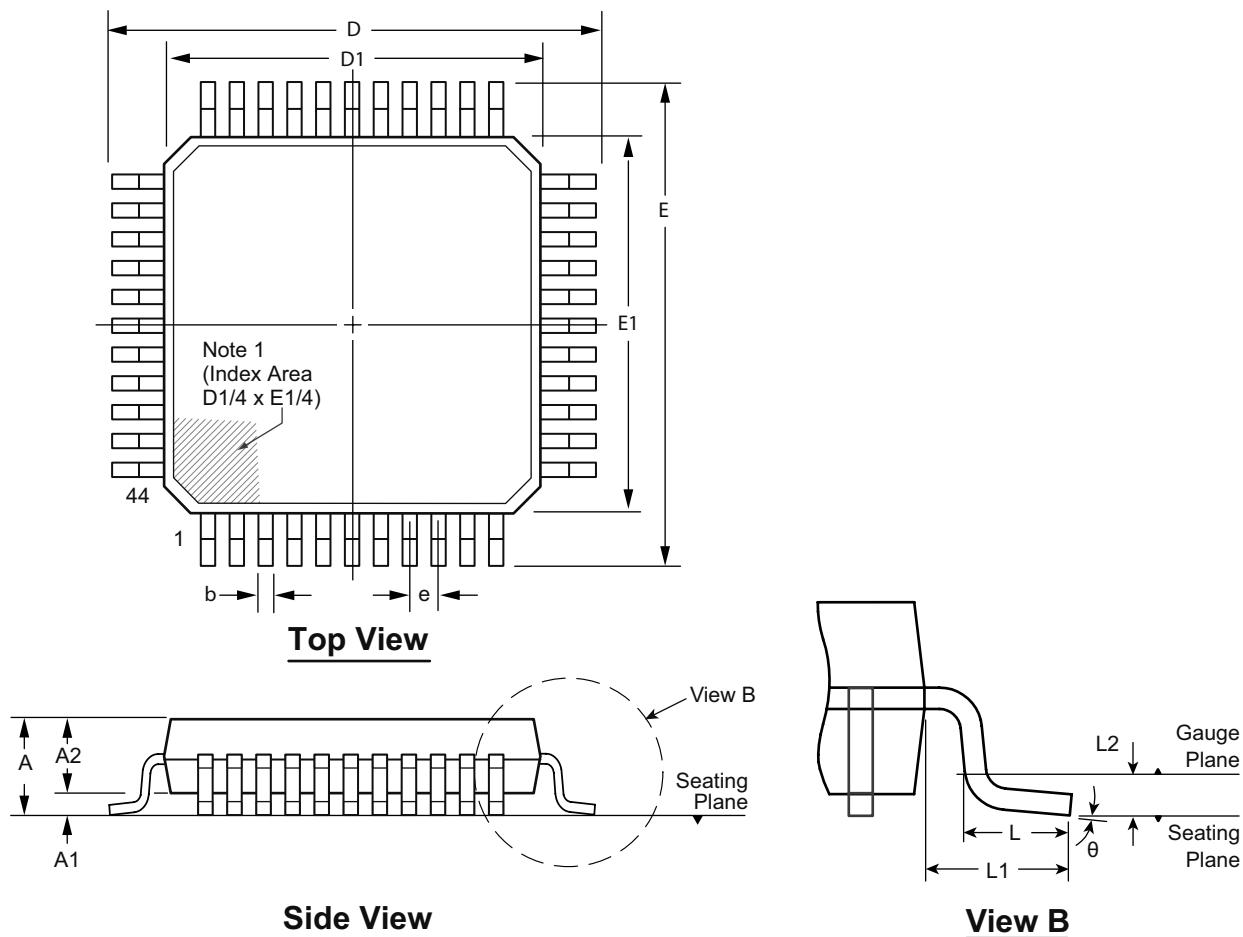
JEDEC Registration MO-087, Variation AB, Issue B, August, 1991.

Drawings not to scale.

Supertex Doc. #: DSPD-44CERPACDJ, Version D090808.

# 44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



**Note:**  
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	1.95 REF	0.25 BSC	0°	
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00				0.73	3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*				0.88	7°
										1.03				

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep. 1995.

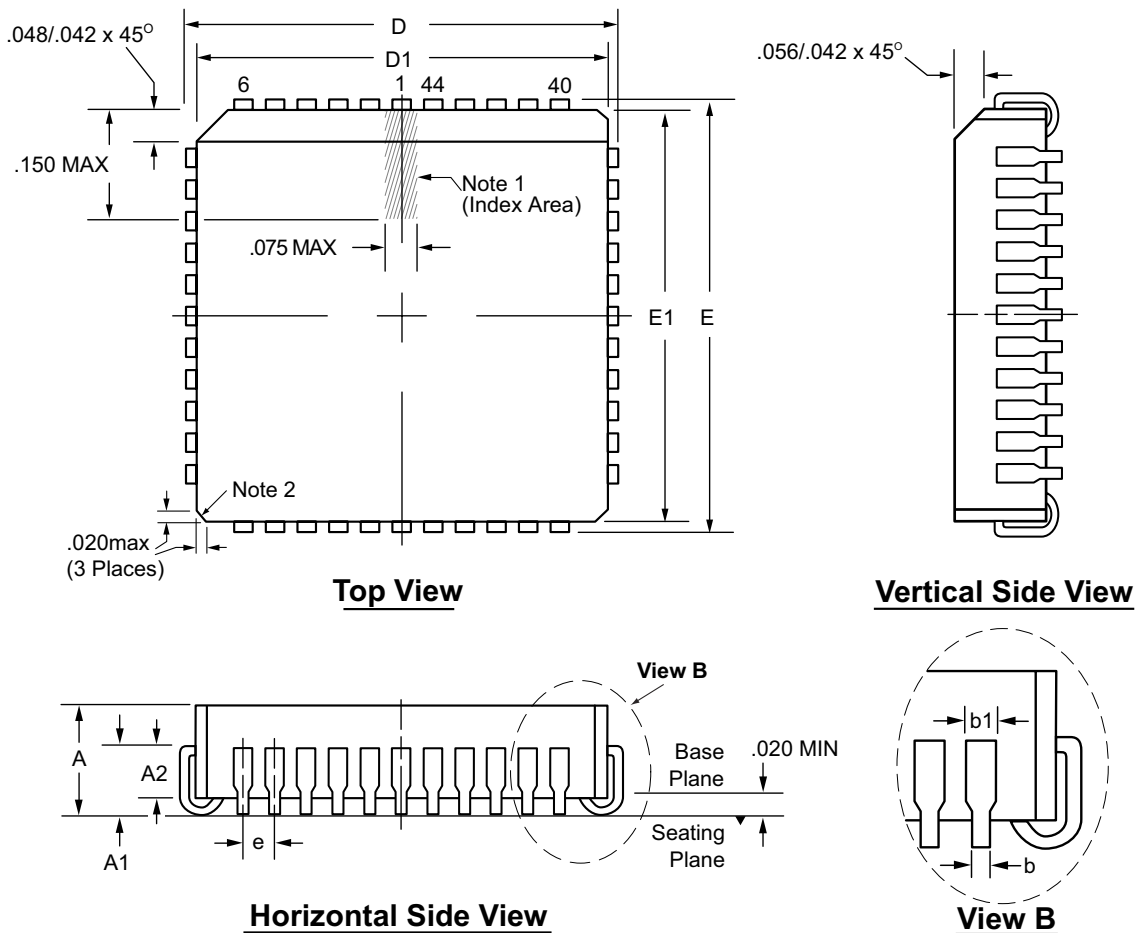
\* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PQFPPG, Version C041309.

# 44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656	

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #: DSPD-44PLCCPJ, Version E041309.**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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