W83195BR-341

W83195BG-341

WINBOND CLOCK GENERATOR FOR VIA P4/KT SERIES CHIPSET

Date: Mar/21/2006 Revision: 1.1

W83195BR-341/W83195BG-341 Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1					All of the versions before 0.50 are for internal use.
2	n.a.	07/07/03	0.5	n.a.	First published preliminary version.
3	n.a.	26/8/03	0.6	n.a.	Some description red text part
4	19	12/18/03	0.7	n.a.	Correction IC version,
5		05/03/04	1.0	1.0	Update on web
6		03/21/06	1.1	1.1	Add lead-free part number W83195BG-341
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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CLOCK GEN. FOR VIA P4/KT SERIES CHIPSET

1. GENERAL DESCRIPTION

The W83195BR-341 is a Clock Synthesizer for Intel P4 Springdale/Prescott series chipset and support AMD Athlon processors. W83195BR-341 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, AGP, and PCI clocks setting. All clocks are externally selectable with smooth transitions.

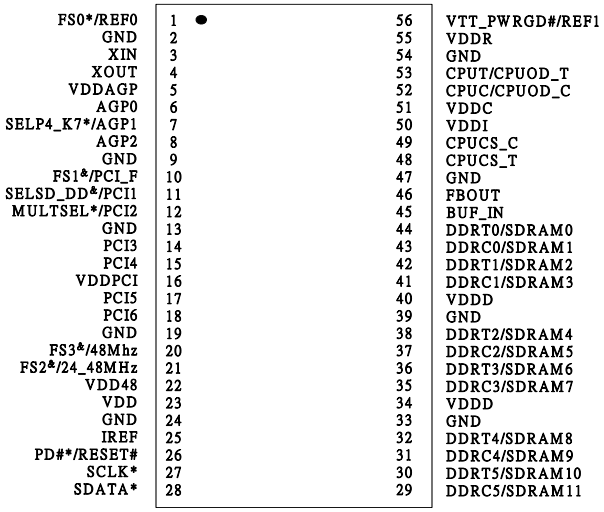
The W83195BR-341 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides +/-0.25%, +/-0.5% center type and –0.5%, -1.0% down type spread spectrum or programmable S.S.T. scale to reduce EMI.

The W83195BR-341 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

- 1 pairs differential clock for CPU (P4 or Athlon)
- 1 pairs differential clock for Chipset
- 3 AGP clock outputs
- Support two DDR DIMMS or three SDRAM DIMMS
- 7 PCI synchronous clocks, 1 free running
- 1 48MHz clock outputs for USB
- 1 24_48MHz for I/O chip, default 24MHz
- 2 REF 14.318MHz clock outputs
- AGP leads PCICLK from 1.5ns to 3.5ns
- I^2C 2-Wire serial interface supports block and byte mode read/write
- Step-less frequency programming
- Smooth frequency switch with selections from 66 to 200MHz
- Programmable clock outputs Slew rate control and Skew control
- +/- 0.25% center type spread spectrum in table mode
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- 56-pin SSOP package

3. PIN CONFIGURATION

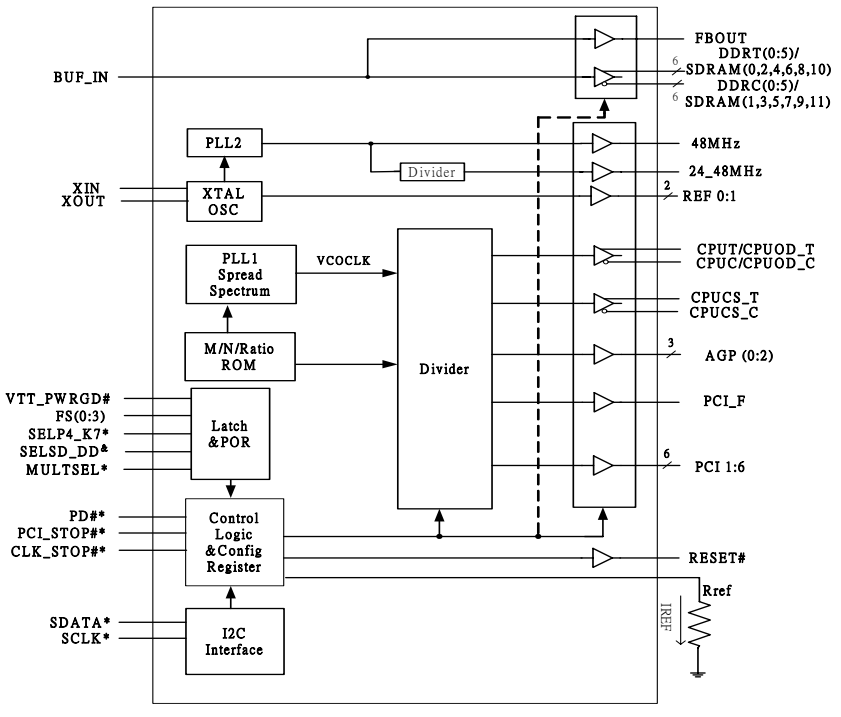


#: Active low

*: Internal pull up resistor 120KΩ to VDD

&: Internal Pull-down resistor 120KΩ to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	FUNCTION DESCRIPTION
IN	Input
IN_{td120k}	Latch input pin and internal 120KΩ pull down
IN_{tp120k}	Latch input pin and internal 120KΩ pull up
OUT	Output
OD	Open Drain
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
3	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
4	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, AGP, PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
53,52	CPUT/CPUOD_T CPUC/CPUOD_C	OUT	Current Mode differential clock outputs for P4 CPU or Open Drain Mode differential clock outputs for K7 CPU, selected by hardware trapping power on 7 pin SELP4_K7* selecting. SELP4_K7=1 Current Mode, SELP4_K7=0 Open Drain Mode.
49,48	CPUCS_C, CPUCS_T	OUT	2.5V differential clock outputs for Chipset.
7	AGP1	OUT	3.3V 66MHz clock output
	SELP4_K7*	IN_{tp120k}	Power up Latched input to selecting pin 53,52 and 56 output type, SELP4_K7=1 the 53,52 is P4 Mode and pin 56 is VTT_PWRGD#, SELP4_K7=0 the 53,52 is K7 Mode and pin 56 is REF1.This is internal 120KΩ pull up.
6	AGP_0	OUT	3.3V 66MHz clock output.

CPU, AGP, PCI Clock Outputs, continued

PIN	PIN NAME	TYPE	DESCRIPTION
8	AGP2	OUT	3.3V 66MHz clock output.
	PCI_STOP#*	IN_{tp120k}	PCI clock stop control pin, This pin is low active. Internal 120kΩ pull up, Selected by Register 1 bit 6= 0 and Register 9 bit 6 = 1, see Page 10 Table 2.
10	PCI_F	OUT	3.3V 33MHz free running clock output.
	FS1&	IN_{td120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down.
11	PCI1	OUT	3.3V 33MHz clock output.
	SELSD_DD&	IN_{td120k}	Latched input at initial power up for DRAM buffer output type selecting, SELSD_DD= 0 DDR Mode SELSD_DD=1 SDR Mode, This is internal 120KΩ pull down.
12	PCI2	OUT	3.3V 33MHz clock output.
	MULTSEL*	IN_{tp120k}	Power on trapping for different current reference. The reference current is referred for Pin 25 (IREF), see page 5 Table 1. This pin is latched during VTT_PWRGD#. This pin is internal pull up 120K.
14, 15, 17, 18	PCI [3:6]	OUT	3.3V 33MHz clock outputs.

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
1	REF0	OUT	14.318MHz output.
	FS0*	IN_{tp120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up.
56	REF1	OUT	If SELP4_K7=0 this pin is 14.318MHz output.
	VTT_PWRGD#	IN	If SELP4_K7=1 this pin is Power good input signal comes from ACPI with low active. This 3.3V input is level sensitive strobe used to determine FS [3:0] and MULTSEL input are valid and is ready to sample. This pin is low active.
20	48MHz	OUT	48MHz clock output.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down.
21	24_48MHz	OUT	24(default) or 48MHz clock output, select by register 4 bit 7 SEL24
	FS2&	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down.

5.4 DRAM Buffer

PIN	PIN NAME	TYPE	DESCRIPTION
45	BUF_IN	IN	Reference input from chipset. 2.5V input for DDR only mode. 3.3V for standard SDRAM mode.
46	FBOUT	OUT	Feedback clock for chipset. Output voltage depends on VDDD
44,42,38,36,32,30	DDRT[0:5] SDRAM [0,2,4,6,8,10]	OUT	Clock outputs. SELSD_DD=1, these pins are copies of BUF_IN. SELSD_DD=0, these pins are copies of BUF_IN. Voltage depends on the VDDD.
43,41,37,35,31,29	DDRC[0:5] SDRAM [1,3,5,7,9,11]	OUT	Clock outputs. SELSD_DD=1, these pins are complementary copies of BUF_IN. SELSD_DD=0, these pins are copies of BUF_IN. Voltage depends on the VDDD.

5.5 I2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
28	SDATA*	I/OD	Serial data of I^2C 2-wire control interface with internal pull-up resistor 120K.
27	SCLK*	IN	Serial clock of I^2C 2-wire control interface with internal pull-up resistor 120K.

5.6 Output Control Pins

<table>
<tr><th>PIN</th><th>PIN NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="3">25</td><td rowspan="3">IREF</td><td rowspan="3">OUT</td><td>Deciding the reference current for the CPUT/C pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. The table is show as follows. TABLE 1
<table>
<tr><th>MULTSEL (PIN 11)</th><th>Board Target Trace/ Term Z</th><th>Reference R, Iref=VDD/(3*Rr)</th><th>Output Current</th><th>Ioh @ Z</th></tr>
<tr><td>1</td><td>50 Ohms</td><td>R=475 1%
Iref=2.32mA</td><td>Ioh=6*Iref</td><td>0.7V @ 50</td></tr>
<tr><td>0</td><td>50 Ohms</td><td>R=221 1%
Iref=5mA</td><td>Ioh=4*Iref</td><td>1.0V @ 50</td></tr>
</table></td></tr>
<tr><td rowspan="2">26</td><td>RESET#</td><td>OD</td><td>Select by register 1 bit 6 L_MODE if L_MODE=1 this pin is System reset signal when the watchdog is time out. This pin will generate 250mS when the watchdog timer is timeout</td></tr>
<tr><td>PD#*</td><td>IN</td><td>Select by register 1 bit 6 L_MODE if L_MODE=0 this pin is Power Down Function. This is internal 120KΩ pull up.</td></tr>
</table>

5.7 Power an GND Pins

PIN	PIN NAME	TYPE	DESCRIPTION
5	VDDAGP	PWR	3.3V power supply for AGP.
16	VDDPCI	PWR	3.3V power supply for PCI.
22	VDD48	PWR	3.3V power supply for 48MHz.
23	VDD	PWR	3.3V power supply analog core.
34,40	VDDD	PWR	3.3V or 2.5V power for DRAM buffer part.
50	VDDI	PWR	2.5V power supply for CPUCS_T/C.
51	VDDC	PWR	3.3V power supply for CPUT/C.
55	VDDR	PWR	3.3V power supply for REF
2,9,13,19,24,33,39,47,54	GND	PWR	Ground pin for 3.3 V

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	AGP (MHZ)	PCI (MHZ)
0	0	0	0	0	66.8	66.8	33.4
0	0	0	0	1	99.9	66.6	33.3
0	0	0	1	0	120.2	60.1	30.0
0	0	0	1	1	133.2	66.6	33.3
0	0	1	0	0	72.0	72.0	36.0
0	0	1	0	1	105.1	70.1	35.0
0	0	1	1	0	160.1	64.0	32.0
0	0	1	1	1	140.1	70.1	35.0
0	1	0	0	0	77.0	77.0	38.5
0	1	0	0	1	110.0	73.3	36.7
0	1	0	1	0	180.3	60.1	30.0
0	1	0	1	1	166.6	66.6	33.3
0	1	1	0	0	90.1	60.1	30.0
0	1	1	0	1	99.9	66.6	33.3
0	1	1	1	0	199.8	66.6	33.3
0	1	1	1	1	133.2	66.6	33.3
1	0	0	0	0	160.1	80.1	40.0
1	0	0	0	1	164.0	82.0	41.0
1	0	0	1	0	166.6	66.6	33.3
1	0	0	1	1	169.9	67.9	34.0
1	0	1	0	0	175.1	70.0	35.0
1	0	1	0	1	180.3	72.1	36.1
1	0	1	1	0	184.8	73.9	37.0
1	0	1	1	1	190.0	76.0	38.0
1	1	0	0	0	66.8	66.8	33.4
1	1	0	0	1	100.9	67.3	33.6
1	1	0	1	0	133.6	66.8	33.4
1	1	0	1	1	200.5	66.8	33.4
1	1	1	0	0	66.6	66.6	33.3
1	1	1	0	1	99.9	66.6	33.3
1	1	1	1	0	199.8	66.6	33.3
1	1	1	1	1	133.2	66.6	33.3

7. I2C CONTROL AND STATUS REGISTERS

(The register No. Is increased by 1 if use byte data read/write protocol)

7.1 Register 0: Frequency Select (Default =08h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	SSEL [4]	0	Software frequency table selection through I^2C
6	SSEL [3]	0	
5	SSEL [2]	0	
4	SSEL [1]	0	
3	SSEL [0]	1	
2	EN_SSEL	0	Enable software table selection FS [4:0]. 0 = Hardware table setting (Jump mode). 1 = Software table setting through Bit7~3. (Jump less mode)
1	SPSPEN	0	Enable spread spectrum mode under clock output. 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable
0	Reserved	0	Reserved

7.2 Register 1: SRC/CPU Clock (1 = Enable, 0 = Disable) (Default: A1h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	CPUCS_T CPUCS_C	1	Pin 48,49 CPUCS_T/C output control
6	L_MODE	0	Selection for Pin 26. Power Down Input / System Reset Control Output 1: System Reset feature 0: Power Down feature (Default)
5	CPUT/C	1	Pin 53,52 CPUT/C output control
4	FS4	0	Mapping software table.
3	FS3	X	Power on latched value of FS3 (20) pin. Default 0 (Read only)
2	FS2	X	Power on latched value of FS2 (21) pin. Default 0 (Read only)
1	FS1	X	Power on latched value of FS1 (10) pin. Default 0 (Read only)
0	FS0	X	Power on latched value of FS (1) pin. Default 1 (Read only)

7.3 Register 2: PCI Clock (1 = Enable, 0 = Disable) (Default: FEh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	PCI_F	1	Pin 10 PCI_F output control
6	PCI6	1	Pin 18 PCI6 output control
5	PCI5	1	Pin 17 PCI5 output control
4	PCI4	1	Pin 15 PCI4 output control
3	PCI3	1	Pin 14 PCI3 output control
2	PCI2	1	Pin 12 PCI2 output control
1	PCI1	1	Pin 11 PCI1 output control
0	INV_CPUCS	0	Invert the CPUCS phase, 0: Default, 1: Inverse

7.4 Register 3: REF, 24_48,48,AGP Clock (1 = Enable, 0 = Disable) (Default: F7h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	PREF1	1	Pin 56 REF1 output control
6	PREF0	1	Pin 1 REF0 output control
5	PUSB24	1	Pin 21 24_48MHz output control
4	PUSB48	1	Pin 20 48MHz output control
3	INV_USB48	0	Invert the 48MHz phase, 0: In phase with 24_48MHz, 1: 180 degrees out of phase
2	AGP2	1	Pin 8 AGP2 output control
1	AGP1	1	Pin 7 AGP1 output control
0	AGP0	1	Pin 6 AGP0 output control

7.5 Register 4,5 Reserved

7.6 Register 6: M/N Program (Default: 8Bh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	N_DIV [8]	1	Programmable N divisor value. Bit 7 ~0 are defined in the Register 7.
6	M_DIV [6]	0	Programmable M divisor value.
5	M_DIV [5]	0	
4	M_DIV [4]	0	
3	M_DIV [3]	1	
2	M_DIV [2]	0	
1	M_DIV [1]	1	
0	M_DIV [0]	1	

7.7 Register 7: M/N Program (Default: 2Fh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	N_DIV [7]	0	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 6, Bit 7. The bit 9 is defined in Register 9, Bit 7.
6	N_DIV [6]	0	
5	N_DIV [5]	1	
4	N_DIV [4]	0	
3	N_DIV [3]	1	
2	N_DIV [2]	1	
1	N_DIV [1]	1	
0	N_DIV [0]	1	

7.8 Register 8: Spread Spectrum Program (Default: 1Fh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.
6	SP_UP [2]	0	
5	SP_UP [1]	0	
4	SP_UP [0]	1	
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0 2's complement representation. Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000
2	SP_DOWN [2]	1	
1	SP_DOWN [1]	1	
0	SP_DOWN [0]	1	

7.9 Register 9: Divider Ratio (Default: 03h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	N<9>	0	Programmable N divisor value bit 9
6	SEL_CLKSTOP	0	Refer to Table-2
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	DS2	0	Define the CPU/AGP/PCI divider ratio Refer to Table-3
1	DS1	1	
0	DS0	1	

Table-2

REGISTER 1 /BIT 6 L_MODE	REGISTER 9/BIT6 SEL_CLKSTOP	PIN 26	PIN8	PIN18
0	0(default)	PD#	AGP2	PCI6
0	1	PD#	PCI_STOP#	CLK_STOP#
1	0	RESET#	AGP2	PCI6
1	1	RESET#	AGP2	PCI6

Table-3 CPU, AGP, PCI divider ratio selection Table

DS2~DS0	CPU	AGP	PCI
000	2	5	10
001	2	6	12
010	3	6	12
011	4	6	12
100	6	6	12
101	3	7	14
110	4	8	16
111	4	10	20

7.10 Register 10: Control (Default: 0Ah)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	EN_MN_PROG	0	0: Output frequency depend on frequency table 1: Program all clock frequency by changing M/N value The equation is **VCO =14.318MHz*(N+4)/ M**.
6	N<10>	0	Programmable N divisor value bit 10
5	Reserve	0	Reserved
4	Reserve	0	
3	IVAL<3>	1	Charge pump current selection
2	IVAL<2>	0	
1	IVAL<1>	1	
0	IVAL<0>	0	

7.11 Register 11: Control (Default: E7h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	CPUT_DRI	1	CPUT output state in during POWER DOWN or Stop mode assertion. 0: Driven (2*Iref), 1: Tristate (Floating) CPUC always tri-state (floating) in power down Assertion.
6	MULTSEL	X	On P4 mode CPU clock output level selection Refer to Page 5 Table-1 Default value follow hardware trapping data on pin12 MULTSEL/PCI2 (Default 1)
5	SPCNT [5]	1	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us
4	SPCNT [4]	0	
3	SPCNT [3]	0	
2	SPCNT [2]	1	
1	SPCNT [1]	1	
0	SPCNT [0]	1	

7.12 Register 12: Control (Default: 3Ch)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	INV_CPU	0	Invert the CPU phase 0: Default, 1: Inverse
6	TRI_EN	0	Tri-state all output if set 1
5	SPSP_TYPE	1	Spread spectrum implementation method 1 : Pendulum type 0 : Original
4	SPSP1	1	Spread Spectrum type select. 00: Down 1% 01: Down 0.5% 10: Center ± 0.5% 11: Center ± 0.25%
3	SPSP0	1	
2	ASKEW [2]	1	CPU to AGP skew control, Skew resolution is 340ps Expand the skew direction is same as CPU_AGP_SKEW [2:0] setting
1	ASKEW [1]	0	
0	ASKEW [0]	0	

7.13 Register 13: Control (Default: 24h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	INV_AGP	0	Invert the AGP phase 0: Default, 1: Inverse
6	INV_PCI	0	Invert the PCI phase 0: Default, 1: Inverse
5	CSKEW [2]	1	CPU to CPUCS skew control, Skew resolution is 340ps
4	CSKEW [1]	0	Expand the skew direction is same as
3	CSKEW [0]	0	CPU_CPUCS_SKEW [2:0] setting
2	PSKEW [2]	1	CPU to PCI skew control, Skew resolution is 340ps
1	PSKEW [1]	0	Expand the skew direction is same as
0	PSKEW [0]	0	CPU_PCI_SKEW [2:0] setting

7.14 Register 14: Control (Default: 56h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	CPUCS_S2	0	CPUCS_T/C slew rate control
6	CPUCS_S1	1	11 : Strong , 00 : Weak , 10/01 : Normal
5	USB48_S2	0	USB48/DOT48/USB24_48 slew rate control
4	USB48_S1	1	11 : Strong , 00 : Weak , 10/01 : Normal
3	AGP_S2	0	AGP2,1,0 slew rate control
2	AGP_S1	1	11 : Strong , 00 : Weak , 10/01 : Normal
1	SELP4_K7	X	Device active mode selection 1: P4 mode 0: K7 mode Default value follow hardware trapping data on pin7 SELP4_K7/AGP1 (Default 1)
0	SELSD_DD	X	DRAM module selection 1: SDRAM mode 0: DDR mode Default value follow hardware trapping data on pin11 SELSD_DD/PCI1 (Default 0)

7.15 Register 15: Slew Rate Control (Default: 55h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	PCI_F_S2	0	PCI_F slew rate control
6	PCI_F_S1	1	11: Strong, 00: Weak, 10/01: Normal
5	PCI_64_S2	0	PCI6, 5,4 slew rate control
4	PCI_64_S1	1	11 : Strong , 00 : Weak , 10/01 : Normal
3	PCI_31_S2	0	PCI3, 2,1 slew rate control
2	PCI_31_S1	1	11 : Strong , 00 : Weak , 10/01 : Normal
1	REF_S2	0	REF0, REF1 slew rate control
0	REF_S1	1	11 : Strong , 00 : Weak , 10/01 : Norma

7.16 Register 16: DRAM Buffer Control (1 = Enable, 0 = Disable) (Default: 7Fh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	Reserve	0	Reserve
6	FBOUT_EN	1	FBOUT output control
5	DDR5	1	DDRT5, DDRC5 / SDRAM10, 11 output control
4	DDR4	1	DDRT4, DDRC4 / SDRAM8, 9 output control
3	DDR3	1	DDRT3, DDRC3 / SDRAM6, 7 output control
2	DDR2	1	DDRT2, DDRC2 / SDRAM4, 5 output control
1	DDR1	1	DDRT1, DDRC1 / SDRAM2, 3 output control
0	DDR0	1	DDRT0, DDRC0 / SDRAM0, 1 output control

7.17 Register 17: Slew Rate Control (Default: CFh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	FBOUT_S2	1	FBOUT slew rate control
6	FBOUT_S1	1	11: Strong, 00: Weak, 10/01: Normal
5	CPUOD_S2	0	CPUODT/C slew rate control
4	CPUOD_S1	0	11: Strong, 00: Weak, 10/01: Normal
3	DDR3_S2	1	DDR3, 4,5/SDRAM6, 7,8,9,10,11 slew rate control
2	DDR3_S1	1	11: Strong, 00: Weak, 10/01: Normal
1	DDR0_S2	1	DDR0, 1,2/SDRAM 0,1,2,3,4,5 slew rate control
0	DDR0_S1	1	11: Strong, 00: Weak, 10/01: Normal

7.18 Register 18: M/N Time & Type Control (Default: 5Bh)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	N_Time<2>	0	M/N mode N value change time control
6	N_Time<1>	1	
5	N_Time<0>	0	
4	M_Time<2>	1	M/N mode M value change time control
3	M_Time<1>	1	
2	M_Time<0>	0	
1	N_TYPE	1	Reserved for Winbond internal use, don't modify it
0	M_TYPE	1	Reserved for Winbond internal use, don't modify it

Note: This Byte only for Winbond internal and BOIS program use, the release version please reserved this byte.

M_TIME<2:0> OR N_TIME<2:0>	M_DIVIDER OR N_DIVIDER TIMING COUNTER
000	6.152us
001	12.304us
010	24.608us
011	49.216us
100	98.432us
101	196.864us
110	393.728us
111	787.456us

7.19 Register 19: Reserved

7.20 Register 20: Winbond Chip ID – (Ready Only) (Default: 61h)

BIT	NAME	PWD	FUNCTION DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83195BR-341 (SA5861).
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	0	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	0	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

7.21 Register 21: Winbond Chip ID – (Ready Only) (Default: 50h)

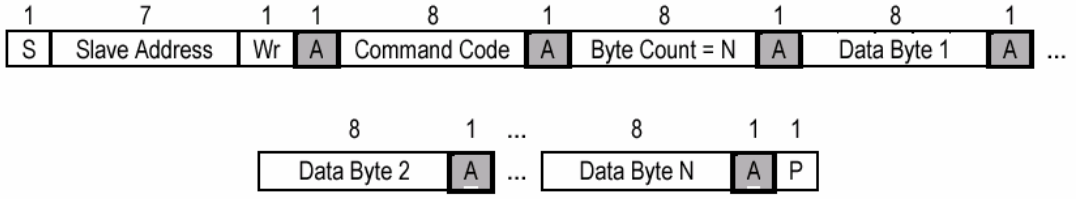
BIT	NAME	PWD	FUNCTION DESCRIPTION
7	MAS_ID [1]	0	MASK definition for master body
6	MAS_ID [0]	1	***A****: 01, ***B****: 10, ***C****: 11, ***D****:00
5	SUB_ID [1]	0	MASK definition for code body
4	SUB_ID [0]	1	*A****001**: 01, *A****002**: 10, *A****003**: 11, *A****004**:00
3	MAS_VER_ID [1]	0	MASK version definition for master body
2	MAS_VER_ID [0]	0	*A****001A**A**: 00, ***A****001A**B**: 01, *A****001A**C**: 10, *A****001A**D**: 11.
1	SUB_VER_ID [1]	0	MASK version definition for code body
0	SUB_VER_ID [0]	0	*A****001**A**: 00, *A****001**B**: 01 *A****001**C**: 10, *A****001**D**: 11

8. ACCESS INTERFACE

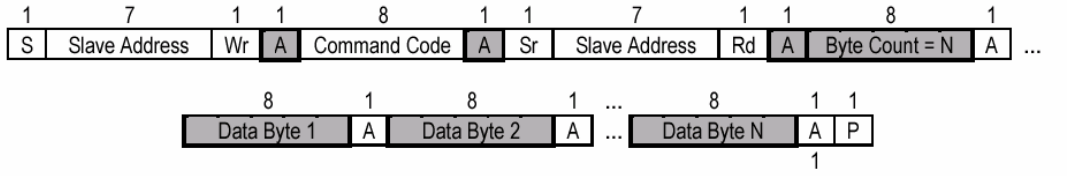
The W83195BR-341 provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83195BR-341 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.

Block Read and Block Write Protocol

8.1 Block Write protocol

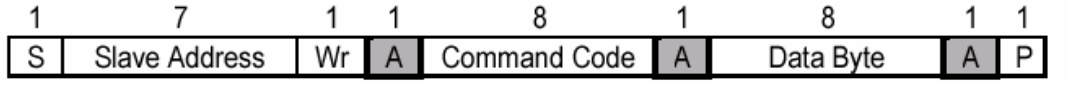


8.2 Block Read protocol

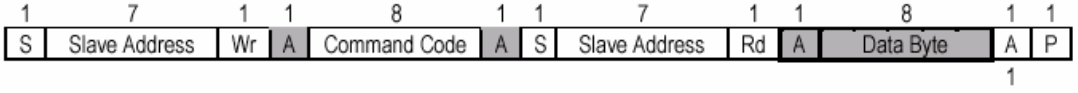


In block mode, the command code must filled 00H

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDD=VDDAGP=VDDC=VDDR=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 200 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDD=VDDAGP=VDDC=VDDR=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
AGP to PCI Skew	1.5	2.6	3.5	ns	Measured at 1.5V
CPU to CPU Skew			200	ps	Crossing point
AGP to AGP Skew			250	ps	Measured at 1.5V
PCI to PCI Skew			500	ps	Measured at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured at 1.5V
REF to REF Skew			500	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

*VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=10pF, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz
Fall Time	175	700	ps	100 to 200Mhz
Absolute crossing point Voltages	250	550	mV	100 to 200Mhz
Cycle to Cycle jitter		150	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.5 CPU 1.0V Electrical Characteristics

*VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=10pF, Vr=221, IREF=5mA, Ioh=4*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz
Fall Time	175	700	ps	100 to 200Mhz
Absolute crossing point Voltages	510	760	mV	100 to 200Mhz
Cycle to Cycle jitter		150	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.6 AGP Electrical Characteristics

VDDAGP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 PCI Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Long term jitter		500	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

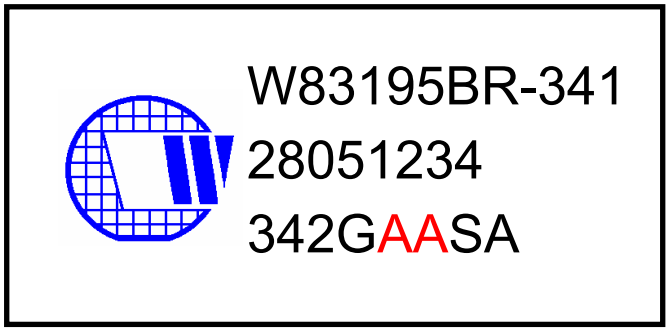
9.9 REF Electrical Characteristics

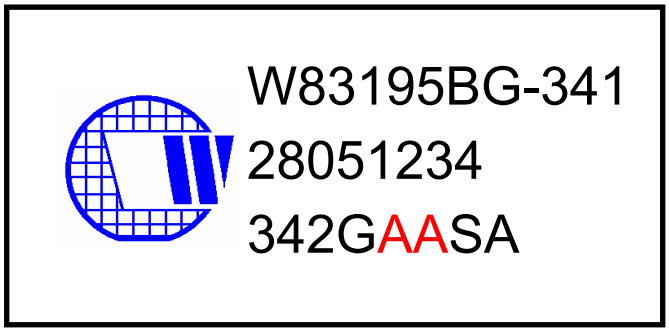
VDDR= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	4000	ps	Measure from 0.4V to 2.4V
Fall Time	1000	4000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		1000	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83195BR-341	56 PIN SSOP	Commercial, 0°C to +70°C
W83195BG-341	56 PIN SSOP (Pb-free package)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING





1st line: Winbond logo and the type number: W83195BR-341/W83195BG-341

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 342 G A A SA

342: packages made in '2003, week 42

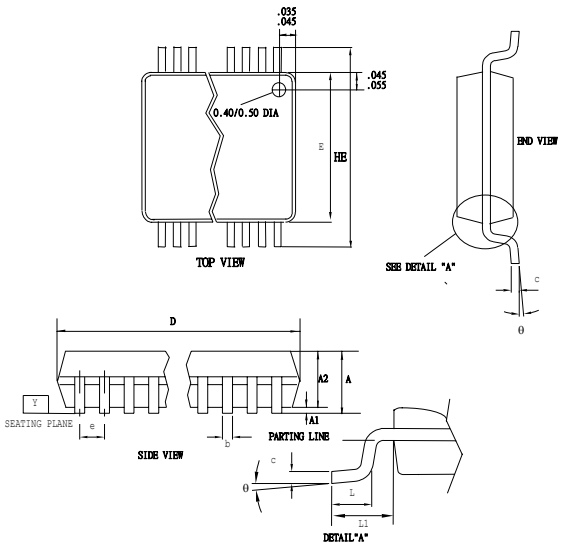
G: assembly house ID; O means OSE, G means GR

A: Internal use code

A: IC revision

SA: mask version

12. PACKAGE DRAWING AND DIMENSIONS



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
θ	0	—	8	0	—	8

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