

54ABT377

Octal D-Type Flip-Flop with Clock Enable

General Description

The 'ABT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

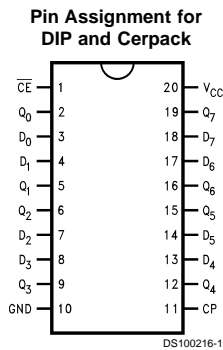
- Clock enable for address and data synchronization applications

- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'ABT273 for master reset version
- See 'ABT373 for transparent latch version
- See 'ABT374 for TRI-STATE® version
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9314801

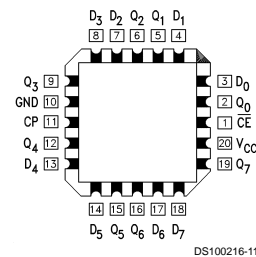
Ordering Code:

Military	Package Number	Package Description
54ABT377J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT377W-QML	W20A	20-Lead Cerpac
54ABT377E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagram



Pin Assignment for LCC



Pin Names	Description
D ₀ -D ₇	Data Inputs
\overline{CE}	Clock Enable (Active LOW)
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

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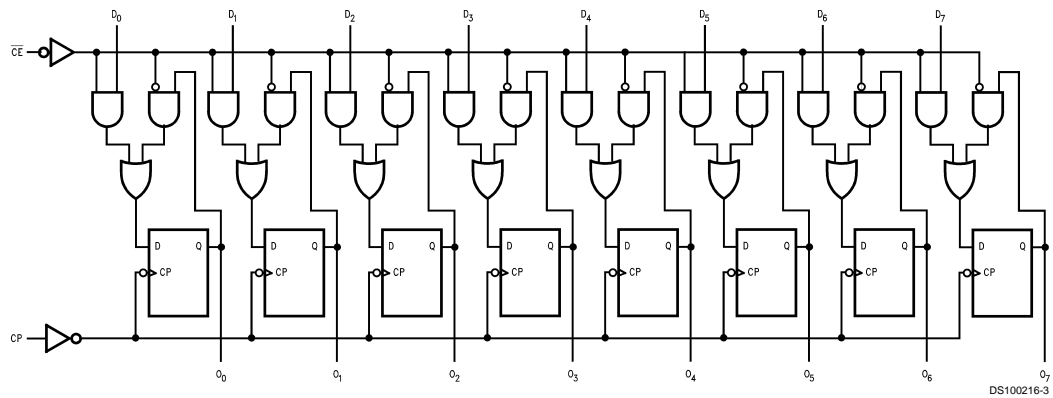
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	\overline{CE}	D_n	Q_n
Load "1"		l	h	H
Load "0"		l	l	L
Hold		h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
= LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +4.75V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	Twice the rated I _{OL} (mA)

DC Latchup Source Current (Across Comm Operating Range)	-500 mA
Over Voltage Latchup	V _{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT377			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA
		54ABT	2.0				I _{OH} = -24 mA
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V (Note 4)
			5				V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		-5		μA	Max	V _{IN} = 0.5V (Note 4)
			-5				V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{CCH}	Power Supply Current		50		μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		30		mA	Max	All Outputs LOW
I _{CCT}	Maximum I _{CC} /Input	Outputs Enabled		1.5	mA	Max	V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC}	No Load		0.3	mA/ MHz	Max	Outputs Open (Note 3) One bit Toggling, 50% Duty Cycle

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 4: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH}	Propagation Delay	2.2	6.0	ns
t_{PHL}	CP to O_n	2.8	6.8	

AC Operating Requirements

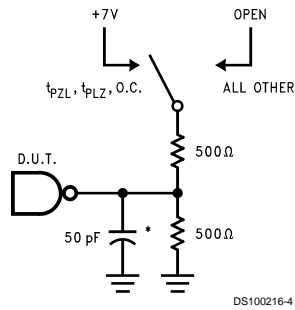
Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
$t_s(\text{H})$	Setup Time, HIGH	2.0		ns
$t_s(\text{L})$	or LOW D_n to CP	2.0		
$t_h(\text{H})$	Hold Time, HIGH	1.8		ns
$t_h(\text{L})$	or LOW D_n to CP	1.8		
$t_s(\text{H})$	Setup Time, HIGH	3.0		ns
$t_s(\text{L})$	or LOW $\overline{\text{CE}}$ to CP	3.0		
$t_h(\text{H})$	Hold Time, HIGH	1.0		ns
$t_h(\text{L})$	or LOW $\overline{\text{CE}}$ to CP	1.0		
$t_w(\text{H})$	Pulse Width, CP,	3.3		ns
$t_w(\text{L})$	HIGH or LOW	3.3		

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$, $T_A = 25^\circ\text{C}$
C_{OUT} (Note 5)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$

Note 5: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

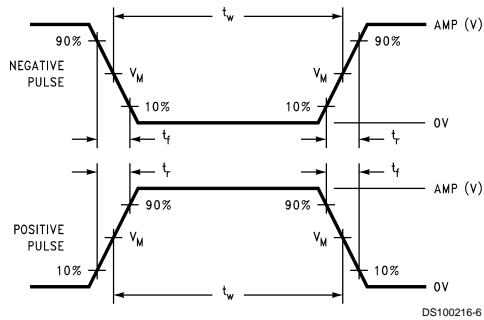


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

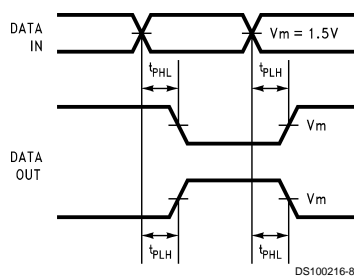


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

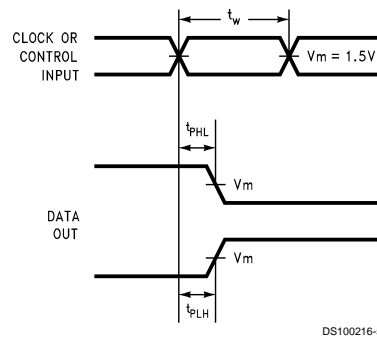


FIGURE 5. Propagation Delay, Pulse Width Waveforms

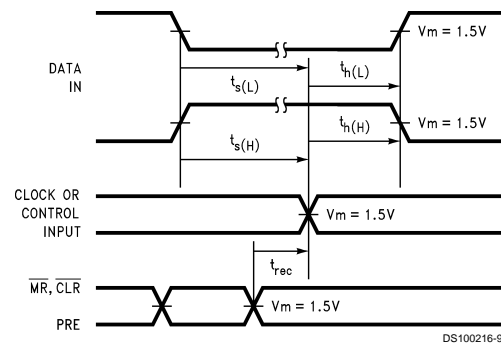
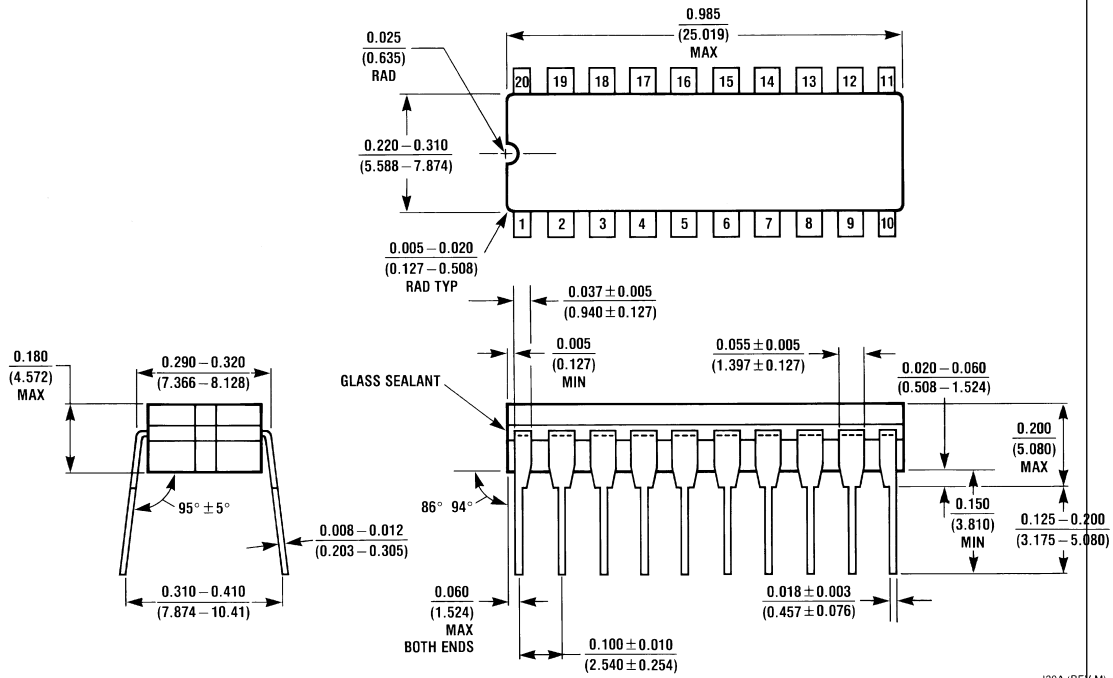
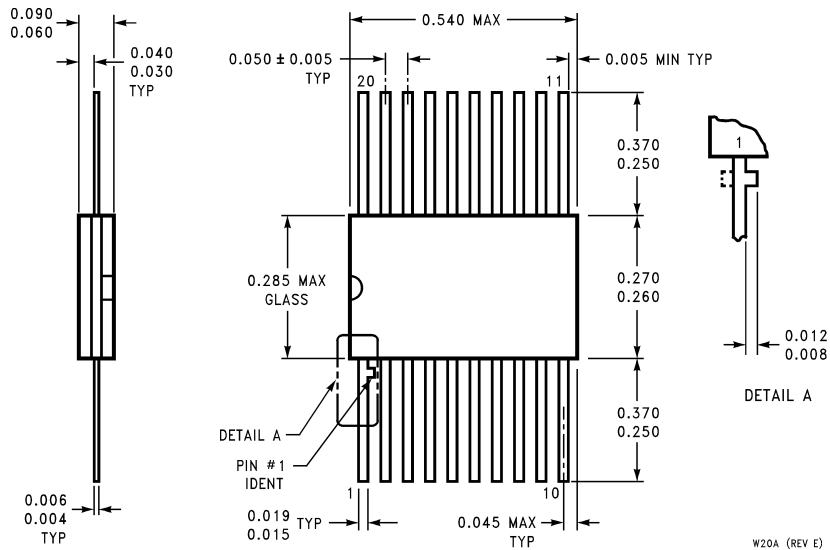


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Dual-In-Line Package
NS Package Number J20A



20-Lead Ceramic Flatpack
NS Package Number W20A

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