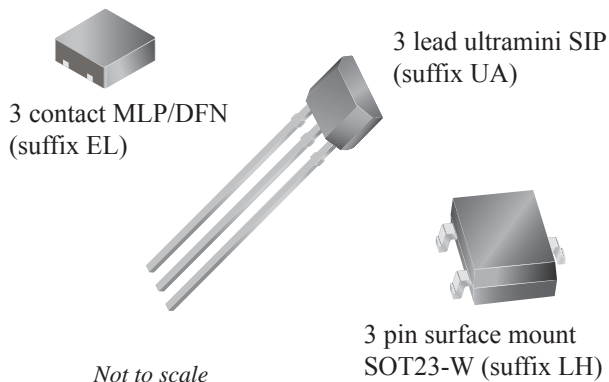


## Micropower Ultra-Sensitive Hall-Effect Switches

### Features and Benefits

- Micropower operation
- Operate with north or south pole
- 2.4 to 5.5 V battery operation
- Chopper stabilized
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- High ESD protection
- Solid state reliability
- Small size
- Easily assembly into applications due to magnetic pole independence

### Packages



### Description

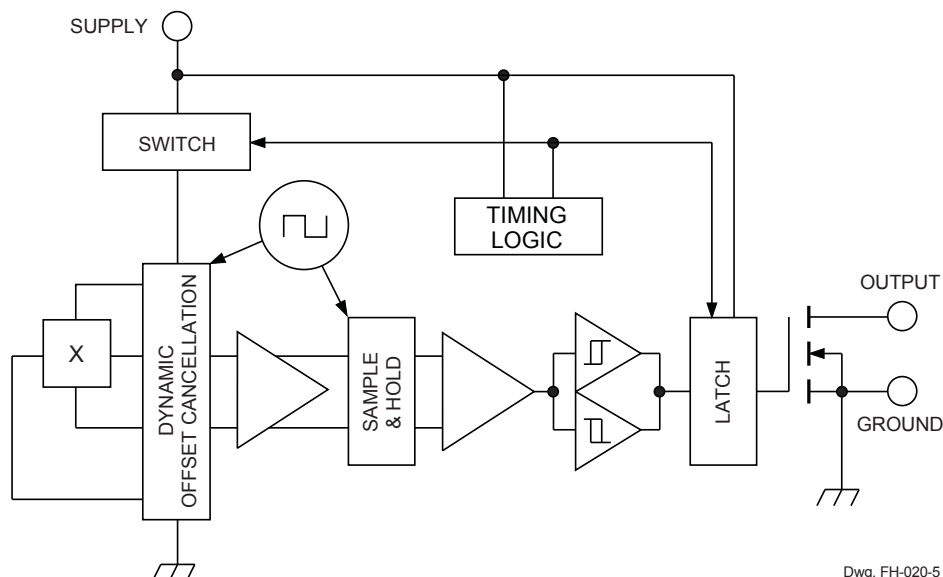
The A3213 and A3214 integrated circuits are ultra-sensitive, pole independent Hall-effect switches with a latched digital output. They are especially suited for operation in battery-operated, hand-held equipment such as cellular and cordless telephones, pagers, and palmtop computers. A 2.4 to 5.5 V operation and a unique clocking scheme reduce the average operating power requirements – the A3213 to 825  $\mu\text{W}$ , the A3214 to 14  $\mu\text{W}$  (typical, at 2.75 V)! Except for operating duty cycle and average operating current, the A3213 and A3214 are identical.

Unlike other Hall-effect switches, either a north or south pole of sufficient strength will turn the output on; in the absence of a magnetic field, the output is off. The polarity independence and minimal power requirement allows these devices to easily replace reed switches for superior reliability and ease of manufacturing, while eliminating the requirement for signal conditioning.

Improved stability is made possible through chopper stabilization (dynamic offset cancellation), which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

*Continued on the next page...*

### Functional Block Diagram



# A3213 and A3214

## Micropower Ultra-Sensitive Hall-Effect Switches

### Description (continued)

These devices include, on a single silicon chip, a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced BiCMOS processing is used to take advantage of low-voltage and low-power requirements, component matching, very low input-offset errors, and small component geometries.

Range 'E' devices are rated for operation over a temperature range of -40°C to 85°C; range 'L' devices are rated for operation over a

temperature range of -40°C to 150°C. Two package styles provide a magnetically optimized package for most applications. 'LH' is a miniature low-profile surface-mount package, 'UA' is a three-lead SIP for through-hole mounting. For the A3213, a microleadless DFN/MLP package 'EL' also is available. Each package is available in a lead (Pb) free version (suffix, -T), with a 100% matte tin plated leadframe.



### Product Selection Guide

| Part Number             | Mounting                       | Packing <sup>1</sup>           | Ambient, T <sub>A</sub><br>(°C) | DC<br>(%) | I <sub>DDAVG(TYP)</sub><br>(μA) |
|-------------------------|--------------------------------|--------------------------------|---------------------------------|-----------|---------------------------------|
| A3213EELLT-T            | EL package<br>Surface mount    | 7-in. reel<br>3000 pieces/reel | -40 to 85                       | 25        | 460                             |
| A3213ELHLT-T            | LH package<br>Surface Mount    |                                |                                 |           |                                 |
| A3213EUA-T              | UA package<br>SIP through hole | Bulk<br>500 pieces/bag         | -40 to 150                      |           |                                 |
| A3213LLHLT-T            | LH package<br>Surface Mount    | 7-in. reel<br>3000 pieces/reel |                                 |           |                                 |
| A3213LUA-T              | UA package<br>SIP through hole | Bulk<br>500 pieces/bag         | -40 to 85                       | 0.10      | 11                              |
| A3214ELHLT-T            | LH package<br>Surface Mount    | 7-in. reel<br>3000 pieces/reel |                                 |           |                                 |
| A3214EUA-T <sup>2</sup> | UA package<br>SIP through hole | Bulk<br>500 pieces/bag         |                                 |           |                                 |
| A3214LLHLT-T            | LH package<br>Surface Mount    | 7-in. reel<br>3000 pieces/reel |                                 |           |                                 |
| A3214LUA-T              | UA package<br>SIP through hole | Bulk<br>500 pieces/bag         | -40 to 150                      |           |                                 |

<sup>1</sup>Contact Allegro for additional packing options.

<sup>2</sup>Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 2, 2009. Deadline for receipt of LAST TIME BUY orders is April 30, 2010. Recommended substitutes: A3214LUA-T.



Allegro MicroSystems, Inc.  
115 Northeast Cutoff  
Worcester, Massachusetts 01615-0036 U.S.A.  
1.508.853.5000; www.allegromicro.com

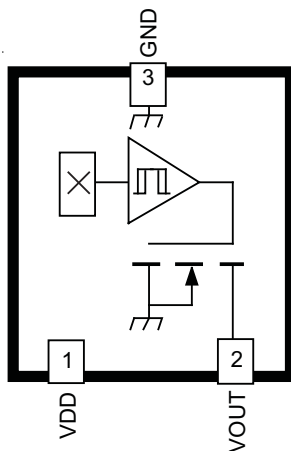
## Absolute Maximum Ratings

| Characteristic                | Symbol       | Notes   | Rating     | Units |
|-------------------------------|--------------|---------|------------|-------|
| Supply Voltage                | $V_{DD}$     |         | 6          | V     |
| Magnetic Flux Density         | B            |         | Unlimited  | G     |
| Output Off Voltage            | $V_{OUT}$    |         | 6          | V     |
| Output Current                | $I_{OUT}$    |         | 1          | mA    |
| Operating Ambient Temperature | $T_A$        | Range E | -40 to 85  | °C    |
|                               |              | Range L | -40 to 150 | °C    |
| Maximum Junction Temperature  | $T_{J(max)}$ |         | 165        | °C    |
| Storage Temperature           | $T_{stg}$    |         | -65 to 170 | °C    |

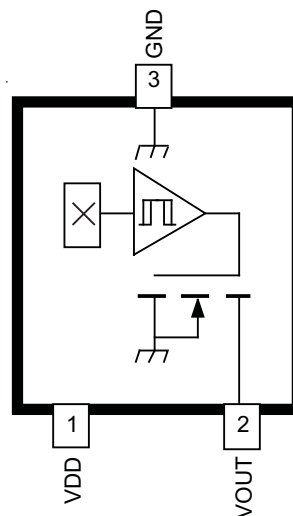
## Pin-out Diagrams

| Number |    | Name | Description  |
|--------|----|------|--|
| EL, LH | UA |      |  |
| 1      | 1  | VDD  | Input power supply; tie to GND with bypass capacitor |
| 3      | 2  | GND  | Ground   |
| 2      | 3  | VOUT | Output signal  |

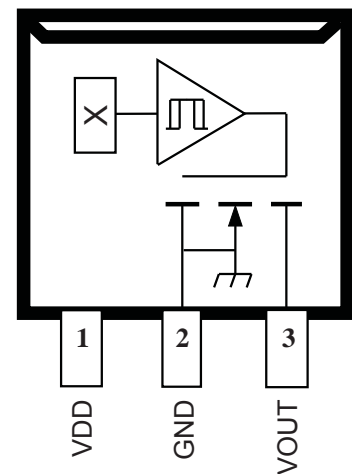
EL Package



LH Package



UA Package



## ELECTRICAL CHARACTERISTICS valid over operating voltage and temperature range, unless otherwise noted

| Characteristic         | Symbol               | Test Conditions   | Min. | Typ. <sup>1</sup> | Max. | Units |
|------------------------|----------------------|---|------|-------------------|------|-------|
| Supply Voltage Range   | V <sub>DD</sub>      | Operating <sup>1</sup> )  | 2.4  | 3.0               | 5.5  | V     |
| Output Leakage Current | I <sub>OFF</sub>     | V <sub>OUT</sub> = 5.5 V, B <sub>RPN</sub> < B < B <sub>RPS</sub> | –    | <1.0              | 1.0  | μA    |
| Output On Voltage      | V <sub>OUT</sub>     | I <sub>OUT</sub> = 1 mA, V <sub>DD</sub> = 3.0 V                  | –    | 100               | 300  | mV    |
| Awake Time             | t <sub>awake</sub>   |   | –    | 60                | 90   | μs    |
| Period                 | t <sub>period</sub>  | A3213   | –    | 240               | 360  | μs    |
|                        |                      | A3214, T <sub>A</sub> = 25°C, V <sub>DD</sub> = 3 V               | –    | 60                | 90   | ms    |
| Duty Cycle             | DC                   | A3213   | –    | 25                | –    | %     |
|                        |                      | A3214   | –    | 0.10              | –    | %     |
| Chopping Frequency     | f <sub>C</sub>       |   | –    | 340               | –    | kHz   |
| Supply Current         | I <sub>DD(EN)</sub>  | Chip awake (enabled)  | –    | –                 | 2.0  | mA    |
|                        | I <sub>DD(DIS)</sub> | Chip asleep (disabled)  | –    | –                 | 8.0  | μA    |
|                        | I <sub>DD(AVG)</sub> | A3213   | –    | 460               | 850  | μA    |
| A3214                  |                      | –   | 11   | 22                | μA   |       |

<sup>1</sup>Typical Data is at T<sub>A</sub> = 25°C and V<sub>DD</sub> = 3.0 V and is for design information only.

<sup>2</sup>Operate and release points will vary with supply voltage. B<sub>OPx</sub> = operate point (output turns ON); B<sub>RPx</sub> = release point (output turns OFF).

## MAGNETIC CHARACTERISTICS valid over operating voltage and temperature range, unless otherwise noted<sup>1</sup>

| Characteristic | Symbol <sup>2</sup> | Test Conditions                     | Min. | Typ. <sup>3</sup> | Max. | Units <sup>4</sup> |
|----------------|---------------------|-------------------------------------|------|-------------------|------|--------------------|
| Operate Points | B <sub>OPS</sub>    | South pole to branded side          | –    | 42                | 70   | G                  |
|                | B <sub>OPN</sub>    | North pole to branded side          | –70  | –48               | –    | G                  |
| Release Points | B <sub>RPS</sub>    | South pole to branded side          | 10   | 32                | –    | G                  |
|                | B <sub>RPN</sub>    | North pole to branded side          | –    | –38               | –10  | G                  |
| Hysteresis     | B <sub>hys</sub>    | B <sub>OPx</sub> - B <sub>RPx</sub> | –    | 10                | –    | G                  |

<sup>1</sup>As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.

<sup>2</sup>B<sub>OPx</sub> = operate point (output turns ON); B<sub>RPx</sub> = release point (output turns OFF).

<sup>3</sup>Typical Data is at T<sub>A</sub> = 25°C and V<sub>DD</sub> = 3.0 V and is for design information only.

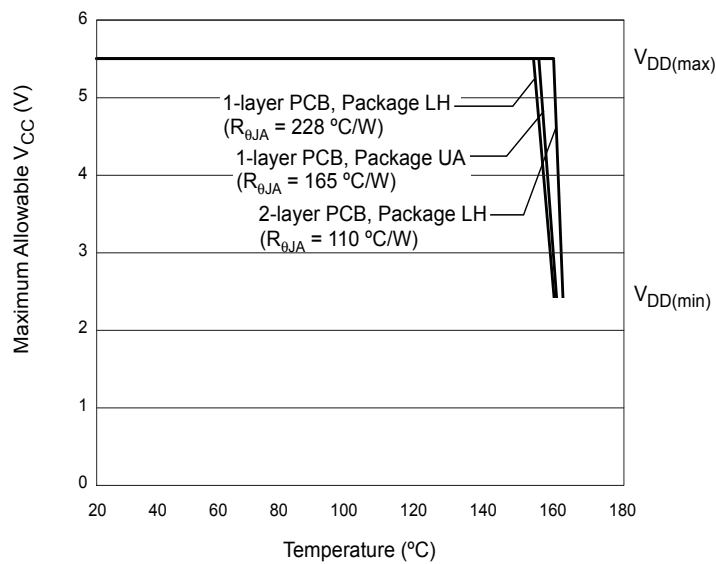
<sup>4</sup>1 gauss (G) is exactly equal to 0.1 millitesla (mT).

Thermal characteristics may require derating at maximum conditions, see application information

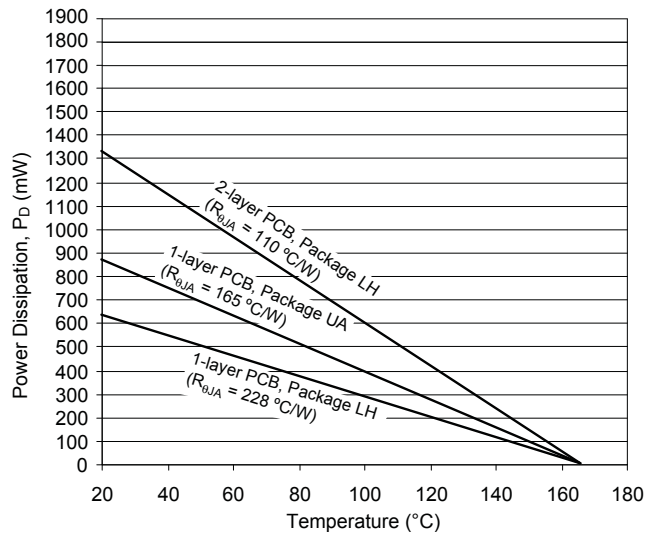
| Characteristic             | Symbol          | Test Conditions*   | Value | Units                       |
|----------------------------|-----------------|--|-------|-----------------------------|
| Package Thermal Resistance | $R_{\theta JA}$ | Package LH, 1-layer PCB with copper limited to solder pads   | 228   | $^{\circ}\text{C}/\text{W}$ |
|                            |                 | Package LH, 2-layer PCB with 0.463 in. <sup>2</sup> of copper area each side connected by thermal vias | 110   | $^{\circ}\text{C}/\text{W}$ |
|                            |                 | Package UA, 1-layer PCB with copper limited to solder pads   | 165   | $^{\circ}\text{C}/\text{W}$ |

\*Additional thermal information available on Allegro website.

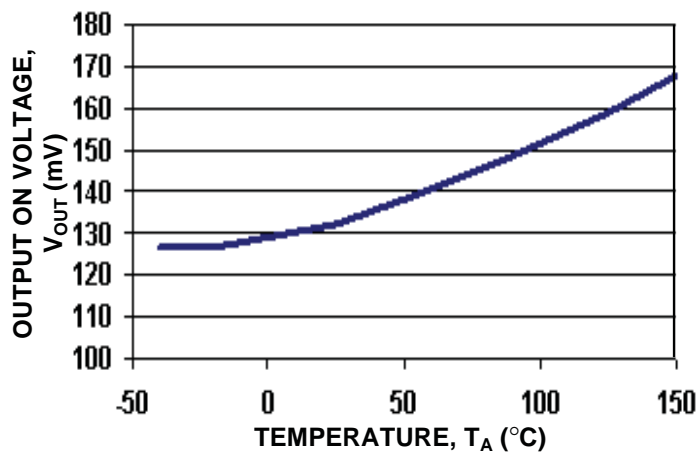
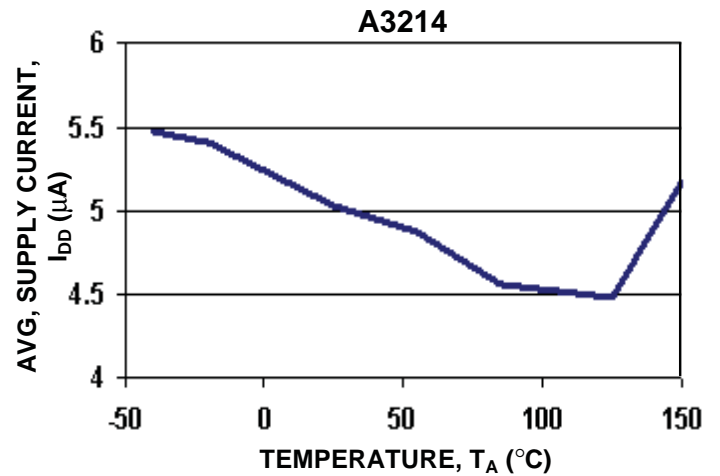
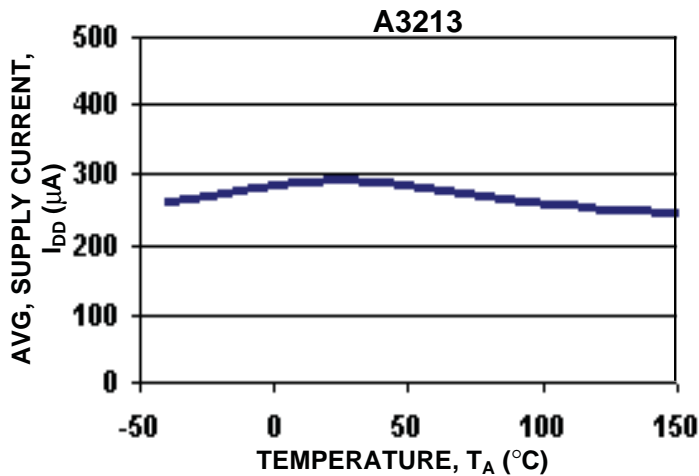
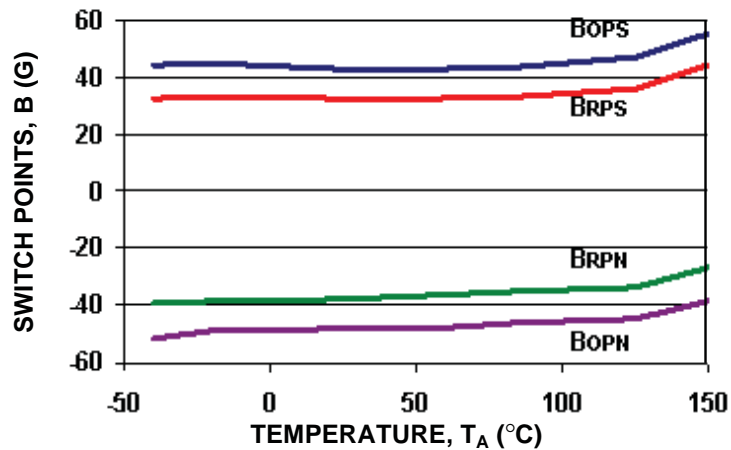
Power Derating Curve



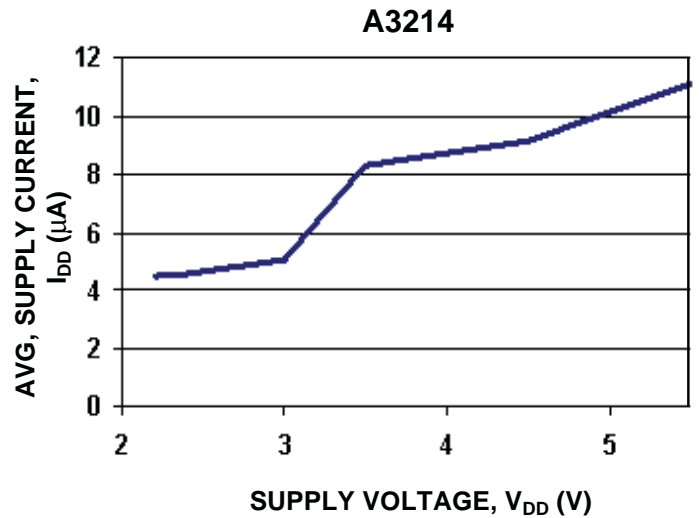
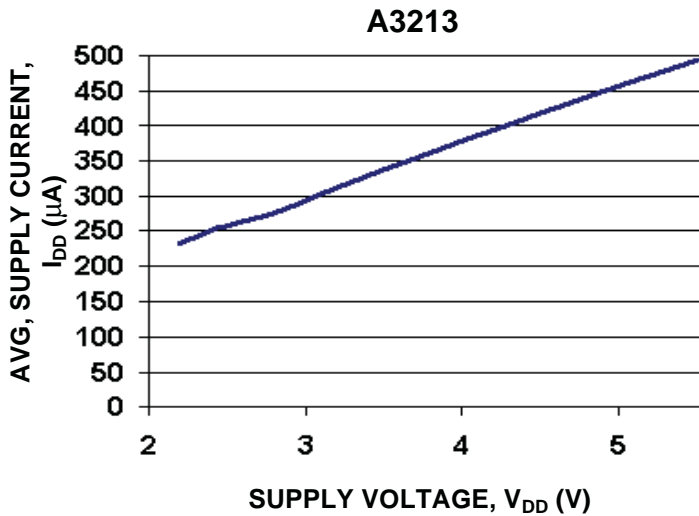
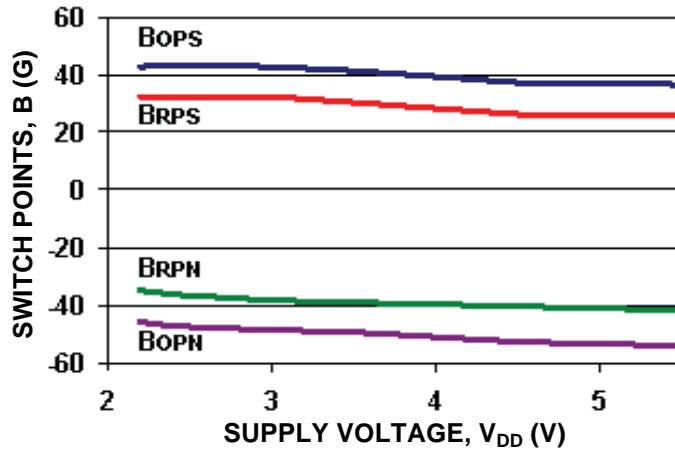
Power Dissipation versus Ambient Temperature



**TYPICAL OPERATING CHARACTERISTICS  
as a function of temperature ( $V_{DD} = 3\text{ V}$ )**

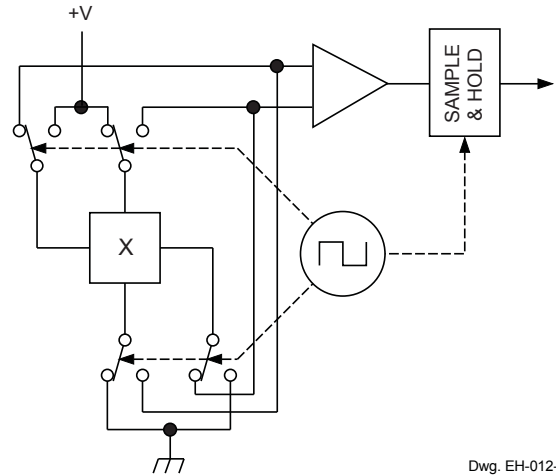
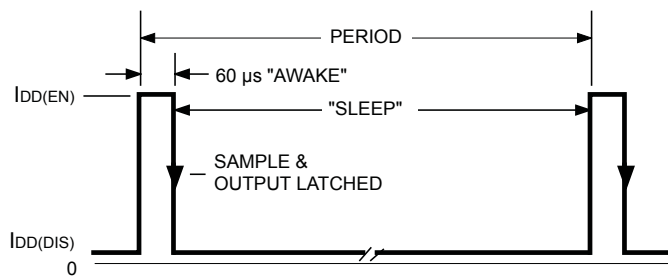


**TYPICAL OPERATING CHARACTERISTICS  
as a function of supply voltage ( $T_A = 25^\circ\text{C}$ )**



**FUNCTIONAL DESCRIPTION**

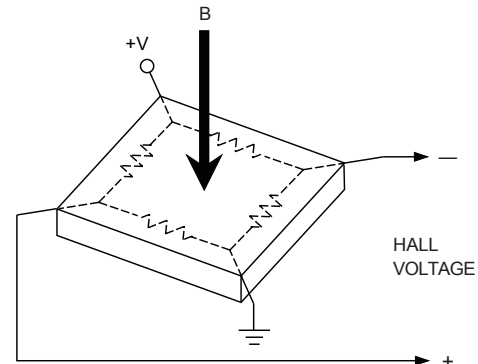
**Low Average Power.** Internal timing circuitry activates the IC for 60  $\mu$ s and deactivates it for the remainder of the period (240  $\mu$ s for the A3213 and 60 ms for the A3214). A short "awake" time allows for stabilization prior to the sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.



Dwg. EH-012-1

**Chopper-Stabilized Technique.** The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaining the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique will also slightly degrade the device output repeatability. A relatively high sampling frequency is used in order that faster signals can be processed.

More detailed descriptions of the circuit operation can be found in Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.



Dwg. AH-011-2

**Operation.** The output of this device switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point  $B_{OPS}$  (or is less than  $B_{OPN}$ ). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is  $V_{OUT(ON)}$ . When the magnetic field is reduced below the release point  $B_{RPS}$  (or increased above  $B_{RPN}$ ), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis ( $B_{hys}$ ) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.

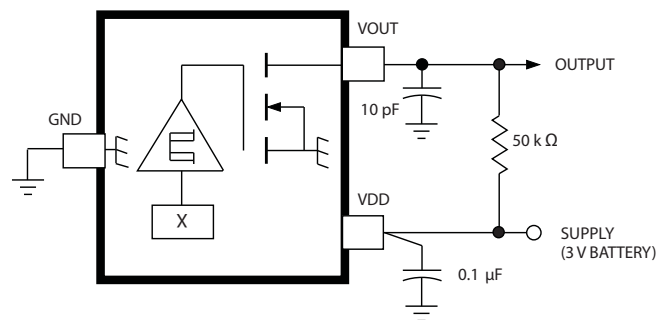
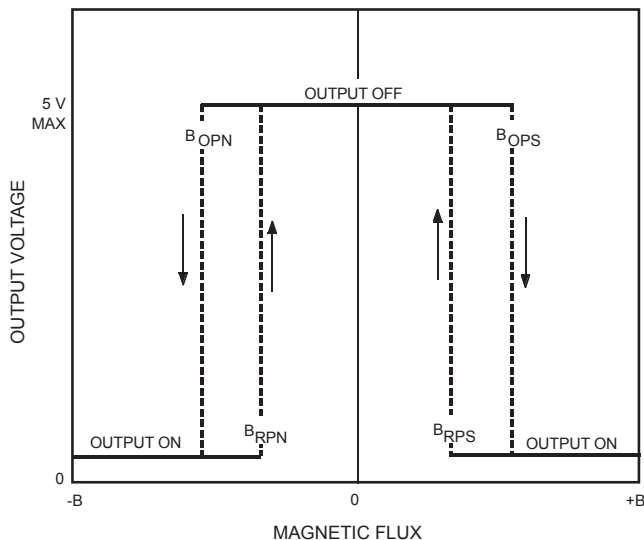


**Applications.** Allegro's pole-independent sensing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the flexibility of the device in application assembling. The state-of-the-art technology provides the same output polarity for either pole face.

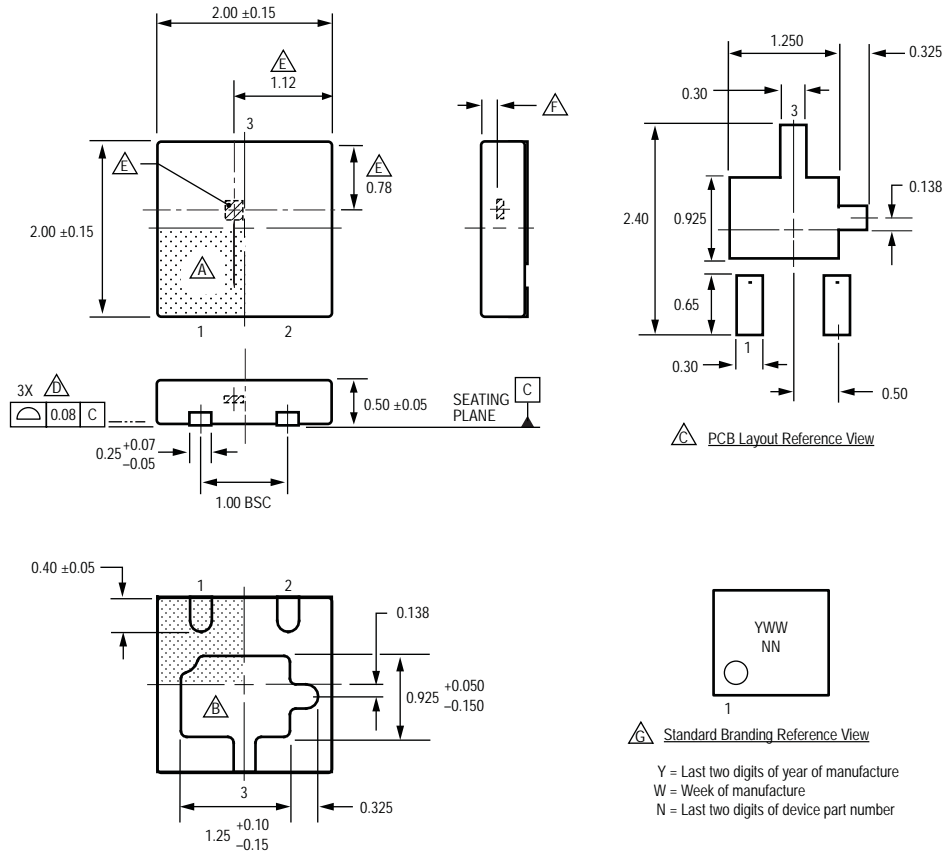
It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.

The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information on magnets and Hall-effect devices is also available in the *Allegro Electronic Data Book AMS-702* or *Application Note 27701*, or at








[www.allegromicro.com](http://www.allegromicro.com)



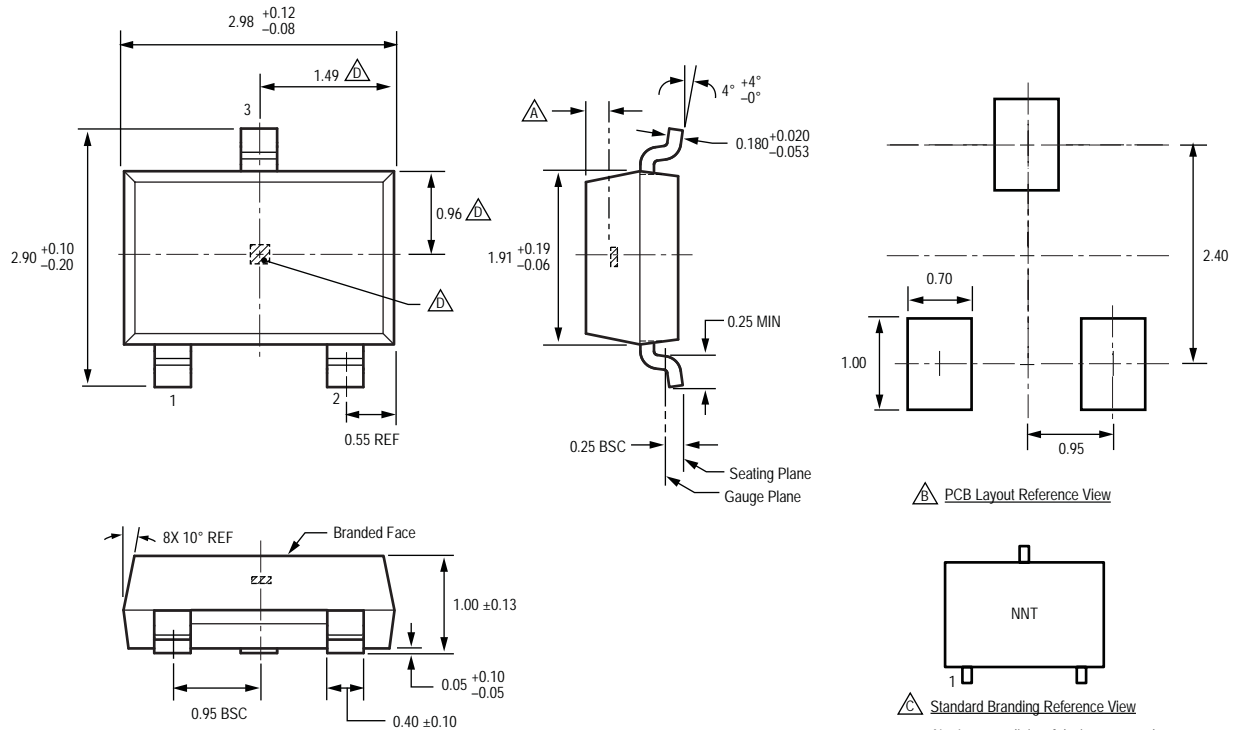
**Package EL, 3-Contact MLP/DFN**



For Reference Only, not for tooling use (reference DWG-2865;  
reference JEDEC MO-229UCCD)  
Dimensions in millimeters  
Exact case and lead configuration at supplier discretion within limits shown

-  Terminal #1 mark area
-  Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
-  Reference land pattern layout (reference IPC7351); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
-  Coplanarity includes exposed thermal pad and terminals
-  Hall Element (not to scale)
-  Active Area Depth, 0.18 mm NOM
-  Branding scale and appearance at supplier discretion

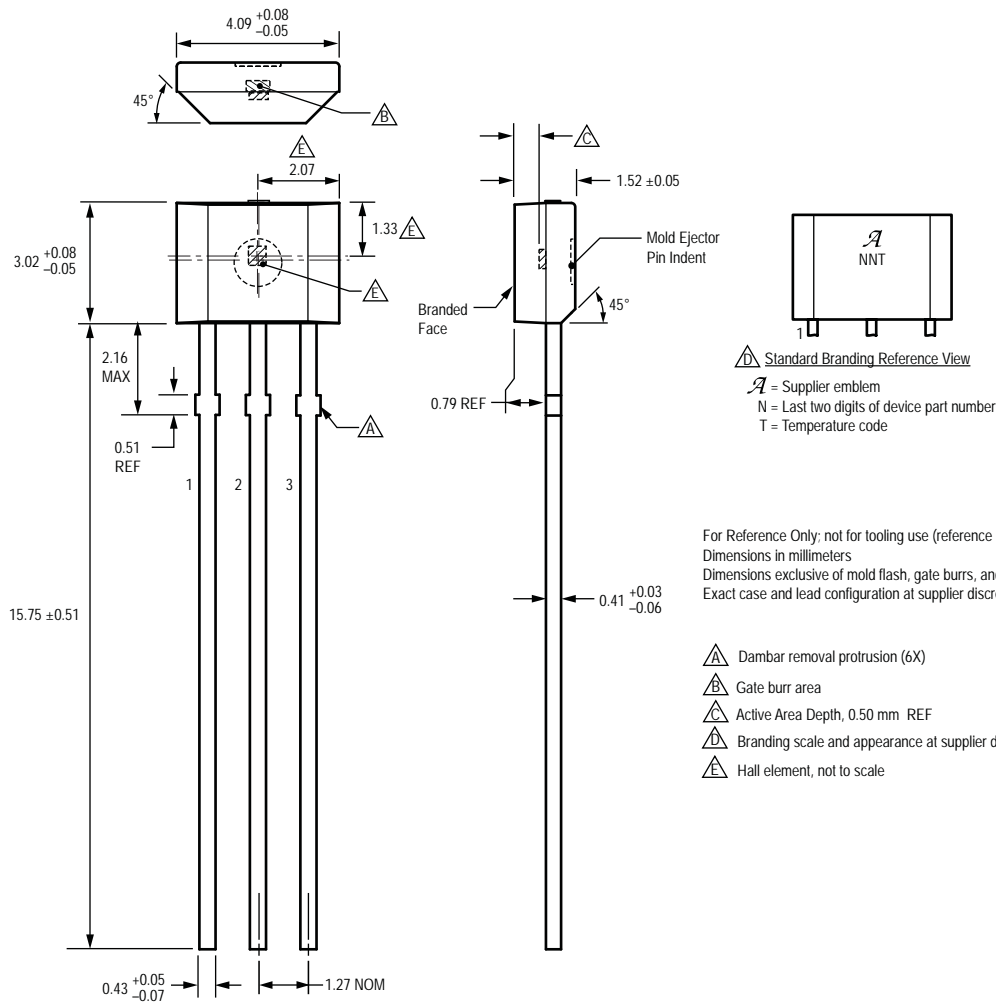
**Package LH, 3-Pin (SOT-23W)**



- For Reference Only; not for tooling use (reference dwg. 802840)  
 Dimensions in millimeters  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown
- $\triangle$  Active Area Depth, 0.28 mm REF
  - $\triangle$  Reference land pattern layout  
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances
  - $\triangle$  Branding scale and appearance at supplier discretion
  - $\triangle$  Hall element, not to scale

$\triangle$  PCB Layout Reference View  
 $\triangle$  Standard Branding Reference View  
 N = Last two digits of device part number  
 T = Temperature code

**Package UA, 3-Pin SIP**



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The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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