REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Add LCC package. Editorial changes throughout. Change code ident. no. from 14933 to 67268.	88-01-27	M. A. Frye
D	Update boilerplate to MIL-PRF-38535 requirements. Correct title to accurately reflect device function. - CFS	05-03-23	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D	D	D							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS OF SHEETS															
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
James E. Jamison

CHECKED BY
D. A. DiCenzo

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
83-04-07

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, MICROPROCESSOR PERIPHERAL COUNTER/TIMER, PARALLEL INPUT/OUTPUT N-CHANNEL, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**83001**

SHEET 1 OF 27

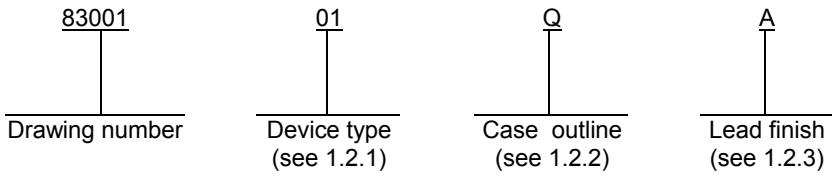
DSCC FORM 2233
APR 97

5962-E207-05

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	Z8536/Z0853604	4 MHz	Counter timer and parallel input/output peripheral unit
02	Z8536A/Z0853606	6 MHz	Counter timer and parallel input/output peripheral unit

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
Y	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) ..... -0.3 V dc to +7.0 V dc 1/
Voltage on any pin ..... -0.3 V dc to V_{CC} + 0.3 V dc 1/
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) at -55°C ..... 1.2 W
Maximum power dissipation (P_D) at +125°C..... 0.60 W
Lead temperature (soldering, 10 seconds) ..... +270°C
Maximum junction temperature (T_J) at T_C = +125°C ..... +170°C
Thermal resistance, junction-to-case (θ_{JC}):
Cases Q and Y..... See MIL-STD-1835

1/ Voltages are referenced to ground.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}) ..... 2.4 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Frequency of operation:
  Device type 01 ..... 0.5 to 4.0 MHz
  Device type 02 ..... 0.5 to 6.0 MHz
Case operating temperature range (T_C) ..... -55°C to +125°C
Maximum clock rise time ..... 20 ns
Maximum clock fall time ..... 20 ns

Timing parameter	Reference number 1/	Minimum	Maximum	Units
Trigger input to PCLK setup time (timer mode) 2/	71	150		ns
Trigger input to counter input setup time (counter mode) 2/	72	150		ns
Trigger input pulse width (high or low)	73	200		ns
Gate input to PCLK setup time (timer mode) 2/	74	100		ns
Gate input to counter input setup time (counter mode) 2/	75	100		ns
Gate input to PCLK hold time (timer mode) 2/	76	100		ns
Gate input to counter input hold time (counter mode) 2/	77	100		ns
PCLK to counter output delay (timer mode)	78		475	ns
Counter input to counter output delay (counter mode)	79		475	ns

1/ The reference number refers to the identified parameter on figure 3 for device type 01 only.

2/ These parameters must be met to guarantee trigger or gate are valid for the next counter/timer cycle.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic functions. The logic functions shall be as specified on figure 2.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		All	1, 2, 3	2.2	V_{CC} + 0.3 1/	V
Low level input voltage	V_{IL}				-0.3 1/	0.8	
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.4	
High level output voltage	V_{OH}	I_{OH} = -250 µA			2.4		
Power supply current	I_{CC}	V_{CC} = 5.5 V Outputs open	All	1, 2, 3		200	mA
Input capacitance	C_{IN}		All	4		10 1/	pF
Output capacitance	C_{OUT}					15 1/	
Bidirectional capacitance	$C_{I/O}$					20 1/	
Output leakage current low, open drain outputs	I_{LOL}	$0.4\ V \le V_{OUT} \le 2.4\ V$	All	1, 2, 3	-10	+10	µA
Output leakage current high, open drain outputs	I_{LOH}				-10	+10	
Input low current (input and bidirectional)	I_{IL}	$0.4\ V \le V_{IN} \le 2.4\ V$			-10	+10	
Input high current (input and bidirectional)	I_{IH}				-10	+10	
Maximum frequency 1/	f_{MAX}		01	9, 10, 11	4.0		MHz
			02		6.0		
Functional tests	I_{CEX}	See paragraph 4.3.1c.	All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
PCLK cycle time	t_{CYC1}	Reference number 1. 2/ 3/ 4/	01	9, 10, 11	250	4000	ns
			02		165	4000	
PCLK width high 1/	t_{PWH1}	Reference number 2. 2/ 3/ 4/	01	9, 10, 11	105	2000	ns
			02		70	2000	
PCLK width low 1/	t_{PWL1}	Reference number 3. 2/ 3/ 4/	01	9, 10, 11	105	2000	ns
			02		70	2000	
PCLK rise time 1/	t_{RC1}	Reference number 4. 2/ 3/ 4/	01	9, 10, 11		20	ns
			02			10	
PCLK fall time 1/	t_{FC1}	Reference number 5. 2/ 3/ 4/	01	9, 10, 11		20	ns
			02			15	
$\overline{\text{INTACK}}$ to PCLK setup time 1/	t_{SHL1}, t_{SLH1}	Reference number 6. 2/ 3/ 4/	All	9, 10, 11	100		ns
$\overline{\text{INTACK}}$ to PCLK hold time 1/	t_{HHL1}, t_{HLH1}	Reference number 7. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{\text{INTACK}}$ to $\overline{\text{RD}}$ setup time 1/	t_{SHL2}, t_{SLH2}	Reference number 8. 2/ 3/ 4/	All	9, 10, 11	200		ns
$\overline{\text{INTACK}}$ to $\overline{\text{RD}}$ hold time 1/	t_{HHL2}, t_{HLH2}	Reference number 9. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{\text{INTACK}}$ to $\overline{\text{WR}}$ setup time 1/	t_{SHL3}, t_{SLH3}	Reference number 10. 2/ 3/ 4/	All	9, 10, 11	200		ns
$\overline{\text{INTACK}}$ to $\overline{\text{WR}}\uparrow$ hold time 1/	t_{HHL3}, t_{HLH3}	Reference number 11. 2/ 3/ 4/	All	9, 10, 11	0		ns
Address to $\overline{\text{RD}}\downarrow$ setup time	t_{SHL4}, t_{SLH4}	Reference number 12. 2/ 3/ 4/	All	9, 10, 11	80		ns
Address to $\overline{\text{RD}}\uparrow$ hold time 1/	t_{HHL4}, t_{HLH4}	Reference number 13. 2/ 3/ 4/	All	9, 10, 11	0		ns
Address to $\overline{\text{WR}}\downarrow$ setup time	t_{SHL5}, t_{SLH5}	Reference number 14. 2/ 3/ 4/	All	9, 10, 11	80		ns
Address to $\overline{\text{WR}}\uparrow$ hold time 1/	t_{HHL5}, t_{HLH5}	Reference number 15. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{\text{CE}}$ low to $\overline{\text{RD}}\downarrow$ setup time 5/	t_{SHL6}	Reference number 16. 2/ 3/ 4/	All	9, 10, 11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
$\overline{CE}$ high to $\overline{RD}\downarrow$ setup time 1/ 5/	t_{SLH7}	Reference number 17. 2/ 3/ 4/	01	9, 10, 11	100		ns
			02		70		
$\overline{CE}$ to $\overline{RD}\uparrow$ hold time 5/	t_{HHL6}, t_{HLH6}	Reference number 18. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{CE}$ low to $\overline{WR}\downarrow$ setup time	t_{SHL8}	Reference number 19. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{CE}$ high to $\overline{WR}\downarrow$ setup time 1/	t_{SLH9}	Reference number 20. 2/ 3/ 4/	01	9, 10, 11	100		ns
			02		70		
$\overline{CE}$ to $\overline{WR}\uparrow$ hold time	t_{HHL7}, t_{HLH7}	Reference number 21. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{RD}$ to low width 1/ 5/	t_{PWL2}	Reference number 22. 2/ 3/ 4/	01	9, 10, 11	390		ns
			02		250		
$\overline{RD}\downarrow$ to read data active delay 1/	t_{PHL1}, t_{PLH1}	Reference number 23. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{RD}\downarrow$ to read data valid delay 1/	t_{PHL2}, t_{PLH2}	Reference number 24. 2/ 3/ 4/	01	9, 10, 11		255	ns
			02			180	
$\overline{RD}\uparrow$ to read data not valid delay 1/	t_{PHL3}, t_{PLH3}	Reference number 25. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{RD}\uparrow$ to read data float delay 6/	t_{PHZ1}, t_{PZH1}	Reference number 26. 2/ 3/ 4/	01	9, 10, 11		70	ns
			02			45	
$\overline{WR}$ low width 1/	t_{PWL3}	Reference number 27. 2/ 3/ 4/	01	9, 10, 11	390		ns
			02		250		
Write data to $\overline{WR}\downarrow$ setup time 1/	t_{SHL10}, t_{SLH10}	Reference number 28. 2/ 3/ 4/	All	9, 10, 11	0		ns
Write data to $\overline{WR}\uparrow$ hold time 1/	t_{HHL8}, t_{HLH8}	Reference number 29. 2/ 3/ 4/	All	9, 10, 11	0		ns
Valid access recovery time 1/ 7/	t_{CYC2}	Reference number 30. 2/ 3/ 4/	01	9, 10, 11	1000		ns
			02		650		
Pattern match to $\overline{INT}$ delay (bit port) 1/	t_{PHL4}	Reference number 31. 2/ 3/ 4/	All	9, 10, 11		$2*(t_{CYC1}) + 800$	ns
$\overline{ACKIN}$ to $\overline{INT}$ delay (port with handshake) 1/ 8/	t_{PHL5}	Reference number 32. 2/ 3/ 4/	All	9, 10, 11		$10*(t_{CYC1}) + 600$	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Counter input to $\overline{INT}$ delay (counter mode) 1/	t_{PHL6}	Reference number 33. 2/ 3/ 4/	All	9, 10, 11		$2*(t_{CYC1}) + 700$	ns
PCLK to $\overline{INT}$ delay (timer mode) 1/	t_{PHL7}	Reference number 34. 2/ 3/ 4/	All	9, 10, 11		$3*(t_{CYC1}) + 700$	ns
$\overline{INTACK}$ to $\overline{RD}\downarrow$ (acknowledge setup time) 1/ 9/	t_{SHL11}, t_{SLH11}	Reference number 35. 2/ 3/ 4/	01	9, 10, 11	350		ns
			02		250		
$\overline{RD}$ acknowledge width 1/	t_{PWL4}	Reference number 36. 2/ 3/ 4/	01	9, 10, 11	350		ns
			02		250		
$\overline{RD}\downarrow$ (acknowledge) to read data valid delay 1/	t_{PHL8}, t_{PLH8}	Reference number 37. 2/ 3/ 4/	01	9, 10, 11		250	ns
			02			180	
$\overline{INTACK}\downarrow$ to IEO$\downarrow$ delay 1/ 9/	t_{PHL9}	Reference number 38. 2/ 3/ 4/	01	9, 10, 11		350	ns
			02			250	
IEI to IEO delay 1/ 9/	t_{PHL10}	Reference number 39. 2/ 3/ 4/	01	9, 10, 11		150	ns
			02			100	
IEI to $\overline{RD}\downarrow$ (acknowledge) setup time 1/ 9/	t_{SHL12}, t_{SLH12}	Reference number 40. 2/ 3/ 4/	01	9, 10, 11	100		ns
			02		70		
IEI to $\overline{RD}\uparrow$ (acknowledge) hold time 1/	t_{HHL9}, t_{HLH9}	Reference number 41. 2/ 3/ 4/	01	9, 10, 11	100		ns
			02		70		
$\overline{RD}\downarrow$ (acknowledge) to $\overline{INT}$ delay 1/	t_{PHL11}	Reference number 42. 2/ 3/ 4/	All	9, 10, 11		600	ns
Data input to $\overline{ACKIN}\downarrow$ setup time 1/	t_{SHL13}, t_{SLH13}	Reference number 43. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{ACKIN}\downarrow$ to RFD$\downarrow$ delay 1/	t_{PHL12}	Reference number 45. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{RFD}\uparrow$ to ACKIN$\downarrow$ delay 1/	t_{HHL10}	Reference number 48. 2/ 3/ 4/	All	9, 10, 11	0		ns
Data out to $\overline{DAV}\downarrow$ setup time 1/ 10/	t_{PHL13}, t_{PLH13}	Reference number 49. 2/ 3/ 4/	01	9, 10, 11	25		ns
			02		20		
$\overline{DAV}\downarrow$ to $\overline{ACKIN}\downarrow$ delay 1/	t_{SHL14}	Reference number 50. 2/ 3/ 4/	All	9, 10, 11	0		ns
Data out to $\overline{ACKIN}\downarrow$ hold time 1/	t_{HHL11}, t_{HLH11}	Reference number 51. 2/ 3/ 4/	All	9, 10, 11	$2*(t_{CYC1})$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
$\overline{ACKIN}\downarrow$ to $\overline{DAV}\uparrow$ delay 1/	t_{PLH14}	Reference number 52. 2/ 3/ 4/	All	9, 10, 11	$2*(t_{CYC1})$		ns
RFD↓ to ACKIN↑ delay (interlocked handshake) 1/	t_{HLH12}	Reference number 54. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{ACKIN}\uparrow$ ($\overline{DAV}$)↑ to RFD↑ delay (interlocked and three wire handshake) 1/	t_{PLH15}	Reference number 55. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{DAV}\uparrow$ $\overline{ACKIN}\uparrow$ to ($\overline{RFD}$)↑ (interlocked and three wire handshake) 1/	t_{HLH13}	Reference number 56. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{ACKIN}\uparrow$ ($\overline{RFD}$)↑ to $\overline{DAV}\downarrow$ delay (interlocked and three wire handshake) 1/	t_{PLH16}	Reference number 57. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{DAV}\downarrow$to DAC↑ delay (input three wire handshake) 1/	t_{PLH17}	Reference number 58. 2/ 3/ 4/	All	9, 10, 11	0		ns
Data input to DAC↑ hold time (three wire handshake) 1/	t_{HHL14}, t_{HLH14}	Reference number 59. 2/ 3/ 4/	All	9, 10, 11	0		ns
DAC↑ to $\overline{DAV}\downarrow$ delay (input three wire handshake) 1/	t_{HLH15}	Reference number 60. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{DAV}\uparrow$ to DAC↓ delay (input three wire handshake) 1/	t_{PHL18}	Reference number 61. 2/ 3/ 4/	All	9, 10, 11	0		ns
$\overline{DAV}\downarrow$ to DAC↑ delay (output three wire handshake) 1/	t_{SLH15}	Reference number 62. 2/ 3/ 4/	All	9, 10, 11	0		ns
Data output to DAC↑ hold time (three wire handshake) 1/	t_{PHL19}, t_{PLH19}	Reference number 63. 2/ 3/ 4/	All	9, 10, 11	$2*(t_{CYC1})$		ns
DAC↑ to $\overline{DAV}\uparrow$ delay (output three wire handshake) 1/	t_{PHL20}	Reference number 64. 2/ 3/ 4/	All	9, 10, 11	$2*(t_{CYC1})$		ns
DAV↑ to $\overline{DAC}\downarrow$ delay (output three wire handshake) 1/	t_{HHL16}	Reference number 65. 2/ 3/ 4/	All	9, 10, 11	0		ns
Counter input cycle time 1/	t_{CYC3}	Reference number 66. 2/ 3/ 4/	01	9, 10, 11	500		ns
			02		330		
Counter input high width 1/	t_{PWH5}	Reference number 67. 2/ 3/ 4/	01	9, 10, 11	230		ns
			02		150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Counter input low width 1/	t_{PWL5}	Reference number 68. 2/ 3/ 4/	01	9, 10, 11	230		ns
			02		150		
Counter input fall time 1/	t_{FC2}	Reference number 69. 2/ 3/ 4/	01	9, 10, 11		20	ns
			02			15	
Counter input rise time 1/	t_{RC2}	Reference number 70. 2/ 3/ 4/	01	9, 10, 11		20	ns
			02			15	
$\overline{RD}\downarrow$ to REQ↓ delay	t_{PHL21}	Reference number 80. 2/ 3/ 4/	01	9, 10, 11		500	ns
$\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$ delay	t_{PHL22}	Reference number 81. 2/ 3/ 4/	01	9, 10, 11		500	ns
$\overline{WR}\downarrow$ to REQ↓ delay	t_{PHL23}	Reference number 82. 2/ 3/ 4/	01	9, 10, 11		500	ns
$\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$ delay	t_{PHL24}	Reference number 83. 2/ 3/ 4/	01	9, 10, 11		500	ns
PCLK↓ to REQ↑ delay	t_{PHL25}	Reference number 84. 2/ 3/ 4/	01	9, 10, 11		300	ns
PCLK↓ to $\overline{WAIT}\uparrow$ delay	t_{PHL26}	Reference number 85. 2/ 3/ 4/	01	9, 10, 11		300	ns
$\overline{ACKIN}\downarrow$ to REQ↑ delay 8/	t_{PHL27}	Reference number 86. 2/ 3/ 4/	01	9, 10, 11		$8*(t_{CYC1}) + 1000$	ns
$\overline{ACKIN}\downarrow$ to $\overline{WAIT}\uparrow$ delay 8/	t_{PHL28}	Reference number 87. 2/ 3/ 4/	01	9, 10, 11		$10*(t_{CYC1}) + 600$	ns
Delay from $\overline{RD}\uparrow$ to $\overline{WR}\downarrow$ for no reset 1/	t_{SHL16}	Reference number 88. 2/ 3/ 4/	All	9, 10, 11	50		ns
Delay from $\overline{WR}\uparrow$ to $\overline{RD}\downarrow$ for no reset 1/	t_{SHL17}	Reference number 89. 2/ 3/ 4/	All	9, 10, 11	50		ns
Width of $\overline{RD}$ and $\overline{WR}$ low to insure reset	t_{PWL6}	Reference number 90. 2/ 3/ 4/	All	9, 10, 11	250		ns
Any input rise time not otherwise specified 1/	t_{RI1}	Reference number 91. 2/ 3/ 4/	All	9, 10, 11		100	ns
Any input fall time not otherwise specified 1/	t_{FI1}	Reference number 92. 2/ 3/ 4/	All	9, 10, 11		100	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
1's catcher high width 1/ 11/	t_{PWH7}	Reference number 93. 2/ 3/ 4/	01	9, 10, 11	250		ns
			02		170		
Pattern match input valid (bit port) 1/	t_{PWL8}, t_{PWH8}	Reference number 94. 2/ 3/ 4/	01	9, 10, 11	750		ns
			02		500		
Data latched on pattern match setup time (bit port) 1/	t_{SHL18}, t_{SLH18}	Reference number 95. 2/ 3/ 4/	All	9, 10, 11	0		ns
Data latched on pattern match hold time (bit port) 1/	t_{HHL17}, t_{HLH17}	Reference number 96. 2/ 3/ 4/	01	9, 10, 11	1000		ns
			02		650		

1/ Guaranteed if not tested.

2/ The reference number refers to the parameter being measured on figure 3.

3/ See figure 3.

4/ C_L = 50 pF ±10%.

5/ Parameter does not apply to Interrupt Acknowledge transactions.

6/ Float delay is measured to the time when the output has changed 0.5 V with minimum ac load and maximum dc load.

7/ t_{CYC2} is 1 μs or t_{CYC1}, whichever is longer.

8/ The delay is from $\overline{DAV}\downarrow$ for three-wire input handshake. The delay is from DAC↑ for three-wire output handshake.

9/ The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}\downarrow$ to RD↓ must be greater than the sum of tdIA(EIO) for the highest priority peripheral, tsIEI(RDA) for the lowest priority peripheral, and tdIEI(IEO) for each peripheral separating them in the chain.

10/ This time can be extended through the use of deskew timers.

11/ If the input is programmed inverting, a low-going pulse of the same width will be detected.

Device types:	01 and 02		
Case outline:	Q		
Terminal number	Terminal name	Terminal number	Terminal name
1	D_4	21	PC_2
2	D_5	22	PC_3
3	D_6	23	+5 V
4	D_7	24	$\overline{INT}$
5	$\overline{RD}$	25	$\overline{INTACK}$
6	$\overline{WR}$	26	PA_7
7	GND	27	PA_6
8	PB_0	28	PA_5
9	PB_1	29	PA_4
10	PB_2	30	PA_3
11	PB_3	31	PA_2
12	PB_4	32	PA_1
13	PB_5	33	PA_0
14	PB_6	34	A_0
15	PB_7	35	A_1
16	PCLK	36	$\overline{CE}$
17	IEI	37	D_0
18	IEO	38	D_1
19	PC_0	39	D_2
20	PC_1	40	D_3

FIGURE 1. Terminal connections.

Device types:	01 and 02		
Case outline:	Y		
Terminal number	Terminal name	Terminal number	Terminal name
1	D_4	23	PC_2
2	D_5	24	PC_3
3	D_6	25	+5 V
4	D_7	26	$\overline{INT}$
5	$\overline{RD}$	27	$\overline{INTACK}$
6	NC	28	NC
7	$\overline{WR}$	29	NC
8	NC	30	PA_7
9	GND	31	PA_6
10	PB_0	32	PA_5
11	PB_1	33	PA_4
12	PB_2	34	PA_3
13	PB_3	35	PA_2
14	PB_4	36	PA_1
15	PB_5	37	PA_0
16	PB_6	38	A_0
17	PB_7	39	A_1
18	PCLK	40	$\overline{CE}$
19	IEI	41	D_0
20	IEO	42	D_1
21	PC_0	43	D_2
22	PC_1	44	D_3

NC = No connection

FIGURE 1. Terminal connections - Continued.

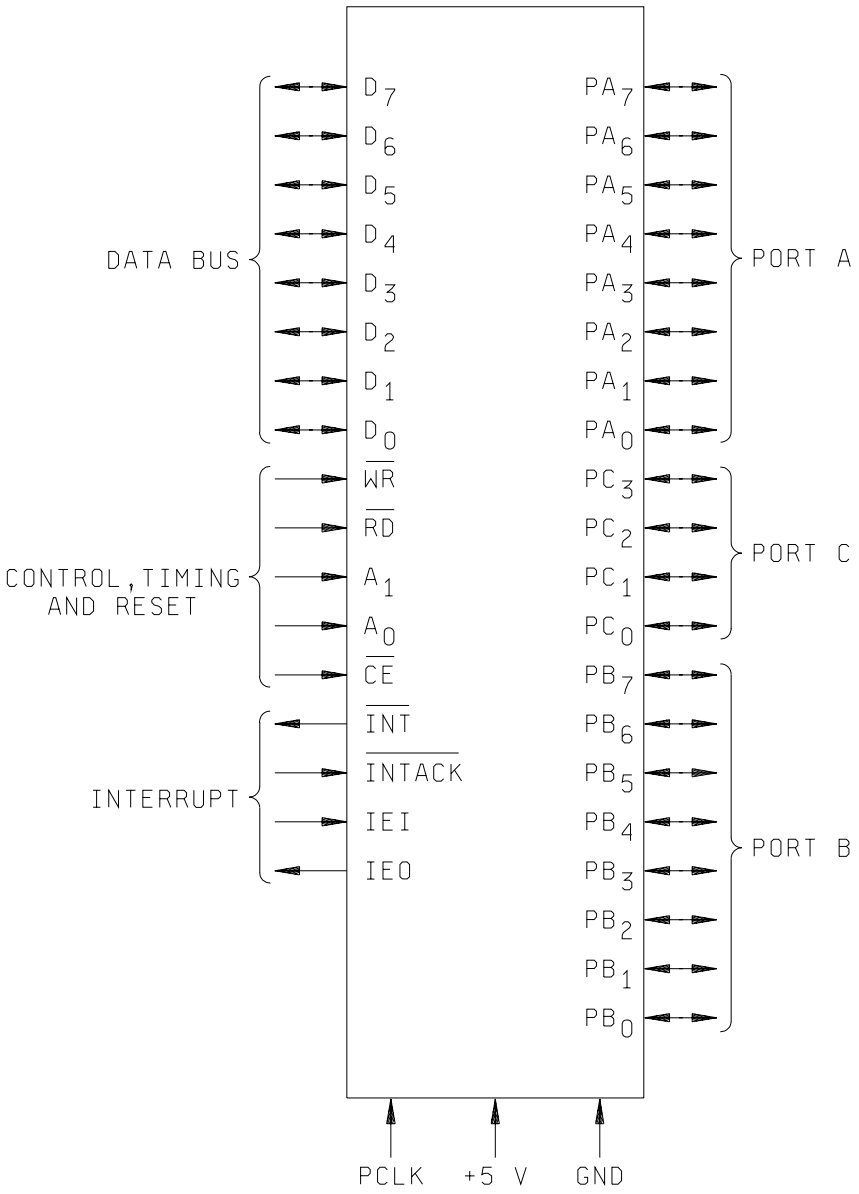
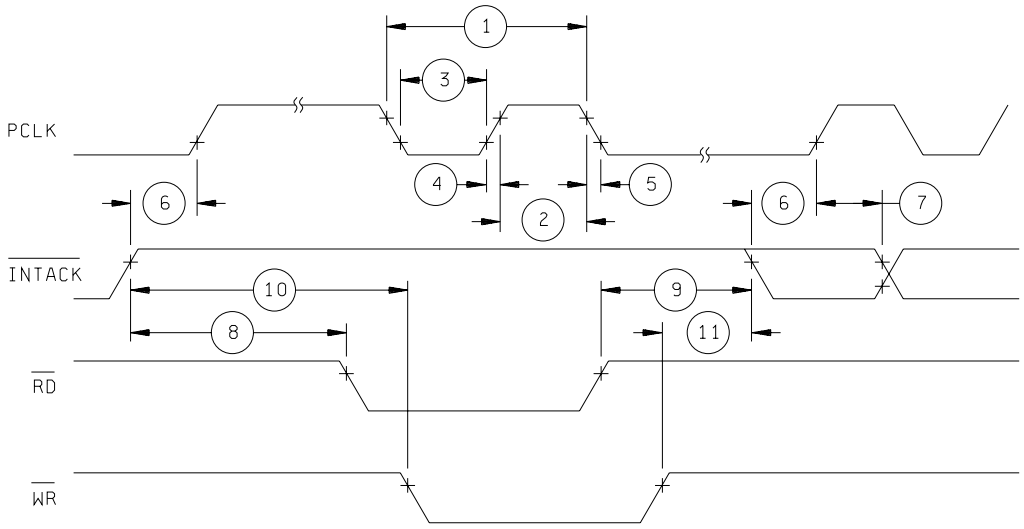
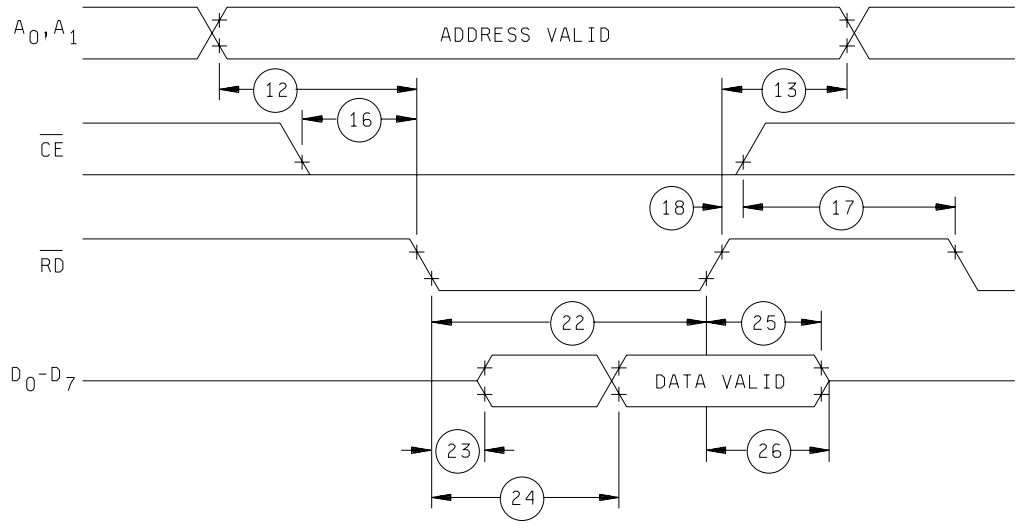


FIGURE 2. Logic functions.

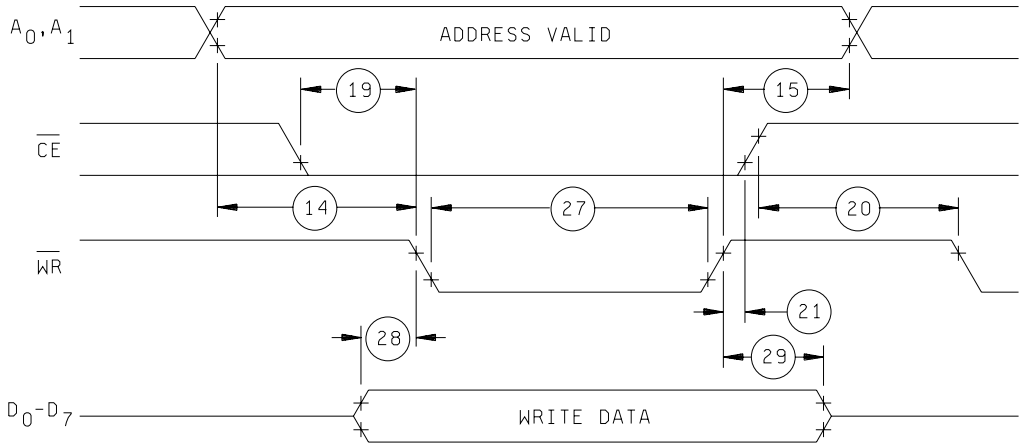


PCLK, $\overline{\text{INTACK}}$ TIMING

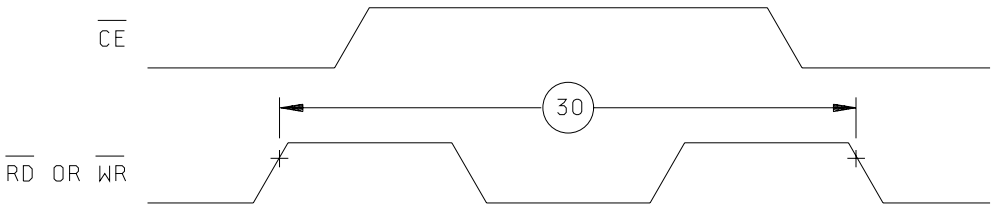


READ CYCLE TIMING

FIGURE 3. Timing waveforms.

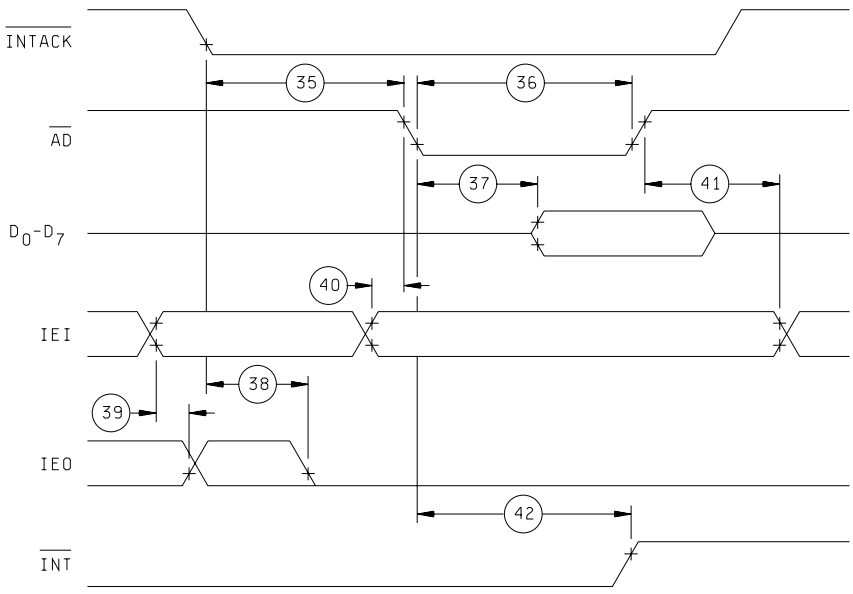


WRITE CYCLE TIMING

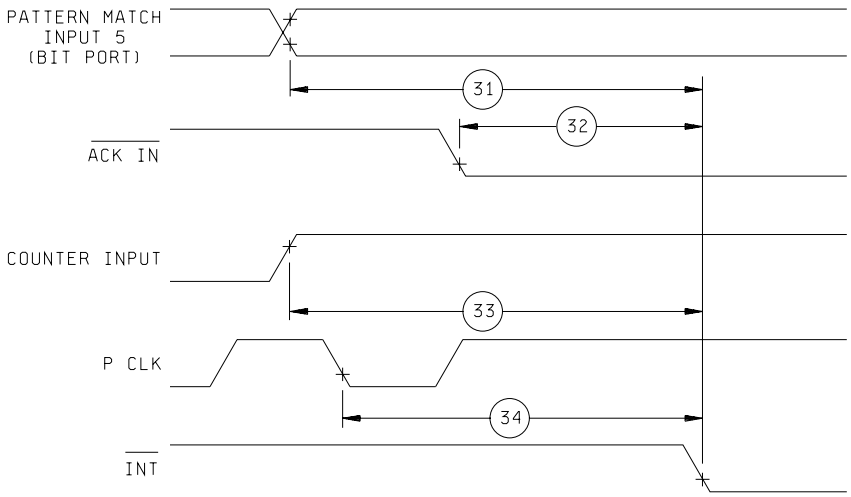


VALID ACCESS RECOVERY TIME

FIGURE 3. Timing waveforms - Continued.

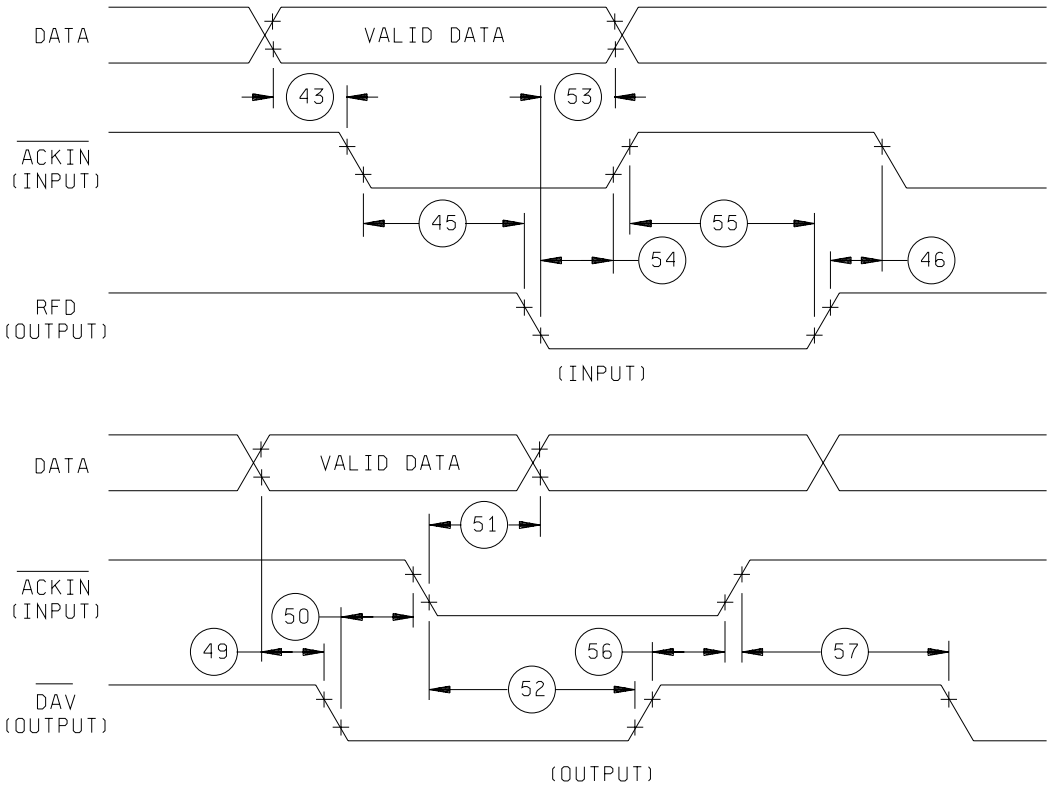


INTERRUPT ACKNOWLEDGE TIMING



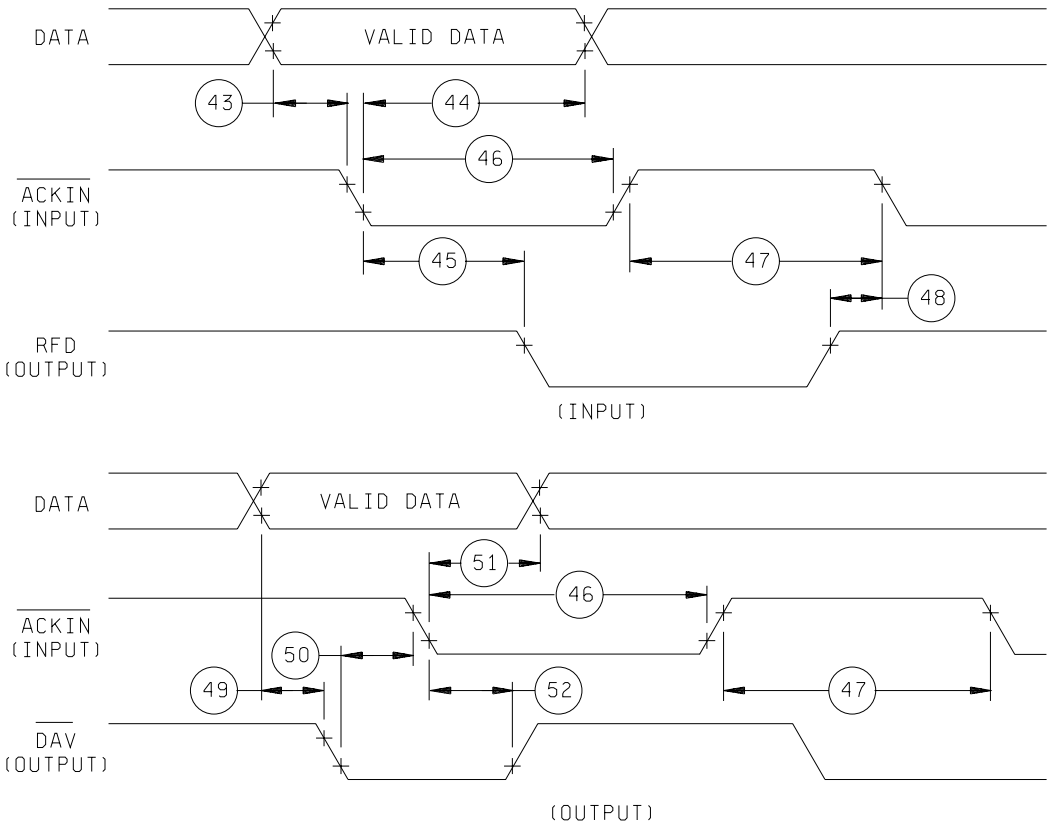
INTERRUPT TIMING

FIGURE 3. Timing waveforms - Continued.



INTERLOCK HANDSHAKE TIMING

FIGURE 3. Timing waveforms - Continued.



STROBED HANDSHAKE TIMING

FIGURE 3. Timing waveforms - Continued.

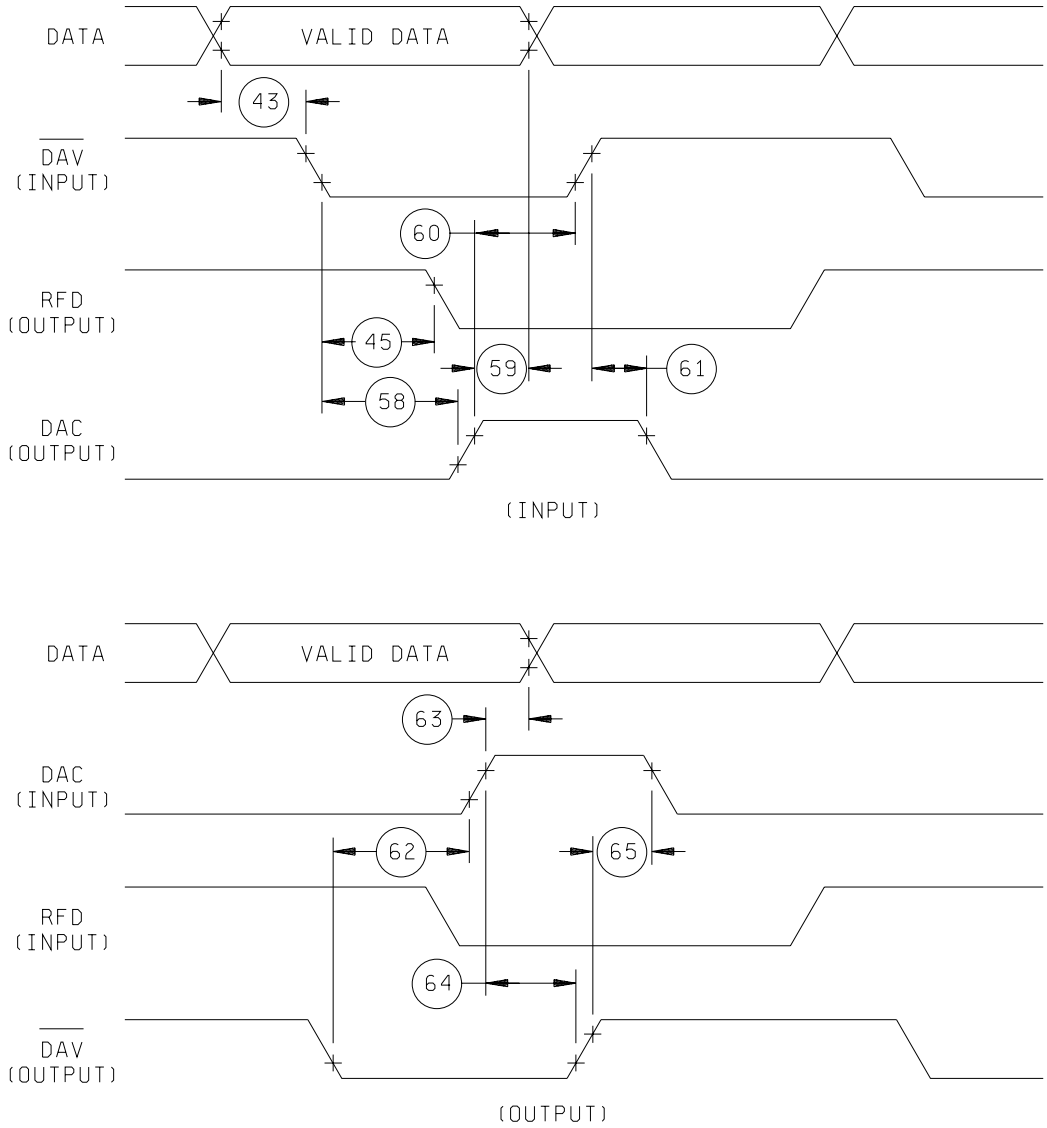
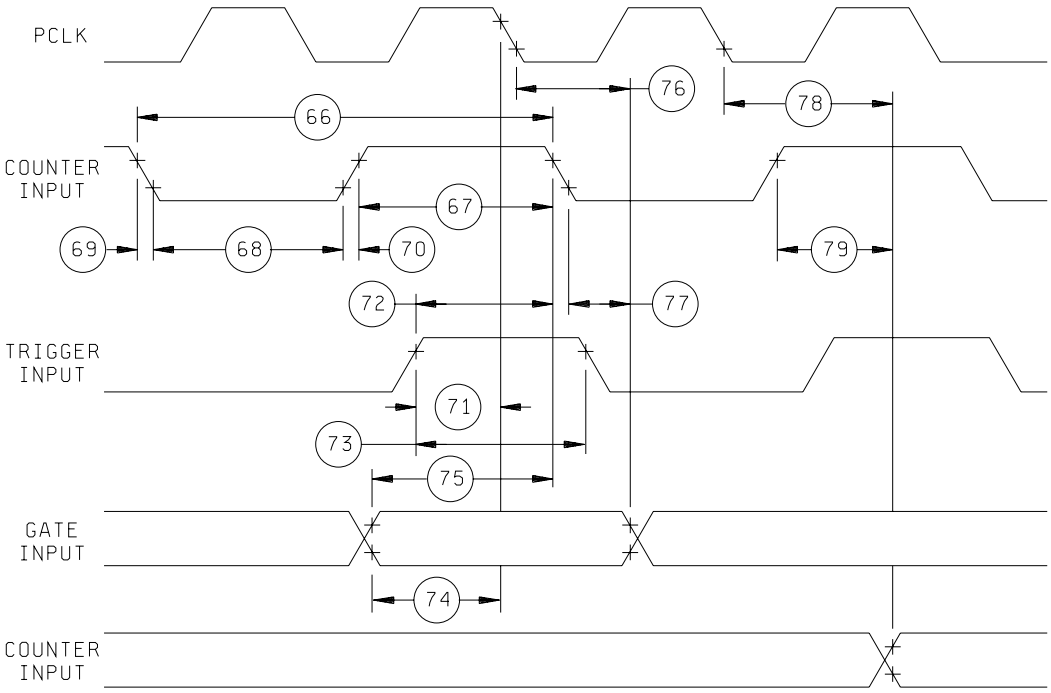
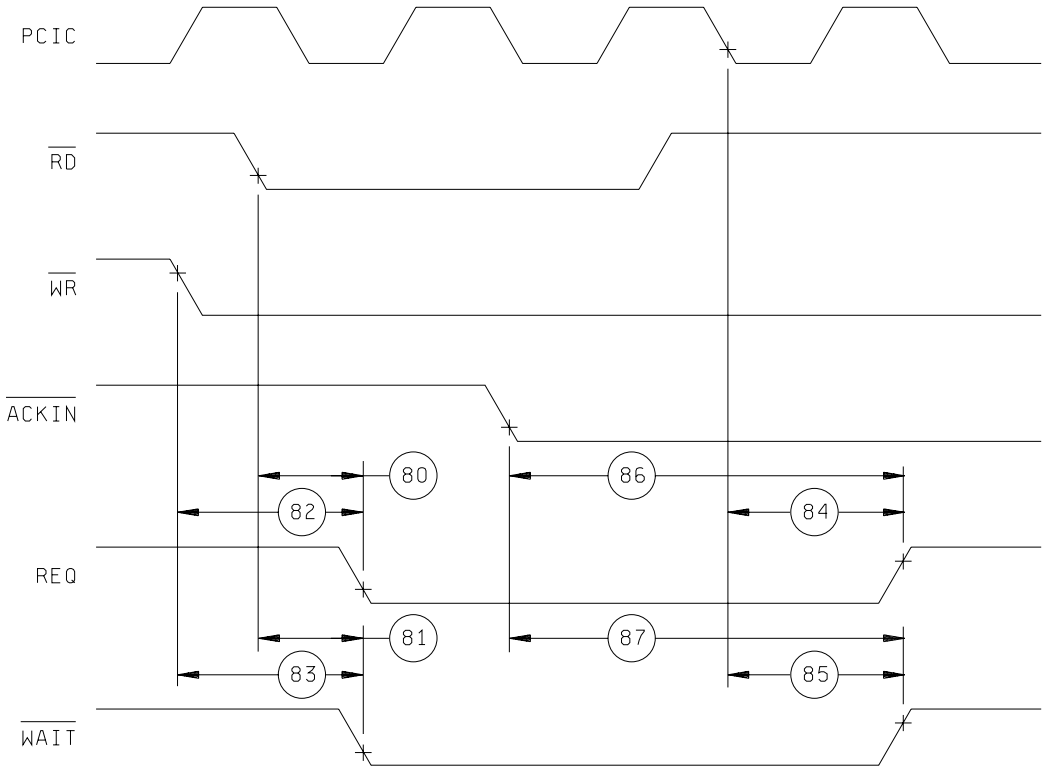


FIGURE 3. Timing waveforms - Continued.

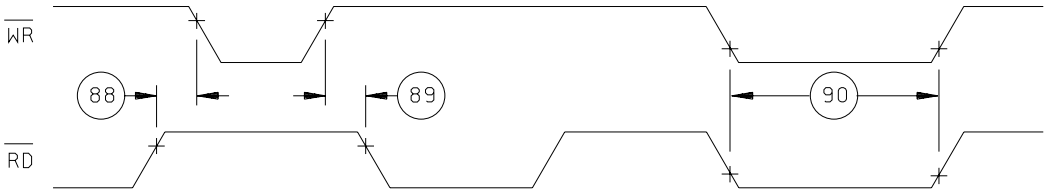


COUNTER/TIMER TIMING

FIGURE 3. Timing waveforms - Continued.

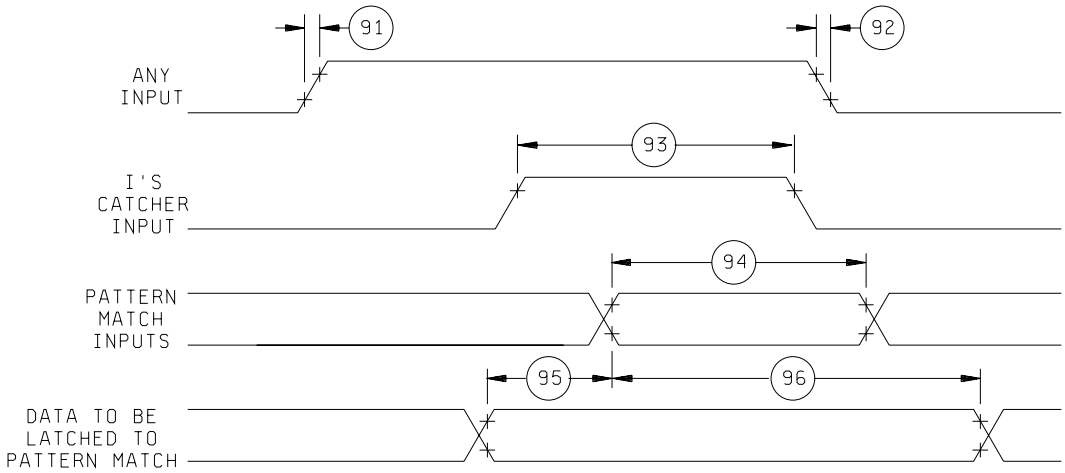


REQUEST/$\overline{\text{WAIT}}$ TIMING



RESET TIMING

FIGURE 3. Timing waveforms - Continued.



MISCELLANEOUS PORT TIMING

FIGURE 3. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 functional test shall include verification of programming set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Terminal and functional definitions. Terminal and functional definitions and descriptions for this device shall be as follows:

IEI	Interrupt enable in (input, active high). When this line is active, the CIO is able to interrupt the CPU.
IEO	Interrupt enable out (output, active high). This output is high only if IEI is high and the CPU is not servicing an interrupt from this CIO. In conjunction with IEI, this line can be used to implement a system-wide interrupt priority daisy chain.
$\overline{\text{INT}}$	Interrupt request (output, open drain, active low). This signal is pulled low when the CIO requests an interrupt.
$\overline{\text{INTACK}}$	Interrupt acknowledge (input, active low). This signal indicates to the CIO that an interrupt acknowledge cycle is in progress. $\overline{\text{INTACK}}$ must be synchronized to P clock.

PA_0-PA_7	Port A I/O lines (bidirectional, tri-state or open drain). These eight I/O lines transfer information between the CIO's port A and external devices.
PB_0-PB_7	Port B I/O lines (bidirectional, tri-state or open drain). These eight I/O lines transfer information between the CIO's port B and external devices. They also provide external access to counter/timers 1 and 2.
PC_0-PC_3	Port C I/O lines (bidirectional, tri-state or open drain). These four I/O lines are used to provide handshake, WAIT, and REQUEST lines for ports A and B, to provide external access to counter/timer 3 or to the CIO's port C.
PCLK	Peripheral clock (input, TTL compatible). This is a peripheral clock that may be, but is not necessarily the CPU clock. It is used with the timers and the REQUEST/WAIT logic. The maximum input frequency is 4 MHz.
A_0-A_1	Address lines (input). These two lines are used to select the register involved in a data transaction between the CIO and CPU.
$\overline{CE}$	Chip enable (input, active low). A low level on this input enables the CPU to be read from or written to.
D_0-D_7	Data bus (bidirectional, tri-state). These eight data lines are used for transfers between the CPU and the CIO.
$\overline{RD}$*	Read (input, active low). This signal indicates that a CPU is reading from the CIO. During an INT ACK cycle, gates the interrupt vector on to the data bus.
$\overline{WR}$*	Write (input, active low). This signal indicates a CPU write to the CIO.
*	When $\overline{RD}$ and $\overline{WR}$ are detected low at the same time (normally an illegal condition) the device is reset.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-03-23

Approved sources of supply for SMD 83001 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8300101QA	0C7V7	Z0853604CMB
8300101YA	0C7V7	Z0853604LMB
8300102QA	0C7V7	Z0853606CMB
8300102YA	0C7V7	Z0853606LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.