TLE6288R

Smart 6 Channel Peak & Hold Switch

Automotive Power

Never stop thinking

Table of Contents

AEC Qualified

RoHS

Features

- 3 Channel high side with adjustable Peak & Hold current control
- 3 Channel high/low side configurable
- Protection
  - Overcurrent (current limitation)
  - Overtemperature
  - Overvoltage (active clamping)
- Diagnosis
  - Overcurrent
  - Overtemperature
  - Open load (Off-State)
  - Short to Ground (Off-state, lowside configuration)
  - Short to V_B (Off-state, highside configuration)
- Interface and Control
  - 16-Bit Serial Peripheral Interface (2 bit/CH)
  - Device programming via SPI
  - Separate diagnosis output for each CH (DIAG1 to 6)
  - General Fault Flag + Overtemperature Flag
  - Direct parallel control of all channels
  - General enable signal to control all channels simultaneously
- Low Quiescent Current
- Compatible with 3.3 V and 5 V microcontrollers

- **E**lectro**s**tatic **d**ischarge (ESD) protection of all pins
- Green Product (RoHS compliant)
- AEC Qualified

Application

- Peak & Hold Loads (valves, coils)
- Solenoids, Relays and Resistive Loads
- Fast protected Highside Switching (PWM up to > 10 kHz)

General Description

The TLE6288R is a 6-channel (150 mΩ) Smart Multichannel Switch in Smart Power Technology. The IC has embedded protection, diagnosis and configurable functions. Channels 1-3 are highside channels with integrated charge pump and can be programmed individually to do autonomous peak and hold current regulation with PWM. Channel 4-6 (also with integrated charge pump) can be configured to work as highside switch or lowside switch. This IC can be used to drive standard automotive loads in highside or lowside applications with switching frequencies up to 10 kHz. In addition the TLE6288R can be used to drive autonomously up to 3 inductive peak & hold (valves, coils) loads with programmable peak and hold current values.

Table 1 Product Summary

Parameter	Symbol	Values	Unit
Logic Supply voltage	V_{CC}	4.5 … 5.5	V
On resistance	$R_{DS(ON)1-6}$	0.15 typ. @ 25 °C	Ω
Lowside clamping voltage	$V_{cll(max)}$	+55	V
Highside clamping voltage	$V_{clh(max)}$	-19	V
Peak current range	I_{pk}	1.2 … 3.6	A
Hold current range	I_{hd}	0.7 … 2	A
Peak time range	I_p	0 … 3.6	ms
Fixed off time range	I_{fo}	100 … 400	µs

Type	Package
TLE6288R	PG-DSO-36-26

1 Block Diagram

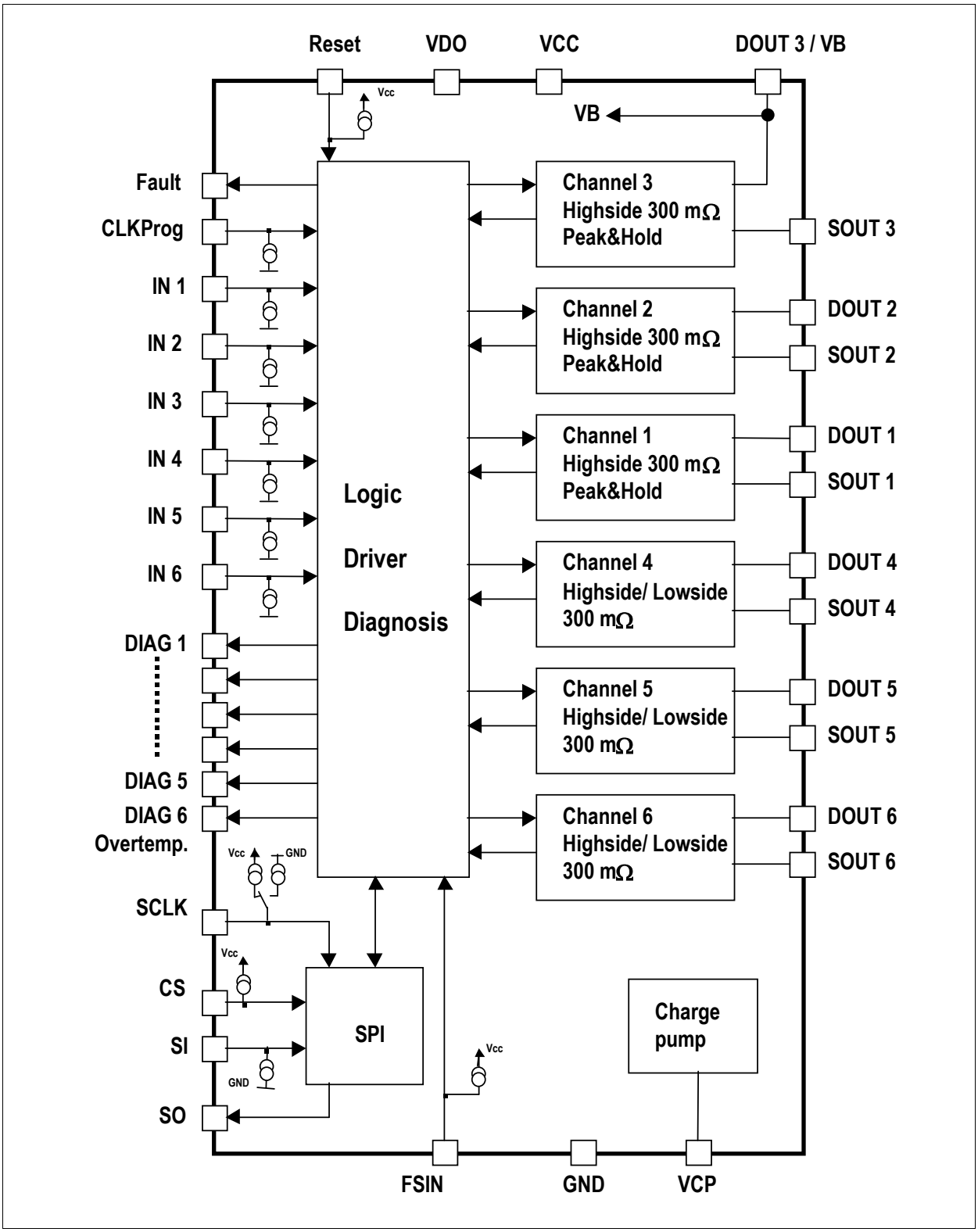

Figure 1 Block Diagram

2 Pin Configuration

2.1 Pin Assignment

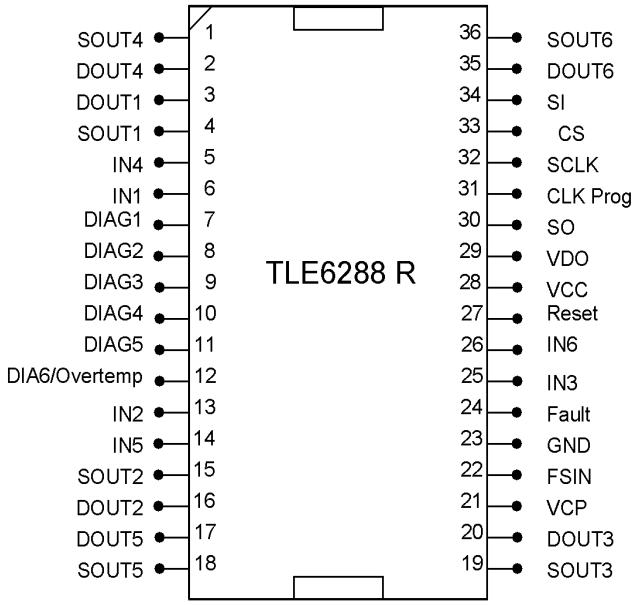

Figure 2 Pin Configuration PG-DSO-36-26

2.2 Pin Definitions and Functions

Pin	Symbol	Function
1	SOUT4	Source Output CH 4 (high/low side)
2	DOUT4	Drain Output CH 4 (high/low side)
3	DOUT1	Drain Output CH 1 (high side)
4	SOUT1	Source Output CH 1 (high side)
5	IN4	Control Input Channel 4
6	IN1	Control Input Channel 1
7	DIAG1	Diagnostic Output CH 1
8	DIAG2	Diagnostic Output CH 2
9	DIAG3	Diagnostic Output CH 3
10	DIAG4	Diagnostic Output CH 4
11	DIAG5	Diagnostic Output CH 5
12	DIAG6/Overtemp	Diagnostic Output CH 6 / Overtemp
13	IN2	Control Input Channel 2
14	IN5	Control Input Channel 5
15	SOUT2	Source Output CH 2 (high side)
16	DOUT2	Drain Output CH 2 (high side)

Pin	Symbol	Function
17	DOUT5	Drain Output CH 5 (high/low side)
18	SOUT5	Source Output CH 5 (high/low side)
19	SOUT3	Source Output CH 3 (high side)
20	DOUT3	Drain Output CH 3 (high side)
21	VCP	Charge Pump capacitor pin
22	FSIN	All Channels Enable/Disable
23	GND	Logic Ground
24	Fault	General Fault Flag
25	IN3	Control Input Channel 3
26	IN6	Control Input Channel 6
27	Reset	Reset pin (+ Standby Mode)
28	V_{CC}	Logic Supply Voltage (5 V)
29	V_{DO}	Supply pin for digital outputs
30	SO	SPI Serial Data Output
31	CLKProg	Program pin of SPI Clock
32	SCLK	SPI Serial Clock
33	CS	SPI Chip Select
34	SI	SPI Serial Data Input
35	DOUT6	Drain Output CH 6 (high/low side)
36	SOUT6	Source Output CH 6 (high/low side)

2.3 Pin Description

Symbol	Description
DOUT1-3	Drain of the 3 highside channels. These pins must always be connected to the same power (battery) supply line (V_B).
SOUT1-3	Source of the 3 highside channels. Outputs of the highside channels where the load is connected.
DOUT4-6	Drain pins of the 3 configurable channels. In highside configuration they must be connected to the same voltage as DOUT1-3. In lowside configuration they are the output pins and connected to the load.
SOUT4-6	Source of the 3 configurable channels. In highside configuration they are the outputs and connected to the load. In lowside configuration they must be connected with GND.
IN1-6	Parallel input pins for the 6 power outputs. These pins have an internal pull-down structure.
GND	Logic ground pin, the heat slug has to be connected to this potential.
FSIN	Disable pin. If the FSIN pin is in a logic low state, it switches all outputs OFF. The pin has an internal pull-up structure.
Reset	Reset pin. When the reset is low all channels are off, the internal biasing is deactivated, all internal registers are cleared and the supply-current consumption is reduced (standby mode). The pin has an internal pull-up structure.
Fault	General Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error is latched into the diagnosis register. When the diagnosis register is cleared this flag is also reset (high ohmic). This fault indication can be used to generate a µC interrupt.

Symbol	Description
CLKProg	Programming pin for the SPI Clock signal. This pin can be used to configure the clock signal input of the SPI. In low state the SPI will read data at the rising clock edge and write data at the falling clock edge. In high state the SPI will read data at the falling clock edge and write data at the rising clock edge. The pin has an internal pull-down structure.
DIAG1-5	Parallel diagnostic pins (push-pull) change state according to the input signal of the corresponding channel. For further details refer to **Chapter 4.3.1**
DIAG6/ Overtemp	
VCP	Pin to connect the external capacitor of the integrated charge pump. Connect a ceramic capacitor with 47 nF between this pin and DOUT3 (V_B).
V_{DO}	Supply pin of the push-pull digital output drivers. This pin can be used to vary the high-state output voltage of the SO pin and the DIAG1-6 pins.
V_{CC}	Logic supply pin. This pin is used to supply the integrated circuitry.
CS	Chip Select of the SPI (active low)
SO	Signal Output of the **S**erial **P**eripheral **I**nterface
SI	Signal Input of the **S**erial **P**eripheral **I**nterface. The pin has an internal pull-down structure.
SCLK	Clock Input of the **S**erial **P**eripheral **I**nterface. The pin has an internal pull-up structure (if CLKProg = L) or an pull-down structure (if CLKProg = H).

For more details about the SPI see **Chapter 5**.

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	PIN / Conditions
			Min.	Max.		
Voltages						
3.1.1	Power Supply Voltage 1 static dynamic: 1 min. 25 °C dynamic: Test cond. see **Figure 3**	V_B V_B V_B	-0.3 – –	20 24 40	V	DOUT1-3 DOUT1-3[2)] DOUT1-3[2)]
3.1.2	Power Supply Voltage 2	V_{CC} V_{DO}	-0.3	7	V	VCC VDO
3.1.3	Continuous Drain Source Voltage (lowside configuration)	V_{DSL}	–	40	V	DOUT - SOUT (channel 4 to 6)
	Continuous Source Voltage (highside configuration)	V_{SH}	-9	V_B	V	SOUT - GND (channel 4 to 6)
3.1.4	Input Voltage	V_{IN}	-0.3	V_{CC} + 0.3	V	IN1-6, Reset, FSIN, CS, SCLK, SI, CLKProg
3.1.5	Output Voltage	V_{OUT}	-0.3	V_{CC} + 0.3	V	Fault DIAG1-6 SO
3.1.6	Output Voltage	V_{CP}	–	V_B + 10	V	VCP; no voltage must be applied
Currents						
3.1.7	Reverse Current (1 ms)	I_{rev}	-4	–	A	between DOUT and SOUT; Channel 4 to 6
Temperatures						
3.1.8	Operating Temperature	T_j	-40	+150	°C	–
3.1.9	Storage Temperature	T_{stg}	-55	+150	°C	–
ESD Susceptibility						
3.1.10	ESD (Human Body Model) C = 100 pF, R = 1.5 kΩ Applied to all terminals 3 times	V_{ESDb}	–	2000	V	–
3.1.11	ESD (Machine Model) C = 200 pF, R = 0 Ω Applied to all terminals 3 times	V_{ESDm}	–	250	V	–

1) Not subject to production test, specified by design.

2) As long as max. junction temperature T_j is not exceeded.

Attention: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Attention: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

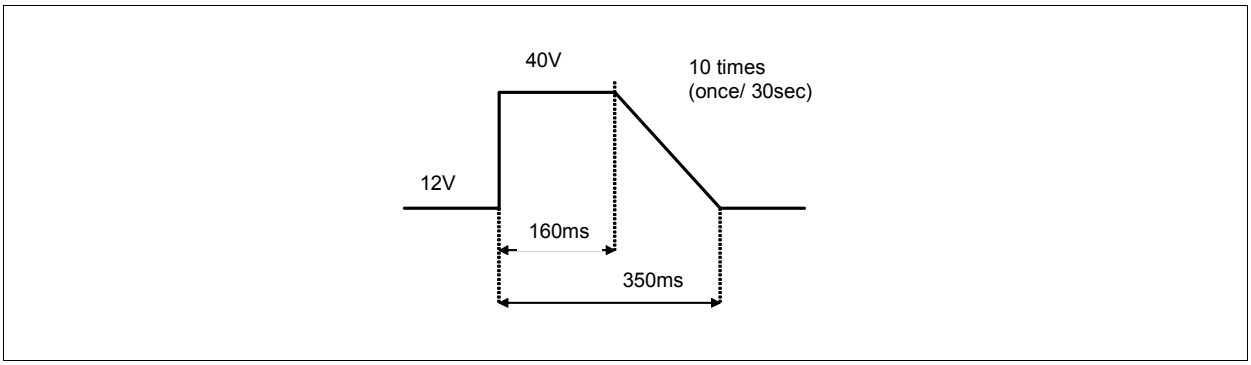

Figure 3 Test Condition

3.2 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
3.2.1							–
3.2.2	Junction to Case[1)]	R_{thjC}			1	K/W	2)
3.2.3	Junction to ambient[1)]	R_{thjA}		15.5		K/W	2) 3)

1) Not subject to production test, specified by design.

2) Channel 1-6 continously turned on, 0.8W power dissipation per channel

3) Specified R_{thjA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board ; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

Further informations can be found in **Chapter 7.2**

4 Description

4.1 General Functional Description

Channel 1 to 3

- High Side Configuration with Charge Pump
- On / off Current Control
- Peak & Hold Current Control with fixed off time, values adjustable by SPI
- Type of current control can be selected by SPI
- Peak Current,Peak Time, Hold Current and Off-Time can be selected by SPI to set average and ripple current for a given load (refer to **Figure 6**)

Channel 4 to 6

- Configurable as either High or Low Side switch (by SPI)
- On / Off operation

4.1.1 Output Stage Control: Parallel Control and SPI Control

A Boolean operation (either AND or OR) is performed on each of the parallel inputs IN 1 … 6 and respective SPI data bits, in order to determine the states of the respective outputs. The type of Boolean operation performed is programmed via the serial interface. Both, parallel inputs and respective SPI databits are high active.

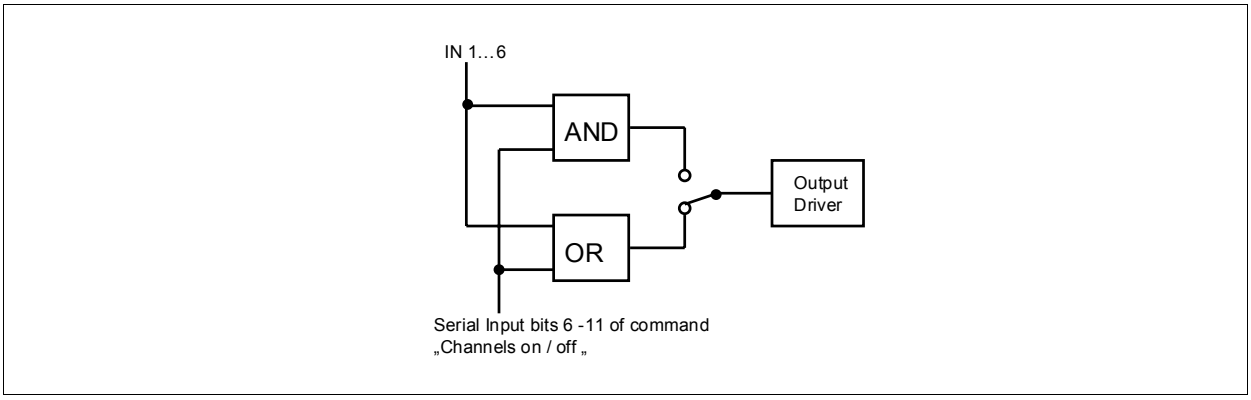

Figure 4 Serial Input Bits 6-11 of Command “Channels on/off”

Each output is independently controlled by an output latch and a common reset line FSIN, which disables all outputs. A logic high input ‘data bit’ turns the respective output channel ON, a logic low ‘data bit’ turns it OFF.

Table 2 Truth Table

Parallel Input	SPI Bit	Output OR	Output AND
0	0	OFF	OFF
0	1	ON	OFF
1	0	ON	OFF
1	1	ON	ON

4.1.2 Current Regulator: Peak Current Control with Fixed Off-Time

- **Hold only:** When the channel is turned on externally (SPI or parallel input) the current rises to the programmed hold current level. Then the channel is internally turned off and a timer is started for a fixed off-time (e.g. 200 µs). After this time the channel is internally turned on again until the hold current level is reached again and so on. This regulation works automatically until the channel is turned of externally.
- **Peak and hold mode with minimum peak time:** When the channel is turned on the current rises to the programmed peak current level. Then the channel is internally turned off, the current regulator changes to hold current values and a timer is started for a constant off-time. After this time the channel is internally turned on again until the hold current value is reached and then again turned off for the fixed off time. This regulation works automatically until the channel is turned of externally.
- **Peak and hold mode with programmed peak time:** When the channel is turned on the current rises to the programmed peak current level. Then the channel is internally turned off and a timer is started for a fixed off-time. After this time the channel is internally turned on again until the peak current value is reached and then again turned off. This works until the programmed peak time is over. Then the current regulator changes to hold current values and works as described under “hold only”.

Peak Current, Peak Time, Hold Current and fixed Off-Time can be set via SPI.

To avoid regulation disturbances by current transients during switching (e.g. caused by ESD capacitors at the outputs) the current regulator has a “leading edge blanking” of typical 20 µs in all three regulation modes. After turning on the DMOS (internally or externally) the current regulation circuit is deactivated for the first 20 µs. This guarantees that switching of the DMOS itself or charging of small capacitors at the output (e.g. ESD) is not disturbing the current regulation.

To detect shorted loads or low inductance loads in all three regulation modes a timer is started when a channel is turned on (t_{li}). If the first rising edge of the load current reaches the programmed current level (peak or hold current depending on the configured current control mode) within this time a overload fault is reported (see **Chapter 7.3**).

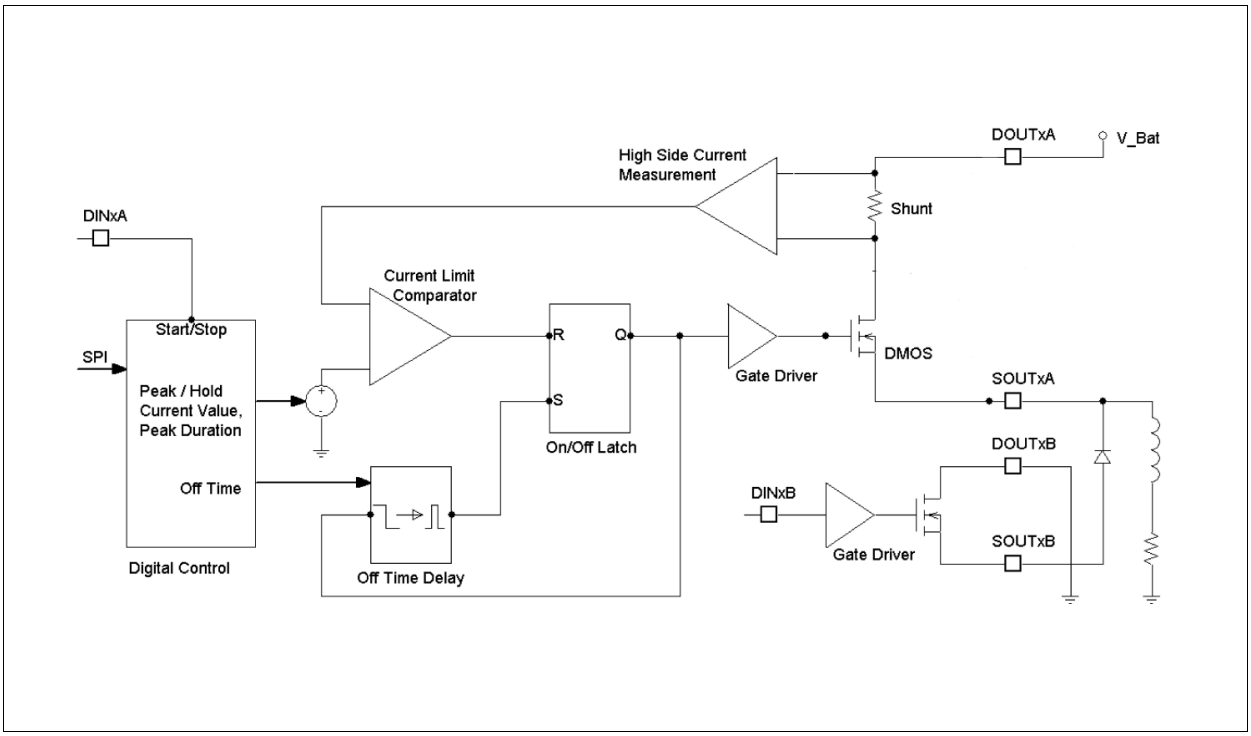

Figure 5 Simplified Functional Block Diagram

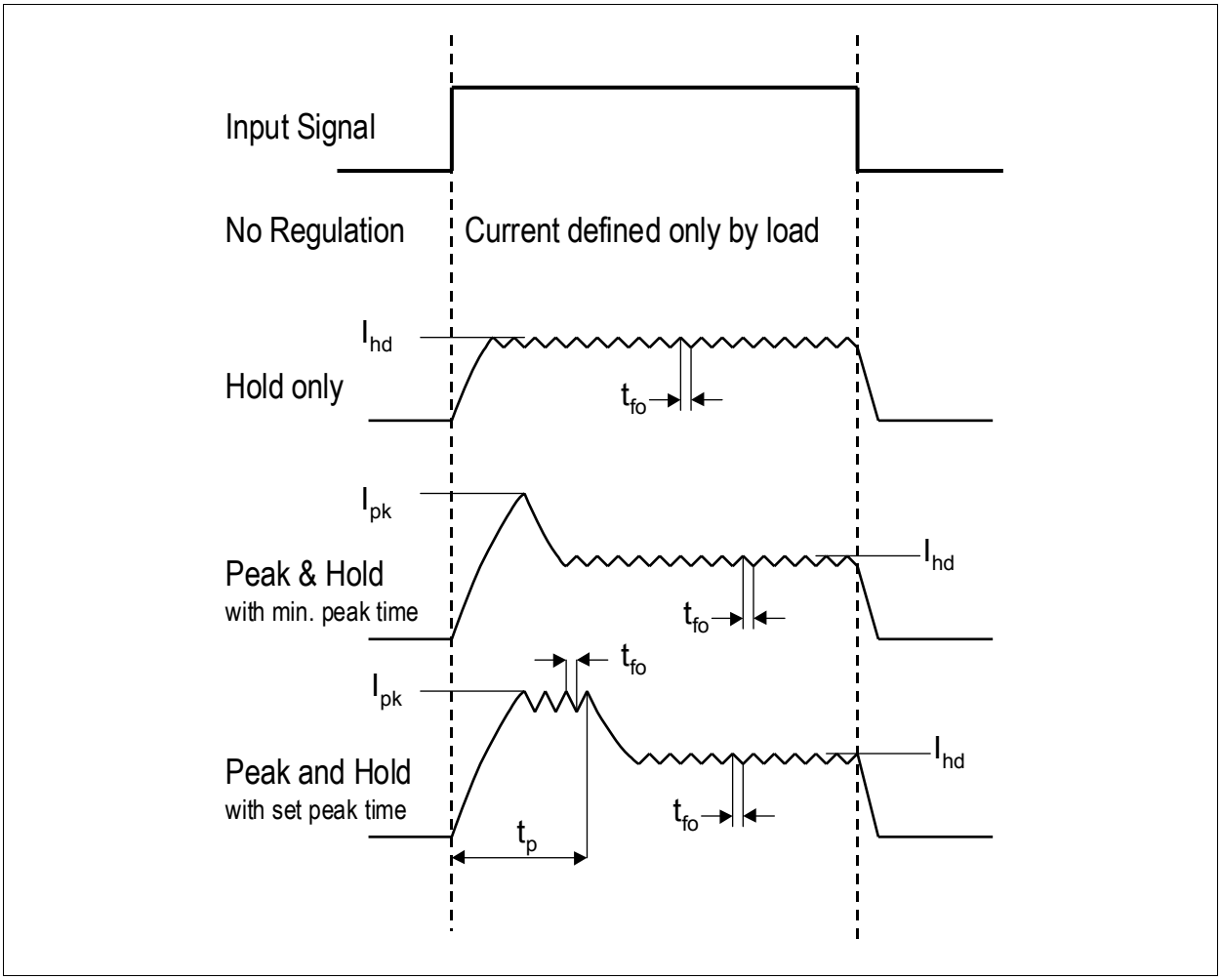

Figure 6 Current Forms of the Different Current Control Modes of Channel 1-3

4.2 Protection

The TLE6288R has integrated protection functions[1)] for overload and short circuit (active current limitation), overtemperature, ESD at all pins and overvoltage at the power outputs (zener clamping).

Overtemperature Behavior

Each channel has an overtemperature sensor and is individually protected against overtemperature.

As soon as overtemperature occurs the channel is immediately turned off. In this case there are two different behaviors of the affected channel that can be selected by SPI (for all channels generally):

Autorestart: as long as the input signals of the channel remains on (e.g. parallel input high) the channel turns automatically on again after cooling down.

Latching: After overtemperature shutdown the channel stays off until the this overtemperature latch is reset by a new L → H transition of the input signal.

Note: These overtemperature sensors of the channels are only active if the channel is turned on.

An additional overtemperature sensor is located in the logic of the device. It monitors permanently the IC temperature. As soon as the IC temperature reaches a specified level an overtemperature fault will be indicated.

1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.3 Diagnostic

The TLE6288R has a parallel diagnosis via 6 output pind (DIAG1 - DIAG6) and a serial diagnosis functionallity via SPI.

4.3.1 Parallel Diagnostic Functions

Parallel diagnostic pins (push-pull) change state according to the input signal of the corresponding channel. As soon as an error occurs at the corresponding channel (overload and overtemperature is detected in on state and open load/switch bypass in off state) the DIAG output shows the inverted input signal. An fault is detected only if it lasts for longer than the fault filter time. The fault information is not latched in a register.

If DIAG6 is configured as Overtemperature Flag: This is a general fault pin which shows a high to low transition as soon as an overtemperature error occurs for any one of the six channels (for longer than the fault filter time) or the IC logic. This fault indication can be used to differ between overload and overtemperature errors in one of the six channels or to detect a general IC overtemperature.

4.3.2 Electrical Characteristics: Diagnostic Functions

Electrical Characteristics: Diagnostic Functions

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
4.3.1	Open Load Detection Voltage	$V_{DS(OL)}$	–	5.5	–	V	–	lowside configuration, V_B = 12 V
4.3.2	Open Load Detection Voltage	$V_{DS(OL)}$	–	4.5	–	V	–	highside configuration, V_B = 12 V
4.3.3	Output Open Load diagnosis Current	$I_{d(OL)}$	-500	-100	-20	µA	–	V_B = V_{out} = 12 V
4.3.4	Fault Filter Time	$t_{f(fault)}$	50	100	200	µs	–	–
4.3.5	Switch Bypass Detection Current	$I_{d(SB)}$	–	–	250	µA	–	–
4.3.6	Overload Detection Threshold (Channel 1 to 3)	$I_{Dd(lim1-3)}$	4	–	6	A	–	no regulation mode
4.3.7	Overload / low inductance load Detection time (Channel 1 to 3)	t_{li}	–	–	t_{fo}	µs	see **Chapter 7.3**	current control mode
4.3.8	Overload Detection Threshold (Channel 4 to 6)	$I_{Dd(lim 4-6)}$	3	–	6	A	–	–

5 SPI

The SPI is a **S**erial **P**eripheral **I**nterface with 4 digital pins and a 16-bit shift register. The SPI is used to configure and program the device, turn on and off channels and to read detailed diagnostic information.

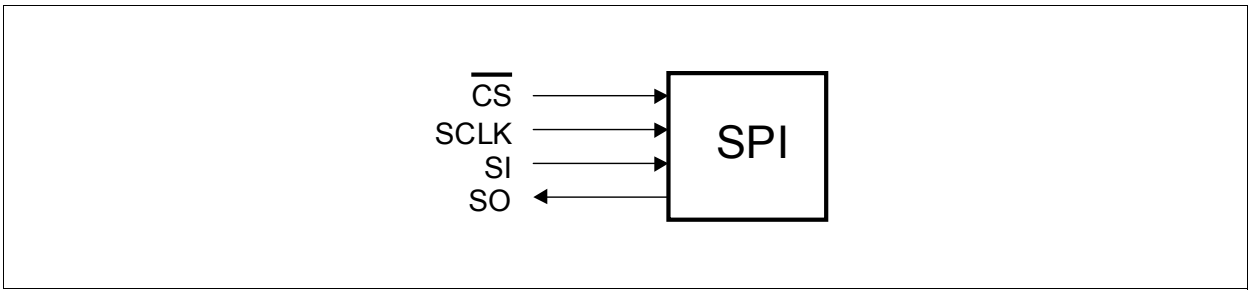

Figure 7 Serial Peripheral Interface

5.1 SPI Signal Description

$\overline{\text{CS}}$ - Chip Select. The system microcontroller selects the TLE6288R by means of the CS pin. Whenever the pin is in a logic low state, data can be transferred from the µC and from the TLE6288R to the µC.

- **$\overline{\text{CS}}$ = H:** Any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.
- **$\overline{\text{CS}}$ = H → L:**
  - diagnostic information is transferred from the diagnosis register into the SPI shift register
  - serial input data can be clocked into the SPI shift register from then on
  - SO changes from high impedance state to logic high or low state corresponding to the SO bits

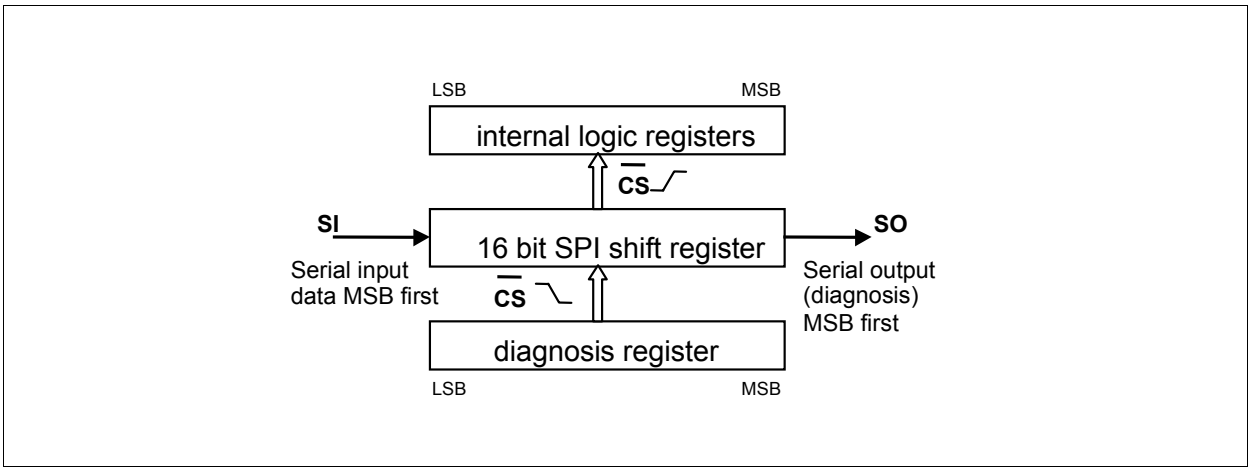

Figure 8

- **$\overline{\text{CS}}$ = L:** SPI is working like a shift register. With each clock signal the state of the SI is read into the SPI shift-register and one diagnosis bit is written out of SO.
- **$\overline{\text{CS}}$ = L → H:**
  - transfer of SI bits from SPI shift register into the internal logic registers
  - reset of diagnosis register if sent command was valid

To avoid any false clocking the serial clock input pin SCLK should be logic high state (if CLKProg = L; low state if CLKProg = H) during high to low transition of $\overline{\text{CS}}$.

SCLK - Serial Clock. The serial clock pin clocks the internal SPI shift register of the TLE6288R. The serial input (SI) accepts data into the input SPI shift register on the rising edge of SCLK (if CLKProg = L; falling edge if CLKProg = H) while the serial output (SO) shifts diagnostic information out of the SPI shift register on the falling

edge (if CLKProg = L; rising edge if CLKProg = H) of serial clock. It is essential that the SCLK pin is in a logic high state (if CLKProg = L; low state if CLKProg = H) whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit (MSB) first. SI information is read in on the rising edge of SCLK (if CLKProg = L; falling edge if CLKProg = H). Input data is latched in the SPI shift register and then transferred to the internal registers of the logic.

The input data consists of 16 bits, made up of 4 control bits and 12 data bits. The control word is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see **Chapter 5.5**).

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit (MSB) first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the falling edge of SCLK (if CLKProg = L; rising edge if CLKProg = H).

5.2 Electrical Characteristics: SPI Timing

Electrical Characteristics: SPI Timing

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
5.2.1	Serial Clock Frequency (depending on SO load)	f_{SCLK}	DC	–	5	MHz	–	–
5.2.2	Serial Clock Period ($1/f_{SCLK}$)	$t_{p(SCLK)}$	200	–	–	ns	–	–
5.2.3	Serial Clock High Time	t_{SCLKH}	50	–	–	ns	–	–
5.2.4	Serial Clock Low Time	t_{SCLKL}	50	–	–	ns	–	–
5.2.5	Enable Lead Time (falling edge of $\overline{CS}$ to falling edge of SCLK)	t_{leadL}	200	–	–	ns	–	CLKProg = L
	Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of SCLK)	t_{leadH}	200	–	–	ns	–	CLKProg = H
5.2.6	Enable Lag Time (rising edge of SCLK to rising edge of $\overline{CS}$)	t_{lagL}	200	–	–	ns	–	CLKProg = L
	Enable Lag Time (falling edge of SCLK to rising edge of $\overline{CS}$)	t_{lagH}	200	–	–	ns	–	CLKProg = H
5.2.7	Data Setup Time (required time SI to rising of SCLK)	t_{SUL}	20	–	–	ns	–	CLKProg = L
	Data Setup Time (required time SI to falling of SCLK)	t_{SUH}	20	–	–	ns	–	CLKProg = H
5.2.8	Data Hold Time (rising edge of SCLK to SI)	t_{HL}	20	–	–	ns	–	CLKProg = L
	Data Hold Time (falling edge of SCLK to SI)	t_{HH}	20	–	–	ns	–	CLKProg = H
5.2.9	Disable Time[1)]	t_{DIS}	–	–	200	ns	–	–

Electrical Characteristics: SPI Timing (cont'd)

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
5.2.10	Transfer Delay Time[2)] ($\overline{CS}$ high time between two accesses)	t_{dt}	200	–	–	ns	–	–
5.2.11	Data Valid Time[1)] C_L = 50 pF to 100 pF C_L = 220 pF	t_{valid}	 – –	 – –	 120 150	ns	–	–

1) Not subject to production test, specified by design.

2) To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault filter time $t_{f(fault)max}$ = 200 µs.

5.3 SPI Diagnostics

As soon as a fault occurs for longer than the fault filter time, the fault information is latched into the diagnosis register (and the Fault pin will change from high to low state). A new error on the same channel will overwrite the old error report. Serial data out pin (SO) is in a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ receives a LOW signal, all diagnosis bits can be shifted out serially. If the sent command was valid (see Note in **Chapter 5.5**) the rising edge of $\overline{CS}$ will reset the diagnosis registers (except the channel OT flag) and restart the fault filter time. In case of an invalid command the device will ignore the data bits and the diagnosis register will not be reset at the rising $\overline{CS}$ edge.

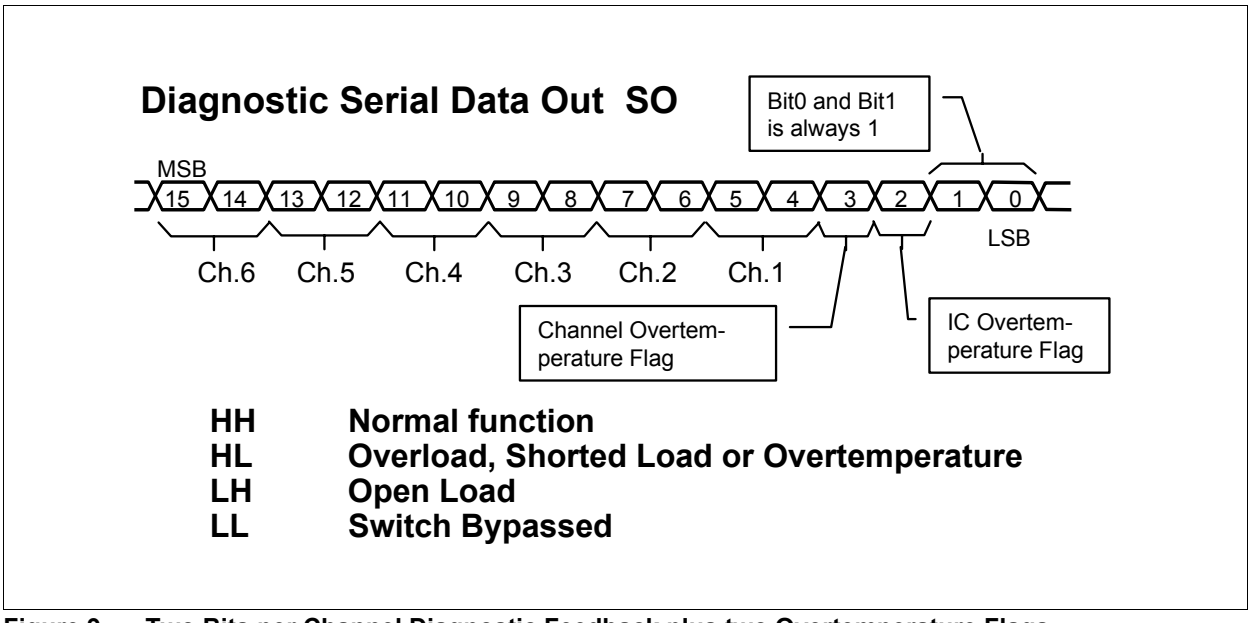

Figure 9 Two Bits per Channel Diagnostic Feedback plus two Overtemperature Flags

For Full Diagnosis there are two diagnostic bits per channel configured as shown in **Figure 9**.

Diagnosis bit 0 and bit 1 are always set to 1.

Normal function: The bit combination **HH** indicates that there is no fault condition, i.e. normal function.

Overload, Shorted Load or Overtemperature: HL is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition. The second reason for this bit combination is overtemperature of the corresponding channel.

In current regulation mode HL is also set if the load current reaches the programmed current value in a time shorter than the fixed off time (t_{fo}). This detection is only performed at the first rising load current edge after a channel is turned on (for channel 1 to 3). See **Chapter 7.3**.

Open load: LH is set when open load is detected (in off state of the channel).

Switch Bypassed:

- **Short to GND:** in lowside configuration LL is set when this condition is detected.
- **Short to Battery:** in highside configuration LL is set when this condition is detected.

Channel Overtemperature Flag: In case of overtemperature in any output channel in on state the overtemperature Flag in the SPI diagnosis register is set (change bit 3 from 0 to 1). This bit can be used to distinguish between Overload and Overtemperature (both HL combination) and is reset by switching OFF/ON the affected channel.

In addition the DIAG6 / Overtemp pin is set low (if configured as Overtemp Flag).

IC Overtemperature Flag: When the IC logic temperature exceeds typ. 170 °C the non-latching IC Overtemperature Flag will be set in the SPI diagnosis register (change bit 2 from 0 to 1).

In addition the DIAG6 / Overtemp pin is set low (if configured as Overtemp. Flag).

5.4 SPI Commands, Values and Parameters

The 16-bit SPI is used to program different IC functions and values, turn on and off the channels and to get detailed diagnosis information. Therefore 4 command bits and 12 data bits are used.

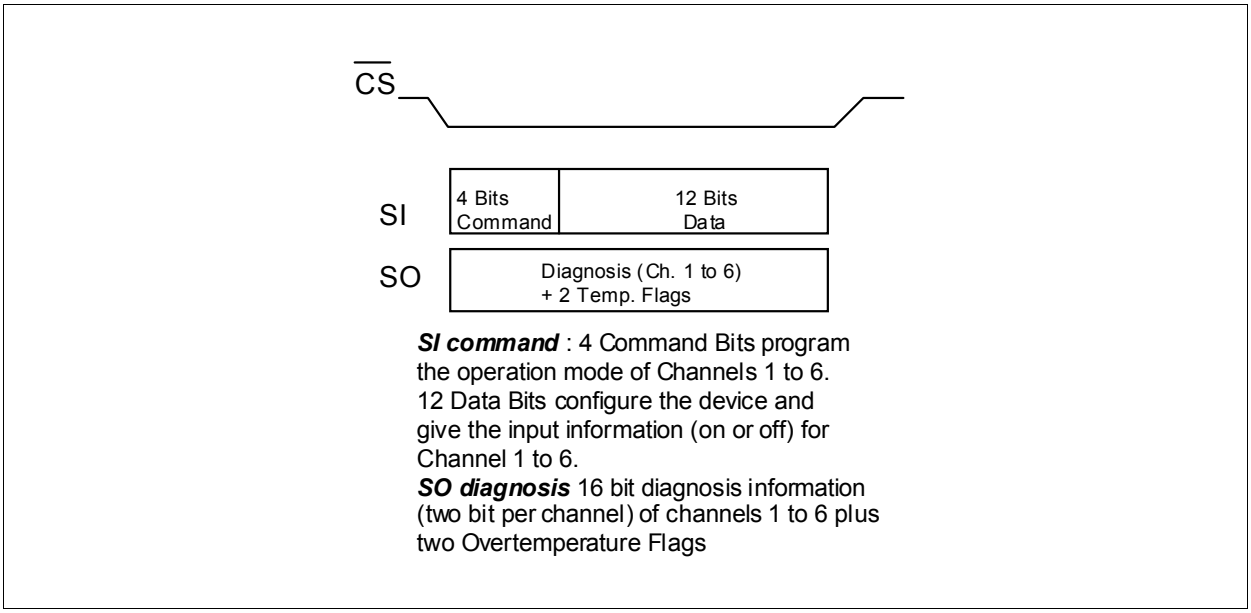

Figure 10

The following parameters and functional behavior can be programmed by SPI:

- **Current regulation mode** (mode): for each of the 3 highside channels individually the operation mode can be set.
  - “no current regulation”
  - current regulation “hold only”
  - current regulation “peak & hold with minimum peak time”
  - current regulation “peak & hold with programmed peak time”
- **Peak Current** (I_{pk}): for each of the 3 highside channels individually the peak current value for P&H current regulation can be programmed. The current range is 1.2 A to 3.6 A.
- **Fixed off time of the current regulator** (t_{fo}): for each of the 3 highside channels (Ch1 to Ch3) individually the fixed off time for all modes with current regulation can be programmed from 100 µs to 400 µs.
- **Hold current** (I_{hd}): for each of the 3 highside channels (Ch1 to Ch3) individually the hold current value for P&H and hold only current regulation can be programmed. The current range is 0.7 A to 2.0 A.
- **Peak time** (t_p): for each of the 3 highside channels (Ch1 to Ch3) individually the peak time value for P&H current regulation can be programmed. The time range is 0.8 ms to 3.6 ms.
- **Highside/Lowside configuration** (H/L): Each of the 3 configurable channels (Ch4 to Ch6) can be programmed for use as Highside switch or Lowside switch.
- **Open load and switch bypassed detection activated or deactivated** (OL+SB): For each of the 3 configurable channels (Ch4 to Ch6) the open load and switch bypassed diagnosis can be deactivated. In lowside configuration the open load and the short to GND detection can be deactivated, in highside configuration the open load and short to battery detection.
- **Boolean operation** (OR/AND): For all channels generally the Boolean operation of the parallel input signal and the SPI bit of the corresponding channel can be defined.
- **Overtemperature behavior** (R/L): The overtemperature behavior of the channels can be programmed by SPI. Autorestart or latching overtemperature shutdown can be selected (for all channels the same behavior).
- **DIAG6 or overtemperature flag** (D/F): With this SPI bit the function of the DIAG6 / Overtemp pin is defined. This output can work as diagnosis output of channel 6 or as Overtemperature Flag.

5.5 SPI Commands

Table 3 Command Table

Command	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Set all to Default	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
Config. Regulator 1	1	0	0	1	Mode		I_{pk}		t_{fo}		I_{hd}		t_p			X
Config. Regulator 2	1	0	1	0	Mode		I_{pk}		t_{fo}		I_{hd}		t_p			X
Config. Regulator 3	1	0	1	1	Mode		I_{pk}		t_{fo}		I_{hd}		t_p			X
Config. Ch1 - Ch6	1	1	0	0	Ch6 H/L	Ch6 OL+ SB	Ch5 H/L	Ch5 OL+ SB	Ch4 H/L	Ch4 OL+ SB	all OR/ AND	all R/L	DIAG 6D/F	X	X	X
Channels on/off	1	1	0	1	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	X	X	X	X	X	X
Diagnosis only	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

Legend of SPI Command Table

- Mode: Operation mode of the current regulator:
  - no regulation
  - hold only
  - peak & hold with minimum peak time
  - peak & hold with programmed peak time
- I_{pk}: Peak current values 1.2 A … 3.6 A
- I_{hd}: Hold current values 0.7 A … 2 A
- t_p: Peak time value 0.8 ms … 3.6 ms
- t_{fo}: Fixed off time value 100 µs … 400 µs
- H/L: Channel 4 to 6 in highside or lowside configuration
- OL+SB: open load detection and switch bypassed detection activated or deactivated
- OR/AND: Boolean Operation (parallel input and corresponding SPI Bit)
- R/L: Autorestart or Latching overtemperature behaviour
- D/F: DIAG6/Overtemp pin set as Diagnosis output of channel 6 or as Overtemperature Flag
- Ch1-Ch6: On/Off information of the output drivers (high active)

Command Description

Config. Regulator 1-3: With this command the values for the current regulation and the functional mode of the channel is written into the internal logic registers.

Config. Ch1 to Ch6: This command writes the configuration data of the 3 configurable channels (4-6) and sets the Boolean operation and overtemperature behavior of all channels. It also sets the DIAG6/Overtemp. pin to Diagnosis of channel 6 or Overtemperature Flag.

Set all to default: This command sets all internal logic registers back to default settings.

Diagnosis only: When this command is sent the 12 data bits are ignored. The internal logic registers are not changed.

Channels on/off: With this command the SPI bits for the ON/OFF information of the 6 Channels are set.

Note: Specified control words (valid commands) are executed and the diagnosis register is reset after the rising CS edge.
Not specified control words are not executed (cause no function) and the diagnosis register is not reset after the CS = L → H signal.

5.6 Bit Assignment and Default Settings for Internal Logic Registers

Mode	**00**	**no current regulation**						
	01	hold only						
	10	P&H minimum peak time						
	11	P&H with programmed times						
Peak Current (I_{pk})	1.2 A	1.8 A	**2.4 A**	3.6 A				
2 Bits	00	01	**10**	11				
Hold Current (I_{hd})	0.7 A	**1.0 A**	1.4 A	2.0 A				
2 Bits	00	**01**	10	11				
Fixed off Time (t_{fo})	100 µs	**200 µs**	300 µs	400 µs				
2 Bits	00	**01**	10	11				
Peak Time (t_p)	0.8 ms	1.2 ms	1.6 ms	2.0 ms	2.4 ms	**2.8 ms**	3.2 ms	3.6 ms
3 Bits	000	001	010	011	100	**101**	110	111
Boolean operation	**OR**		AND					
1 Bit	**0**		1					
Overtemp. behavior	**Restart**		Latch					
1 Bit	**0**		1					
Diag6 / Overtemp	**Diag6**		Overtemp. Flag					
1 Bit	**0**		1					
Highside / Lowside	**Highside**		Lowside					
1 Bit	**0**		1					
Open Load & SB (4-6)	**Yes**		No					
1 Bit	**0**		1					
Channels on / off	**off**		on					
1 Bit	**0**		1					

Default Settings are in **bold print**.

5.7 SPI Timing Diagrams

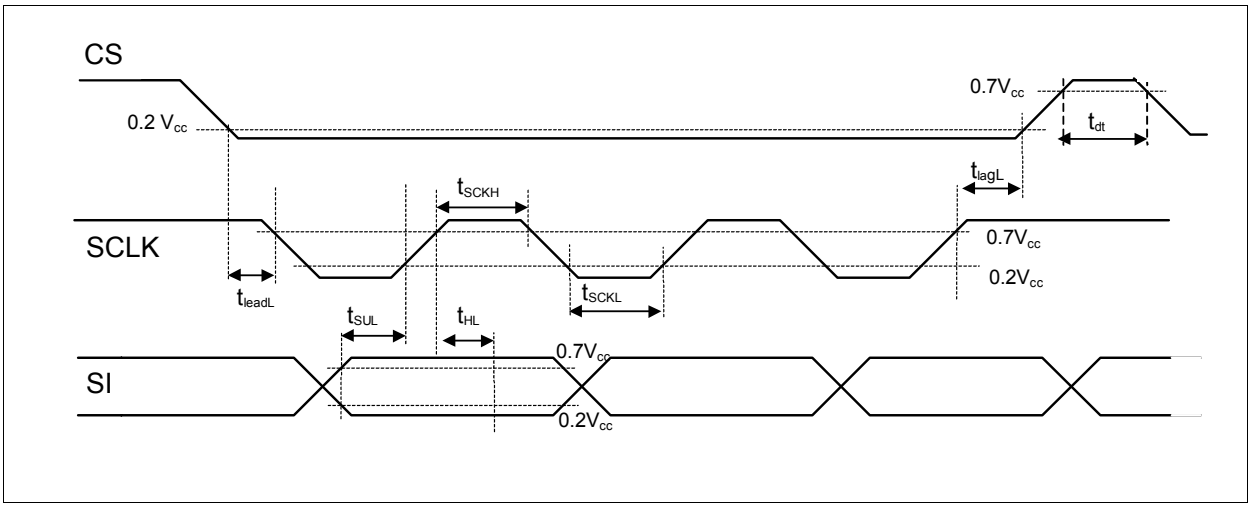

Figure 11 Input Timing Diagram (CLKProg = L)

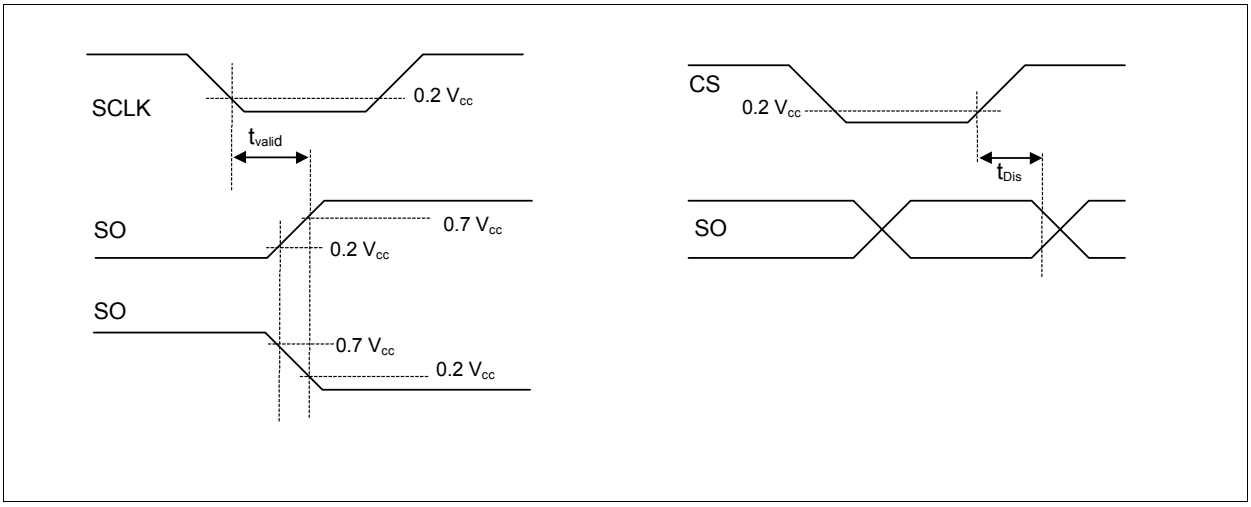

Figure 12 SO Valid Time Waveforms and Enable and Disable Time Waveforms (CLKProg = L)

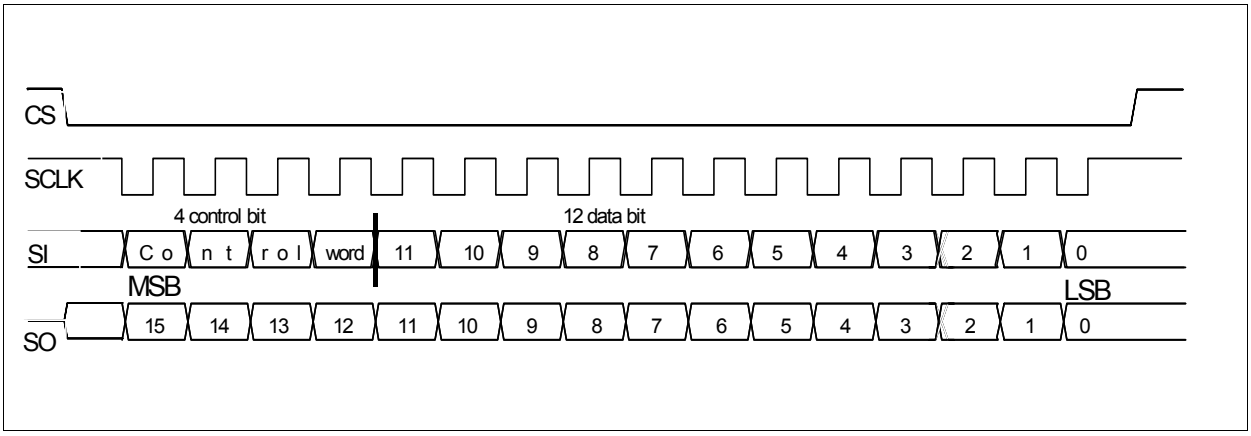

Figure 13 Serial Interface

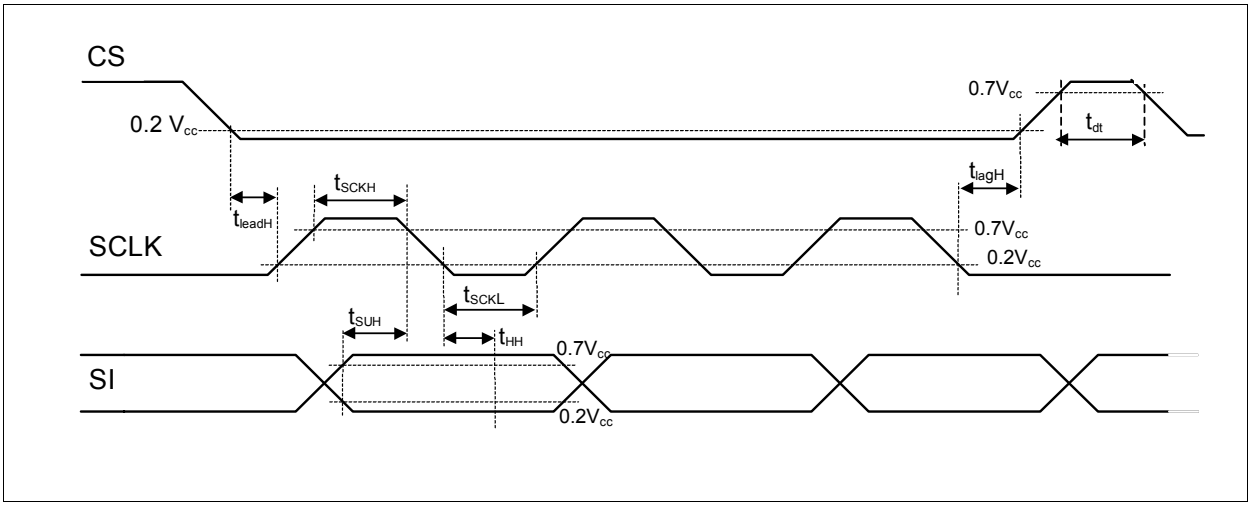

Figure 14 Input Timing Diagram (CLKProg = H)

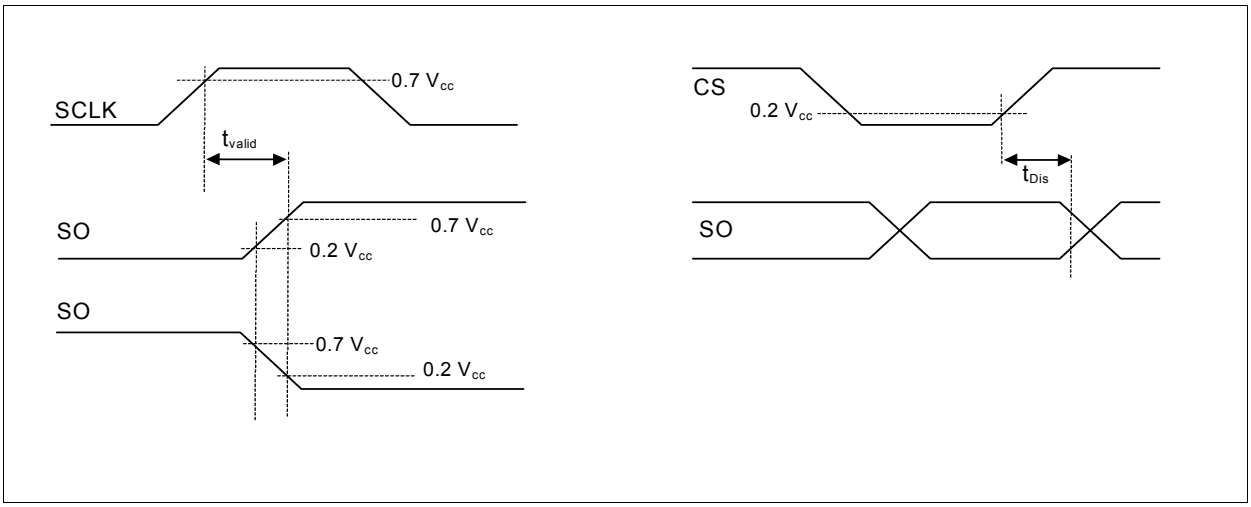

Figure 15 SO Valid Time Waveforms and Enable and Disable Time Waveforms (CLKProg = H)

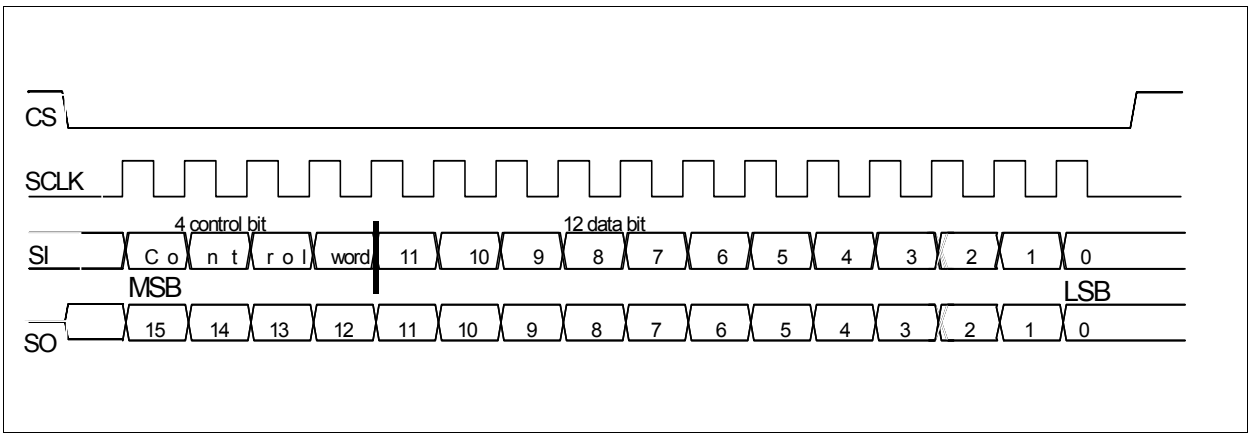

Figure 16 Serial Interface

6 Electrical Characteristics Input / Output Pins

6.1 Power Supply, Reset

Electrical Characteristics: Power Supply, Reset

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
6.1.1	Power Supply Current 1	I_B	–	–	10	mA	DOUT1-3	Ch1-Ch6: Off
6.1.2	Power Supply Current 2	I_{CC}	–	–	10	mA	V_{CC}	–
6.1.3	Power Supply Current in Standby Mode	I_{CC} + I_b	–	–	50	µA	DOUT1-3, V_{CC}	Reset = L
6.1.4	Minimum Reset Duration	$t_{Reset,min}$	50	–	–	µs	–	–
6.1.5	Wake-up time after reset	t_{wakeup}	–	–	5	ms	–	C_{CP} = 10 nF

6.2 Power Outputs

Electrical Characteristics: Power Outputs

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
6.2.1	On Resistance	$R_{DS(ON)}$	–	–	350	mΩ	DOUTx - SOUTx	I_D = 2.4 A V_B = 10 V
6.2.2	Forward Voltage Revers Diode	V_{RDf}	–	–	2	V	SOUTx - DOUTx	I_D = -4 A T_j = 150 °C
6.2.3	Peak Current range	I_{pk}	–	1.2 … 3.6	–	A	–	–
6.2.4	Peak Current accuracy	I_{pka}	–	–	±15 ±20	% %	–	T_j = 25, 150 °C T_j = -40 °C
6.2.5	Hold Current range	I_{hd}	–	0.7 … 2	–	A	–	–
6.2.6	Hold Current accuracy	I_{hda}	–	–	±15 ±20	% %	–	T_j = 25, 150 °C T_j = -40 °C
6.2.7	Peak time range	t_p	–	0.8 … 3.6	–	ms	–	–
6.2.8	Peak time accuracy	t_{pa}	–	–	±20	%	–	–
6.2.9	Fixed off Time range	t_{fo}	–	100 … 400	–	µs	–	–
6.2.10	Fixed off Time accuracy	t_{foa}	–	–	±30	%	–	100 µs
6.2.11	Fixed off Time accuracy	t_{foa}	–	–	±20	%	–	200 µs - 400 µs
6.2.12	Output ON Delay time1	t_{dON}	–	–	10	µs	–	see **Figure 17**
6.2.13	Output ON Rise time1	t_r	–	–	10	µs	–	see **Figure 17**

Electrical Characteristics: Power Outputs (cont'd)

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
6.2.14	Output OFF Delay time	t_{dOFF}	–	–	20	µs	–	HS- Mode LS- Mode see **Figure 17**
6.2.15	Output OFF Fall time	t_f	–	–	10	µs	–	see **Figure 17**
6.2.16	Leakage Current	–	–	–	10	µA	–	Reset = L
6.2.17	Leak Current in OFF (highside configuration)	I_{loff}	–	–	-250	µA	SOUT1-6	–
6.2.18	Leak Current in OFF (lowside configuration)	I_{loff}	–	–	500	µA	DOUT4-6	–
6.2.19	Output Clamp Voltage (highside configuration)	V_{clh}	-19	-14	-9	V	SOUT1-6	Refers to GND level
6.2.20	Output Clamp Voltage (lowside configuration)	V_{cll}	40	–	55	V	DOUT4-6	Refers to GND level
6.2.21	Current limitation (Channel 1 to 3)	$I_{Dlim1-3}$	4	–	6	A	–	–
6.2.22	Current limitation (Channel 4 to 6)	$I_{Dlim4-6}$	3	–	6	A	–	–
6.2.23	IC Overtemp. Warning[1)] Hysteresis	T_{ot} T_{hys}	160 –	– 10	180 –	°C °C	–	–

1) Not subject to production test, specified by design.

6.3 Digital Inputs

Electrical Characteristics: Digital Inputs

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
6.3.1	Input Low Voltage	V_{INL}	–	–	1	V	all digit. inputs	–
6.3.2	Input High Voltage	V_{INH}	2	–	–	V	all digit. inputs	–
6.3.3	Input Voltage Hysteresis	V_{INHys}	–	100	–	mV	all digit. inputs	–
6.3.4	Input pull-down current	I_{pd}	20	50	100	µA	IN1-6; CLKProg	V_{IN} = 5 V
6.3.5	Input pull-up current	I_{pu}	-100	-50	-20	µA	Reset; FSIN	V_{IN} = GND

Electrical Characteristics: Digital Inputs (cont'd)

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
6.3.6	SPI Input pull-down current	I_{pd}	10	20	50	µA	SI, SCLK (CLKProg = H)	V_{IN} = 5 V
6.3.7	SPI Input pull-up current	I_{pu}	-50	-20	-10	µA	CS, SCLK (CLKProg = L)	V_{IN} = GND

6.4 Digital Outputs

Electrical Characteristics: Digital Outputs

V_{CC} = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, V_B = 6 V to 16 V, Reset = H, V_{DO} = V_{CC}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Pin/ Comment	Conditions
			Min.	Typ.	Max.			
6.4.1	SO Low State Output Voltage	V_{SOL}	–	–	0.4	V	SO	I_{SOL} = 2.5 mA
6.4.2	SO High State Output Voltage	V_{SOH}	V_{DO} - 0.4 V	–	–	V	SO	I_{SOH} = -2 mA
6.4.3	DIAG Low State Output Voltage	V_{DIAGL}	–	–	0.4	V	DIAG1-6	I_{DIAGL} = 50 µA
6.4.4	DIAG High State Output Voltage	V_{DIAGH}	V_{DO} - 0.4 V	–	–	V	DIAG1-6	I_{DIAGH} = -50 µA
6.4.5	Fault Low Output Voltage	V_{ol}	–	–	0.4	V	Fault	I_{out} = 1 mA
6.4.6	Fault Output leak Current	I_{oh}	–	–	1	µA	Fault	Output: OFF $V_{(fault)}$ = 5 V

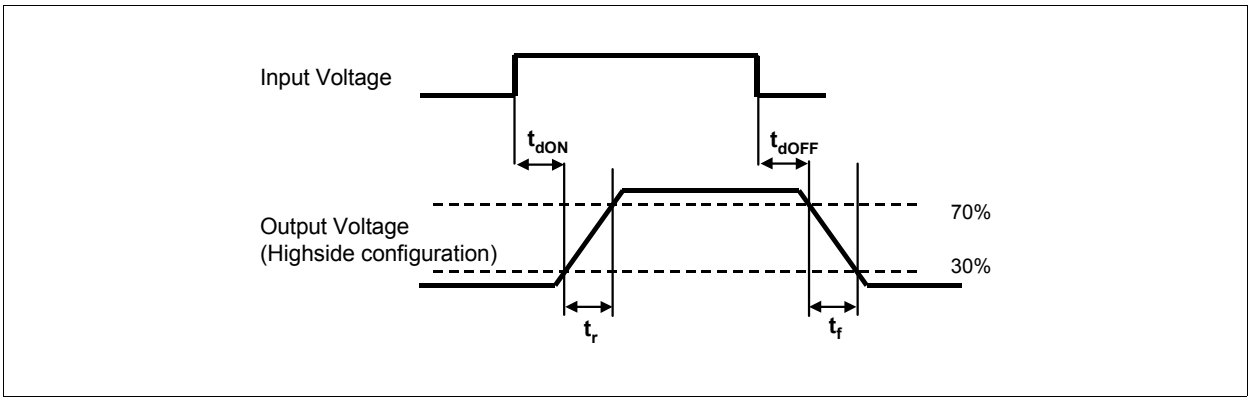

Figure 17 Turn on/off Timings with Resistive Load

7 Application Information

7.1 Z_{thjc} Diagram Junction - Case for Single channel operation

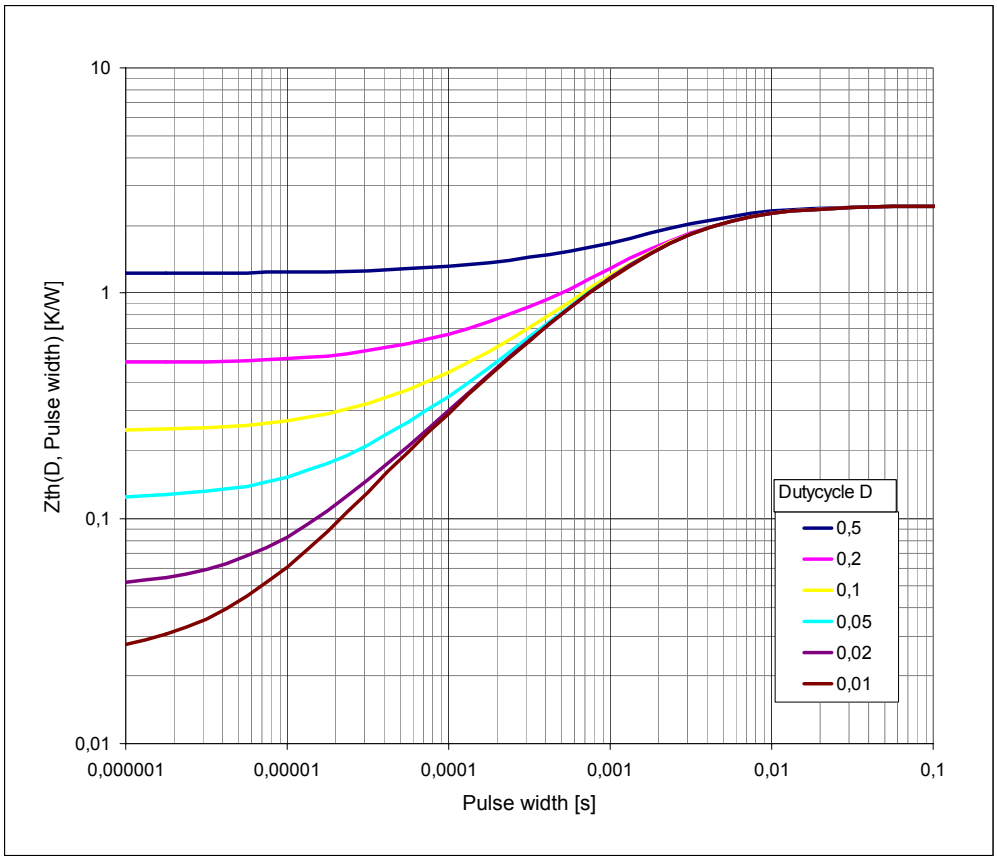

Figure 18 Z_{thjc} Diagram

- Conditions for **Figure 18**
  - Results based on FEM Simulations
  - T_{case} = 125 °C
  - Single Channel operation, 0.8W power dissipation

7.2 Thermal Application Information

All thermal resistance values in this document are data from FEM (Finite Element Modelling). The boundary conditions are chosen according to the JESD51 standard. Therefore, all values can be viewed as reliable and reproducible.

The high effective thermal conductivity test PCB (2s2p) gives a near best case thermal performance value. compared to the single layer low effective thermal conductivity PCB (1s). It should be emphasized that values measured/simulated with these test boards cannot be used to directly predict any particular system application performance.

In real applications, the R_{thjA} can be influenced by the environment and PCB conditions. Thermal vias, application specific multi layer PCBs and a direct thermal connection to the ECU metal-case are often used to improve the thermal impedance R_{thjA}.

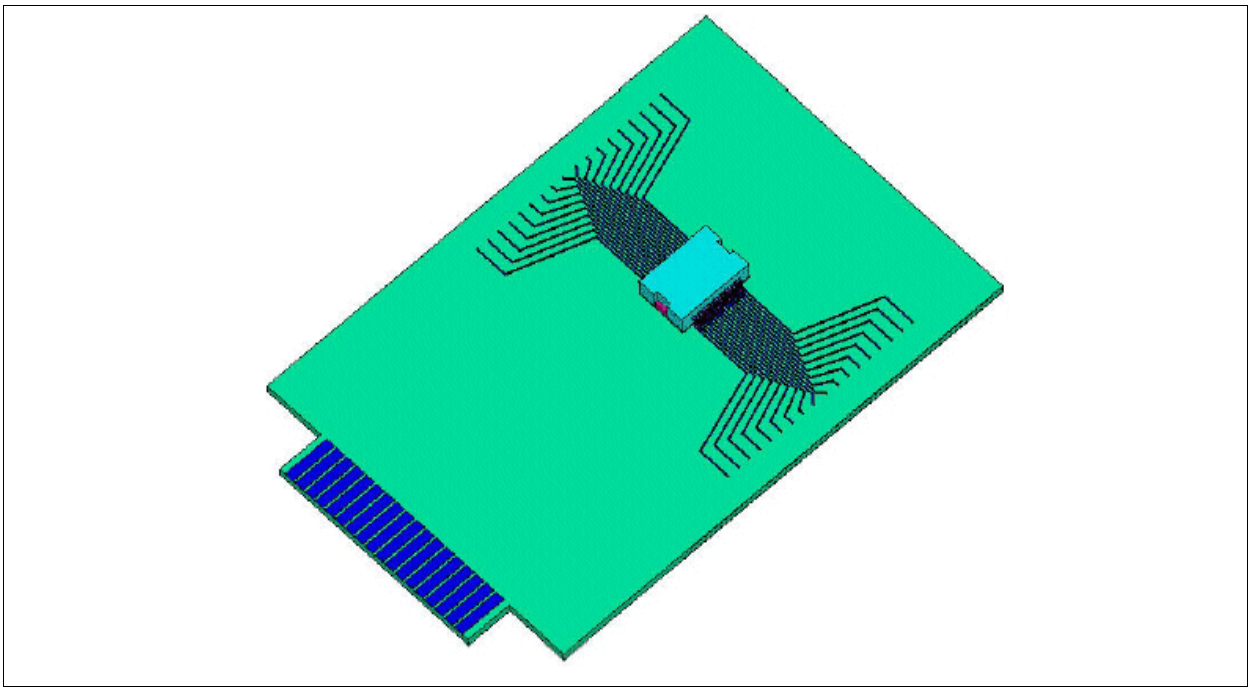

Figure 19 FE Model of the JEDEC 2s2p PCB

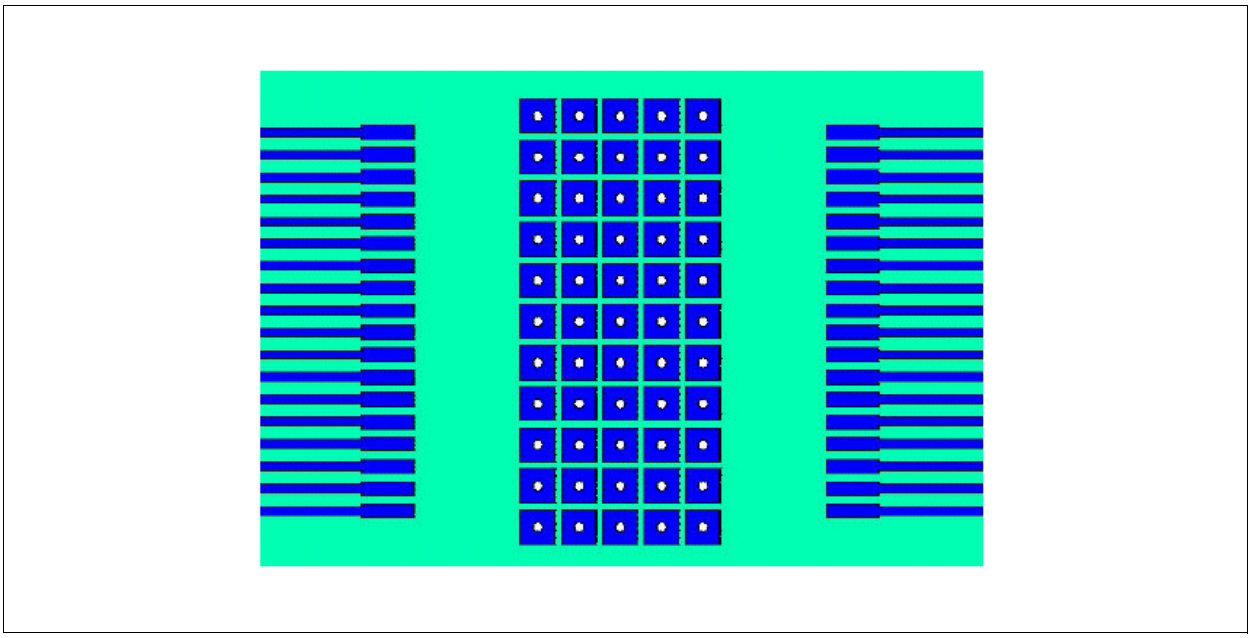

Figure 20 Thermal via layout

Figure 19 showes the Product TLE6288R on the 2s2p board used to specify the typical R_{thjA} value in **Chapter 3.2**. In **Figure 20**, the thermal via layout according to JESD51-5 is shown.

7.3 Overload/Low Inductance Load Detection in Current Regulation Mode

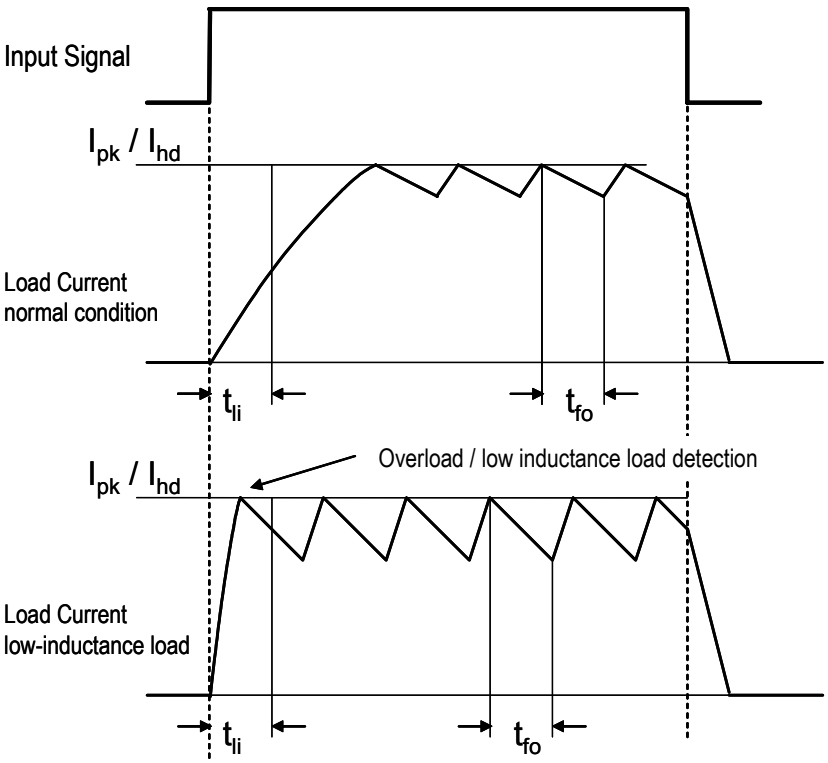

Figure 21

8 Package Outlines

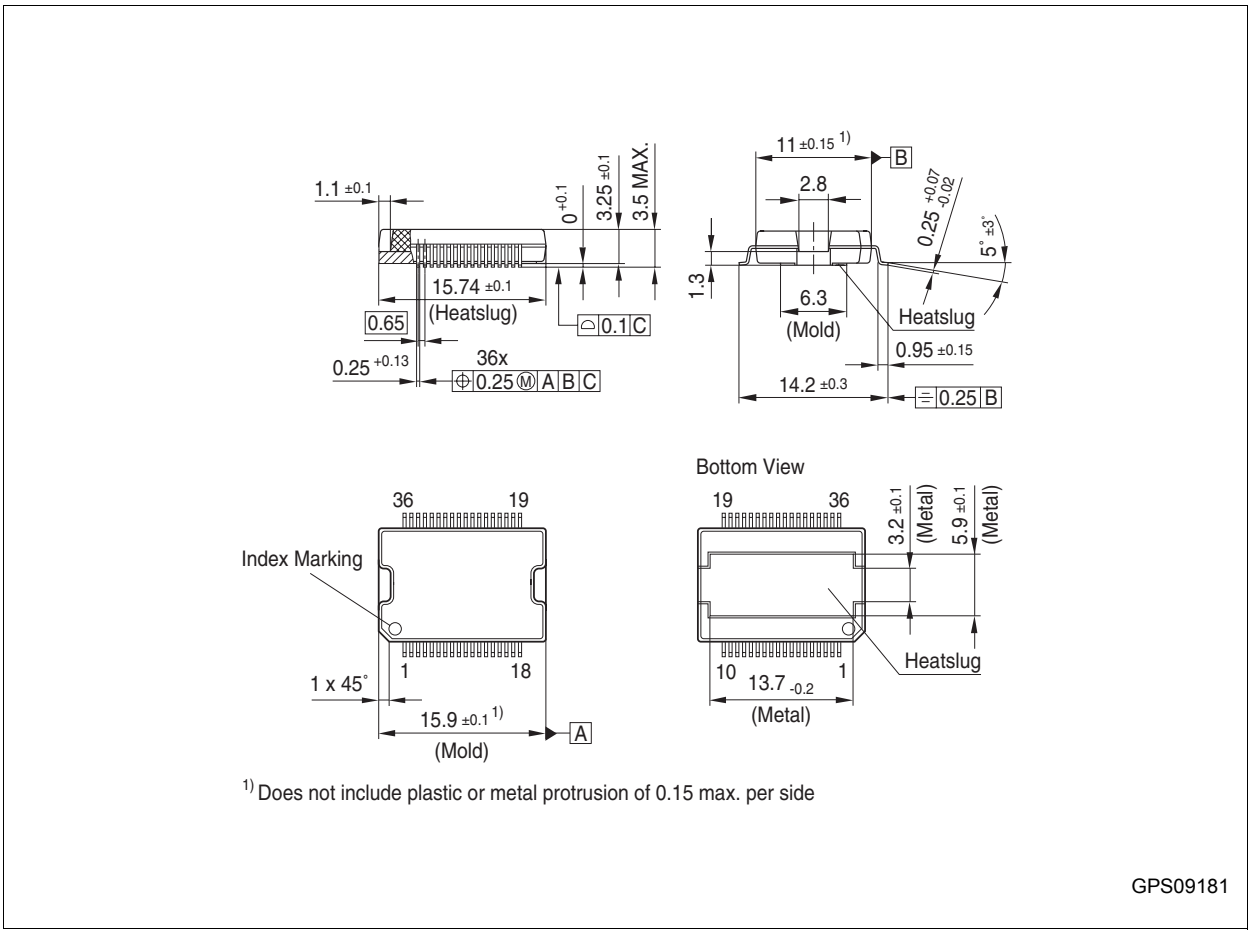

Figure 22 PG-DSO-36-26 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

9 Revision History

Revision	Date	Changes
2.2	2004-03-25	Preliminary Datasheet TLE6288R Vp2.2
2.3	2006-05-03	Formal changes, Thermal information added, Spec. values not changed
2.4	2007-08-08	RoHS-compliant version of the TLE6288R Page 3: “AEC qualified” and “RoHS” logo added, “Green Product (RoHS compliant)” and “AEC qualified” statement added to feature list, package names changed to RoHS compliant versions, package pictures updated Page 30: Package names changed to RoHS compliant versions, “Green Product” description added Revision History updated Legal Disclaimer updated

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