ML4425

Sensorless BLDC Motor Controller

Features

- Stand-alone operation
- Motor starts and stops with power to IC
- On-board start sequence: Align ♦ Ramp ♦ Set Speed
- Patented Back-EMF commutation technique provides jitterless torque for minimum “spin-up” time
- Onboard speed control loop
- PLL used for commutation provides noise immunity from PWM spikes, compared to noise sensitive zero crossing technique
- PWM control for maximum efficiency
- Direct FET drive for 12V motors; drives high voltage motors with IC buffers

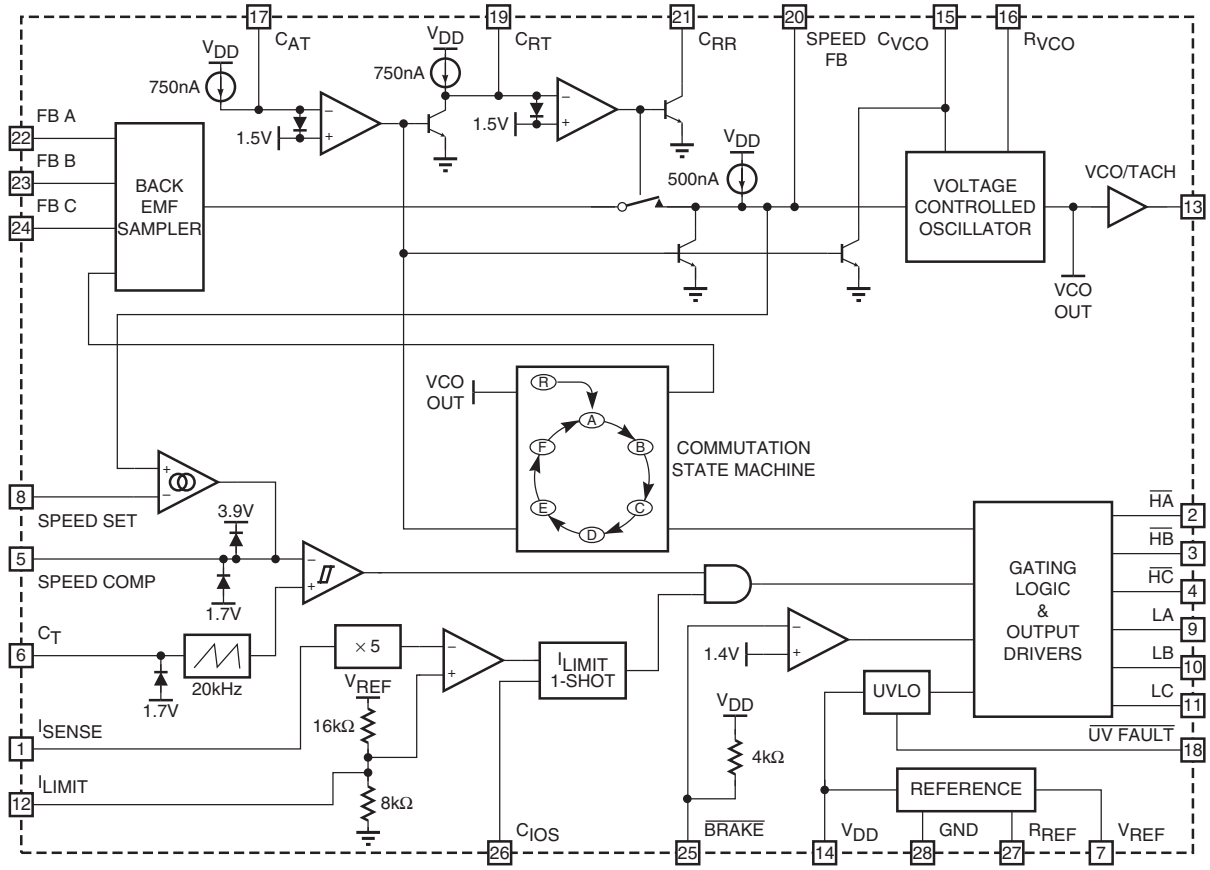
General Description

The ML4425 PWM motor controller provides all of the functions necessary for starting and controlling the speed of delta or wye wound Brushless DC (BLDC) motors without Hall Effect sensors. Back EMF voltage is sensed from the motor windings to determine the proper commutation phase sequence using a PLL. This patented sensing technique will commutate a wide range of 3-Phase BLDC motors and is insensitive to PWM noise and motor snubbing circuitry.

The ML4425 limits the motor current using a constant off-time PWM control loop. The velocity loop is controlled with an onboard amplifier. The ML4425 has circuitry to ensure that there is no shoot-through in directly driven external power MOSFETs.

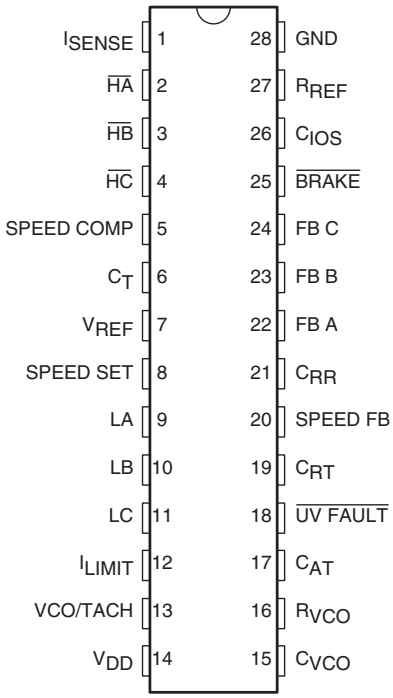
The timing of the start-up sequence is determined by the selection of three timing capacitors. This allows optimization for a wide range of motors and loads.

Block Diagram



Pin Configuration

ML4425
28-Pin Narrow PDIP (P28N)
28-Pin SOIC (S28)



TOP VIEW

Pin Description

Pin	Name	Function
1	I_{SENSE}	Motor current sense input. When I_{SENSE} exceeds 0.2 ↔ I_{LIMIT}, the output drivers LA, LB, and LC are shut off for a fixed time determined by C_{IOS}.
2	$\overline{HA}$	Active low output driver for the phase A high-side switch.
3	$\overline{HB}$	Active low output driver for the phase B high-side switch.
4	$\overline{HC}$	Active low output driver for the phase C high-side switch.
5	SPEED COMP	Speed control loop compensation is set by a series resistor and capacitor from SPEED COMP to GND.
6	C_T	A capacitor from C_T to GND sets the PWM oscillator frequency.
	V_{REF}	6.9V reference voltage output.
8	SPEED SET	Speed loop input which ranges from 0 (stopped) to V_{REF} (maximum speed).
9	LA	Active high output driver for the phase A low-side switch.
10	LB	Active high output driver for the phase B low-side switch.
11	LC	Active high output driver for the phase C low-side switch.
12	I_{LIMIT}	Voltage on this pin sets the I_{SENSE} threshold voltage at 0.2 ↔ I_{LIMIT}, leaving this pin unconnected selects an internally set threshold.
13	VCO/TACH	This TTL level output corresponds to the signal used to clock the commutation state machine. The output frequency is proportional to the motor speed when the back-EMF sensing loop is locked onto the rotor position.
14	V_{DD}	12V power supply input.
15	C_{VCO}	A capacitor to GND sets the voltage-to-frequency ratio of the VCO.

Pin Description (continued)

Pin	Name	Function
16	R_{VCO}	An resistor to GND sets up a current proportional to the input voltage of the VCO.
17	C_{AT}	A capacitor to GND sets the time that the controller stays in the align mode.
18	$\overline{UV\ FAULT}$	This output goes low when V_{DD} drops below the UVLO threshold, and indicates that all output drivers have been disabled.
19	C_{RT}	A capacitor to GND sets the time that the controller stays in the ramp mode.
20	SPEED FB	Output of the back-EMF sampling circuit and input to the VCO. An RC network connected to SPEED FB sets the compensation for the PLL loop formed by the back-EMF sampling circuit, the VCO, and the commutation state machine.
21	C_{RR}	A capacitor to between C_{RR} and SPEED FB sets the ramp rate (acceleration) of the motor when the controller is in ramp mode.
22	FB A	The motor feedback voltage from phase A is monitored through a resistor divider for back-EMF sensing at this pin.
23	FB B	The motor feedback voltage from phase B is monitored through a resistor divider for back-EMF sensing at this pin.
24	FB C	The motor feedback voltage from phase C is monitored through a resistor divider for back-EMF sensing at this pin.
25	$\overline{BRAKE}$	A logic low input activates motor braking by shutting off the high-side output drivers and turning on the low-side output drivers.
26	C_{IOS}	A capacitor to GND sets the time that the low-side output drivers remain off after I_{SENSE} exceeds its threshold .
27	R_{REF}	An 137kΩ resistor to GND sets a current proportional to V_{REF} that is used to set all the internal bias currents except for the VCO.
28	GND	Signal and power ground.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Units
V_{DD}		14	V
Logic Inputs (SPEED FB, $\overline{BRAKE}$)	GND – 0.3	7	V
All Other Inputs and Outputs	GND – 0.3	V_{DD} + 0.3	V
Output Current (LA, LB, LC, $\overline{HA}$, $\overline{HB}$, $\overline{HC}$)		±50	mA
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering 10 sec.)		260	°C
Thermal Resistance (θ_{JA}) 28-Pin Narrow PDIP 28-Pin SOIC		 48 75	 °C/W °C/W

Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range ML4425CX ML4425IX	 0 –40	 70 85	 °C °C
V_{DD}	10.8	13.2	V

Electrical Characteristics

Unless otherwise specified, V_{DD} = 12V ± 10%, R_{SENSE} = 1Ω, C_{VCO} = 10nF, C_{IOS} = 100pF, R_{REF} = 137kΩ, T_A = Operating Temperature Range (Notes 1, 2).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Reference							
V_{REF}	Total Variation	Line, Temp		6.5	6.9	7.5	V
PWM Oscillator							
	Total Variation	C_T = 1nF			28		kHz
	Ramp Peak				3.9		V
	Ramp Valley				1.7		V
	Ramp Charging Current						µA
Speed Control Loop							
	SPEED SET Input Voltage Range			0		V_{REF}	V
	SPEED FB Input Voltage Range			0		V_{REF}	V
	SPEED COMP Output Current			±5		±20	µA
	SPEED SET Error Amp Transconductance	$V_{SPEED\ SET}$ = xV, $V_{SPEED\ FB}$ = yV			144		µ℧
Start-up							
	C_{AT} Charging Current		C Suffix	0.68		0.98	µA
			I Suffix	0.5		1.1	µA
	C_{AT} Threshold Voltage			1.4		1.7	V
	C_{RT} Charging Current		C Suffix	0.68		0.98	µA
			I Suffix	0.5		1.1	µA
	C_{RT} Threshold Voltage			1.4		1.7	V
Voltage Controlled Oscillator							
	Frequency Range	R_{VCO} = 5V, SPEED FB = 6V		1.5	1.85	2.2	kHz
	Frequency vs. SPEED FB	R_{VCO} = 5V, 0.5V ≤ SPEED FB ≤ 7V			300		Hz/V
Current Limit							
	I_{SENSE} Gain	$V(I_{LIMIT})$ ≤ 2.5V		4.5	5.0	5.5	V/V
	One Shot OFF-Time	C_{IOS} = 100pF	C Suffix	9		18	µs
			I Suffix	9		20	µs
Logic Inputs ($\overline{BRAKE}$) (Note 3)							
V_{IH}	Input High Voltage			2			V
V_{IL}	Input Low Voltage					0.8	V
I_{IH}	Input High Current	V_{IH} = 2.4V			2.4		mA
I_{IL}	Input Low Current	V_{IL} = 0.4V			2.9		mA

Electrical Characteristics (continued)

Unless otherwise specified, V_{DD} = 12V ± 10%, R_{SENSE} = 1Ω, C_{VCO} = 10nF, C_{IOS} = 100pF, R_{REF} = 137kΩ, T_A = Operating Temperature Range (Notes 1, 2).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Logic Outputs (VCO/TACH, $\overline{UV\ FAULT}$) (Note 3)							
	VCO/TACH Output High Voltage	I_{OUT} = –100µA		2.2			V
	VCO/TACH Output Low Voltage	I_{OUT} = 400µA				0.6	V
	UV FAULT Output High Voltage	I_{OUT} = –10µA	C Suffix	3.4	4.5	5.4	V
			I Suffix	3.2		5.6	V
	$\overline{UV\ FAULT}$ Output Low Voltage	I_{OUT} = 400µA				0.6	V
Back-EMF Sampler							
	SPEED FB Align Mode Voltage				125	250	mV
	SPEED FB Ramp Mode Current		C Suffix	500		720	nA
			I Suffix	500		750	nA
	SPEED FB Run Mode Current	State A, C_{RT} = 5V, $V_{PHB} = V_{DD}/3$	C Suffix	30		90	µA
			I Suffix	27		90	µA
		State A, C_{RT} = 5V, $V_{PHB} = V_{DD}/2$		–15		15	µA
		State A, C_{RT} = 5V, $V_{PHB} = 2 \leftrightarrow V_{DD}/3$	C Suffix	–90		–30	µA
			I Suffix	–90		–27	µA
Output Drivers							
	High Side Driver Output Low Current	$V_{\overline{HX}}$ = 2V		0.5		1.2	mA
	High Side Driver Output High Voltage	$I_{\overline{HX}}$ = –10µA		V_{CC} – 1.3			V
	Low Side Driver Output Low Voltage	$I_{\overline{LX}}$ = 1mA			0.2	0.7	V
	Low Side Driver Output High Voltage	V(I_{SENSE}) = 0V	C Suffix	V_{DD} – 2.2			V
			I Suffix	V_{DD} – 2.9			V
	Phase C Cross-conduction Lockout Threshold				V_{DD} – 3.0		V
Supply							
I_{DD}	V_{DD} Current				32	50	mA
	UVLO Threshold		C Suffix	8.8	9.5	10.2	V
			I Suffix	8.6		10.3	V
	UVLO Hysteresis				150		mV

Notes:

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.
2. For explanation of states, see Figure 4 and Table 1.
3. The BRAKE and UV FAULT pins each have an internal 4kΩ resistor to the internal reference.

Functional Description

General

The ML4425 provides all the circuitry for sensorless speed control of 3-phase Brushless DC (BLDC) motors. Controller functions include start-up circuitry, back-EMF commutation control, Pulse Width Modulation (PWM) speed control, fixed OFF-time current limiting, braking, and undervoltage protection.

The start-up circuitry aligns the motor to a known position, then ramps up the motor speed to generate a back-EMF signal. A back-EMF sampling circuit controls commutation timing by forming a Phase Locked Loop (PLL). The commutation control circuitry also outputs a speed feedback (SPEED FB) signal used in the speed control loop. The speed control loop consists of an error amplifier and PWM comparator that produce a PWM duty cycle for speed regulation. Motor current is limited by a fixed OFF-time PWM shutdown comparator that is controlled by an external sense resistor. Commutation control, PWM speed control, and current limiting are combined to produce the output driver signals. Six output drivers are used to provide gating signals to an external 3 phase bridge power stage sized for the BLDC motor voltage and current requirements. Additional functions include a braking function and undervoltage protection circuit to shut down the output drivers in the event of a low voltage condition on V_{DD} of the ML4425.

Component Selection

Selecting external components for the ML4425 requires calculations based on the motor's electrical and mechanical parameters. The following is a list of the motor parameters needed for these calculations :

- DC motor supply voltage – V_{MOTOR} (V)
- Maximum operating current – I_{MAX} (A)
- Number of magnetic poles – N
- Back EMF constant – K_e (V-s/Rad)
- Motor torque constant – K_t (Nm/A) ($K_t = K_e$ in SI units)
- Maximum speed of operation RPM_{MAX} (RPM)
- Moment of inertia of the motor and load – J ($Kg\text{-}m^2$)
- Viscous damping factor of the motor and load – ζ

If one or more of the above values is not known, it is still possible to pick components for the ML4425, but some experimentation may be necessary to determine the optimal values. All quantities are in SI units unless otherwise specified. The following formulas should be considered as a starting point for optimization. All calculations for capacitors and resistors should be used as the first approximation for selecting the closest standard value.

Power Supply and Reference

The supply voltage (V_{DD}) is nominally 12V ±10%. A 100nF bypass capacitor to ground should be placed as close as possible to V_{DD}. A 6.9V voltage reference output (V_{REF}) is provided to set the speed command and current limit of the ML4425. A 137kΩ from R_{REF} to GND is required to set up a reference current for internal functions.

Output Drivers

The output drivers LA, LB, LC, $\overline{HA}$, $\overline{HB}$, and $\overline{HC}$ provide totem pole output drive signals for a 3 phase bridge power stage. All control functions in the ML4425 translate to outputs at these pins. LA, LB, and LC provide the low-side drive signals for phases A, B, and C of the 3 phase power stage and are 12V active high signals. $\overline{HA}$, $\overline{HB}$, and $\overline{HC}$ provide the high-side signals and are 12V active low signals.

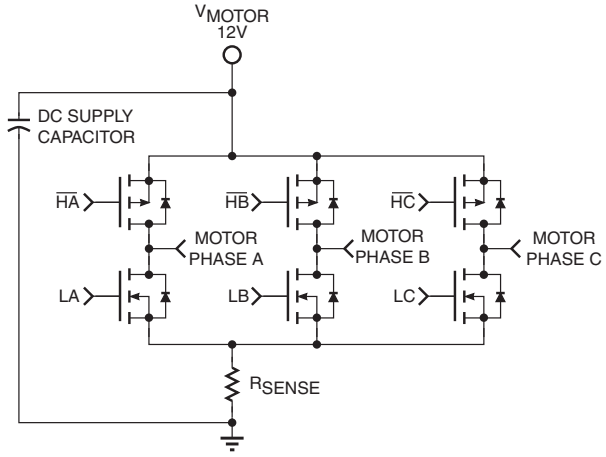


Figure 1. Using R_{SENSE} in a 3-Phase 12V Power Stage

Current Limiting in the Power Stage

The current sense resistor (R_{SENSE}) shown in Figure 1 regulates the maximum current in the power stage and the BLDC motor. Current regulation is accomplished by shutting off the output drivers LA, LB, and LC for a fixed amount of time if the voltage across R_{SENSE} exceeds the current limit threshold.

I_{LIMIT}

The voltage on the I_{LIMIT} pin sets the current limit threshold. The ML4425 has an internal voltage divider from V_{REF} that sets a default current limit threshold of 2.3V (see Figure 2). An external voltage divider referenced to V_{REF} can be used to override the default I_{LIMIT} setting. The external divider should have at least 10 times the current flow of the internal divider.

R_{SENSE}

The function of R_{SENSE} is to provide a voltage proportional to the motor current to set the current limit trip point. The default trip voltage across R_{SENSE} is 460mV, set by the internal I_{LIMIT} divider ratio. The current sense resistor should be a low inductance resistor such as a carbon composition. For resistors in the milliohms range, wire-wound resistors tend to have low values of inductance. R_{SENSE} should be sized to handle the power dissipation ($I_{MAX}^2 \leftrightarrow R_{SENSE}$).

I_{SENSE} Filter

The I_{SENSE} RC lowpass filter is placed in series with the current sense signal as shown in Figure 2. The purpose of this filter is to remove the diode reverse recovery shoottthrough current. This current causes a voltage spike on the leading edge of the current sense signal which may falsely trigger the current limit. The current sense voltage waveform is shown before and after filtering in Figure 3. The recommended starting values for this circuit are R = 1kΩ and C = 330pF. This gives a time constant of 330ns, and will filter out spikes of shorter duration. C can be increased to as much as 2.2nF, but should not exceed a time constant of more than a few microseconds.

C_{IOS}

When I_{SENSE} exceeds $0.2 \leftrightarrow I_{LIMIT}$, the current limit one-shot is activated, turning off LA, LB, and LC for a fixed amount of time (t_{OFF}). t_{OFF} is set by the amount of capacitance connected to C_{IOS}. C_{IOS} is usually set for a fixed off time equal to or less than the PWM period. For a 25kHz PWM frequency, the PWM period is 40μs; t_{OFF} should be between 20μs and 40μs. The lower limit of t_{OFF} is dictated by the minimum on time of the power stage; a safe approximation is 5μs or less. The equation for finding the C_{IOS} capacitance value is as follows:

$$C_{OS} = \frac{t_{OFF} \times 50\mu A}{2.4V} \quad (1)$$

Commutation Control

A 3-phase BLDC motor requires electronic commutation to achieve rotational motion. Electronic commutation requires the switching on and off of the power switches of a 3-phase half bridge. For torque production to be achieved in one direction, the commutation is dictated by the rotor position. Electronic commutation in the ML4425 is achieved by turning on and off, in the proper sequence, one N output from one phase and one P output from another phase. There are six combinations of N and P outputs (six switching states) that constitute a full commutation cycle. These combinations are illustrated in Table 1 and Figure 4, and are labeled states A through F. This sequence is programmed into the commutation state machine. Clocking of the commutation state machine is provided by a voltage controlled oscillator (VCO).

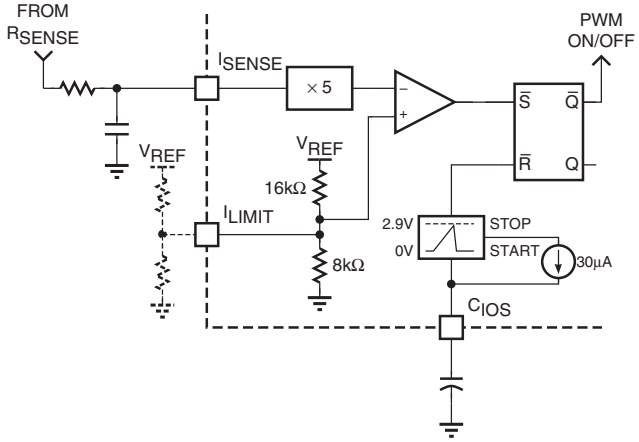


Figure 2. Current Sense Circuitry

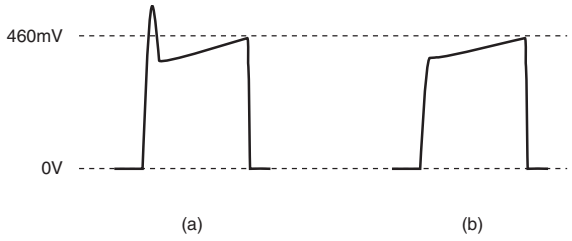


Figure 3. Current Sense Resistor Waveforms (a) Without Filtering, and (b) With Filtering

State	Outputs						Input Sampling
	LA	LB	LC	$\overline{HA}$	$\overline{HB}$	$\overline{HC}$	
R	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	FB B
B	OFF	OFF	ON	OFF	ON	OFF	FB A
C	ON	OFF	OFF	OFF	ON	OFF	FB C
D	ON	OFF	OFF	OFF	OFF	ON	FB B
E	OFF	ON	OFF	OFF	OFF	ON	FB A
F	OFF	ON	OFF	ON	OFF	OFF	FB C

Table 1. Commutation State Functions

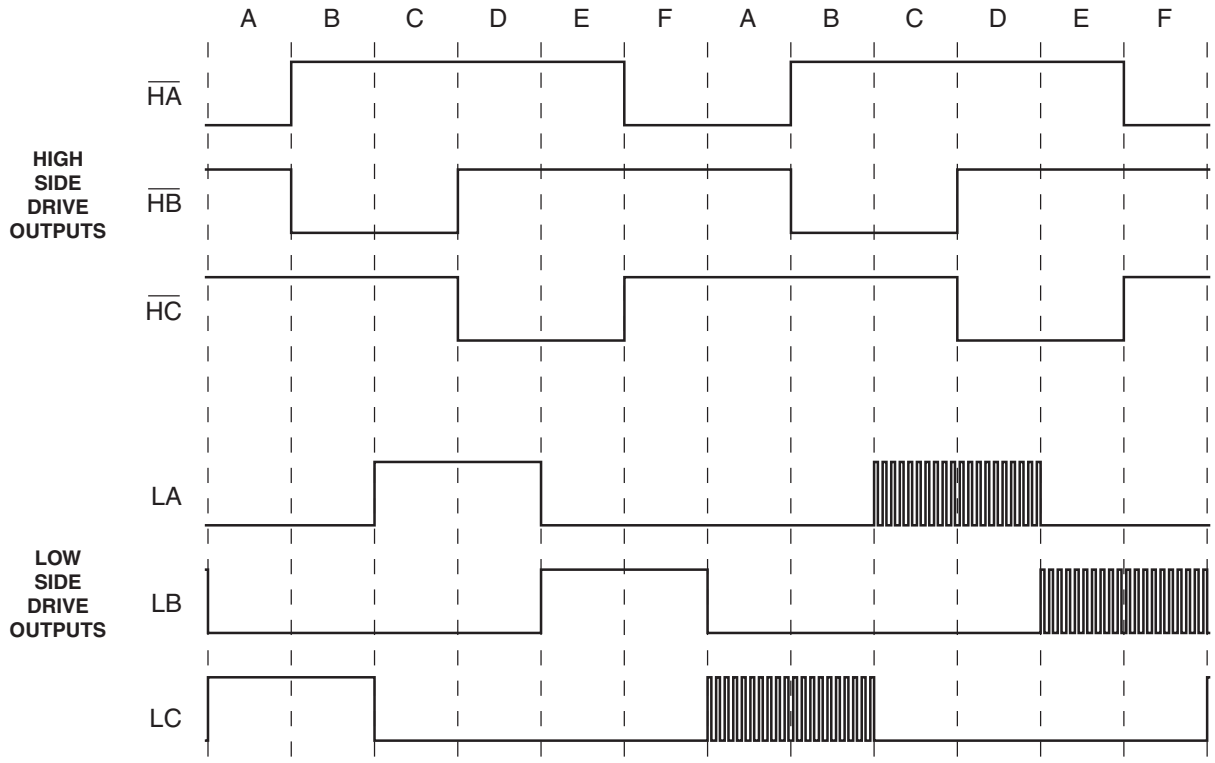


Figure 4. Output Commutation Sequence Timing Diagram
Cycle 1 – Full Commutation, Cycle 2 – Commutation with 50% PWM Duty Cycle

Voltage Controlled Oscillator (VCO)

The VCO provides a TTL compatible clock output on the VCO/TACH pin proportional to the VCO input voltage at the SPEED FB pin. The proportion of frequency to voltage (VCO constant, K_v) is set by an 80.6kΩ resistor on R_{VCO} and a capacitor on C_{VCO} as shown in Figure 5. R_{VCO} sets up a current proportional the VCO input voltage at SPEED FB. This current is used to charge and discharge C_{VCO} between the threshold voltages of 2.3V and 4.3V. The resulting triangle wave on C_{VCO} corresponds to the clock on VCO. K_v should be set so that the VCO output frequency corresponds to the maximum commutation frequency or maximum motor speed when the VCO input is equal to or slightly less than V_{REF}. C_{VCO} is calculated using the following equation:

$$C_{VCO} = \frac{6.5V \times 3.101 \times 10^{-6} \frac{Hz \bullet Farad}{V}}{0.05 \frac{Hz}{RPM} \times N \times SPEED_{MAX}} \quad (2)$$

The closest standard value that is equal to or less than the calculated C_{VCO} should be used.

The maximum frequency on the VCO pin is found by:

$$f_{MAX} = 0.05 \times N \times RPM_{MAX} \quad (3)$$

The voltage at the VCO/TACH pin is equal to the rotor speed. The voltage at SPEED FB is controlled by the back EMF sampler.

Back EMF Sampler

The input to the voltage controlled oscillator is the back EMF sampler. The back EMF sense pins FB A, FB B, and FB C inputs to the back EMF sampler require a signal from the motor phase leads that is below the V_{DD} of the ML4425. The phase sense input impedance is 8kΩ. This requires a series resistor RES1 from the motor phase lead as shown in Figure 6 based on the following equation:

$$RES1 = 670\Omega/V \times (V_{MOTOR} - 10V) \quad (4)$$

The back EMF sampler takes the motor phase voltages divided down to signals that are less than V_{DD} (12V nominal) and calculates the neutral point of the motor by the following equation:

$$Neutral = \frac{PH1 + PH2 + PH3}{3} \quad (5)$$

This allows the ML4425 to compare the back EMF signal to the motor's neutral point without the need for bringing out an extra wire on a WYE wound motor. For DELTA wound motors there is no physical neutral to bring out, so this reference point must be calculated in any case.

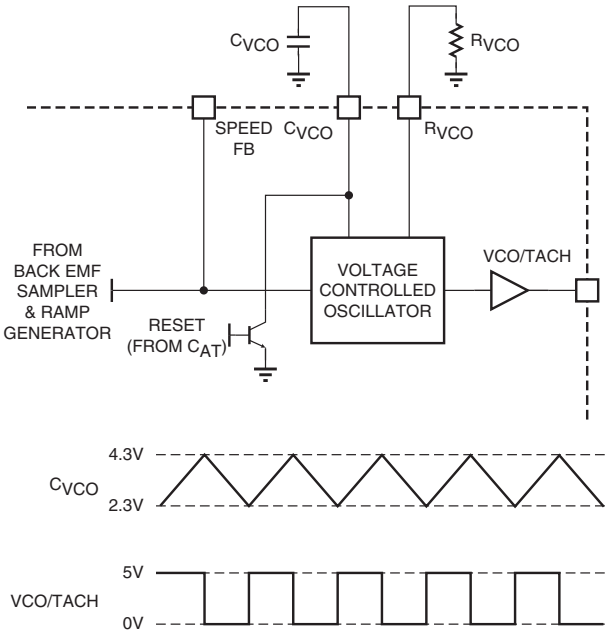


Figure 5. External VCO Component Connections

The back EMF sampler measures the motor phase that is not driven (i.e. if LA and HB are on, then phase A is driven low, phase B is driven high, and phase C is sampled). The sampled phase provides a back EMF signal that is compared against the neutral of the motor. The sampler is controlled by the commutation state machine. The sampled back EMF is compared to the neutral through an error amplifier. The output of the error amplifier outputs a charging or discharging current to SPEED FB, which provides the control voltage to the VCO.

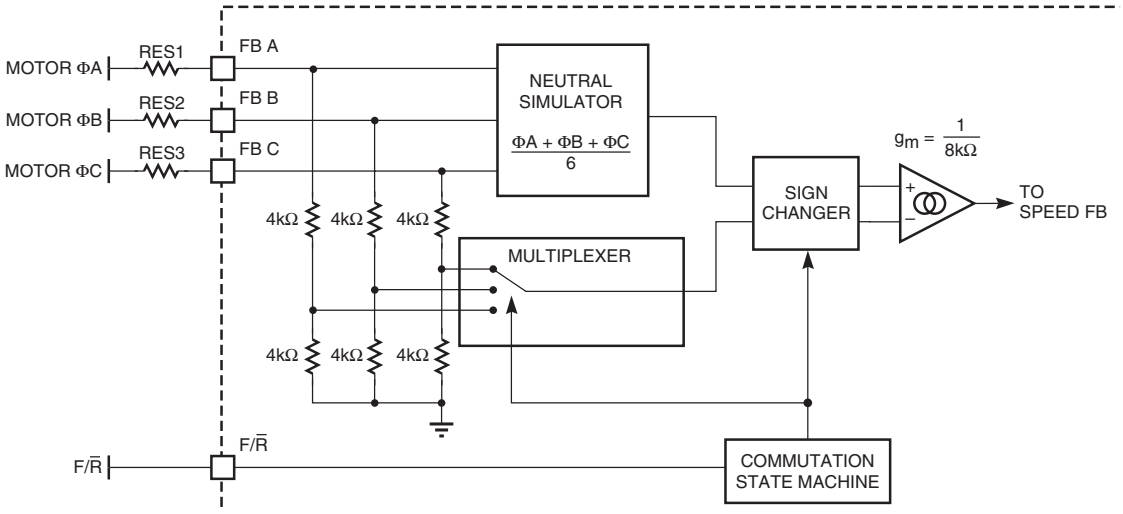


Figure 6. Back EMF Sampler Detailed Block Diagram

Back EMF Sensing PLL Commutation Control

Three blocks form a phase locked loop that locks the commutation clock onto the back EMF signal: the commutation state machine, the voltage controlled oscillator, and the back EMF sampler. The complete phase locked loop is illustrated in Figure 7. The phased locked loop requires a lead lag filter that is set by external components on SPEED FB. The components are selected as follows:

$$C_{SPEEDFB1} = 0.25 \times \frac{K_{O1}}{\sqrt{M}} \times \left(\frac{N_S^2}{\left(\ln\left(\frac{d}{100}\right)^2 \times f_{VCO}^2 \right)} \right) \quad (6a)$$

$$R_{SPEEDFB} = 2 \times M \times \ln\left(\frac{d}{100}\right) \times \frac{f_{VCO}}{N_S \times K_{O1} \times (1 - M)} \quad (6b$$

$$C_{SPEEDFB2} = C_{SPEEDFB1} \times (M - 1) \quad (6c)$$

Start-Up Sequence

When power is first applied to the ML4425 and the motor is at rest, the back EMF is equal to zero. The motor needs to be rotating for the back EMF sampler to lock onto the rotor position and commutate the motor. The ML4425 uses an open loop start-up technique to bring the rotor from rest up to a speed fast enough to allow back EMF sensing. Start-up is comprised of three modes: align mode, ramp mode, and run mode.

Align Mode (RESET)

Before the motor can be started, the rotor must be in a known position. When power is first applied to the ML4425, the controller is reset into the align mode. Align mode turns on the output drivers LB, $\overline{HA}$, and $\overline{HC}$ which aligns the motor into a position 30 electrical degrees before the center of the first commutation state. This is shown as state R in the commutation states of Table 1. Align mode must last long enough to allow the motor and its load to settle into this position. The align mode time is set by a capacitor connected to the C_{AT} pin as shown in Figure 8. C_{AT} is charged by a constant 750μA current from GND to 1.5 V until the align comparator trips to end the align mode. A starting point for C_{AT} is calculated as follows:

$$C_{AT} = \frac{t_S \times 7.5 \times 10^{-7} \times amp}{1.5V} \quad (7)$$

If the align time is not long enough to allow the rotor to settle for reliable starting, then increase C_{AT} until the desired performance is achieved.

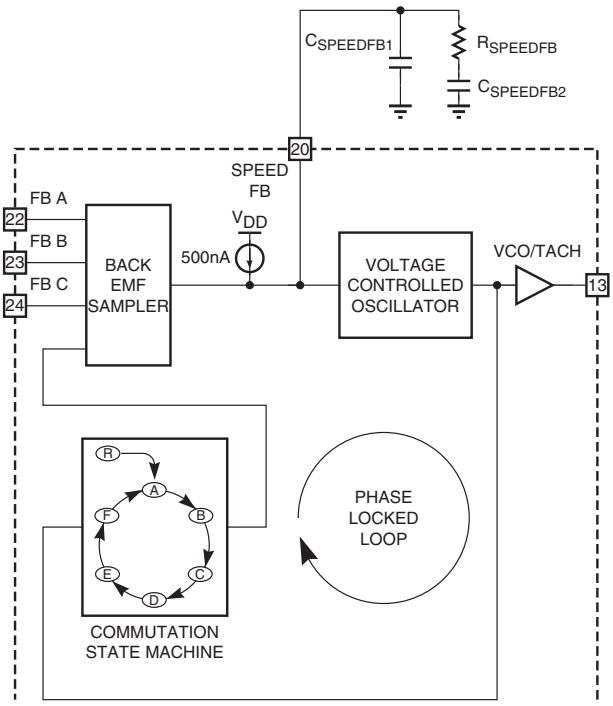


Figure 7. Back EMF Commutation Phase Locked Loop

Ramp Mode

At the end of align mode the controller goes into ramp mode. Ramp mode starts commutating through the states A through F as shown in Table 1. This ramps up the commutation frequency, and therefore the motor speed, for a fixed length of time. This allows the motor to reach a sufficient speed for the back EMF sampler to lock commutation onto the motor's back EMF. The amount of time the ML4425 stays in ramp mode is determined by a capacitor connected to the C_{RT} pin as shown in Figure 8. C_{RT} is charged by a constant 750μA current from GND to 1.5 V until the ramp comparator trips to end the ramp mode. This gives a fixed ramp time. C_{RT} is calculated as follows:

$$C_{RT} = \frac{2\pi \times J \times 5 \times 10^{-7} \times amp \times K_V}{I_{MAX} \times K_t \times 3 \times N} \quad (8)$$

The rate at which the ML4425 ramps up the motor speed is determined by a fixed 500μA current source on the SPEED FB pin. The current sources charges up the PLL filter components causing the VCO frequency to ramp up. During ramp mode, the back EMF sampler is disabled to allow control of the ramping to be set only by the 500μA current source. The ramp based on the SPEED FB filter is generally too fast for the motor to keep up, so a capacitor from C_{RR} to SPEED FB can be added to slow down the ramping rate. The optimal ramp rate is based on the motor and load parameters and is can be adjusted by varying the value of C_{RR}.

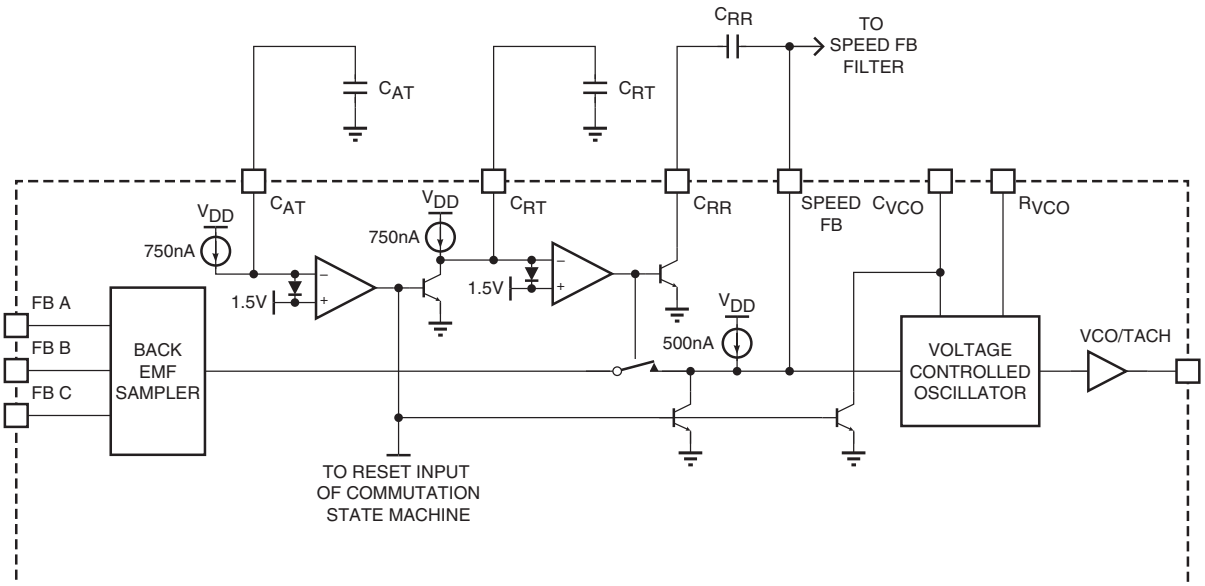


Figure 8. ML4425 Start-up Circuitry for Controlling the Align and Ramp Times

Run Mode (Back EMF Sensing)

At the end of ramp mode the controller goes into run mode. In run mode, the back EMF sensing is enabled and commutation is now under the control of the phase locked loop. Motor speed is now regulated by the speed control loop.

PWM Speed Control

Speed control is accomplished by setting a speed command at SPEED SET with an input voltage from 0 to 6.9V (V_{REF}). The accuracy of the speed command is determined by the external components R_{VCO} and C_{VCO}. There are a number of methods that can be used to control the speed command of the ML4425. One is to use a 10kΩ potentiometer from V_{REF} to ground with the wiper connected to SPEED SET. If SPEED SET is controlled from a microcontroller, one of its DACs can be used with V_{REF} as its input reference.

The speed command is compared with the sensed speed from SPEED FB through a transconductance error amplifier. The output of the speed error amplifier is SPEED COMP. SPEED COMP is clamped between one diode drop above 3.9V (approximately 4.6V) and one diode drop below 1.7V (approximately 1V) to prevent speed loop "wind-up". Speed loop compensation components are connected to this pin as shown in Figure 9. The speed loop compensation components are calculated as follows:

$$C_{SC} = \frac{26.9 \times N \times V_{MOTOR} \times C_{VCO}}{f_{SB} \times K_e \sqrt{2.5 + 98.696 \times \tau m^2 \times f_{SB}^2}} \quad (9a)$$

$$R_{SC} = \frac{10}{2\pi \times f_{SB} \times C_{SC}} \quad (9b)$$

Where f_{SB} is the speed loop bandwidth in Hz.

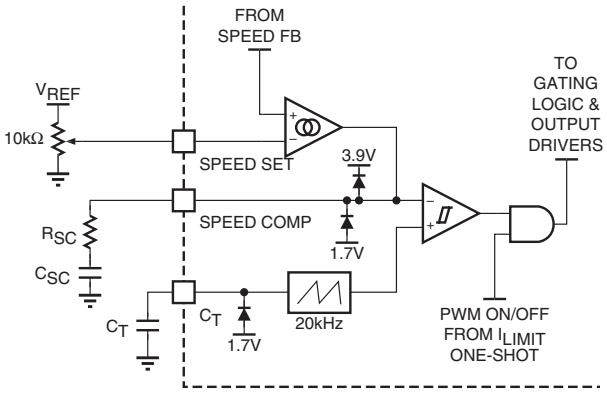


Figure 9. Speed Control Loop Component Connections

The voltage on SPEED COMP is compared with a ramp oscillator to create a PWM duty cycle. The PWM ramp oscillator creates a sawtooth function from 1.7V to 3.9V as shown in Figure 9. A negative clamp at one diode drop below 1.7V (approximately 1V) starts the oscillator on power up. The frequency of the ramp oscillator is set by a capacitor to ground C_{IOS} and is selected using the following equation:

$$C_T = \frac{\frac{I}{f_{PWM}} \times 50\mu A}{2.4V} \quad (10)$$

Where f_{PWM} is the PWM frequency in Hz. The PWM duty cycle from the speed control loop is gated the current limit one shot that controls the LA, LB, and LC output drivers.

Cross Conduction Comparator

When the ML4425 goes from align mode into ramp mode, there is a possibility of cross conduction in phase 3 of the bridge power stage. This cross conduction can happen when $\overline{HC}$ is on in the align mode shown as state R in Table 1, and the controller transitions to state A in ramp mode where $\overline{HC}$ is turned off and LC is turned on. Cross conduction can appear due to the differences in turn on and turn off times of the power devices. To solve this problem, the LC output driver is gated off until the $\overline{HC}$ is equal to V_{DD} – 3V as shown in Figure 10.

Braking

When the $\overline{BRAKE}$ pin is pulled below 1.4V, the low side output drivers LA, LB, and LC are turned on and the high side output drivers HA, HB, HC are turned off. Braking causes rapid deceleration of the motor and current limiting is de-activated, and care should be taken when using the $\overline{BRAKE}$ pin. $\overline{BRAKE}$ is has an internal 4kΩ pull-up as shown in Figure 10, and can be driven by a switch to ground, an open collector or drain logic signal, or a TTL logic signal.

Undervoltage Lockout

Undervoltage lockout is used to protect the 3-phase bridge power stage from a low V_{DD} condition. Undervoltage is triggered at V_{DD} of 9.5V or less and is indicated by a TTL low output on the $\overline{UV\ FAULT}$ pin. Undervoltage lockout also turns off all output drivers (LA, LB, LC, $\overline{HA}$, $\overline{HB}$, and $\overline{HC}$). The comparator that triggers undervoltage lockout has 150mV of hystresis.

Design Considerations

Interfacing to a 3-Phase Bridge Power Stage

The ML4425 output drivers are configured to drive a 3 phase bridge power stage. For applications with buss voltages from 12V up to 80V, level shifting circuitry can be used to drive higher voltage P-channel MOSFETS for the high side switches as shown in Figure 11.

The most flexible configuration is to use high side drivers to control N-Channel MOSFETs (or IGBTs) which allows applications from less than 12V up to 600V. Figure 12 shows the interface between the ML4425 and IR2118 high side drivers from International Rectifier. This configuration is capable of driving motors from busses of up to 320V. The $\overline{BRAKE}$ pin can be pulsed prior to startup with an RC circuit. This charges the bootstrap capacitors (C19, C20, and C21) for the three high side drivers, allowing the reset phase to operate normally. These capacitors must be sized so that they stay sufficiently charged during the align mode. Refer to AN-43 for additional applications information on the ML4425.

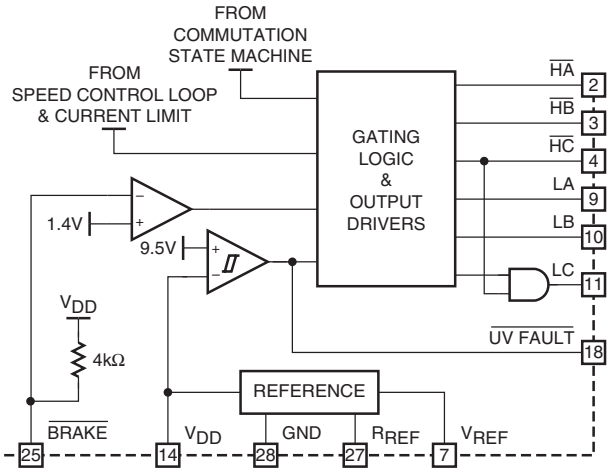


Figure 10. Cross Conduction, Brake, and UVLO Circuits

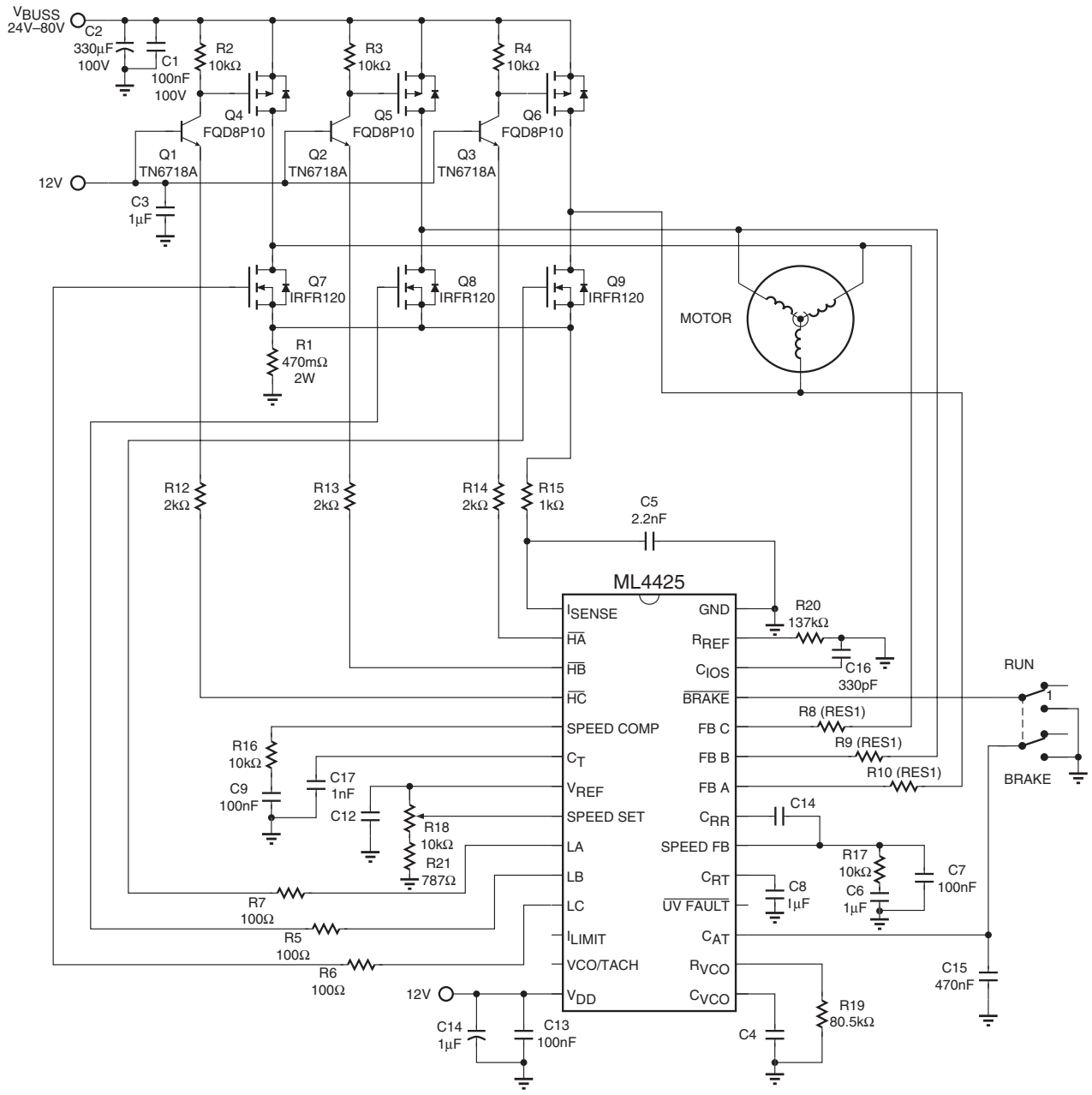


Figure 11. Driving Lower Voltage Motors (12 to 80V)

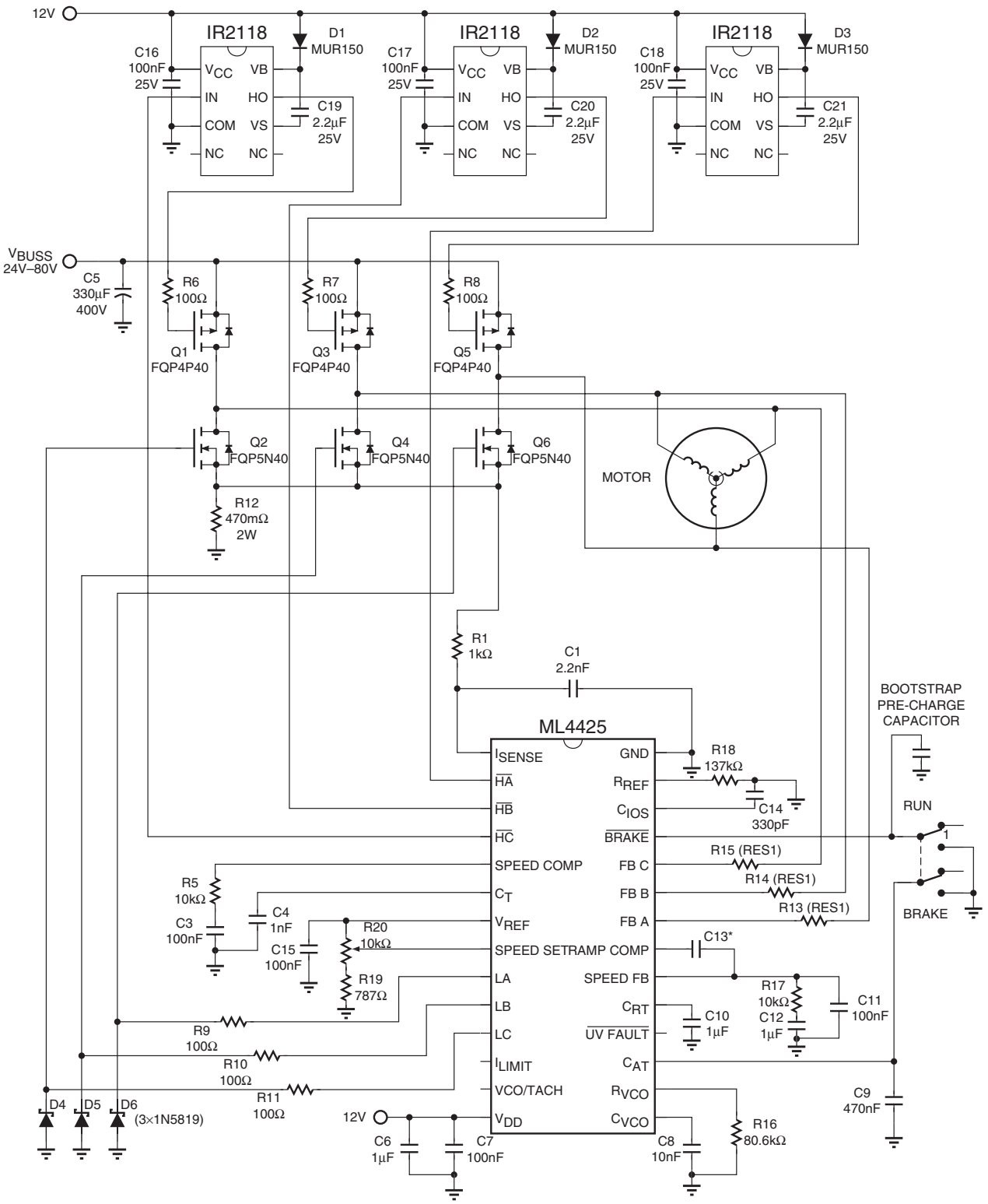
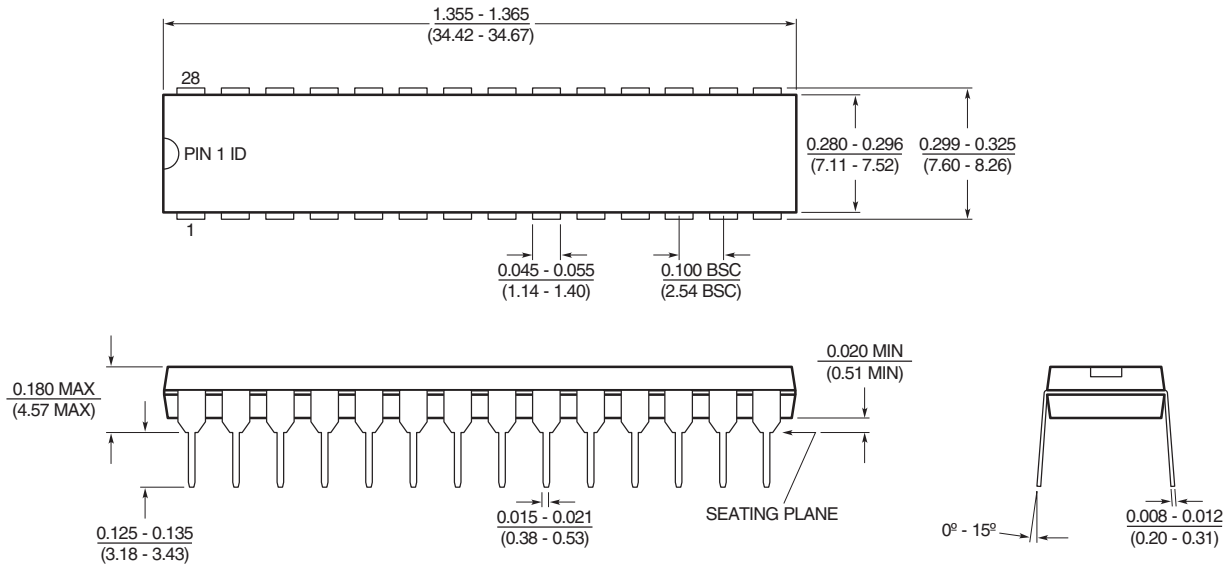


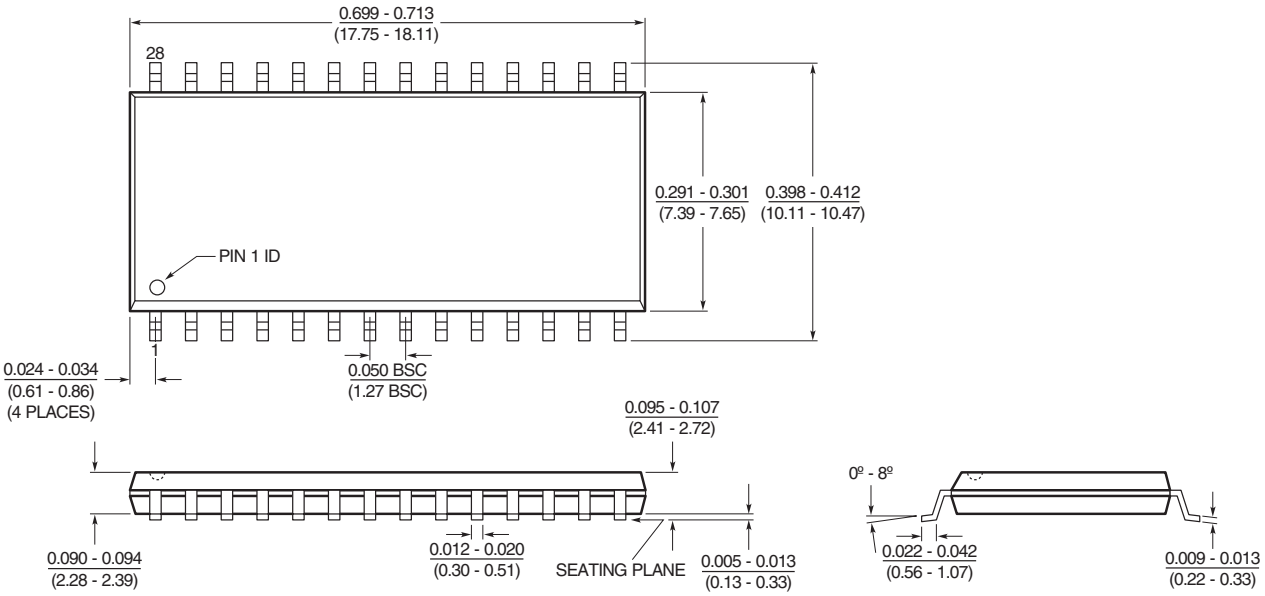
Figure 12. ML4425 High Voltage Motor Drive Application Circuit

Mechanical Dimensions inches (millimeters)

Package: P28N
28-Pin Narrow PDIP



Package: S28
28-Pin SOIC



Ordering Information

Part Number	Temperature Range	Package
ML4425CP	0°C to 70°C	28-Pin PDIP (P28N)
ML4425CS	0°C to 70°C	28-Pin SOIC (S28)
ML4425IP	-40°C to 85°C	28-Pin PDIP (P28N)
ML4425IS	-40°C to 85°C	28-Pin SOIC (S28)

7/2/01 0.0m 003
Stock#DS300042003