# FAN8034

## 6-CH Motor Driver

## Features

- 5-CH Balanced Transformerless (BTL) Driver
- 1-CH (Forward Reverse) Control DC Motor Driver
- Operating Supply Voltage (4.5 V ~ 13.2 V)
- Built in Thermal Shut Down Circuit (TSD)
- Built in Channel Mute Circuit
- Built in Power Save Mode Circuit
- Built in TSD Monitor Circuit
- Built in 2-OP AMPs

## Description

The FAN8034 is a monolithic integrated circuit suitable for a 6-CH motor driver which drives the tracking actuator, focus actuator, sled motor, spindle motor, and tray motor of the CDP/CAR-CD/DVDP systems.

**48-QFPH-1414**

## Typical Application

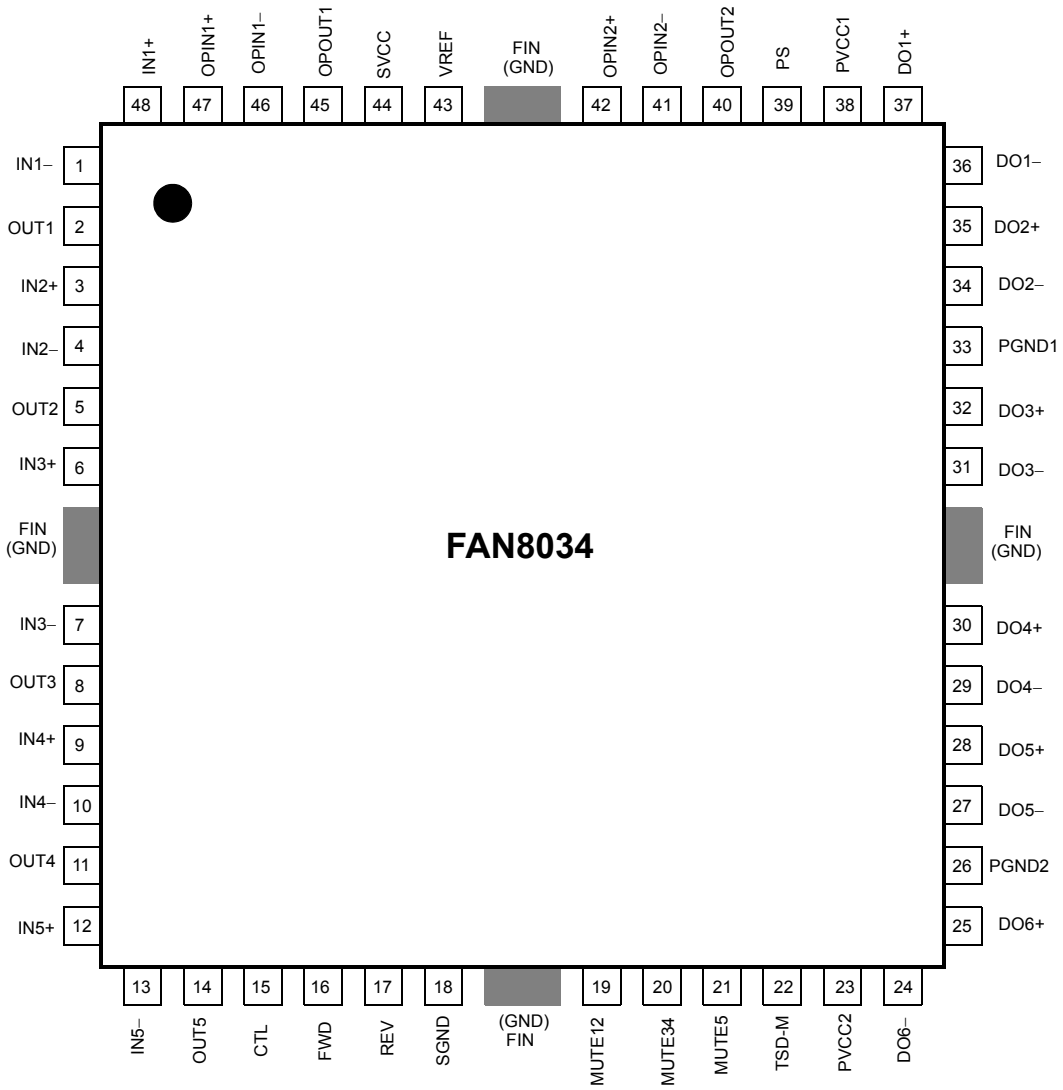
- Compact Disk Player
- Video Compact Disk Player
- Car Compact Disk Player
- Digital Video Disk Player

## Ordering Information

| Device | Package | Operating Temperature |
|---|---|---|
| FAN8034 | 48-QFPH-1414 | -35°C ~ +85°C |
| FAN8034L | 48-QFPH-1414 | -35°C ~ +85°C |
| FAN8034_NL[note] | 48-QFPH-1414 | -35°C ~ +85°C |

**Note:**
NL : Lead free Type

## Pin Assignments



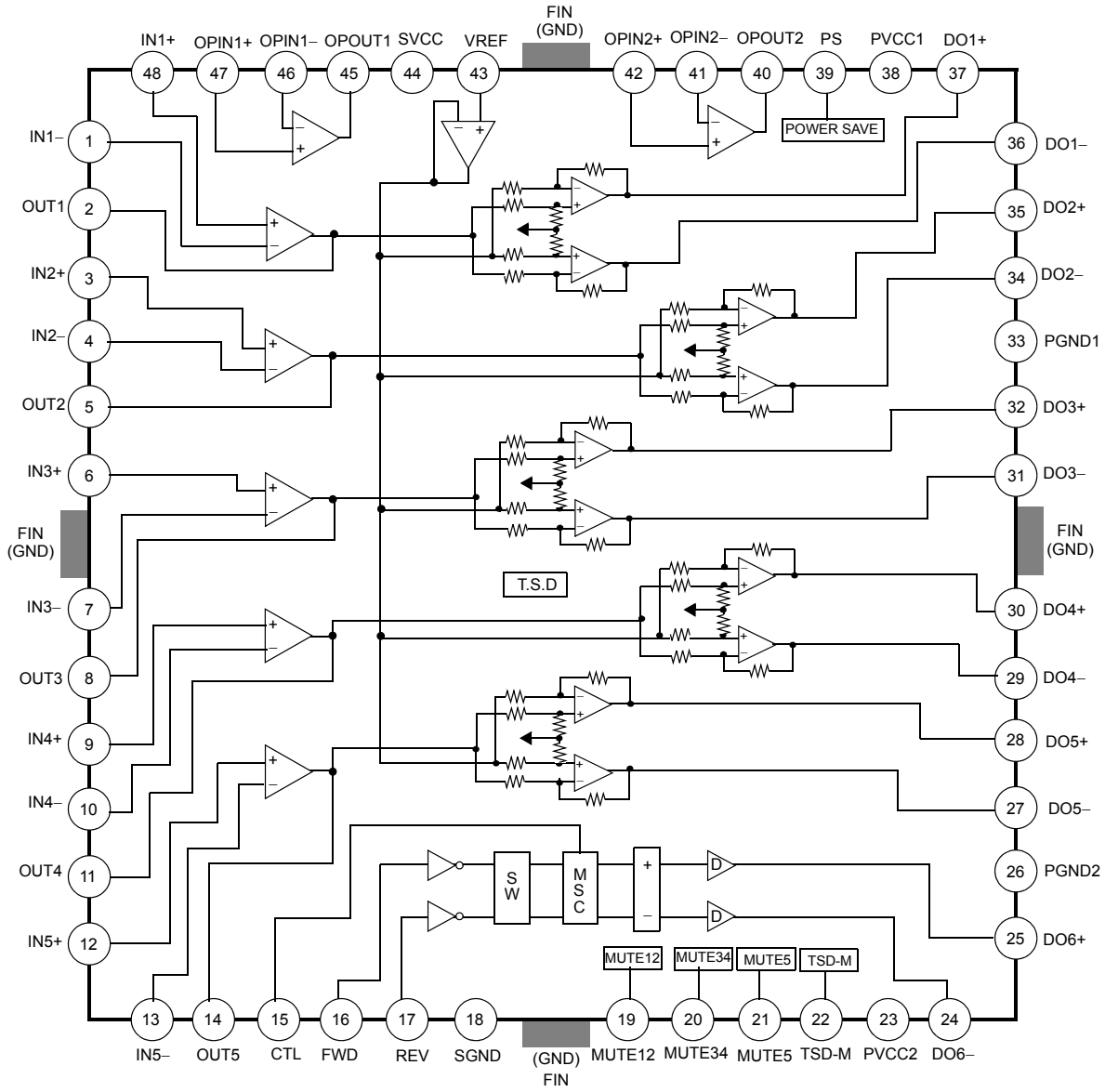
## Pin Definitions

| Pin Number | Pin Name | I/O | Pin Function Description |
|---|---|---|---|
| 1 | IN1- | I | CH1 OP-AMP Input (-) |
| 2 | OUT1 | O | CH1 OP-AMP Output |
| 3 | IN2+ | I | CH2 OP-AMP Input (+) |
| 4 | IN2- | I | CH2 OP-AMP Input (-) |
| 5 | OUT2 | O | CH2 OP-AMP Output |
| 6 | IN3+ | I | CH3 OP-AMP Input (+) |
| 7 | IN3- | I | CH3 OP-AMP Input (-) |
| 8 | OUT3 | O | CH3 OP-AMP Output |
| 9 | IN4+ | I | CH4 OP-AMP Input (+) |
| 10 | IN4- | I | CH4 OP-AMP Input (-) |
| 11 | OUT4 | O | CH4 OP-AMP Output |
| 12 | IN5+ | I | CH5 OP-AMP Input (+) |
| 13 | IN5- | I | CH5 OP-AMP Input (-) |
| 14 | OUT5 | O | CH5 OP-AMP Output |
| 15 | CTL | I | CH6 Motor Speed Control |
| 16 | FWD | I | CH6 Forward Input |
| 17 | REV | I | CH6 Reverse Input |
| 18 | SGND | - | Signal Ground |
| 19 | MUTE12 | I | Mute For CH1,2 |
| 20 | MUTE34 | I | Mute For CH3,4 |
| 21 | MUTE5 | I | Mute For CH5 |
| 22 | TSD-M | O | TSD Monitor |
| 23 | PVCC2 | - | Power Supply Voltage 2 (For CH5, CH6) |
| 24 | DO6- | O | CH6 Drive Ouptut (-) |
| 25 | DO6+ | O | CH6 Drive Output (+) |
| 26 | PGND2 | - | Power Ground 2 (FOR CH5, CH6) |
| 27 | DO5- | O | CH5 Drive Ouptut (-) |
| 28 | DO5+ | O | CH5 Drive Output (+) |
| 29 | DO4- | O | CH4 Drive Ouptut (-) |
| 30 | DO4+ | O | CH4 Drive Output (+) |
| 31 | DO3- | O | CH3 Drive Ouptut (-) |
| 32 | DO3+ | O | CH3 Drive Output (+) |

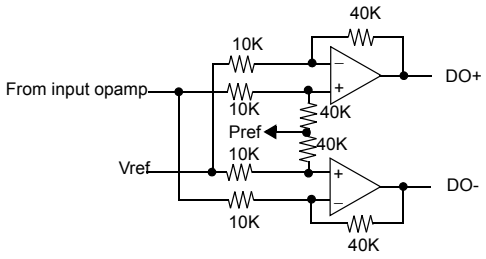
## Pin Definitions (Continued)

| Pin Number | Pin Name | I/O | Pin Function Description |
|---|---|---|---|
| 33 | PGND1 | - | Power Ground 1 (FOR CH1, CH2, CH3, CH4) |
| 34 | DO2- | O | CH2 Drive Ouptut (-) |
| 35 | DO2+ | O | CH2 Drive Output (+) |
| 36 | DO1- | O | CH1 Drive Ouptut (-) |
| 37 | DO1+ | O | CH1 Drive Output (+) |
| 38 | PVCC1 | - | Power Supply Voltage 1 (FOR CH1, CH2, CH3, CH4) |
| 39 | PS | I | Power Save |
| 40 | OPOUT2 | O | Normal OP-AMP2 output |
| 41 | OPIN2- | I | Normal OP-AMP2 Input (-) |
| 42 | OPIN2+ | I | Normal OP-AMP2 Input (+) |
| 43 | VREF | I | Bias Voltage Input |
| 44 | SVCC | - | Signal & OPAMPs Supply Voltage |
| 45 | OPOUT1 | O | Normal OP-AMP1 Output |
| 46 | OPIN1- | I | Normal OP-AMP1 Input (-) |
| 47 | OPIN1+ | I | Normal OP-AMP1 Input (+) |
| 48 | IN1+ | I | CH1 OP-AMP Intput (+) |

## Internal Block Diagram

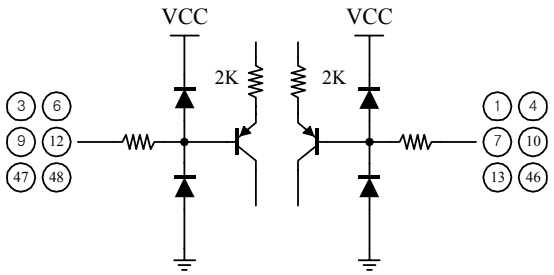
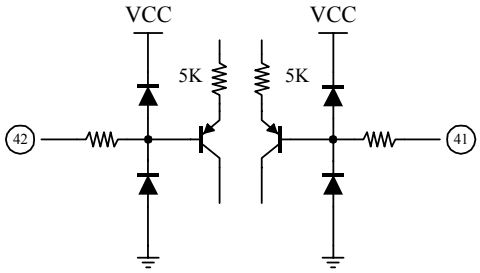
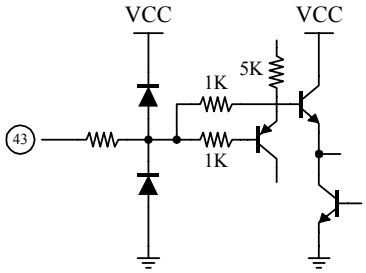
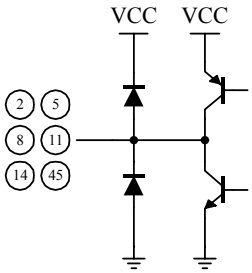



Note. Detailed circuit of the output power amp

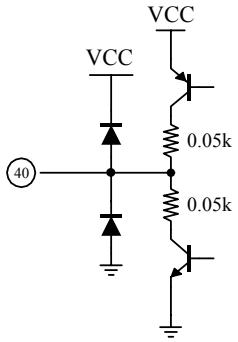
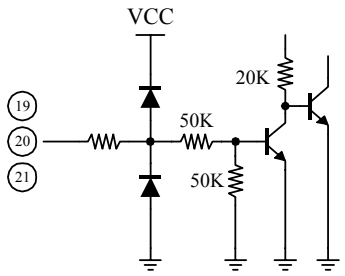
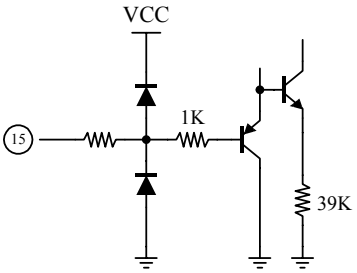
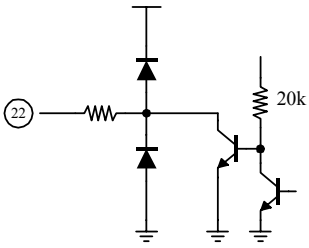



Pref1 is almost PVCC1 / 2
Pref2 is almost PVCC2 / 2

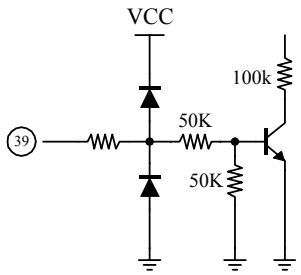
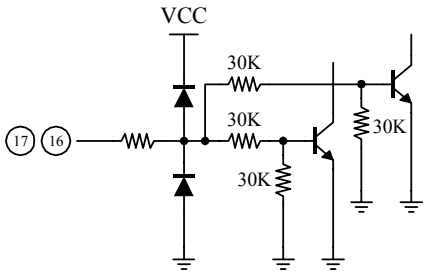
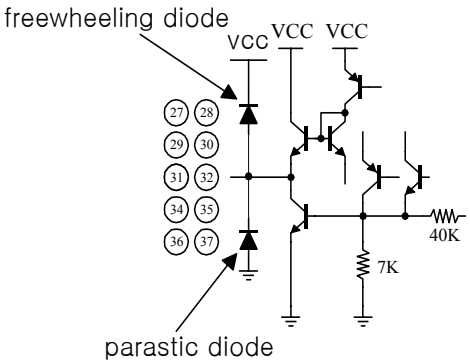
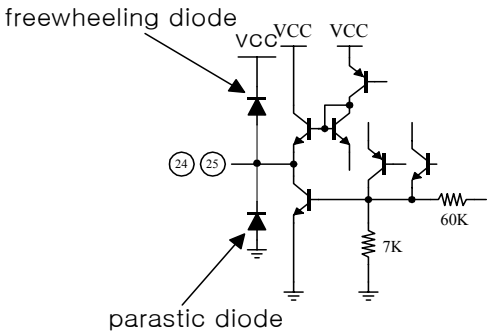
## Equivalent Circuits

| Description | Pin No | Internal Circuit |
|---|---|---|
| BTL INPUT<br>&<br>OP-AMP1 INPUT | 1,4,7,10,13,46<br>3,6,9,12,47,48 |  |
| OP-AMP2 INPUT | 41,42 |  |
| VREF | 43 |  |
| BTL OP-AMP OUT<br>&<br>OP-AMP1 OUT | 2,5,8,11,14,45 |  |

## Equivalent Circuits (Continued)

| Description | Pin No | Internal Circuit |
|---|---|---|
| OP-AMP2 OUT | 40 |   |
| MUTE12,34,5 | 19,20,21 |   |
| CTL | 15 |   |
| TSD-M | 22 |   |

## Equivalent Circuits (Continued)

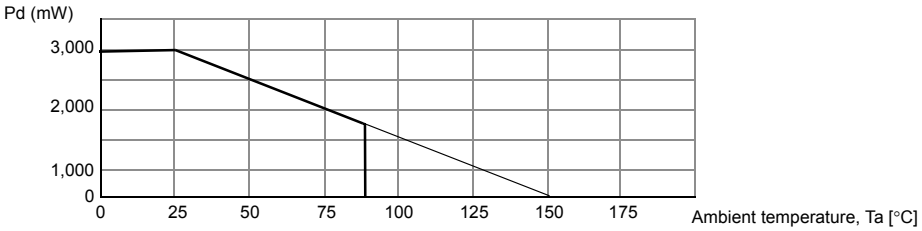
| Description | Pin No | Internal Circuit |
|---|---|---|
| PS | 39 |  |
| FWD,REV | 16,17 |  |
| BTL CH1,2,3,4,5 OUTPUT | 27,28,29,30,31 32,34,35,36,37 |  |
| BTL CH6 OUTPUT | 24,25 |  |

## Absolute Maximum Ratings ( Ta=25°C)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Maximum Supply Voltage | $SVCC_{MAX}$ | 18 | V |
| | $PV_{CC1}$ | 18 | V |
| | $PV_{CC2}$ | 18 | V |
| Power Dissipation | $P_D$ | 3[note] | W |
| Operating Temperature | $T_{OPR}$ | -35 ~ +85 | °C |
| Storge Temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Maximum Output Current | $I_{OMAX}$ | 1 | A |

**Notes:**

1. When mounted on 70mm × 70mm × 1.6mm PCB.
2. Power dissipation is derated with the rate of -24mW/°C for TA≥25°C.
3. Do not exceed $P_D$ and SOA.




## Recommended Operating Conditions ( Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating Supply Voltage | $SV_{CC}$ | 4.5 | - | 13.2 | V |
| | $PV_{CC1}$ | 4.5 | - | 13.2 | V |
| | $PV_{CC2}$ | 4.5 | - | 13.2 | V |

## Electrical Characteristics

($SV_{CC}$ =5V, $PV_{CC1}$ = $PV_{CC2}$ = 11V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Quiescent Circuit Current | $I_{CC}$ | Under no-load | - | 30 | - | mA |
| Power Save On Current | $I_{PS}$[note1] | Under no-load | - | - | 1 | mA |
| Power Save On Voltage | $V_{PSON}$ | Pin39 = Variation | - | - | 0.5 | V |
| Power Save Off Voltage | $V_{PSOFF}$ | Pin39 = Variation | 2 | - | - | V |
| Mute12 On Voltage | $V_{MON12}$ | Pin19 = Variation | - | - | 0.5 | V |
| Mute12 Off Voltage | $V_{MOFF12}$ | Pin19 = Variation | 2 | - | - | V |
| Mute34 On Voltage | $V_{MON34}$ | Pin20 = Variation | - | - | 0.5 | V |
| Mute34 Off Voltage | $V_{MOFF34}$ | Pin20 = Variation | 2 | - | - | V |
| Mute5 On Voltage | $V_{MON5}$ | Pin21 = Variation | - | - | 0.5 | V |
| Mute5 Off Voltage | $V_{MOFF5}$ | Pin21 = Variation | 2 | - | - | V |
| **BTL DRIVER CIRCUIT** | | | | | | |
| Output Offset Voltage | $V_{OO}$ | $V_{IN}$ = 2.5V | -100 | - | +100 | mV |
| Maximum Output Voltage1 | $V_{OM1}$ | $R_L$ = 10Ω | 7.5 | 9.0 | - | V |
| Maximum Output Voltage2 | $V_{OM2}$ | $R_L$ = 18Ω | 8.5 | 9.5 | - | V |
| Closed-loop Voltage Gain | $A_{VF}$ | $V_{IN}$ = 0.1Vrms | 16.8 | 18 | 19.2 | dB |
| Ripple Rejection Ratio[note2] | RR | $V_{IN}$ = 0.1Vrms, f = 120Hz | - | 60 | - | dB |
| Slew Rate[note2] | SR | Square, Vout = 4Vp-p | 1 | 2 | - | V/μs |
| **INPUT OPAMP CIRCUIT** | | | | | | |
| Input Offset Voltage1 | $V_{OF1}$ | - | -10 | - | +10 | mV |
| Input Bias Current1 | $I_{B1}$ | - | - | - | 400 | nA |
| High Level Output Voltage1 | $V_{OH1}$ | - | 4.4 | 4.7 | - | V |
| Low Level Output Voltage1 | $V_{OL1}$ | - | - | 0.2 | 0.5 | V |
| Output Sink Current1 | $I_{SINK1}$ | $R_L$ = 50Ω | 1 | 2 | - | mA |
| Output Source Current1 | $I_{SOU1}$ | $R_L$ = 50Ω | 1 | 2 | - | mA |
| Common Mode Input Range1[note2] | Vicm1 | - | -0.3 | - | 4.0 | V |
| Open Loop Voltage Gain1[note2] | $G_{VO1}$ | $V_{IN}$ = -75dB | - | 80 | - | dB |
| Ripple Rejection Ratio1[note2] | RR1 | $V_{IN}$ = -20dB, f = 120Hz | - | 65 | - | dB |
| Common Mode Rejection Ratio1[note2] | CMRR1 | $V_{IN}$ = -20dB | - | 80 | - | dB |
| Slew Rate1[note2] | SR1 | Square, Vout = 3Vp-p | - | 1.5 | - | V/μs |

**Note :**

1. When the voltage at pin39 goes below 0.5V, the power save circuit makes the main bias current sources stop operating. As a result, the whole circuits are disable. ( The whole circuits mean the driver circuit, the input Op-amp circuit, and the normal Op-amp circuit.)
2. Guaranteed field.(No EDS/Final test)

## Electrical Characteristics (Continued)

($SV_{CC}$ = 5V, $PV_{CC1}$ = $PV_{CC2}$ = 11V, $T_A$ = 25°C, unless otherwise specified)

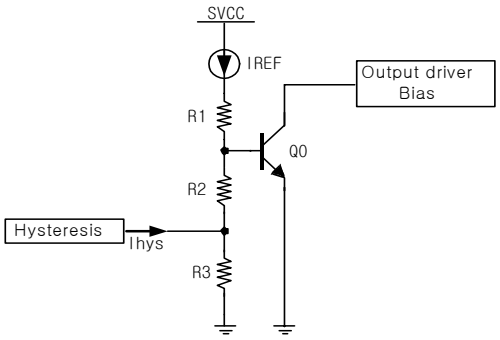
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **NORMAL OP AMP CIRCUIT 1** | | | | | | |
| Input Offset Voltage2 | $V_{OF2}$ | - | -10 | - | +10 | mV |
| Input Bias Current2 | $I_{B2}$ | - | - | - | 400 | nA |
| High Level Output Voltage2 | $V_{OH2}$ | - | 4.4 | 4.7 | - | V |
| Low Level Output Voltage2 | $V_{OL2}$ | - | - | 0.2 | 0.5 | V |
| Output Sink Current2 | $I_{SINK2}$ | $R_L$= 50Ω | 2 | 4 | - | mA |
| Output Source Current2 | $I_{SOU2}$ | $R_L$= 50Ω | 2 | 4 | - | mA |
| Common Mode Input Range2[note] | Vicm2 | - | -0.3 | - | 4.0 | V |
| Open Loop Voltage Gain2[note] | $G_{VO2}$ | $V_{IN}$ = -75dB | - | 80 | - | dB |
| Ripple Rejection Ratio2[note] | RR2 | $V_{IN}$ = -20dB, f = 120Hz | - | 65 | - | dB |
| Common Mode Rejection Ratio2[note] | CMRR2 | $V_{IN}$ = -20dB | - | 80 | - | dB |
| Slew Rate2[note] | SR2 | Square, Vout = 3Vp-p | - | 1.5 | - | V/μs |
| **NORMAL OP AMP CIRCUIT 2** | | | | | | |
| Input Offset Voltage3 | $V_{OF3}$ | - | -15 | - | +15 | mV |
| Input Bias Current3 | $I_{B3}$ | - | - | - | 400 | nA |
| High Level Output Voltage3 | $V_{OH3}$ | - | 3 | 3.8 | - | V |
| Low Level Output Voltage3 | $V_{OL3}$ | - | - | 1.0 | 1.5 | V |
| Output Sink Current3 | $I_{SINK3}$ | $R_L$ = 50Ω | 10 | - | - | mA |
| Output Source Current3 | $I_{SOU3}$ | $R_L$ = 50Ω | 10 | - | - | mA |
| Open Loop Voltage Gain3[note] | $G_{VO3}$ | $V_{IN}$ = -75dB | - | 80 | - | dB |
| Ripple Rejection Ratio3[note] | RR3 | $V_{IN}$ = -20dB, f = 120Hz | - | 65 | - | dB |
| Common Mode Rejection Ratio3[note] | CMRR3 | $V_{IN}$ = -20dB | - | 80 | - | dB |
| Slew Rate3[note] | SR3 | Square, Vout = 3Vp-p | - | 1.5 | - | V/μs |
| **TRAY DRIVE CIRTUIT** | | | | | | |
| Input High Level Voltage | $V_{IH}$ | - | 2 | - | - | V |
| Input Low Level Voltage | $V_{IL}$ | - | - | - | 0.5 | V |
| Output Voltage1 | $V_{O1}$ | $PV_{CC2}$ = 11V, $V_{CTL}$ = 3V, $R_L$= 45Ω | - | 6 | - | V |
| Output Voltage2 | $V_{O2}$ | $PV_{CC2}$ = 13V, $V_{CTL}$ = 4.5V, $R_L$= 45Ω | - | 9 | - | V |
| Output Voltage3 | $V_{O3}$ | $PV_{CC2}$ = 11V, $V_{CTL}$ = 1.5V, $R_L$ = 10Ω | 2.5 | 3 | 3.5 | V |
| Output Load Regulation | $\Delta V_{RL}$ | $V_{CTL}$=3V, $I_L$=100mA → 400mA | - | 300 | 700 | mV |
| Output Offset Voltage1 | $V_{OO1}$ | $V_{IN}$ = 5V, 5V | -40 | - | +40 | mV |
| Output Offset Voltage2 | $V_{OO2}$ | $V_{IN}$ = 0V, 0V | -40 | - | +40 | mV |

**Note:** Guaranteed field.(No EDS/Final test)

# Application Information

## 1. Thermal Shutdown

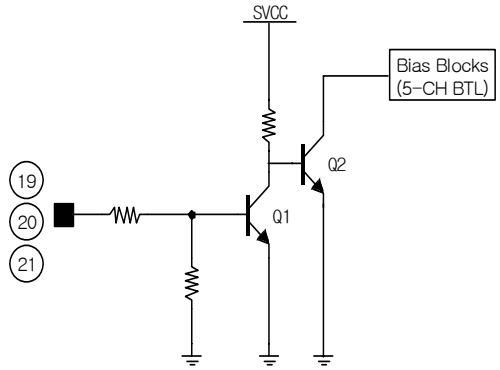
- The TSD circuit is activated at the junction temperature of 160°C and deactivated at 135°C with the hysteresis of 25°C. During the thermal shutdown, the TSD circuit keeps all the output driver off.




## 2. CH Mute Function

- When the mute pin is high, the TR Q1 is on and Q2 is off, so the bias circuit is enabled. When the mute pin is low (GND), the TR Q1 is off and Q2 is on, so the bias circuit is disabled.
- During the mute on state, all the circuit blocks except for the variable regulator remain off, and the low power quiescent state is established.
- Truth table is as follows;

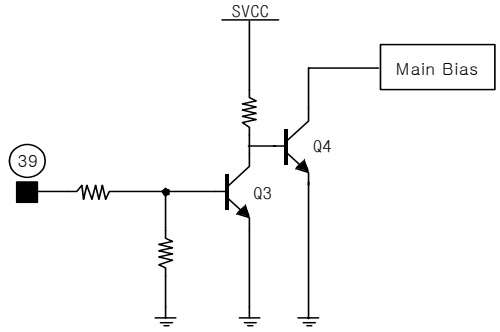
| Pin 19, 20, 21 | Mute |
|---|---|
| High | Mute-Off |
| Low | Mute-On |




## 3. Power Save Function

- When the pin39 is high, the TR Q3 becomes on and Q4 off, so the bias circuit is enabled. When the pin39 is low (GND) , the TR Q3 becomes off and Q4 is on, so the bias circuit is disabled.
- During the power save on state, this function keeps all the circuit blocks off, and the low power quiescent state is established.
- Truth table is as follows;

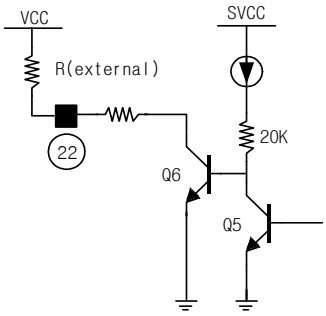
| Pin39 | Power Save |
|---|---|
| High | Power Save Off |
| Low | Power Save On |



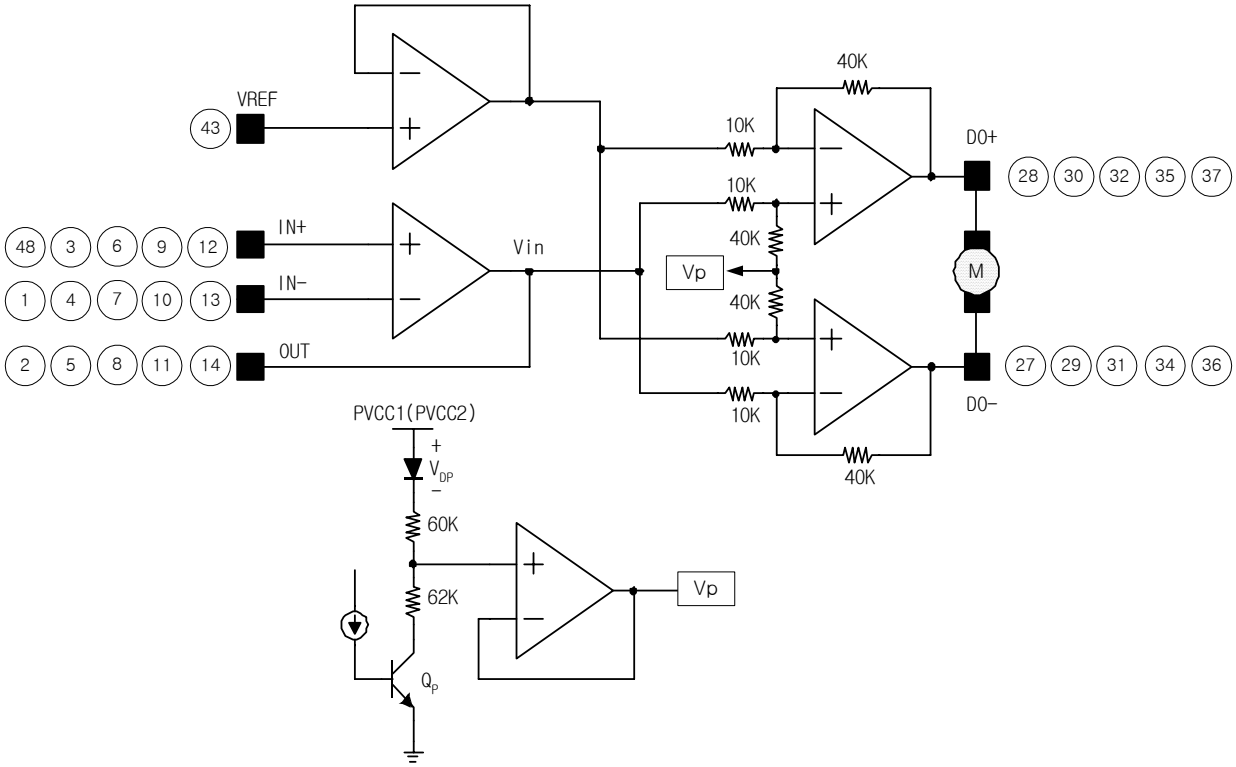

## 4. TDS Monitor Function

- Pin22 is TSD monitor pin, which detects the state of the TSD block and generates the TSD-monitor signal.
- In the normal state Q5 is on, and Q6 is off. When the TSD block is activated Q5 becomes off, and thus the voltage of pin22 keeps low.
- Truth table is as follows;

| TSD | Pin22 |
|---|---|
| TSD Off | High |
| TSD On | Low |



## 5. Focus, Tracking Actuator, Spindle, Sled Motor Drive Part



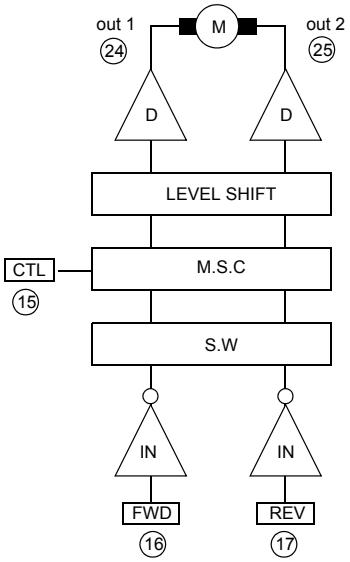

- The Vref at pin 43 is for eliminating the dc components from the input signals and can set by an exteranl circuit.
- The voltage gain from Vin to output is as follows ;

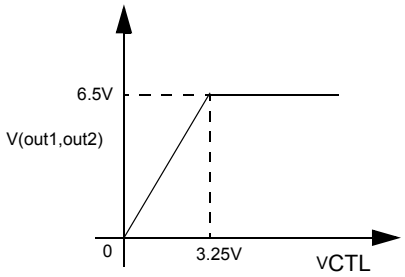
$$Vin = Vref + \Delta V$$
$$DOP = V_D + 4\Delta V$$
$$DON = V_D - 4\Delta V$$
$$Vout = DOP - DON = 8\Delta V$$
$$Gain = 20\log\frac{Vout}{\Delta V} = 20\log 8 = 18dB$$

- Where $\Delta V$ means just ac component.
- The total input to output voltage gain is the sum of the input OP amp network gain and 18dB.
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage Vp is expressed as ;

$$V_P = (PVCC1 - V_{DP} - V_{CESAT}Q_P) \times \frac{62k}{60k + 62k} + V_{CESAT}Q_P$$
$$= \frac{PVCC1 - V_{DP} - V_{CESAT}Q_P}{1.97} + V_{CESAT}Q_P \quad \text{---------- (1)}$$

## 6. Tray, Changer,panel Motor Drive Part



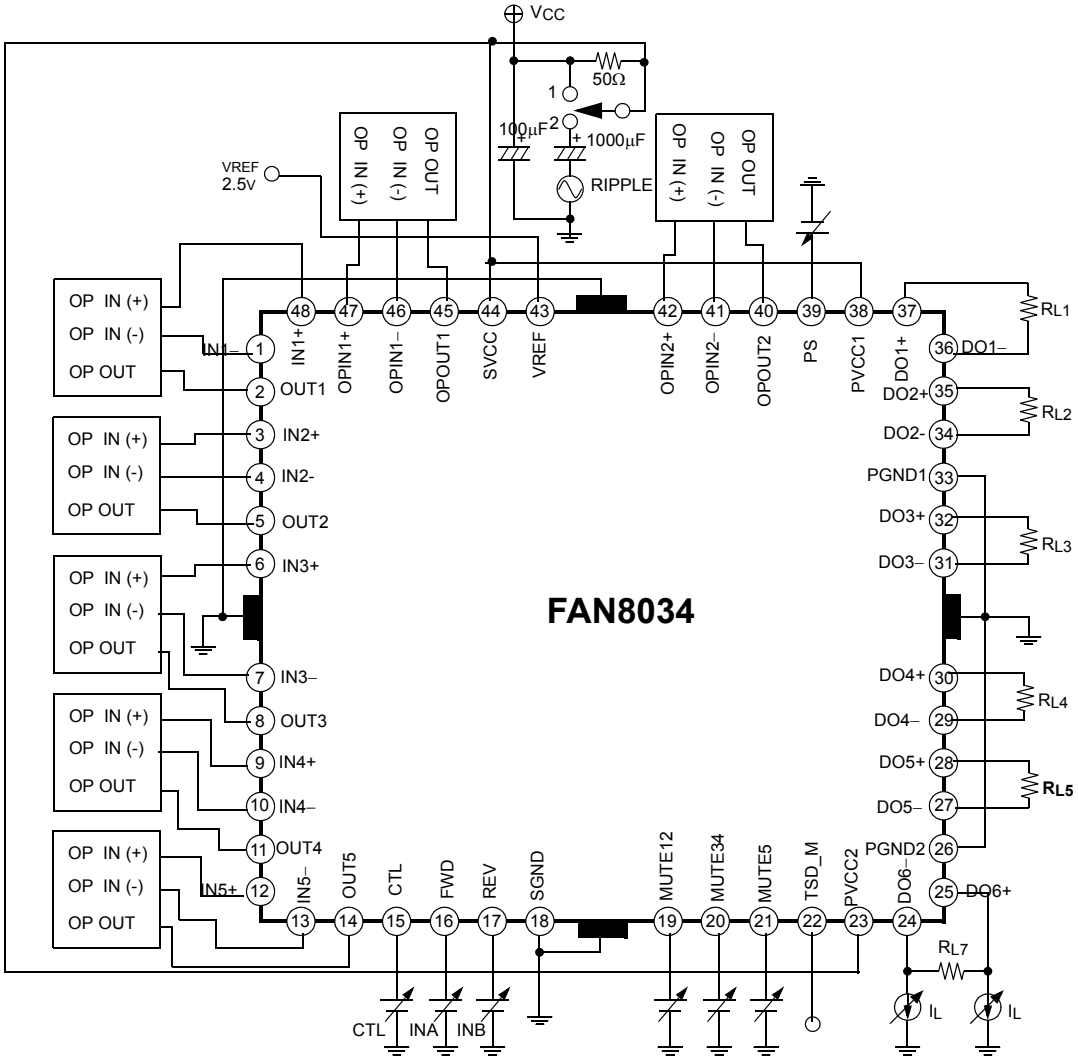



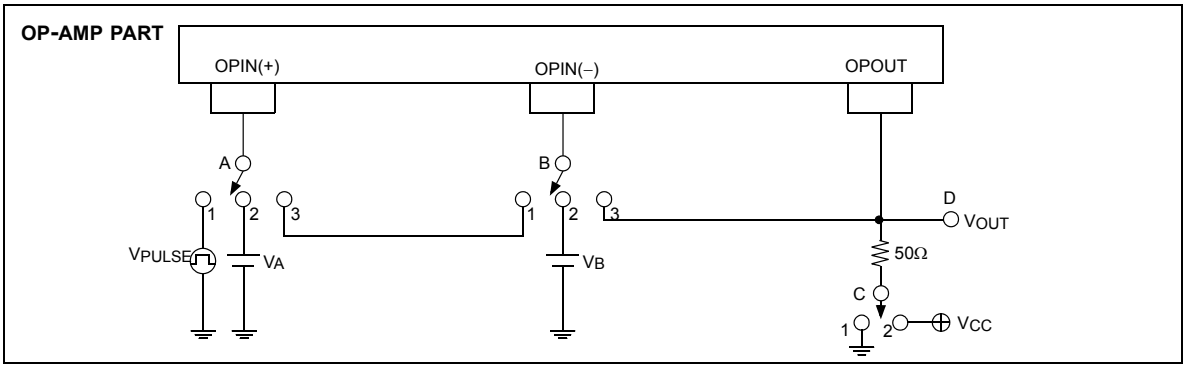

- Rotational direction control
  The forward and reverse rotational direction is controlled by FWD (pin16) and REV (pin17) and the input conditions are as follows;

| INPUT | | OUTPUT | | |
|---|---|---|---|---|
| **FWD** | **REV** | **OUT 1** | **OUT 2** | **State** |
| H | H | Vp | Vp | Brake |
| H | L | H | L | Forward |
| L | H | L | H | Reverse |
| L | L | - | - | Hign impedance |

- Where Vp(Power reference voltage) is approximately 3.75V at $PV_{CC2}$=8V according to equation (1).
- Motor speed control (When $SV_{CC}$=$PV_{CC2}$=8V)
  - The maximum torque is obtained when the pin15(CTL) is open.
  - If the voltage of the pin15 (CTL) is 0V, the motor will not operate.
  - When the control voltage (pin15) is between 0 and 3.25V, the differential output voltage V(out1,out2) is about two times of control voltage. The output gain is 6dB.
  - When the control voltage is greater than 3.25V, the output voltage is saturated at the 6.5V because of the output swing limitation.

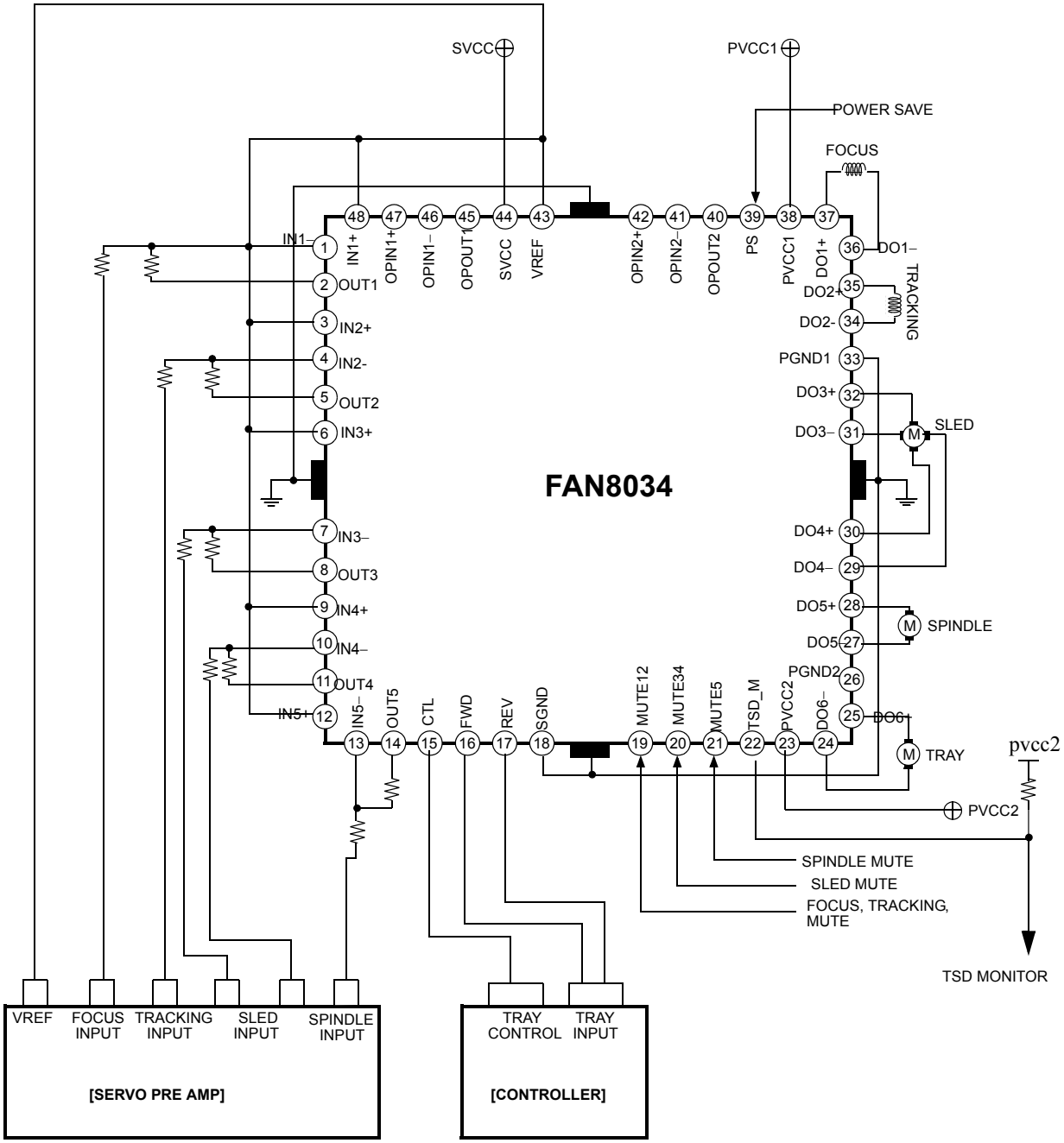
## Test Circuits



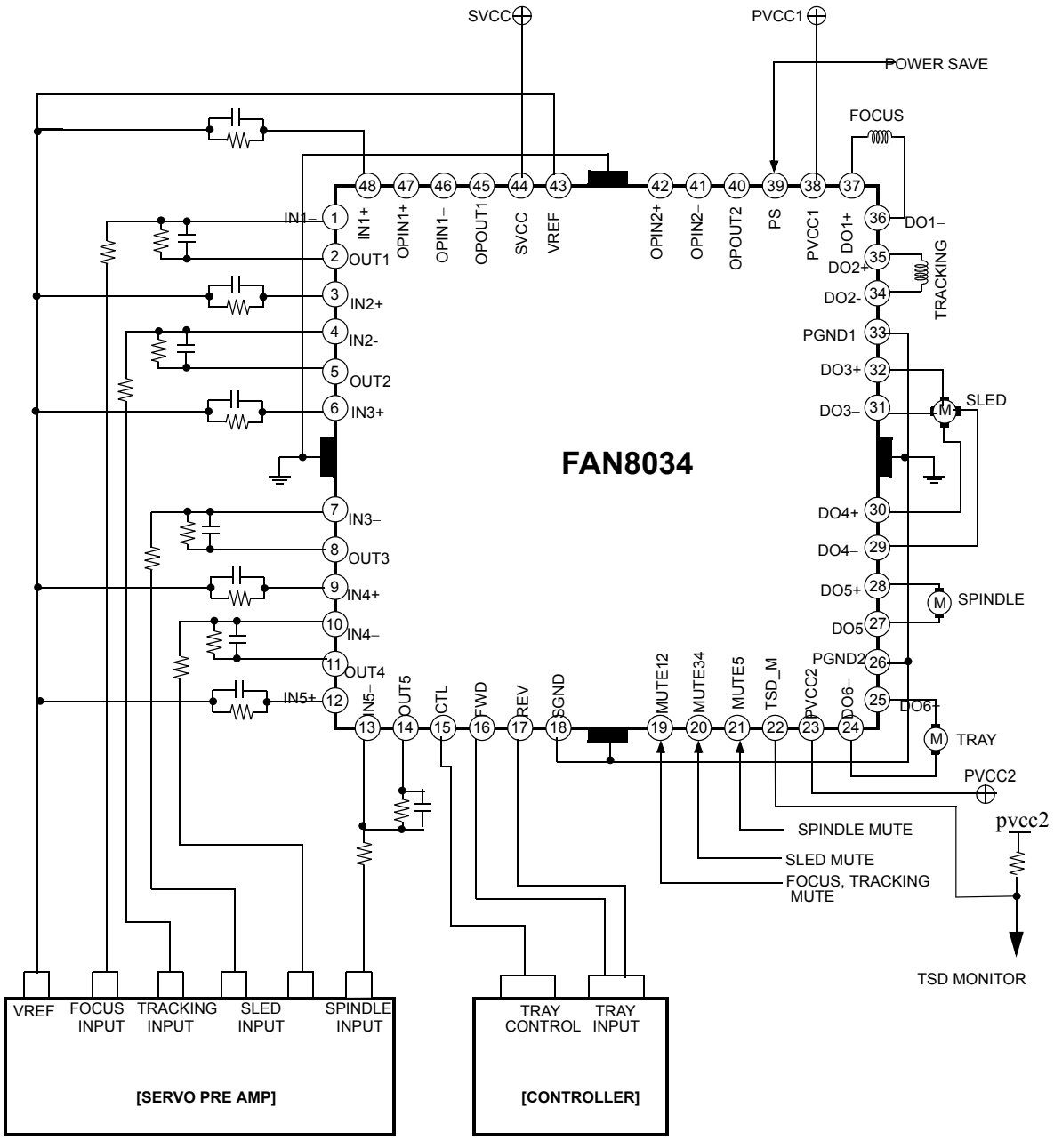
## Typical Application Circuits 1

[Voltage control mode]



## Typical Application Circuits 2

[Differential PWM control mode ]




**Note:**
Radiation pin is connected to the internal GND of the package.

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