SAA7133HL

PCI audio and video broadcast decoder

Rev. 02 — 18 February 2008 **Product data sheet**

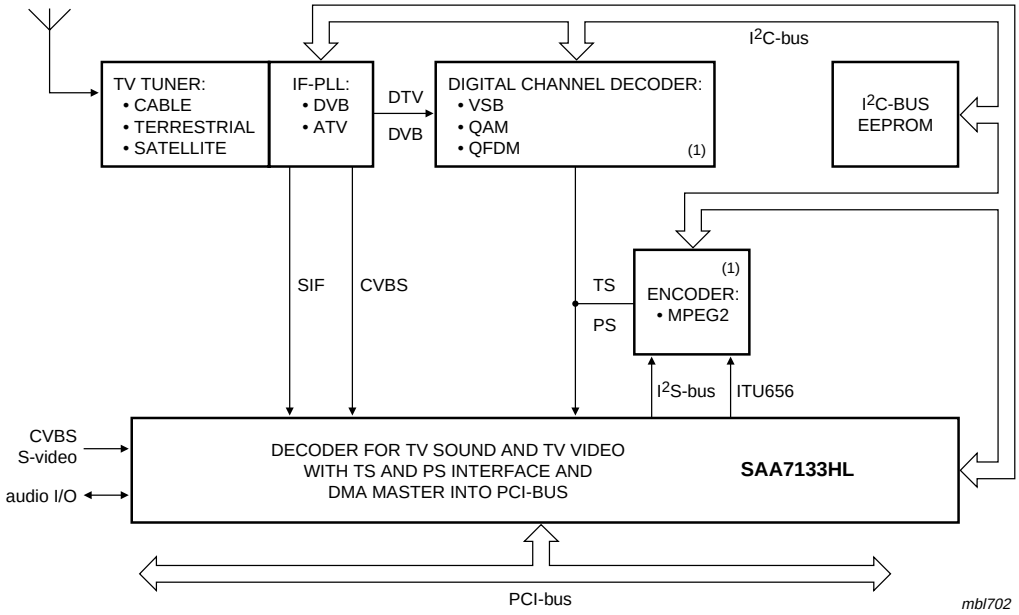
1. General description

1.1 Introduction

The PCI audio and video broadcast decoder SAA7133HL is a highly integrated, low cost and solid foundation for TV capture in the PC, for analog TV and digital video broadcast (DTV and DVB). The various multimedia data types are transported over the PCI-bus by bus-master-write, to optimize the streaming capabilities of a modern host based system; see Figure 1. Legacy requirements are also taken care of.

The SAA7133HL meets the requirements of PC Design Guides 1998, 1999 and 2001 and is PCI 2.2 and Advanced Configuration and Power Interface (ACPI) compliant.

The analog video is sampled by 9-bit ADCs, decoded by a multi-line adaptive comb filter and scaled horizontally, vertically and by field rate. Multiple video output formats (YUV and RGB) are available, including packed and planar, gamma-compensated or black-stretched.



(1) Options.

Fig 1. Application diagram for capturing live TV video and audio streams in the PC, with optional extensions for DTV and DVB capture and MPEG encoding for time shift viewing

Analog TV sound is digitized and stereo decoded (BTSC and EIAJ). Audio is streamed digitally via the PCI-bus or the I^2S-bus or routed as an analog signal via the loop back cable to the sound card. The SAA7133HL provides a versatile peripheral interface to support system extensions, e.g. MPEG encoding for time shift viewing.

The channel decoder for digital video broadcast reception (ATSC or DVB) can re-use the integrated video ADCs.

The Transport Stream (TS) or Program Stream (PS) is collected by a tailored interface and pumped through the PCI-bus to the system memory in well-defined buffer structures. Various internal events, or peripheral status information, can be enabled as an interrupt on the PCI-bus.

2. Features

2.1 General

- Package: LQFP128
- Power supply: 3.3 V only
- Power consumption of typical application: 1.35 W
- PCI-bus power management interface specification, rev. 1.1, compliant (supported states: D0, D1, D2 and D3-hot)
- Power-down state (D3-hot): < 20 mW
- All interface signals 5 V tolerant
- Reference designs available
- Software Development Kit (SDK) for Windows (2000 and XP), Video for Windows (VfW), Windows Driver Model (WDM) and Broadcast Driver Architecture (BDA)

2.2 TV video decoder and video scaling

- All-standards TV decoder: NTSC, PAL and SECAM
- Five analog video inputs: CVBS and S-video
- Video digitizing by two 9-bit ADCs at 27 MHz
- Sampling according *ITU-R BT.601* with 720 pixels per line
- Adaptive comb filter for NTSC and PAL, also operating for non-standard signals
- Automatic TV standard detection
- Three level Macrovision copy protection detection according to *Macrovision detect specification Rev.1*
- Control of brightness, contrast, saturation and hue
- Versatile filter bandwidth selection
- Horizontal and vertical downscaling or zoom
- Adaptive anti-alias filtering
- Capture of raw VBI samples
- Two alternating settings for active video scaling, e.g. for independent capturing and preview definition
- Output in YUV or RGB
- Gamma compensation, black stretching

2.3 TV sound decoder and TV audio I/O

- BTSC and EIAJ TV sound decoder
- dbx-TV Noise Reduction decoding for BTSC systems
- FM radio stereo decoding
- Input of analog SIF signal and 8-bit ADC at 24.576 MHz
- Automatic sound standard detection
- Automatic dematrixing (stereo, dual)
- Volume, balance, bass and treble control
- Automatic Volume Levelling (AVL)
- Incredible Mono, Incredible Stereo
- Audio sampling clock can be locked to video frame rate (no drift of audio stream against video stream)
- Four analog audio baseband inputs (two stereo pairs) and on-chip stereo ADCs
- Supported audio sampling rates: 32 kHz, 44.1 kHz and 48 kHz
- Input of external audio reference clock, e.g. 24.576 MHz
- Output of audio master clock ($768 \times f_s$, $512 \times f_s$, $384 \times f_s$ or $256 \times f_s$ selectable)

2.4 PCI and DMA bus mastering

- PCI 2.2 compliant including full Advanced Configuration and Power Interface (ACPI)
- 3.3 V and 5 V compliant
- System vendor ID, etc. via I^2C-bus EEPROM
- DMA bus master write for video, audio, VBI and TS or PS
- Configurable PCI FIFOs, graceful overflow recovery
- Packed and planar video formats, overlay clipping
- Hardware support for virtual addressing by Memory Management Unit (MMU)

2.5 Peripheral interface

- I^2C-bus master interface: 3.3 V and 5 V compatible, 100 kHz and 400 kHz mode
- The device can operate without PCI-bus (using I^2C-bus) for stand-alone applications
- Digital video output: ITU, VIP, VMI and ZV formats
- Two digital audio outputs: I^2S-bus for up to 4 channels
- Analog stereo audio output
- Integrated analog audio pass-through
- Support for analog audio loop back cable to sound card
- TS input: serial or parallel
- MPEG elementary or program stream input, parallel
- General purpose I/O, e.g. for strapping and interrupt
- Propagate reset and ACPI state D3

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAA7133HL	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

4. Block diagram

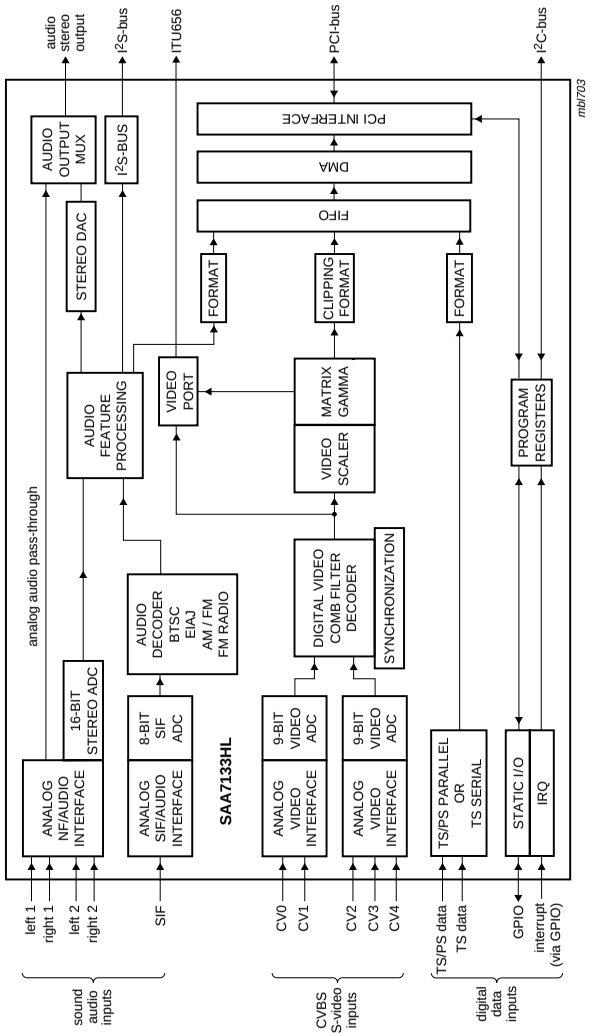


Fig 2. Block diagram

5. Pinning information

5.1 Pinning

The SAA7133HL is packaged in a rectangular LQFP (low profile quad flat package) with 128 pins (see Figure 3).

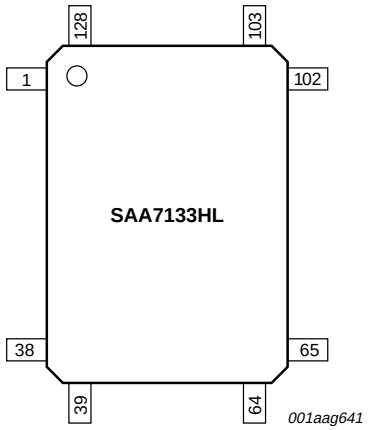


Fig 3. Pin configuration

The pin description for the functional groups is given in Section 5.2:

Table 2. Pin allocation table.

Pins sorted by number

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{DDD}	33	C/BE[1]#	65	V_{DDD}	97	V_{SSA}
2	GNT#	34	AD[15]	66	V_CLK	98	RIGHT1
3	REQ#	35	AD[14]	67	GPIO17	99	V_{REF0}
4	AD[31]	36	AD[13]	68	GPIO16	100	RIGHT2
5	AD[30]	37	AD[12]	69	GPIO15	101	V_{REF1}
6	AD[29]	38	V_{DDD}	70	GPIO14	102	V_{REF2}
7	AD[28]	39	V_{SSD}	71	GPIO13	103	OUT_RIGHT
8	AD[27]	40	PCI_CLK	72	GPIO12	104	OUT_LEFT
9	AD[26]	41	AD[11]	73	V_{DDD}	105	$\overline{\text{PROP\_RST}}$
10	AD[25]	42	AD[10]	74	V_{SSD}	106	SIF
11	AD[24]	43	AD[09]	75	GPIO11	107	V_{REF3}
12	C/BE[3]#	44	AD[08]	76	GPIO10	108	V_{SSA}
13	IDSEL	45	C/BE[0]#	77	GPIO9	109	CV2_C
14	AD[23]	46	AD[07]	78	GPIO8	110	V_{DDA}
15	AD[22]	47	AD[06]	79	GPIO7	111	V_{REF4}
16	AD[21]	48	AD[05]	80	GPIO6	112	DRCV_Y
17	AD[20]	49	AD[04]	81	GPIO5	113	V_{SSA}
18	AD[19]	50	AD[03]	82	GPIO4	114	CV0_Y

Table 2. Pin allocation table. *…continued*

Pins sorted by number

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
19	V_{DDD}	51	AD[02]	83	GPIO3	115	V_{DDA}
20	V_{SSD}	52	AD[01]	84	GPIO2	116	CV1_Y
21	AD[18]	53	AD[00]	85	GPIO1	117	DRCV_C
22	AD[17]	54	V_{DDD}	86	GPIO0	118	CV3_C
23	AD[16]	55	V_{SSD}	87	GPIO27	119	V_{SSA}
24	C/BE[2]#	56	GPIO23	88	GPIO26	120	CV4
25	FRAME#	57	GPIO22	89	GPIO25	121	$\overline{TRST}$
26	IRDY#	58	GPIO21	90	SCL	122	TCK
27	TRDY#	59	GPIO20	91	SDA	123	TMS
28	DEVSEL#	60	GPIO19	92	V_{DDD}	124	TDO
29	STOP#	61	GPIO18	93	V_{SSD}	125	TDI
30	PERR#	62	XTALI	94	LEFT2	126	INT_A
31	SERR#	63	XTALO	95	V_{DDA}	127	PCI_RST#
32	PAR	64	V_{SSD}	96	LEFT1	128	V_{SSD}

5.2 Pin description

Table 3. Pin description overview

Pin category	Table number
Power supply pins	Table 4
Joint Test Action Group (JTAG) test interface pins for Boundary Scan Test (BST)	Table 5
I^2C-bus multi-master interface	Table 6
PCI interface pins	Table 7
General purpose interface (pins GPIO) and the main functions	Table 8
Analog interface pins	Table 9
Characteristics of pin types and remarks	Table 10

Table 4. Power supply pins

Symbol	Pin	Type	Description
V_{SSA}	97, 108, 113 and 119	AG	analog ground for integrated analog signal processing
V_{DDA}	95, 110 and 115	AS	3.3 V analog supply voltage for integrated analog signal processing
V_{SSD}	20, 39, 55, 64, 74, 93 and 128	VG	digital ground for digital circuit, core and I/Os
V_{DDD}	1, 19, 38, 54, 65, 73 and 92	VS	3.3 V digital supply voltage for digital circuit, core and I/Os[1]

[1] The next generation products of this product family will be pin compatible with its predecessors but with a core supply voltage of 1.8 V.

Table 5. JTAG test interface pins

Symbol	Pin	Type	Description
$\overline{\text{TRST}}$	121	I	test reset input: drive LOW for normal operating (active LOW)
TCK	122	I	test clock input: drive LOW for normal operating
TMS	123	I	test mode select input: tie HIGH or let float for normal operating
TDO	124	O	test serial data output: 3-state
TDI	125	I	test serial data input: tie HIGH or let float for normal operating

Table 6. I^2C-bus multi-master interface

Symbol	Pin	Type	Description
SCL	90	IO2	serial clock input (slave mode) or output (multi-master mode)
SDA	91	IO2	serial data input and output; always available
$\overline{\text{PROP\_RST}}$	105	GO	propagate reset and D3-hot output; to peripheral board circuitry (active LOW)

Table 7. PCI interface pins [1]

Symbol	Pin	Type	Description
PCI_CLK	40	PI	PCI clock input: reference for all bus transactions, up to 33.33 MHz
PCI_RST#	127	PI	PCI reset input: will 3-state all PCI pins (active LOW)
AD[31] to AD[00]	4 to 11, 14 to 18, 21 to 23, 34 to 37, 41 to 44 and 46 to 53	PIO and T/S	multiplexed address and data input or output: bidirectional, 3-state
C/BE[3]# to C/BE[0]#	12, 24, 33 and 45	PIO and T/S	command code input or output: indicates type of requested transaction and byte enable, for byte aligned transactions (active LOW)
PAR	32	PIO and T/S	parity input or output: driven by the data source, even parity over all pins AD and C/BE#
FRAME#	25	PIO and S/T/S	frame input or output: driven by the current bus master (owner), to indicate the beginning and duration of a bus transaction (active LOW)
TRDY#	27	PIO and S/T/S	target ready input or output: driven by the addressed target, to indicate readiness for requested transaction (active LOW)
IRDY#	26	PIO and S/T/S	initiator ready input or output: driven by the initiator, to indicate readiness to continue transaction (active LOW)
STOP#	29	PIO and S/T/S	stop input or output: target is requesting the master to stop the current transaction (active LOW)
IDSEL	13	PI	initialization device select input: this input is used to select the SAA7133HL during configuration read and write transactions
DEVSEL#	28	PIO and S/T/S	device select input or output: driven by the target device, to acknowledge address decoding (active LOW)
REQ#	3	PO	PCI request output: the SAA7133HL requests master access to PCI-bus (active LOW)
GNT#	2	PI	PCI grant input: the SAA7133HL is granted to master access PCI-bus (active LOW)

Table 7. PCI interface pins *...continued*[1]

Symbol	Pin	Type	Description
INT_A	126	PO and O/D	interrupt A output: this pin is an open-drain interrupt output, conditions assigned by the interrupt register
PERR#	30	PIO and S/T/S	parity error input or output: the receiving device detects data parity error (active LOW)
SERR#	31	PO and O/D	system error output: reports address parity error (active LOW)

[1] PCI-bus pins are located on the long side of the package to simplify PCI board layout requirements

Table 8. GPIO pins and functions [1]

Symbol	Pin	Type	Function			
			Audio and video port outputs	TS and PS capture inputs	Raw DTV/DVB outputs	GPIO
GPIO27	87	GIO	A_SDO (I^2S-bus 1 data)	-	-	R/W
GPIO26	88	GIO	A_WS (I^2S-bus word select)	-	-	R/W
GPIO25	89	GIO	A_SCK (I^2S-bus clock)	-	-	R/W
V_CLK	66	GO	V_CLK (also gated)	-	ADC_CLK (out)	-
GPIO23	56	GIO	HSYNC	-	ADC_C[0] (LSB)	R/W, INT
GPIO22	57	GIO	VSYNC	TS_LOCK (channel decoder locked)	-	R/W, INT
GPIO21	58	GIO	-	TS_S_D (bit-serial data)	-	R/W
GPIO20	59	GIO	-	TS_CLK (< 33 MHz)	-	R/W
GPIO19	60	GIO	-	TS_SOP (packet start)	-	R/W
GPIO18	61	GIO	VAUX2; A_CLK_master, A_REF_CLK	-	X_CLK_IN	R/W, INT
GPIO17	67	GIO	VAUX1 (e.g. VACTIVE); A_SDO_aux, I^2S-bus 2 data	-	ADC_Y[0] (LSB)	R/W
GPIO16	68	GIO	-	TS_VAL (valid flag)	-	R/W, INT
GPIO15 to GPIO8	69 to 72 and 75 to 78	GIO	VP[7:0] for formats: ITU-R BT.656, VMI, VIP (1.1, 2.0), etc.	-	ADC_Y[8:1]	R/W
GPIO7 to GPIO0	79 to 86	GIO	VP extension for 16-bit formats: ZV, VIP-2, DMSD, etc.	TS_P_D[7:0] (transport stream or program stream, byte-parallel data)	ADC_C[8:1]	R/W

[1] The SAA7133HL offers a peripheral interface with General Purpose Input/Output (GPIO) pins. Dedicated functions can be selected:

a) Digital Video Port (VP): output only; in 8-bit and 16-bit formats, such as VMI, DMSD (ITU-R BT.601); zoom-video, with discrete sync signals; ITU-R BT.656; VIP (1.1 and 2.0), with sync encoded in SAV and EAV codes.

b) Transport Stream (TS) capture input: from the peripheral DTV/DVB channel decoder; synchronized by Start Of Packet (SOP); in byte-parallel or bit-serial protocol.

c) Digitized raw DTV/DVB samples stream output: from internal ADCs; to feed the peripheral DTV/DVB channel decoder.

d) Program Stream (PS) capture input, e.g. from an external MPEG encoder chip.

e) GPIO: as default (no other function selected); static (no clock); read and write from or to individually selectable pins; latching 'strap' information at system reset time.

f) Use an external 4.7 kΩ pull-up resistor at GPIO16 for an external 24.576 MHz crystal; due to an internal pull-down resistor, an open-circuit GPIO16 pin requires an external 32.11 MHz crystal.

g) Peripheral interrupt (INT) input: enabled by interrupt enable register; routed to PCI interrupt (INT_A).

Table 9. Analog interface pins [1]

Symbol	Pin	Type	Description
XTALI	62	CI	quartz oscillator input: 32.11 MHz or 24.576 MHz
XTALO	63	CO	quartz oscillator output
LEFT2	94	AI	analog audio stereo left 2 input or mono input
V_{DDA}	95	AS	analog supply voltage (3.3 V)
LEFT1	96	AI	analog audio stereo left 1 input or mono input; default analog pass-through to pin OUT_LEFT after reset
V_{SSA}	97	AG	analog ground (for audio)
RIGHT1	98	AI	analog audio stereo right 1 input or mono input; default analog pass-through to pin OUT_RIGHT after reset
V_{REF0}	99	AR	analog reference ground for audio sigma delta ADC; to be connected V_{SSA}
RIGHT2	100	AI	analog audio stereo right 2 input or mono input
V_{REF1}	101	AR	analog reference voltage for audio sigma delta ADC; to be connected to V_{DDA} and via a 220 nF capacitor to pin V_{REF0}
V_{REF2}	102	AR	analog reference voltage for audio sigma delta ADC; to be supported with two parallel capacitors of 47 µF and 0.1 µF to V_{SSA}
OUT_RIGHT	103	AO	analog audio stereo right channel output; 1 V (RMS) line-out, feeding the audio loop back cable via a coupling capacitor of 2.2 µF
OUT_LEFT	104	AO	analog audio stereo left channel output; 1 V (RMS) line-out, feeding the audio loop back cable via a coupling capacitor of 2.2 µF
$\overline{\text{PROP\_RST}}$	105	AO	analog output for test and debug purpose
SIF	106	AI	sound IF input from TV tuner (4.5 MHz to 9.2 MHz); coupling capacitor of 47 pF after the termination with 50 Ω
V_{REF3}	107	AR	analog reference voltage for audio FIR-DAC and SCART audio input buffer; to be supported with two parallel capacitors of 47 µF and 0.1 µF to V_{SSA}
V_{SSA}	108	AG	analog ground
CV2_C	109	AI	composite video input (mode 2) or C input (modes 6 and 8)
V_{DDA}	110	AS	analog supply voltage (3.3 V)
V_{REF4}	111	AR	analog reference voltage; to be supported with a capacitor of 220 nF to V_{SSA}
DRCV_Y	112	AR	differential reference connection (for CV0 and CV1); to be supported with a capacitor of 47 nF to V_{SSA}
V_{SSA}	113	AG	analog ground
CV0_Y	114	AI	composite video input (mode 0) or Y input (modes 6 and 8)
V_{DDA}	115	AS	analog supply voltage (3.3 V)
CV1_Y	116	AI	composite video input (mode 1) or Y input (modes 7 and 9)
DRCV_C	117	AR	differential reference connection (for CV2, CV3 and CV4); to be supported with a capacitor of 47 nF to V_{SSA}
CV3_C	118	AI	composite video input (mode 3) or C input (modes 7 and 9)
V_{SSA}	119	AG	analog ground
CV4	120	AI	composite video input (mode 4)

[1] The SAA7133HL offers an interface for analog video and audio signals. The related analog supply pins are included in this table.

5.2.1 Pin type

Table 10. Characteristics of pin types and remarks

Pin type	Description
AG	analog ground
AI	analog input; video, audio and sound
AO	analog output
AR	analog reference support pin
AS	analog supply voltage (3.3 V)
CI	CMOS input; 3.3 V signal level (not 5 V tolerant)
CO	CMOS output; 3.3 V signal level (not 5 V tolerant)
GIO	digital input/output (GPIO); 3.3 V signal level (5 V tolerant)
GO	digital output (GPIO); 3.3 V signal level (5 V tolerant)
I	JTAG test input
IO2	digital input and output of the I^2C-bus interface; 3.3 V and 5 V compatible, auto-adapting
O	JTAG test output
O/D	open-drain output (for certain PCI pins); multiple clients can drive LOW at the same time, wired-OR, floating back to 3-state over several clock cycles
PI	input according to PCI requirements
PIO	input and output according to PCI requirements
PO	output according to PCI requirements
S/T/S	sustained 3-state (for certain PCI pins); previous owner drives HIGH for one clock cycle before leaving to 3-state
T/S	3-state I/O according to PCI requirements; bidirectional
VG	ground for digital supply
VS	supply voltage (3.3 V)
With overscore or #	this pin or ‘signal’ is active LOW, i.e. the function is ‘true’ if the logic level is LOW

6. Functional description

6.1 Overview of internal functions

The SAA7133HL is able to capture TV signals over the PCI-bus in personal computers by a single chip (see Figure 4).

The SAA7133HL incorporates two 9-bit video ADCs and the entire decoding circuitry of any analog TV signal: NTSC, PAL and SECAM, including non-standard signals, such as playback from a VCR. The adaptive multi-line comb filter provides superb picture quality, component separation, sharpness and high bandwidth. The video stream can be cropped and scaled to the needs of the application. Scaling down as well as zooming up is supported in the horizontal and vertical direction, and an adaptive filter algorithm prevents aliasing artifacts. With the acquisition unit of the scaler two different 'tasks' can be defined, e.g. to capture video to the CPU for compression, and write video to the screen from the same video source but with different resolution, color format and frame rate.

The SAA7133HL contains TV sound stereo decoding from Sound IF (SIF), for the BTSC and EIAJ stereo sound standards, FM and AM mono sound and also non-standard signals. Baseband stereo audio sampling is also implemented, e.g. for capturing from a camcorder or other external devices. The audio sampling rate can be locked to the video frame rate to ensure synchronization (lip-sync) between the video and audio data flow, e.g. for storage, compression or time shift viewing applications.

The SAA7133HL incorporates analog audio pass-through and support for the analog audio loop back cable to the sound card function.

The decoded video streams are fed to the PCI-bus, and are also applied to a peripheral streaming interface, in ITU, VIP or VMI format. A possible application extension is on-board hardware MPEG compression, or other feature processing. The compressed data as PS or TS is fed back through the peripheral interface, in parallel or serial format, to be captured by the system memory through the PCI-bus. The Transport Stream (TS) from a DTV/DVB channel decoder can be captured through the peripheral interface in the same way.

Audio, video and transport streams are collected in a configurable FIFO with a total capacity of 1 kB. The DMA controller monitors the FIFO filling degree and master-writes the audio and video stream to the associated DMA channel. The virtual memory address space (from OS) is translated into physical (bus) addresses by the on-chip hardware Memory Management Unit (MMU).

The application of the SAA7133HL is supported by reference designs and a set of drivers for the Windows operating system (Video for Windows and Windows Driver Model compliant).

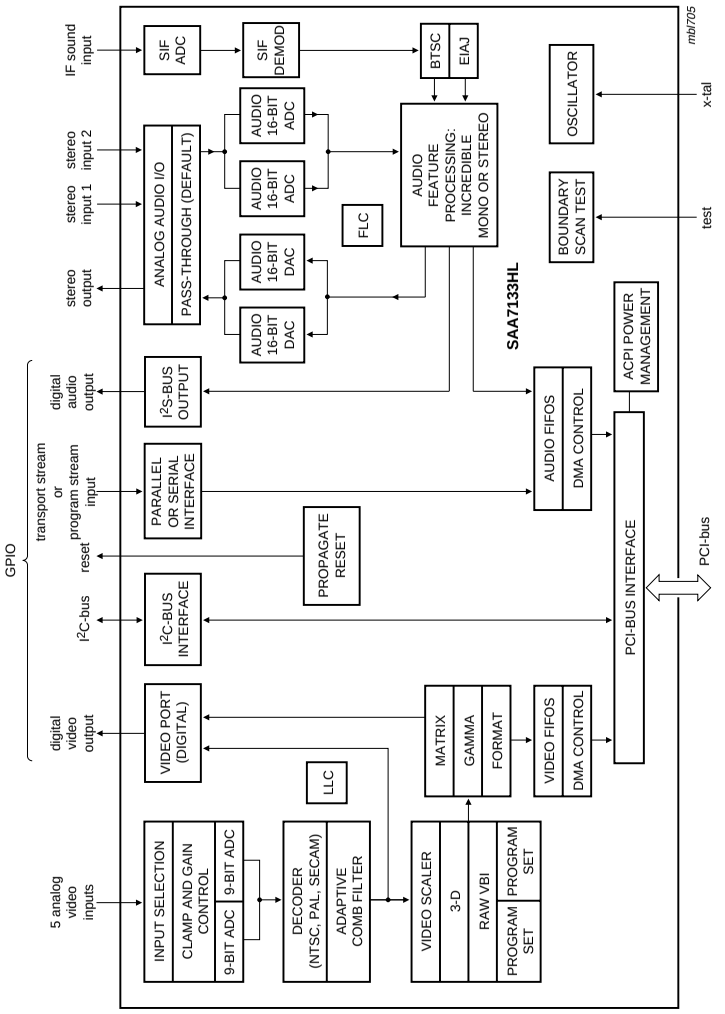


Fig 4. Functional block diagram

6.2 Application examples

The SAA7133HL enables PC TV capture applications both on the PC mother board and on PCI add-on TV capture cards. Figure 5 and Figure 6 illustrate some examples of add-on card applications.

Figure 5 shows the basic application to capture video from analog TV sources. The proposed tuner types incorporate the RF tuning function and the IF downconversion. Usually the IF downconversion stage also includes a single channel and analog sound FM demodulator. The NXP tuners FI1286 (Japan) and FI1236MK2 (USA and other NTSC countries) are suitable for M standard. The FM12x6 are special versions for additional FM radio reception. All types are suited for terrestrial broadcast and for cable reception. The tuners provide composite video CVBS and audio as second SIF. These analog video and sound signals are fed to the appropriate input pins of the SAA7133HL.

Further analog video input signals, CVBS and/or Y-C, can be connected via the board back-panel, or the separate front connectors, e.g. from a camcorder. Accompanying stereo audio signals can also be fed to the SAA7133HL.

Video is digitized and decoded to YUV. TV sound is digitized and decoded. The SAA7133HL is able to decode stereo audio according to BTSC [also including the Secondary Audio Program (SAP)] and stereo/dual audio according to EIAJ. In addition mono decoding of FM and AM sound is possible. The digital streams are pumped via DMA into the PCI memory space.

The SAA7133HL incorporates means for legacy analog audio signal routing. The on-chip audio DACs convert the digital decoded stereo signal into analog audio. This analog audio input signal is fed via an analog audio loop back cable into the line-in of a legacy sound card. An external audio signal, that would have otherwise connected directly to the sound card, is now routed through the SAA7133HL. This analog pass-through is enabled as default by a system reset, i.e. without any driver involvement and before system set-up.

During the power-up procedure, the SAA7133HL will investigate the on-board EEPROM to load the board specific system vendor ID and board version ID into the related places of the PCI configuration space. The board vendor can store other board specific data in the EEPROM that is accessible via the I^2C-bus.

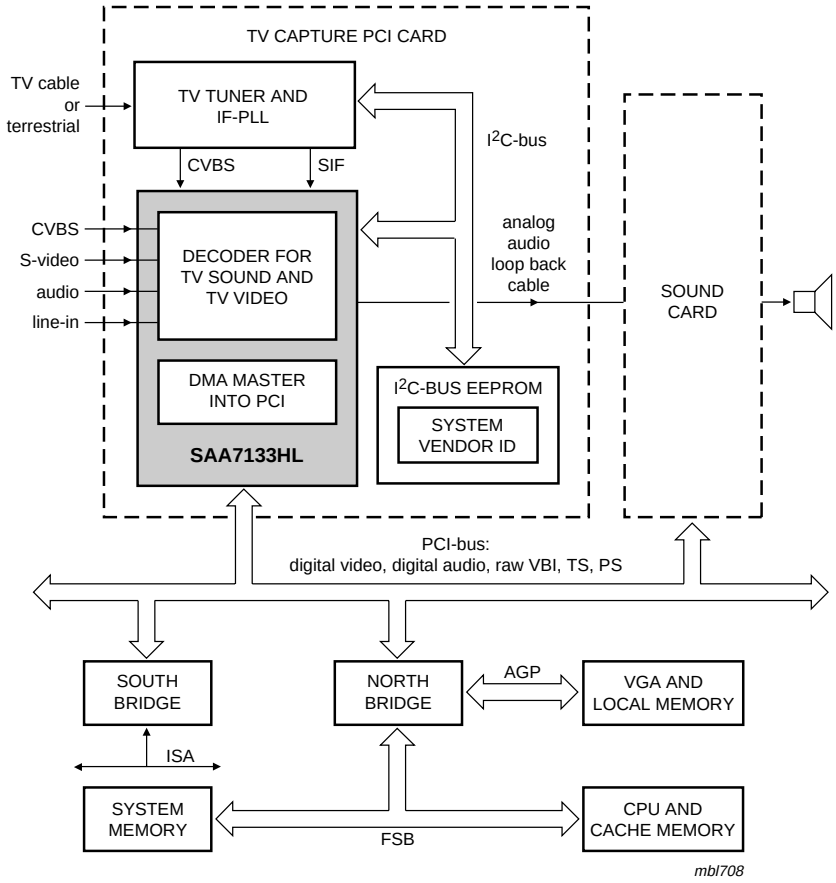


Fig 5. Basic TV capture with BTSC and EIAJ stereo decoding

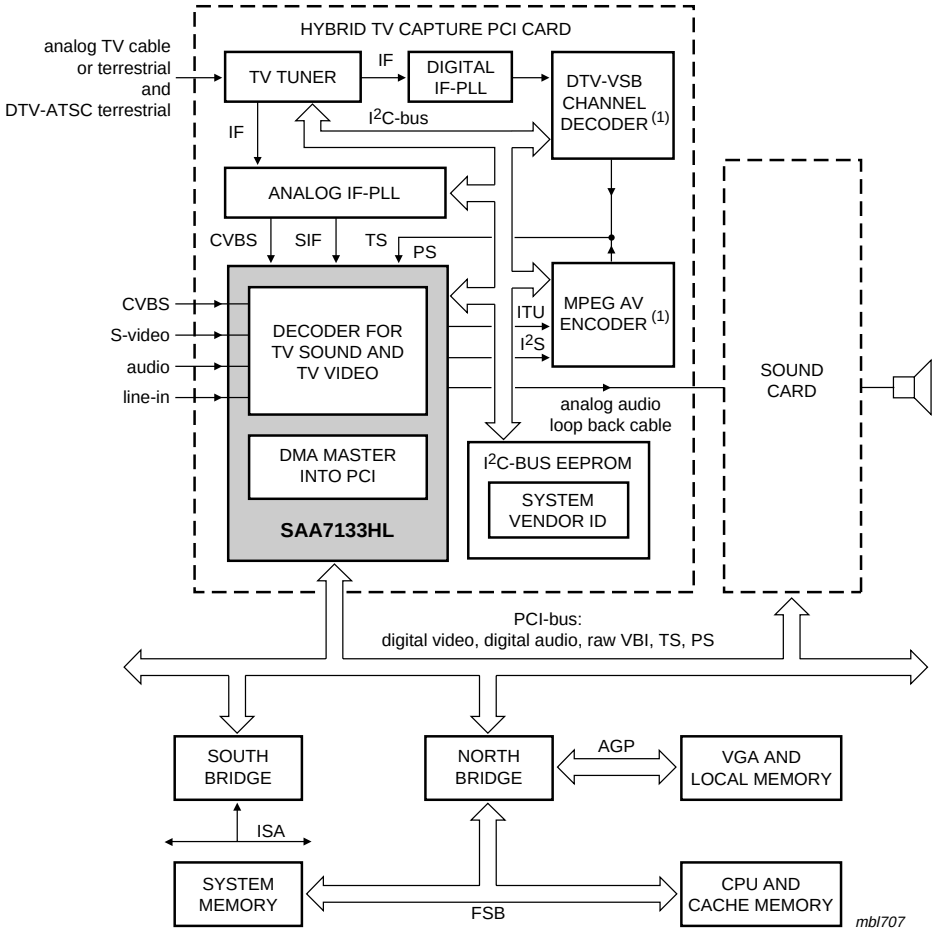
Figure 6 shows an application extension with VSB channel decoding for DTV-ATSC or peripheral MPEG encoding.

A combi-tuner, e.g. NXP NTSC tuner FM1236, provides a dedicated DTV-IF signal that can be routed directly to the channel decoder device, which converts also the decoded signal into a DTV (or BS-digital) Transport Stream (TS).

The SAA7133HL captures this TS via the dedicated peripheral interface into the configurable internal FIFO for DMA into the PCI memory space.

The packet structure is maintained in a well-defined buffer structure in the system memory, and therefore can easily be sorted (de-multiplexed) by the CPU for proper MPEG decoding.

Alternatively, an external MPEG encoder chip can be inserted into the data path. This device gets the video data in ITU-R BT.656 format and the audio data in I^2S format from the SAA7133HL and gives back the MPEG encoded program stream to the SAA7133HL.



(1) Alternative

Fig 6. Hybrid TV capture board with MPEG encoding or DTV channel decoder, e.g. VSB-ATSC

6.3 Device driver

A complex and powerful software packet is provided for all PCI chips from the SAA713x family. This packet includes plug-and-play driver and capture driver installations for all commonly used 32-bit and 64-bit Windows platforms.

All platform related drivers support the following:

- Analog audio, video and VBI capture interfaces
- Digital capture interfaces for DVB-T, DVB-C, DVB-S and ATSC
- Custom application interface, that enables the development of specialized applications in cases where the published direct show Application Programming Interface (API) may not be sufficient

Table 11. Microsoft Operating System (MS-OS) support

MS-OS	Driver support
Windows 2000	the driver is validated for passing the Microsoft WLP (Windows Logo Program) test for obtaining the Win2000 driver signature
Windows XP	the driver is validated for passing the Microsoft WLP (Windows Logo Program) test for obtaining the WinXP driver signature

6.4 PCI interface

6.4.1 PCI configuration registers

The PCI interface of the SAA7133HL complies with the *"PCI specification 2.2"* and supports power management and Advanced Configuration and Power Interface (ACPI) as required by the *"PC Design Guide 2001"*.

The PCI specification defines a structure of the PCI configuration space that is investigated during the boot-up of the system. The configuration registers (see Table 12) hold information essential for plug-and-play, to allow system enumeration and basic device set-up without depending on the device driver, and support association of the proper software driver. Some of the configuration information is hard-wired in the device; some information is loaded during the system start-up.

The device vendor ID is hard coded to 1131h, which is the code for NXP as registered with PCI-SIG.

The device ID is hard coded to 7133h.

During power-up, initiated by PCI reset, the SAA7133HL fetches additional system information via the I^2C-bus from the on-board EEPROM, to load actual board type specific codes for the system vendor ID, sub-system ID (board version) and ACPI related parameters into the configuration registers.

Table 12. PCI configuration space registers

Function	Register address	Value	Remark
Device vendor ID	00h and 01h	1131h	for NXP
Device ID	02h and 03h	7133h	for SAA7133HL
Revision ID	08h	F0h	or higher
Class code	09h to 0Bh	04 8000h	multimedia
Memory address space required	10h to 13h	XXXX XXXX XXXX XXXX XXXX X000 0000 0000b	2 kB
System (board) vendor ID	2Ch and 2Dh	loaded from EEPROM	
Sub-system (board version) ID	2Eh and 2Fh	loaded from EEPROM	

6.4.2 ACPI and power states

The *"PCI specification 2.2"* requires support of *"Advanced Configuration and Power Interface specification 1.0"* (ACPI); more details are defined in the *"PCI Power Management Specification 1.0"*.

The power management capabilities and power states are reported in the extended configuration space. The main purpose of ACPI and PCI power management is to tailor the power consumption of the device to the actual needs.

The SAA7133HL supports all four ACPI device power states (see Table 13).

The pin $\overline{\text{PROP\_RST}}$ of the peripheral interface is switched active LOW during the PCI reset procedure, and for the duration of the D3-hot state. Peripheral devices on board of the add-on card should use the level of the signal on pin $\overline{\text{PROP\_RST}}$ to switch themselves in any power-save mode (e.g. disable device) and reset to default settings on the rising edge of the signal. The length of this signal is programmable.

6.4.3 DMA and configurable FIFO

The SAA7133HL supports seven DMA channels to master-write captured active video, audio, raw VBI and DTV/DVB Transport Streams (TS) and MPEG streams (PS and TS) into the PCI memory. Each DMA channel contains inherently the definition of two buffers in the system address space, e.g. for odd and even fields in case of interlaced video, or two alternating buffers to capture continuous audio stream.

The DMA channels share in time and space one common FIFO pool of 256 Dwords (1024 B) total. It is freely configurable how much FIFO capacity is associated with which DMA channel. Furthermore, a preferred minimum burst length can be programmed, i.e. the amount of data to be collected before the request for the PCI-bus is issued. This means that latency behavior per DMA channel can be tailored and optimized for a given application.

In the event that the FIFO of a certain channel overflows due to latency conflict on the bus, graceful overflow recovery is applied. The amount of data that gets lost because it could not be transmitted, is monitored (counted) and the PCI-bus address pointer is incremented accordingly. Thus new data will be written to the correct memory place, after the latency conflict is resolved.

Table 13. Power management table

Power state	Description
D0	normal operation: all functions accessible and programmable; the default setting after reset and before driver interaction (D0 un-initialized) switches most of the circuitry of the SAA7133HL into the power-down mode, effectively same as D3-hot
D1	first step of reduced power consumption: no functional operation; program registers are not accessible, but content is maintained; most of the circuitry of the SAA7133HL is disabled with exception of the crystal and real-time clock oscillators, so that a quick recovery from D1 to D0 is possible
D2	second step of reduced power consumption: no functional operation; program registers are not accessible, but content is maintained; all functional circuitry of the SAA7133HL is disabled, including the crystal and clock oscillators
D3-hot	lowest power consumption: no functional operation; the content of the programming registers gets lost and is set to default values when returning to D0

Table 14. FIFO configuration: typical example

DMA	Data stream	Data rate	FIFO size programmable to	Tolerant to latency of
1	Y	13.5 MB/s	384 B	28.4 µs
2	U	6.75 MB/s	256 B	37.9 µs
3	V	6.75 MB/s	256 B	37.9 µs
4	audio	160 kB/s	128 B	800 µs

Table 15. FIFO configuration: fastidious example

DMA	Data stream	Data rate	FIFO size programmable to	Tolerant to latency of
1	raw VBI[1]	27 MB/s	640 B	22.5 µs
2	-	-	-	-
3	MPEG stream	9.5 Mbit/s	256 B	202.1 µs
4	audio	192 kB/s	128 B	583.3 µs

[1] Active video, unscaled YUV 4 : 2 : 2.

6.4.4 Virtual and physical addressing

Most operating systems allocate memory to requesting applications for DMA as continuous ranges in virtual address space. The data flow over the PCI-bus points to physical addresses, usually not continuous and split in pages of 4 kB (Intel architecture, most UNIX systems, Power PC).

The association between the virtual (logic) address space and the fragmented physical address space is defined in page tables (system files); see Figure 7. The SAA7133HL incorporates hardware support (MMU) to translate virtual to physical addresses on the fly, by investigating the related page table information. This hardware support reduces the demand for real-time software interaction and interrupt requests, and therefore saves system resources.

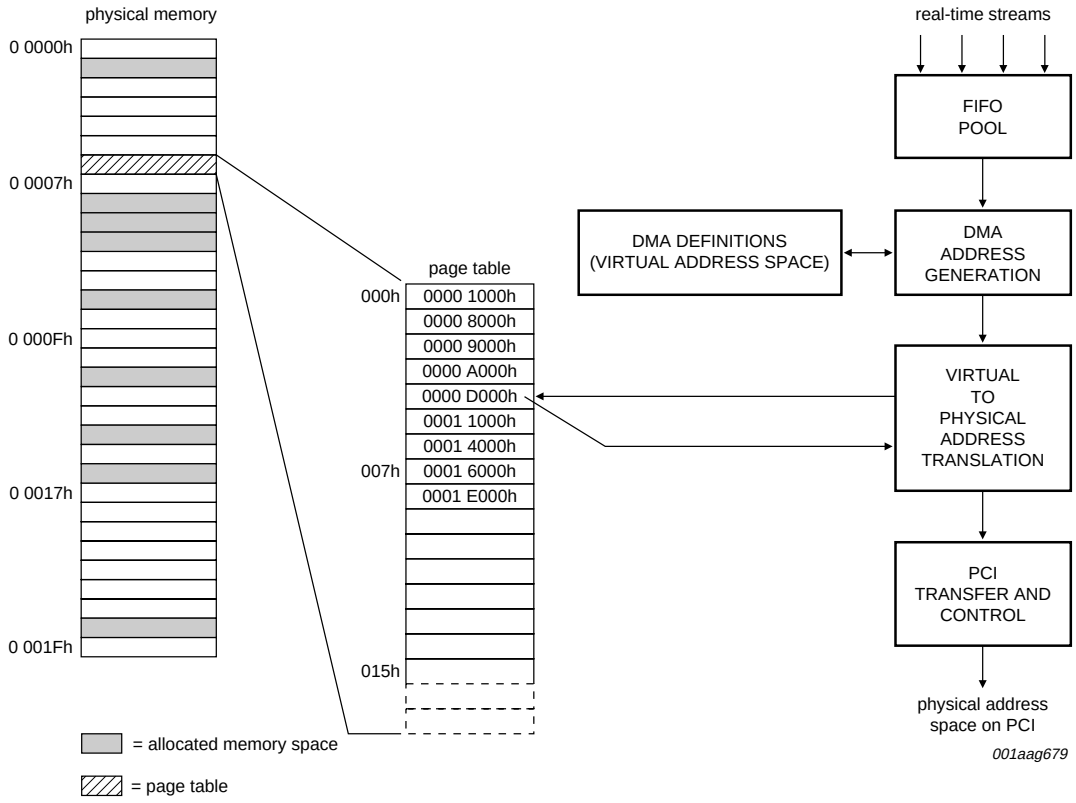


Fig 7. MMU implementation (shown bit width indication is valid for 4 kB mode)

6.4.5 Status and interrupts on PCI-bus

The SAA7133HL provides a set of status information about internal signal processing, video and audio standard detection, peripheral inputs and outputs (pins GPIO) and behavior on the PCI-bus. This status information can be conditionally enabled to raise an interrupt on the PCI-bus, e.g. completion of a certain DMA channel or buffer, or change in a detected TV standard, or the state of peripheral devices.

The cause of an issued interrupt is reported in a dedicated register, even if the original condition has changed before the system was able to investigate the interrupt.

6.5 Analog TV standards

Analog TV signals are described in three categories of standards:

- Basic TV systems: defining frame rate, number of lines per field, levels of synchronization signals, blanking, black and white, signal bandwidth and the RF modulation scheme
- Color transmission: defining color coding and modulation method
- Sound and stereo: defining coding for transmission

TV signals that are broadcast usually conform fairly accurately to the standards. Transmission over the air or through a cable can distort the signal with noise, echoes, crosstalk or other disturbances.

Video signals from local consumer equipment, e.g. VCR, camcorder, camera, game console, or even DVD player, often do not follow the standard specification very accurately.

Playback from video tape cannot be expected to maintain correct timing, especially not during feature mode (fast forward, etc.).

Table 16, Table 17 and Table 18 list some characteristics of the various TV standards.

The SAA7133HL decodes all color TV standards and non-standard signals as generated by video tape recorders e.g. automatic video standard detection can be applied, with preference options for certain standards, or the decoder can be forced to a dedicated standard.

The SAA7133HL incorporates BTSC and EIAJ stereo decoding and TV mono sound decoding on chip. Baseband stereo audio can be fed into the device as analog signal.

Table 16. Overview of basic TV standards

Main parameter	Standard							Unit
	M	N	B	G/H	I	D/K	L	
RF channel width	6	6	7	7	8	7	8	MHz
Video bandwidth	4.2	4.2	5	5	5.5	6	6	MHz
1st sound carrier[1]	4.5	4.5	5.5	5.5	6.0	6.5	6.5	MHz
Field rate f_v	59.94006	50	50	50	50	50	50	Hz
Lines per frame	525	625	625	625	625	625	625	-
Line frequency f_h	15.734	15.625	15.625	15.625	15.625	15.625	15.625	kHz
ITU clocks per line	1716	1728	1728	1728	1728	1728	1728	-
Sync (set-up level)[2]	–40 (7.5)	–40 (7.5)	–43 (0)	–43 (0)	–43 (0)	–43 (0)	–43 (0)	-
Gamma correction	2.2	2.2	2.8	2.8	2.8	2.8	2.8	-
Associated color TV standard	NTSC, PAL	PAL	PAL	PAL	PAL	SECAM, PAL	SECAM	-
Associated stereo TV sound system	BTSC, EIAJ, A2	BTSC	dual FM, A2	NICAM	NICAM	NICAM, A2	NICAM	-
Country examples	USA, Brazil, Japan	Argentina	part of Europe, Australia	Spain, Malaysia, Singapore	UK, Northern Europe	China, Eastern Europe	France, Eastern Europe	-

[1] AM for standard L, FM for all other standards listed.

[2] In IRE units.

Table 17. TV system color standards

Main parameter	NTSC	PAL			SECAM		PAL 4.4 (60 Hz)	Unit
	M	M	N	B, G, H, I, D	L, D, G, H, K			
Field rate f_v	59.94	59.94	50	50	50		≈60	Hz
Lines per frame	525	525	625	625	625		525	-
Chrominance subcarrier f_{sub}	3.580	3.576	3.582	4.434	4.406	4.250	4.434	MHz
f_{sub} to f_h ratio	227.5	227.25	229.25	283.75	282	272	n.a.	-
f_{sub} offset (PAL)	-	-	50	50	-	-	n.a.	Hz
Alternating phase	no	yes	yes	yes	-	-	yes	-
Country examples	USA, Japan, Asia-Pacific	Brazil	Middle and South America	Europe, China, Commonwealth	Africa, France, Eastern Europe, Middle East		transcoding VCR tapes from NTSC to PAL	-

Table 18. TV stereo sound standards

Main parameter	Analog systems				Digital coding	Unit
	Mono	BTSC	EIAJ	A2 (dual FM)	NICAM	
Stereo coding scheme	-	internal carrier (MPX)	internal carrier (MPX)	2-carrier systems	2-carrier systems	-
		AM	FM	2nd FM carrier	DQPSK on FM	-
2nd language	-	mono SAP on internal FM	as alternative to stereo	as alternative to stereo	mono on 1st carrier	-
De-emphasis	75	75[1]	50	50 or 75	50 or J17	µs
Audio bandwidth	15	15	15	15	15	kHz
Country examples	worldwide	USA, South America	Japan	part of Europe, Korea	part of Europe, China	-

[1] dbx-TV noise reduction system

6.6 Video processing

6.6.1 Analog video inputs

The SAA7133HL provides five analog video input pins:

- Composite Video Signals (CVBS), from tuner or external source
- S-video signals (pairs of Y-C), e.g. from camcorder
- DTV/DVB ‘low-IF’ signal, from an appropriate DTV or combi-tuner

Analog anti-alias filters are integrated on chip and therefore, no external filters are required. The device also contains automatic clamp and gain control for the video input signals, to ensure optimum utilization of the ADC conversion range. The nominal video signal amplitude is 1 V (p-p) and the gain control can adapt deviating signal levels in the range of +3 dB to –6 dB. The video inputs are digitized by two ADCs of 9-bit resolution, with a sampling rate of nominal 27 MHz (the line-locked clock) for analog video signals.

6.6.2 Video synchronization and line-locked clock

The SAA7133HL recovers horizontal and vertical synchronization signals from the selected video input signal, even under extremely adverse conditions and signal distortions. Such distortions are ‘noise’, static or dynamic echoes from broadcast over air, crosstalk from neighboring channels or power lines (hum), cable reflections, time base errors from video tape play-back and non-standard signal levels from consumer type video equipment (e.g. cameras, DVD).

The heart of this TV synchronization system is the generation of the Line-Locked Clock (LLC) of nominal 27 MHz, as defined by ITU-R BT.601. The LLC ensures orthogonal sampling, and always provides a regular pattern of synchronization signals, that is a fixed and well defined number of clock pulses per line. This is important for further video processing devices connected to the peripheral video port (pins GPIO). It is very effective to run under the LLC of 27 MHz, especially for on-board hardware MPEG encoding devices, since MPEG is defined on this clock and sampling frequency.

6.6.3 Video decoding and automatic standard detection

The SAA7133HL incorporates color decoding for any analog TV signal. All color TV standards and flavours of NTSC, PAL, SECAM and non-standard signals (VCR) are automatically recognized and decoded into luminance and chrominance components, i.e. Y-C_B-C_R, also known as YUV.

The video decoder of the SAA7133HL incorporates an automatic standard detection, that does not only distinguish between 50 Hz and 60 Hz systems, but also determines the color standard of the video input signal. Various preferences (‘look first’) for automatic standard detection can be chosen, or a selected standard can be forced directly.

6.6.4 Adaptive comb filter

The SAA7133HL applies adaptive comb filter techniques to improve the separation of luminance and chrominance components in comparison to the separation by a chroma notch filter, as used in traditional TV color decoder technology. The comb filter compares the signals of neighboring lines, taking into account the phase shift of the chroma subcarrier from line to line. For NTSC the signals of three adjacent lines are investigated, and in the event of PAL the comb filter taps are spread over four lines.

Comb filtering achieves higher luminance bandwidth, resulting in sharper picture and detailed resolution. Comb filtering further minimizes color crosstalk artifacts, which would otherwise produce erroneous colors on detailed luminance structures.

The comb filter as implemented in the SAA7133HL is adaptive in two ways:

- Adaptive to transitions in the picture content
- Adaptive to non-standard signals (e.g. VCR)

The integrated digital delay lines are always exactly correct, due to the applied unique line-locked sampling scheme (LLC). Therefore the comb filter does not need to be switched off for non-standard signals and remains operating continuously.

6.6.5 Macrovision detection

The SAA7133HL detects if the decoded video signal is copy protected by the Macrovision system. The detection logic distinguishes the three levels of the copy protection as defined in rev. 7.01, and are reported as status information. The Macrovision detection works also for copy protected video signals, which contain inverted bursts but no AGC pulses and no pseudo syncs. Those signals come from some so-called Macrovision-killer boxes. The decoded video stream is not effected directly, but application software and Operation System (OS) has to ensure, that this video stream maintains tagged as ‘copy protected’, and such video signal would leave the system only with the reinforced copy protection. The multi-level Macrovision detection on the video capture side supports proper TV re-encoding on the output point, e.g. by NXP TV encoders SAA712x or SAA7102.

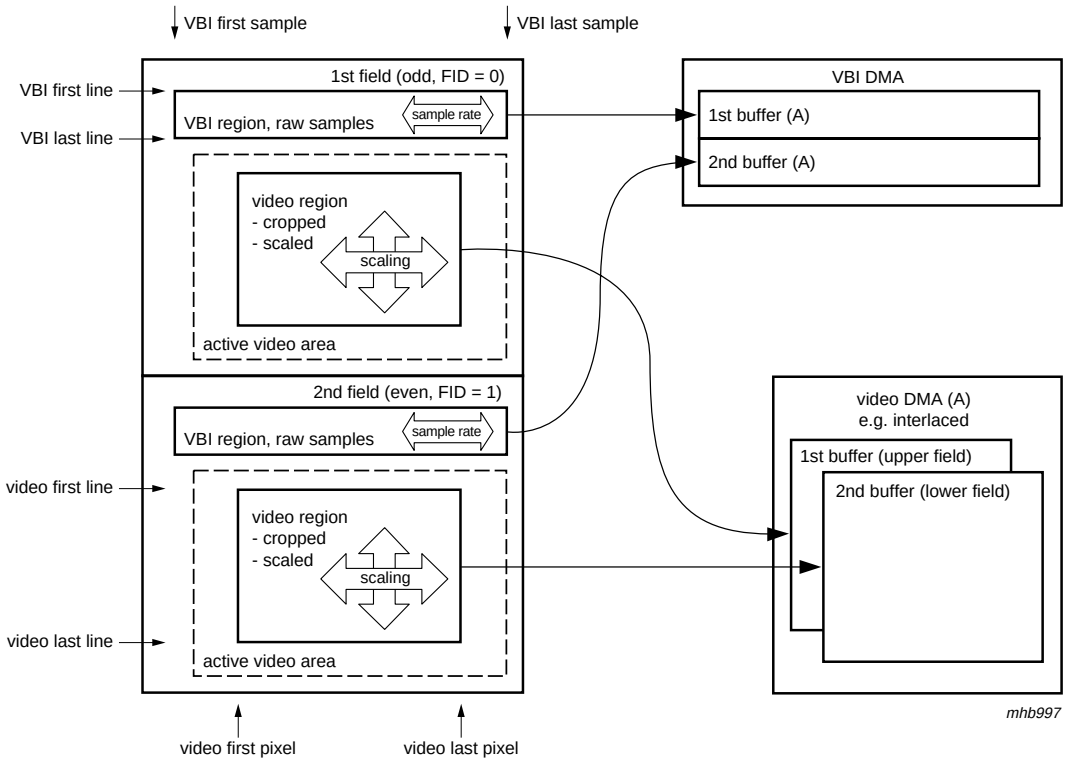
6.6.6 Video scaling

The SAA7133HL incorporates a filter and processing unit to downscale or upscale the video picture in the horizontal and vertical dimension, and in frame rate (see Figure 8 and Figure 9). The phase accuracy of the re-sampling process is $^{1}/_{64}$ of the original sample distance. This is equivalent to a clock jitter of less than 1 ns. The filter depth of the anti-alias filter adapts to the scaling ratio, from 10 taps horizontally for scaling ratios close to 1 : 1, to up to 74 taps for an icon sized video picture.

Most video capture applications will typically require for downscaling. But some zooming is required for conversion of ITU sampling to square pixel, or to convert the 240 lines of an NTSC field to 288 lines to comply with ITU-T video phone formats.

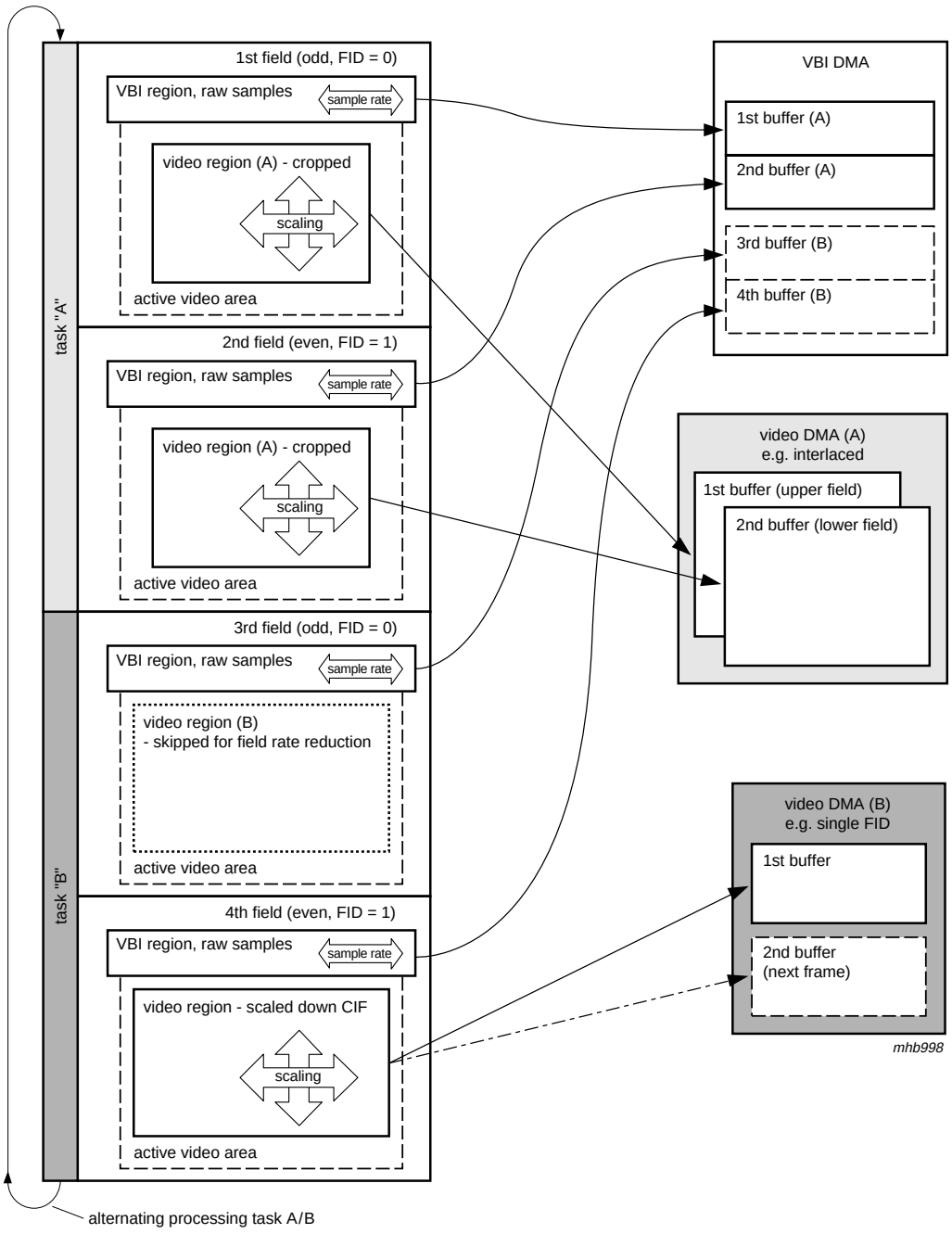
The scaling acquisition definition also includes cropping, frame rate reduction, and defines the amount of pixels and lines to be transported through DMA over the PCI-bus.

Two programming pages are available to enable re-programming of the scaler in the ‘shadow’ of the running processing, without holding or disturbing the flow of the video stream. Alternatively, the two programming pages can be applied to support two video destinations or applications with different scaler settings, e.g. firstly to capture video to CPU for compression (storage, video phone), and secondly to preview the picture on the monitor screen. A separate scaling region is dedicated to capture raw VBI samples, with a specific sampling rate, and be written into its own DMA channel.



The capture acquisition for scaling and DMA has separate programming parameters for VBI and video region and associated DMA channels.

Fig 8. Scaler processing with DMA interfacing



Two video capture tasks can be processed in an alternating manner, without need to reprogram any scaling parameters or DMA definition.

Fig 9. Example of scaler task processing with DMA interfacing

6.6.7 VBI data

The Vertical Blanking Interval (VBI) is often utilized to transport data over analog video broadcast. Such data can closely relate to the actual video stream, or just be general data (e.g. news). Some examples for VBI data types are:

- Closed Caption (CC) for the hearing impaired (CC, on line 21 of first field)
- Intercast data [in US coded in North-American Broadcast Text System (NABTS) format, in Europe in World Standard Teletext (WST)], to transmit internet related services, optionally associated with actual video program content
- Teletext, transporting news services and broadcast related information, Electronic Program Guide (EPG), widely used in Europe (coded in WST format)
- EPG, broadcaster specific program and schedule information, sometimes with proprietary coding scheme (pay service), usually carried on NABTS, WST, Video Programming Service (VPS), or proprietary data coding format
- Video Time Codes (VTC) as inserted in camcorders e.g. use for video editing
- Copy Guard Management System (CGMS) codes, to indicate copy protected video material, sometimes combined with format information [Wide Screen Signalling (WSS)]

This information is coded in the unused lines of the vertical blanking interval, between the vertical sync pulse and the active visible video picture. So-called full-field data transmission is also possible, utilizing all video lines for data coding.

The SAA7133HL supports capture of VBI data by the definition of a VBI region to be captured as raw VBI samples, that will be sliced and decoded by software on the host CPU. The raw sample stream is taken directly from the ADC and is not processed or filtered by the video decoder. The sampling rate of raw VBI can be adjusted to the needs of the data slicing software.

6.6.8 Signal levels and color space

Analog TV video signals are decoded into its components luminance and color difference signals (YUV) or in its digital form Y-C_B-C_R. ITU-R BT.601 defines 720 pixels along the line (corresponding to a sampling rate of 27 MHz divided by two), and a certain relationship from level to number range (see Figure 10).

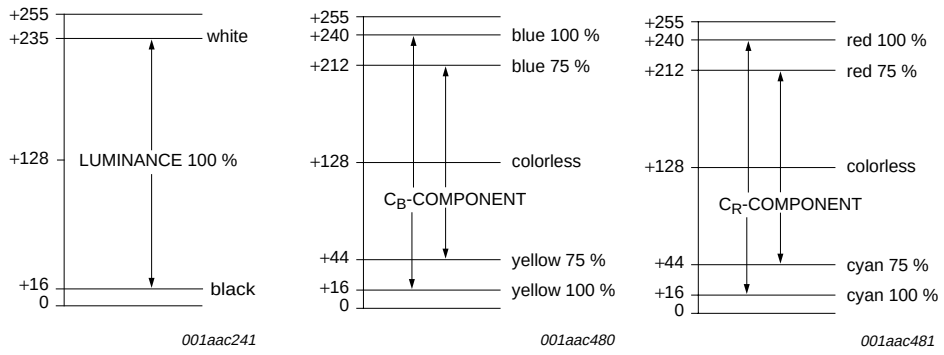
The video components do not use the entire number range, but leave some margin for overshoots and intermediate values during processing. For the raw VBI samples there is no official specification how to code, but it is common practice to reserve the lower quarter of the number range for the sync, and to leave some room for overmodulation beyond the nominal white amplitude (see Figure 11).

The automatic clamp and gain control at the video input, together with the automatic chroma gain control of the SAA7133HL, ensures that the video components stream at the output comply to the standard levels. Beyond that additional brightness, contrast, saturation and hue control can be applied to satisfy special needs of a given application. The raw VBI samples can be adjusted independent of the active video.

The SAA7133HL incorporates the YUV-to-RGB matrix (optional), the RGB-to-YUV matrix and a three channel look-up table in between (see Figure 12). Under nominal settings, the RGB space will use the same number range as defined by the ITU and shown in Figure 10 (a.) for luminance, between 16 and 235. As graphic related applications are based on full-scale RGB, i.e. 0 to 255, the range can be stretched by applying appropriate brightness, contrast and saturation values. The look-up table supports gamma correction (freely definable), and allows other non-linear signal transformation such as black stretching.

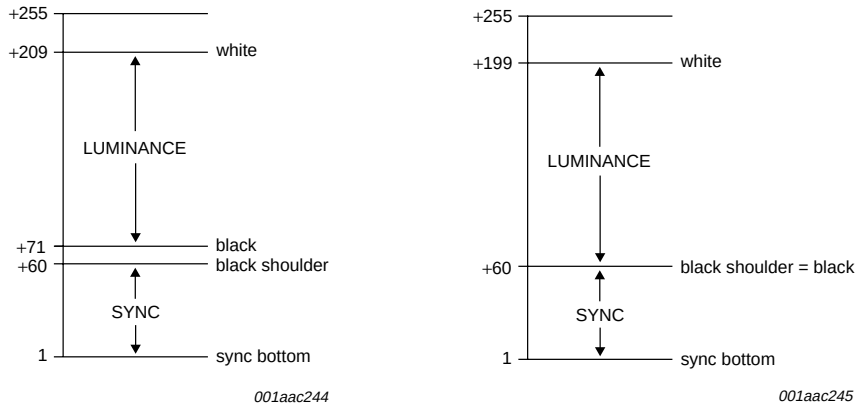
The analog TV signal applies a quite strong gamma pre-compensation (2.2 for NTSC and 2.8 for PAL). As computer monitors exhibit a gamma (around 2.5), the difference between gamma pre-compensation and actual screen gamma has to be corrected, to achieve best contrast and color impression.

The SAA7133HL offers a multitude of formats to write video streams over the PCI-bus: YUV and RGB color space, 15-bit, 16-bit, 24-bit and 32-bit representation, packed and planar formats. For legacy requirements (VfW) a clipping procedure is implemented, that allows the definition of 8 overlay rectangles. This process can alternatively be used to associate ‘alpha’ values to the video pixels.



a. Y output range b. C_B output range c. C_R output range

Fig 10. Nominal digital levels for YUV (Y, C_B and C_R) in accordance with *ITU-R BT.601*



a. For sources containing 7.5 IRE black-level offset (e.g. NTSC M)

b. For sources not containing black-level offset

Fig 11. Nominal digital levels for CVBS and raw VBI samples

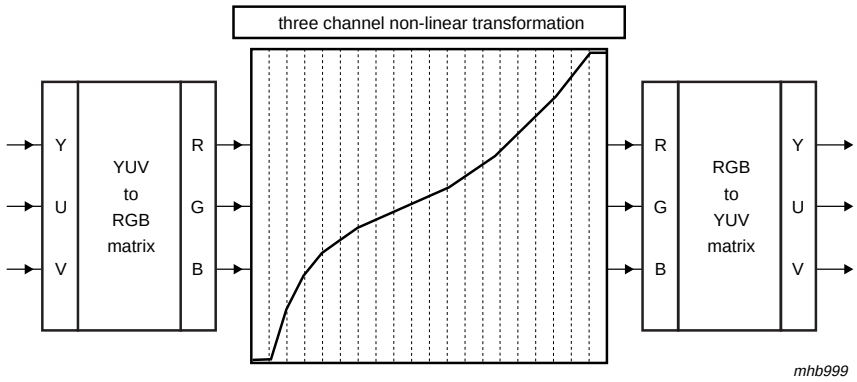


Fig 12. Color space conversion and look-up table

6.6.9 Video port, ITU and VIP codes

The decoded and/or scaled video stream can be captured via PCI-DMA to the system memory, and/or can be made available locally through the video side port (VP), using some of the GPIO pins. Two types of applications are intended:

- Streaming real-time video to a video side port at the VGA card, e.g. via ribbon cable over the top
- Feeding video stream to a local MPEG compression device on the same PCI board, e.g. for a time shift viewing application

The video port of the SAA7133HL supports the following 8 and 16-bit wide YUV video signalling standards (see Table 8):

- VMI: 8-bit wide data stream, clocked by LLC = 27 MHz, with discrete sync signals HSYNC, VSYNC and VACTIVE
- ITU-R BT.656, parallel: 8-bit wide data stream, clocked by LLC = 27 MHz, synchronization coded in SAV and EAV codes
- VIP 1.1 and 2.0: 8-bit or 16-bit wide data stream, clocked by LLC = 27 MHz, synchronization coded in SAV and EAV codes (with VIP extensions)
- Zoom Video (ZV): 16-bit wide pixel stream, clocked by LLC / 2 = 13.5 MHz, with discrete sync signals HSYNC and VSYNC
- ITU-R BT.601 direct (DMSD): 16-bit wide pixel stream, clocked by LLC = 27 MHz, with discrete sync signals HSYNC, VSYNC/FID and CREF
- Raw DTV/DVB sample stream: 9-bit wide data, clocked with a copy of signal X_CLK_IN

The VIP standard is designed to transport scaled video and discontinuous data stream by allowing the insertion of ‘logic 0’ as a marker for empty clock cycles. For the other video port standards, a data valid flag or gated clock can be applied.

6.7 TV sound

6.7.1 TV sound stereo decoding

The SAA7133HL incorporates TV sound decoding from the Sound Intermediate Frequency (SIF) signal. The analog SIF signal is taken from the tuner, digitized and digitally FM or AM demodulated. If one of the supported TV sound standards is found (BTSC, EIAJ, mono), the pilot tone is investigated (mono, stereo, dual) and the signal is properly stereo or dual decoded.

The SAA7133HL supports the stereo audio standards BTSC (+SAP) and EIAJ and all mono standards on-chip. dbx-TV noise reduction and de-emphasis filters are also integrated.

The digital FM demodulation maintains stable phase accuracy, resulting into improved channel separation, compared to traditional analog demodulation. TV sound decoding operates at a 32 kHz sample rate, resulting in an audio bandwidth of up to 15 kHz.

The SAA7133HL incorporates baseband stereo audio ADCs, to capture sound signals associated with external video sources, e.g. camera, camcorder or VCR.

For concurrent capture of audio and video signals, it is important to maintain synchronization between the two streams. The spoken word and other sound should match the displayed picture within a video frame ($^{1}/_{30}$ s respectively $^{1}/_{25}$ s ‘lip-sync’). The SAA7133HL has special means to lock the audio sampling clock to the video Frame Locked Clock (FLC), so that a programmable but constant number of audio samples is associated with each video frame. This is especially important for video editing, compression and recording, e.g. time shift viewing. There is no drift between the audio and video streams, not even for longer recording times.

Table 19. TV sound decoding, supported feature processing and sampling rate

Supported function	Input and sound standard					
	SIF from tuner				Baseband audio	
	BTSC	EIAJ	FM radio	Other AM/FM	L or R	L and R
Decoding	mono or stereo and SAP[1]	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo
Analog audio output to loop back cable	mono or stereo or SAP	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo[2]
I^2S output						
Signal	mono or stereo or SAP	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo
Sample rate	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz, 44.1 kHz or 48 kHz	32 kHz, 44.1 kHz or 48 kHz
PCI (audio streaming)						
Sample	mono or stereo and/or SAP	mono or stereo or dual	mono or stereo	mono	mono or 2 × mono	stereo
Sample rate	32 kHz	32 kHz or 48 kHz	32 kHz or 48 kHz	32 kHz or 48 kHz	32 kHz, 44.1 kHz or 48 kHz	32 kHz, 44.1 kHz or 48 kHz
Feature processing						
Volume and balance	X	X	X	X	X	X
Bass and treble	X	X	X	X	X	X
Incredible Stereo	X	X	X	-	-	X
Incredible Mono	if SAP	either or dual	-	X	X	-

[1] Simultaneous decoding of stereo and SAP. dbx-TV noise reduction either on stereo or on SAP.

[2] Default pass-through of L1 and R1.

6.7.2 Additional audio features

The SAA7133HL provides several audio control and enhancement features, like

- Bass, treble, balance and volume control
- Automatic volume levelling (this algorithm lowers louder parts, e.g. commercials)
- Incredible Mono (this algorithm adds stereo-like sound impression to monaural audio signals)
- Incredible Stereo (this algorithm makes stereo sound impression ‘wider’. The distance between the two loudspeakers seems to become larger)
- FM radio stereo decoding

6.7.3 Audio interfaces

The SIF input can handle the sound subcarrier signal from the tuner. Baseband audio signals can be captured through the stereo line-in inputs LEFT1, RIGHT1, LEFT2 and RIGHT2 or the I^2S-bus input.

The decoded and possibly enhanced digital audio stream can be captured through dedicated DMA into the PCI memory space, or to the output in I^2S-bus format, e.g. to a peripheral digital sound amplifier. The third way is to re-convert the audio signal to analog via the integrated audio stereo DACs and feed it directly through the loop back cable to the sound card or to headphones for local monitoring.

A master clock output (A_CLK_master) for synchronous clocking of external devices is available via a GPIO output. The audio block is also able to work synchronously to an external audio reference clock (A_REF_CLK).

6.7.4 Default analog audio pass-through and loop back cable

Most operating systems are prepared to deal with audio input at only one single entry point, namely at the sound card function. Therefore the sound associated with video has to get routed through the sound card.

The SAA7133HL supports analog audio pass-through and the loop back cable on-chip. No external components are required. The audio signal, that was otherwise connected to the sound card line-in, e.g. analog sound from a CD-ROM drive, has to be connected to one of the inputs of the SAA7133HL. By default, after a system reset and without involvement of any driver, this audio signal is passed through to the analog audio output pins, that will feed the loop back cable to the sound card line-in connector. The AV capture driver has to open the default pass-through and switch in the TV sound signal by will.

6.8 DTV/DVB channel decoding and MPEG TS or PS capture

The SAA7133HL also supports application extension to cover the reception of digital TV broadcast [DTV/ATSC, DVB (T/C/S) or BS-digital]. The low IF signal from a hybrid tuner is fed to a peripheral channel decoder, to decode it into the transport stream. This TS, accompanied by a clock and handshake signals [Start Of Packet (SOP), etc.] can be captured by the SAA7133HL, in serial or parallel format. The TS packets are written in a structured way in dedicated DMA definition into the PCI memory space. Toggling between two DMA buffers is supported automatically.

The SAA7133HL supports also capturing of MPEG elementary and program streams. This expands the connectivity to MPEG encoders like the NXP SAA6752HS or similar devices.

6.9 Control of peripheral devices

6.9.1 I^2C-bus master

The SAA7133HL incorporates an I^2C-bus master to set-up and control peripheral devices such as tuner, DTV/DVB channel decoder, audio DSP co-processors, etc. The I^2C-bus interface itself is controlled from the PCI-bus on a command level, reading and writing byte by byte. The actual I^2C-bus status is reported (status register) and, as an option, can raise error interrupts on the PCI-bus.

At PCI reset time, the I^2C-bus master receives board specific information from the on-board EEPROM to update the PCI configuration registers.

The I²C-bus interface is multi-master capable and can assume slave operation too. This allows application of the device in the stand-alone mode, i.e. with the PCI-bus not connected. Under the slave mode, all internal programming registers can be reached via the I²C-bus with exception of the PCI configuration space.

6.9.2 Propagate reset

The PCI system reset and ACPI power management state D3 is propagated to peripheral devices by the dedicated pin $\overline{\text{PROP\_RST}}$. This signal is switched to active LOW by reset and D3, and is only switched HIGH under control of the device driver 'by will'. The intention is that peripheral devices will use signal $\overline{\text{PROP\_RST}}$ as Chip-Enable (CE). The peripheral devices should enter a low power consumption state if pin $\overline{\text{PROP\_RST}}$ = LOW, and reset into default setting at the rising edge.

6.9.3 GPIO

The SAA7133HL offers a set of General Purpose Input/Output (GPIO) pins, to interface to on-board peripheral circuits; see also Table 8. These GPIOs are intended to take over dedicated functions:

- Digital video port output: 8-bit or 16-bit wide (including raw DTV)
- Digital audio serial output: i.e. I²S-bus output
- Transport stream input:
  - parallel (also applicable for program stream and elementary stream)
  - serial (also applicable as I²S-bus input)
- Peripheral interrupt input: four GPIO pins of the SAA7133HL can be enabled to raise an interrupt on the PCI-bus; by this means, peripheral devices can directly intercept with the device driver on changed status or error conditions

Any GPIO pin that is not used for a dedicated function is available for direct read and write access via the PCI-bus. Any GPIO pin can be selected individually as input or output (masked write). By these means, very tailored interfacing to peripheral devices can be created via the SAA7133HL capture driver running on Windows operating systems.

At system reset (PCI reset) all GPIO pins will be set to 3-state and input, and the logic level present on the GPIO pins at that moment will be saved into a special 'strap' register. All GPIO pins have an internal pull-down resistor (LOW level), but can be strapped externally with a 4.7 kΩ resistor to the supply voltage (HIGH level). The device driver can investigate the strap register for information about the hardware configuration of a given board.

7. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDD}	digital supply voltage		–0.5	+4.6	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
ΔV_{SS}	ground supply voltage difference		-	100	mV
$V_{I(a)}$	analog input voltage		–0.5	+4.6	V
V_I	input voltage	at pins XTALI, SDA and SCL	–0.5	V_{DDD} + 0.5	V
$V_{I(D)}$	digital input voltage	at digital I/O stages, outputs in 3-state			
		outputs in 3-state; –0.5 V < V_{DDD} < 3.0 V	–0.5	+4.6	V
		outputs in 3-state; 3.0 V < V_{DDD} < 3.6 V	–0.5	+5.5	V
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		0	70	°C
V_{esd}	electrostatic discharge voltage	human body model[1]	-	±2000	V
		machine model[2]	-	±150	V

[1] Class 2 according to *EIA/JESD22-A114E*.

[2] Class A according to *EIA/JESD22-A115-A*.

8. Thermal characteristics

Table 21. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	30	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all power and ground pins must be connected to the power and ground layers directly. An ample copper area directly under the SAA7133HL with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition, the usage of soldering glue with a high thermal conductance after curing is recommended.

9. Characteristics

Table 22. Characteristics

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
P	power dissipation	power state				
		D0 for typical application	-	1.35	1.6	W
		D0 after reset	-	0.15	-	W
		D1	-	0.2	-	W
		D2	-	0.15	-	W
		D3-hot	-	-	0.02	W
Crystal oscillator						
V_{IH}	HIGH-level input voltage	at pin XTALI	2	-	V_{DDD} + 0.3	V
V_{IL}	LOW-level input voltage	at pin XTALI	–0.3	-	+0.8	V
P_{drive}	drive power	at pin XTALO	-	0.5	-	mW
$f_{xtal(nom)}$	nominal crystal frequency	crystal 1; see Table 23	-	32.11	-	MHz
		crystal 2; see Table 23	-	24.576	-	MHz
$\Delta f/f_{xtal(nom)}$	nominal crystal frequency deviation		-	-	±70	ppm
f_{xtal}	crystal frequency		24	-	33	MHz
t_{jit}	jitter time	oscillator	-	-	±100	ps
PCI-bus inputs and outputs						
V_{IH}	HIGH-level input voltage		2	-	5.75	V
V_{IL}	LOW-level input voltage		–0.5	-	+0.8	V
I_{LI}	input leakage current	HIGH-level; V_I = 2.7 V	[1] -	-	10	µA
		LOW-level; V_I = 0.5 V	[1] -	-	–10	µA
V_{OH}	HIGH-level output voltage	I_O = –2 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_O = 3 mA or 6 mA	[2] -	-	0.55	V
C_i	input capacitance					
		at pin PCI_CLK	5	-	12	pF
		at pin IDSEL	-	-	8	pF
		other input pins	-	-	10	pF
SR_r	rising slew rate	0.4 V to 2.4 V	[3] 1	-	5	V/ns
SR_f	falling slew rate	2.4 V to 0.4 V	[3] 1	-	5	V/ns

Table 22. Characteristics *...continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{val}	CLK to signal valid delay time - bused signals	see Figure 13	2	-	11	ns
$t_{val(ptp)}$	CLK to signal valid delay time - point-to-point		[4] 2	-	12	ns
t_{on}	float to active delay time	see Figure 13	[5] 2	-	-	ns
t_{off}	active to float delay time	see Figure 13	[5] -	-	28	ns
t_{su}	input set-up time to CLK - bused signals	see Figure 13	7	-	-	ns
$t_{su(ptp)}$	input set-up time to CLK - point-to-point		[4] 10 (12)	-	-	ns
t_h	input hold time from CLK	see Figure 13	0	-	-	ns
$t_{rst-clk}$	reset active time after CLK stable		[6] 100	-	-	µs
$t_{rst-off}$	reset active to output float delay time		[5][6][7] -	-	40	ns
I²C-bus interface, compatible to 3.3 V and 5 V signalling (pins SDA and SCL)						
V_{IL}	LOW-level input voltage		[8] –0.5	-	$0.3V_{DD(I2C)}$	V
V_{IH}	HIGH-level input voltage		[8] $0.7V_{DD(I2C)}$	-	$V_{DD(I2C)}$ + 0.5	V
V_{OL}	LOW-level output voltage	$I_{o(sink)}$ = 3 mA	-	-	0.4	V
f_{bit}	bit rate		0	-	400	kbit/s
Analog video inputs						
Inputs (pins CV0 to CV4)						
I_{CL}	clamping current	DC input voltage V_I = 0.9 V	-	±8	-	µA
$V_{i(p-p)}$	peak-to-peak input voltage		[9] 0.375	0.75	1.07	V
C_i	input capacitance		-	-	10	pF
9-bit analog-to-digital converters						
$\alpha_{ct(ch)}$	channel crosstalk	f_i < 5 MHz	-	-	–50	dB
$B_{video(-3dB)}$	–3 dB video bandwidth	at ADC only	[10] -	7	-	MHz
φ_{dif}	differential phase	amplifier plus anti-alias filter bypassed	-	2	-	deg
G_{dif}	differential gain	amplifier plus anti-alias filter bypassed	-	2	-	%
DLE_{DC}	DC differential linearity error		-	1.4	-	LSB
ILE_{DC}	DC integral linearity error		-	2	-	LSB

Table 22. Characteristics *…continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S/N	signal-to-noise ratio	f_i = 4 MHz; anti-alias filter bypassed; AGC = 0 dB		-	50	-	dB
ENOB	effective number of bits	f_i = 4 MHz; anti-alias filter bypassed; AGC = 0 dB		-	8	-	bit
Analog sound input (pin SIF)							
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	input level adjustment at 0 dB		-	941	-	mV
		input level adjustment at –10 dB		-	2976	-	mV
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	input level adjustment at 0 dB		-	59	-	mV
		input level adjustment at –10 dB		-	188	-	mV
$V_{i(AGC)}$	AGC input voltage	in addition to 0 dB and –10 dB switch		-	24	-	dB
f_i	input frequency			3	-	12	MHz
R_i	input resistance	default pre-gain selection for pin SIF (0 dB)		10	-	-	kΩ
C_i	input capacitance			-	7.5	11	pF
Analog audio inputs (pins LEFT1, RIGHT1, LEFT2 and RIGHT2) and outputs (pins OUT_LEFT and OUT_RIGHT)							
$V_{i(nom)(rms)}$	nominal input voltage (RMS value)		[11]	-	200	-	mV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	THD < 3 %	[12]	-	1	2	V
$V_{o(nom)(rms)}$	nominal output voltage (RMS value)		[11]	-	180	-	mV
$V_{o(max)(rms)}$	maximum output voltage (RMS value)	THD < 3 %		-	1	-	V
R_i	input resistance	$V_{i(max)}$ = 1 V (RMS)		-	145	-	kΩ
		$V_{i(max)}$ = 2 V (RMS)		-	48	-	kΩ
R_o	output resistance			150	250	375	Ω
$R_{L(AC)}$	AC load resistance			10	-	-	kΩ
C_L	load capacitance	output		-	-	12	nF
$V_{offset(DC)}$	DC offset voltage	static		-	10	30	mV
THD+N	total harmonic distortion-plus-noise	$V_i = V_o$ = 1 V (RMS); f_i = 1 kHz; bandwidth B = 20 Hz to 20 kHz		-	0.1	0.3	%
S/N	signal-to-noise ratio	reference voltage V_o = 1 V (RMS); f_i = 1 kHz; *"ITU-R BS.468"* weighted; quasi peak		70	75	-	dB
α_{ct}	crosstalk attenuation	between any analog input pairs; f_i = 1 kHz		60	-	-	dB
α_{cs}	channel separation	between left and right of each input pair		60	-	-	dB

Table 22. Characteristics *…continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Sound demodulator performance[13]						
Audio AM mono characteristics (DDEP standard code = 10)						
S/N	signal-to-noise ratio	AM carrier 6.5 MHz; 54 % AM; f_i = 1 kHz; second SIF AGC off; *"ITU-R BS.468"* weighted; quasi peak	-	47	-	dB
THD+N	total harmonic distortion-plus-noise	AM carrier 6.5 MHz; 54 % AM; f_i = 1 kHz; second SIF AGC off; *"ITU-R BS.468"* weighted; quasi peak	-	0.43	-	%
ΔG_f	frequency gain variation	from 20 Hz to 15 kHz; f_{ref} = 1 kHz; no clipping	-	–0.5 to +0.1	-	dB
Audio M standard BTSC characteristics (DDEP standard code = 13)						
S/N	signal-to-noise ratio	**BTSC stereo** with L or R only; 100 % modulation; f_i = 1 kHz; unweighted RMS	-	77	-	dB
		SAP decoder output; 100 % modulation; f_i = 1 kHz; compromise de-emphasis (SAPDBX = 0b); bandwidth = 0 kHz to 15 kHz; unweighted RMS	-	59	-	dB
THD+N	total harmonic distortion-plus-noise	**BTSC stereo** with L or R only; 100 % modulation; f_i = 1 kHz; unweighted RMS	-	0.23	-	%
		SAP decoder output; 100 % modulation; f_i = 1 kHz; compromise de-emphasis (SAPDBX = 0b); bandwidth = 0 kHz to 15 kHz; unweighted RMS	-	0.27	-	%
α_{ct}	crosstalk attenuation	1 kHz L or R or SAP; 100 % modulation; spectral at 1 kHz				
		BTSC to SAP	-	> 80	-	dB
		SAP to BTSC	-	> 80	-	dB
$\alpha_{cs(stereo)}$	stereo channel separation	L or R only; 50 Hz to 10 kHz	[14]			
		10 % EIM	-	≥ 32	-	dB
		1 to 66 % EIM	-	≥ 27	-	dB
ΔG_f	frequency gain variation	30 % modulation; f_{ref} = 1 kHz				
		stereo; L or R only	-	–0.4 to +1.5	-	dB
		mono; L = R	-	–0.2 to +0.04	-	dB

Table 22. Characteristics *…continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Audio M standard EIAJ characteristics (DDEP standard code = 14)						
S/N	signal-to-noise ratio	100 % modulation; f_i = 1 kHz; unweighted RMS				
		EIAJ stereo with L or R; at EIAJ decoder output	-	61	-	dB
		EIAJ dual; at EIAJ sub-channel decoder output	-	59	-	dB
THD+N	total harmonic distortion-plus-noise	100 % modulation; f_i = 1 kHz; unweighted RMS				
		EIAJ stereo with L or R; at EIAJ decoder output	-	0.17	-	%
		EIAJ dual; at EIAJ sub-channel decoder output	-	0.8	-	%
$\alpha_{ct(dual)}$	dual crosstalk attenuation	100 % modulation; f_i = 1 kHz				
		main to sub-channel	-	80	-	dB
		sub to main channel	-	80	-	dB
$\alpha_{cs(stereo)}$	stereo channel separation	50 % modulation; selective RMS; L or R				
		100 Hz to 5 kHz	-	38	-	dB
		50 Hz to 8 kHz	-	28	-	dB
ΔG_f	frequency gain variation	**EIAJ stereo**; from 20 Hz to 12 kHz; 15 % modulation; f_{ref} = 1 kHz	-	–0.9 to +0.1	-	dB
Audio FM radio characteristics (DDEP standard code = 15 to 18)						
S/N	signal-to-noise ratio	**FM radio stereo** with L or R only; 10.7 MHz carrier; 100 % modulation; f_i = 1 kHz; 75 µs de-emphasis; unweighted RMS	-	55	-	dB
THD+N	total harmonic distortion-plus-noise	**FM radio stereo** with L or R only; 10.7 MHz carrier; 100 % modulation; f_i = 1 kHz; 75 µs de-emphasis; unweighted RMS	-	0.2	-	%
$\alpha_{cs(stereo)}$	stereo channel separation	60 % modulation; selective RMS; pre-emphasis off; 100 Hz to 14 kHz	-	45 to 55	-	dB
ΔG_f	frequency gain variation	**FM radio stereo**; from 20 Hz to 15 kHz; 10.7 MHz carrier; 75 µs de-emphasis; 30 % modulation; f_{ref} = 1 kHz	-	–0.2 to +0.4	-	dB
Audio identification of EIAJ mono/stereo (Japanese) standards						
m_{pilot}	modulation degree of pilot tone	nominal pilot level and identification frequency; no overmodulation				
		European system	-	10	-	%
		Japanese system	-	21	-	%

Table 22. Characteristics *...continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Δf_{ident}	identification frequency window	M standard (EIAJ)				
		stereo; slow mode	-	981.9 to 983.0	-	Hz
		stereo; fast mode	-	979.7 to 985.1	-	Hz
		slow mode	-	921.8 to 923.0	-	Hz
		fast mode	-	919.3 to 925.8	-	Hz
$t_{d(on)(ident)}$	identification on delay time	slow mode	-	2	-	s
		fast mode	-	0.5	-	s
$t_{d(off)(ident)}$	identification off delay time	slow mode	-	2	-	s
		fast mode	-	0.5	-	s
Audio Automatic Standard Detection (ASD) timing; STDSEL = 1Dh						
$t_{asd(mono)}$	mono automatic standard detection time	default threshold settings	-	65	-	ms
$t_{asd(stereo)}$	stereo automatic standard detection time	BTSC stereo	-	0.25	-	s
		BTSC SAP	-	0.3	-	s
		EIAJ	-	0.5	-	s
All digital I/Os: GPIO pins and BST test pins (5 V tolerant)						
Pins GPIO0 to GPIO23, V_CLK, GPIO25 to GPIO27, TDI, TDO, TMS, TCK and $\overline{TRST}$						
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
V_{IL}	LOW-level input voltage		–0.3	-	+0.8	V
I_{LI}	input leakage current		-	-	1	µA
$I_{L(I/O)}$	leakage current (I/O)	3.3 V signal levels at $V_{DDD} \geq 3.3$ V	-	-	10	µA
C_i	input capacitance	I/O at high-impedance	-	-	8	pF
R_{pd}	pull-down resistance	$V_I = V_{DDD}$	-	50	-	kΩ
R_{pu}	pull-up resistance	$V_I = 0$	-	50	-	kΩ
V_{OH}	HIGH-level output voltage	I_O = –2 mA	2.4	-	V_{DDD} + 0.5	V
V_{OL}	LOW-level output voltage	I_O = 2 mA	0	-	0.4	V
Audio-video port outputs (digital video stream from comb filter decoder or scaler, digital audio from sound decoder or baseband audio inputs via I^2S-bus)						
LLC and LLC2 clock output on pin V_CLK (see Figure 14)						
C_L	load capacitance		15	-	50	pF
T_{cy}	cycle time	LLC active	35	-	39	ns
		LLC2 active	70	-	78	ns

Table 22. Characteristics *...continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
δ	duty cycle	C_L = 40 pF	[15]				
		LLC active		35	-	65	%
		LLC2 active		35	-	65	%
t_r	rise time	0.4 V to 2.4 V		-	-	5	ns
t_f	fall time	2.4 V to 0.4 V		-	-	5	ns
Video data output with respect to signal V_CLK on pins GPIO0 to GPIO17, GPIO22 and GPIO23 (see Figure 14)							
C_L	load capacitance			15	-	50	pF
t_h	hold time		[16][17]				
		LLC active		5	-	-	ns
		LLC2 active		15	-	-	ns
t_{PD}	propagation delay	from positive edge of signal V_CLK	[16][17]				
		LLC active		-	-	28	ns
		LLC2 active		-	-	55	ns
Raw DTV/DVB outputs (reuse of video ADCs in DVB/TV applications)							
Clock input signal X_CLK_IN on pin GPIO18							
T_{cy}	cycle time			27.8	37	333	ns
δ	duty cycle		[15]	40	50	60	%
t_r	rise time	0.8 V to 2.0 V		-	-	5	ns
t_f	fall time	2.0 V to 0.8 V		-	-	5	ns
Clock output signal ADC_CLK on pin V_CLK							
C_L	load capacitance			-	-	25	pF
T_{cy}	cycle time			27.8	-	-	ns
δ	duty cycle	C_L = 40 pF	[15]	40	-	60	%
t_r	rise time	0.4 V to 2.4 V		-	-	5	ns
t_f	fall time	2.4 V to 0.4 V		-	-	5	ns
VSB data output signals with respect to signal ADC_CLK							
C_L	load capacitance			25	-	50	pF
t_h	hold time	inverted and not delayed	[16]	5	-	-	ns
t_{PD}	propagation delay	from positive edge of signal ADC_CLK; inverted and not delayed	[16]	-	-	23	ns
TS capture inputs with parallel transport streaming (TS-P); e.g. DVB applications							
Clock input signal TS_CLK on pin GPIO20 (see Figure 15)							
T_{cy}	cycle time			-	333	-	ns
δ	duty cycle		[15]	40	-	60	%
t_r	rise time	0.8 V to 2.0 V		-	-	5	ns
t_f	fall time	2.0 V to 0.8 V		-	-	5	ns
Data and control input signals on TS-P port (with respect to signal TS_CLK) on pins GPIO0 to GPIO7, GPIO16, GPIO19 and GPIO22 (see Figure 15)							
$t_{su(D)}$	data input set-up time			3	-	-	ns

Table 22. Characteristics *…continued*

For minimum and maximum values: V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; for typical values: V_{DDD} = 3.3 V; V_{DDA} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(D)}$	data input hold time		8	-	-	ns
TS capture inputs with serial transport streaming (TS-S); e.g. DVB applications						
Clock input signal TS_CLK on pin GPIO20 (see Figure 15)						
T_{cy}	cycle time		37	-	-	ns
δ	duty cycle		[15] 40	-	60	%
t_r	rise time	0.8 V to 2.0 V	-	-	5	ns
t_f	fall time	2.0 V to 0.8 V	-	-	5	ns
Data and control input signals on TS-S port (with respect to signal TS_CLK) on pins GPIO16, GPIO19, GPIO21 and GPIO22 (see Figure 15)						
$t_{su(D)}$	data input set-up time		3	-	-	ns
$t_{h(D)}$	data input hold time		8	-	-	ns

[1] Input leakage currents include high-impedance output leakage for all bidirectional buffers with 3-state outputs.

[2] Pins without pull-up resistors must have a 3 mA output current. Pins requiring pull-up resistors must have 6 mA; these are pins FRAME#, TRDY#, IRDY#, DEVSEL#, SERR#, PERR#, INT_A and STOP#.

[3] This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range.

[4] REQ# and GNT# are point-to-point signals and have different output valid delay and input set-up times than bused signals. GNT# has a set-up time of 10 ns. REQ# has a set-up time of 12 ns.

[5] For purposes of active or float timing measurements, the high-impedance or 'off' state is defined to be when the total current delivered through the device is less than or equal to the leakage current specification.

[6] $\overline{RST}$ is asserted and de-asserted asynchronously with respect to CLK.

[7] All output drivers floated asynchronously when $\overline{RST}$ is active.

[8] $V_{DD(I2C)}$ is the extended pull-up voltage of the I^2C-bus (3.3 V or 5 V bus).

[9] Nominal analog video input signal is to be terminated by 75 Ω that results in 1 V (p-p) amplitude. This termination resistor should be split into 18 Ω and 56 Ω, and the dividing tap should feed the video input pin, via a coupling capacitor of 47 nF, to achieve a control range from −3 dB (attenuation) to +6 dB (amplification) for the internal automatic gain control. See also the application note of the SAA7133HL.

[10] See *user manual SAA7133HL* for Anti-Alias Filter (AAF).

[11] Definition of levels and level setting:

The full-scale level for analog audio signals V_{FS} = 0.8 V (RMS). The nominal level at the digital crossbar switch is defined at −15 dB (FS).

Nominal audio input levels: external, mono, V_i = 180 mV (RMS); −15 dB (FS).

[12] The analog audio inputs (pins LEFT1, RIGHT1, LEFT2 and RIGHT2) are supported by two input levels: 1 V (RMS) and 2 V (RMS), selectable independently per stereo input pair, LEFT1, RIGHT1 and LEFT2, RIGHT2.

[13] V_{DDA} = 3.3 V; $V_{i(SIF)}$ = 196 mV (RMS); level and gain settings according to Table note 11; for external components see the application diagram in *SAA7133HL application notes*; unless otherwise specified.

[14] Effective Input Modulation (EIM) means 75 µs de-emphasis applied to audio input signals of the BTSC stereo encoder.

[15] The definition of the duty factor: $\delta = \frac{t_{clk(H)}}{T_{cy}}$

[16] The output timing must be measured with the load of a 30 pF capacitor to ground and a 500 Ω resistor to 1.4 V.

[17] Signal V_CLK inverted; not delayed (default set-up).

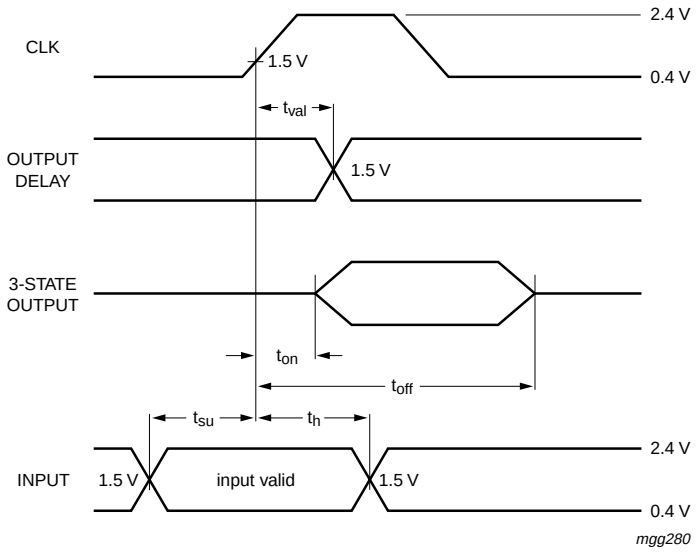


Fig 13. PCI I/O timing

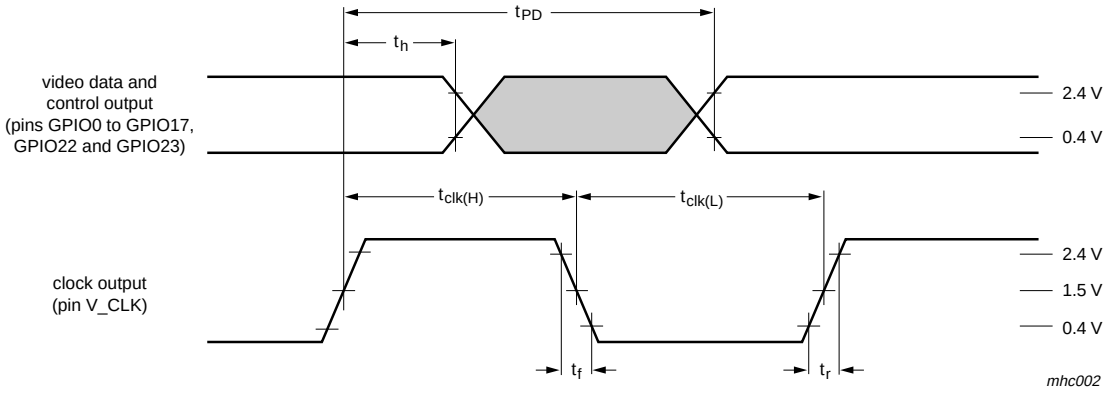


Fig 14. Data output timing (video data, control outputs and raw DTV/DVB)

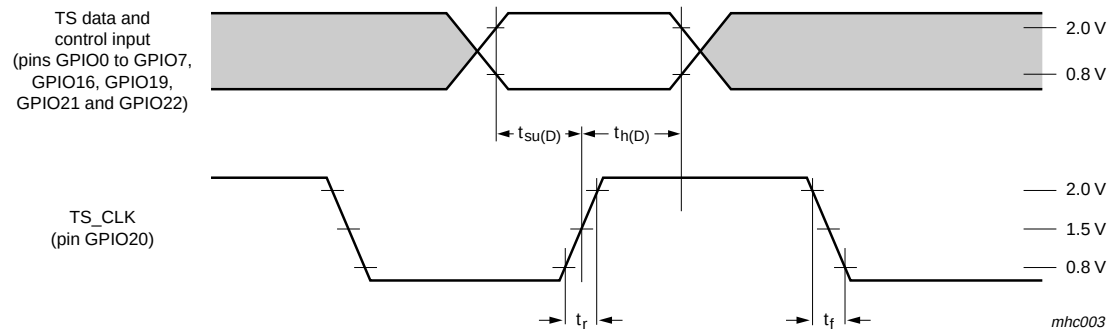


Fig 15. Data input timing (TS data and control inputs)

Table 23. Specification of crystals and related applications (examples) [1]

Standard	Crystal frequency 32.11 MHz			Crystal frequency 24.576 MHz			Unit
	Fundamental		3rd harmonic	Fundamental		3rd harmonic	
	1B	1C	1A	2B	2C	2A	
Crystal specification							
Typical load capacitance	20	8	8	20	8	10	pF
Maximum series resonance resistance	30	60	50	30	60	80	Ω
Typical motional capacitance	20	13.5	1.5	20	1	1.5	fF
Maximum parallel capacitance	7	3 ± 1	4.3	7	3.3	3.5	pF
Maximum permissible deviation	±30	±30	±30	±30	±30	±50	ppm
Maximum temperature deviation	±30	±30	±30	±30	±30	±20	ppm
External components							
Typical load capacitance at pin XTALI	33	10	15	27	5.6	18	pF
Typical load capacitance at pin XTALO	33	10	15	27	5.6	18	pF
Typical capacitance of LC filter	n.a.	n.a.	1	n.a.	n.a.	1	nF
Typical inductance of LC filter	n.a.	n.a.	4.7	n.a.	n.a.	4.7	µH

[1] For oscillator application, see *SAA7133HL application note*.

10. Support information

10.1 Related documents

This document describes the functionality and characteristics of the SAA7133HL. Other documents related to the SAA7133HL are:

- User manual SAA7133HL, describing the programmability
- Application note SAA7133HL, pointing out recommendations for system implementation
- Data sheets of other devices referred to in this document, e.g:
  - Tuners:

    FI1236 for NTSC (US)

    FI1286 for NTSC (Japan)

    combi-tuner derivatives for FM radio: FM12x6
  - SAA6752HS: MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

11. Test information

11.1 Boundary scan test

The SAA7133HL has built-in logic and five dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7133HL follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary - Scan Architecture"* set by the Joint Test Action Group (JTAG).

The five special pins are: Test Mode Select (TMS), Test Clock (TCK), Test Reset ($\overline{\text{TRST}}$), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 24). Details about the JTAG BST-test can be found in the specification "*IEEE Std. 1149.1"*. A file containing the detailed Boundary Scan Description Language (BSDL) description of the SAA7133HL is available on request.

11.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in the functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state if pin $\overline{\text{TRST}}$ is at LOW level.

11.1.2 Device identification codes

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected internally between pins TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level, this code can be used to verify component manufacturer,

type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO) (see Figure 16).

A device identification register is specified in *"IEEE Std. 1149.1b-1994"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

Table 24. BST instructions supported by the SAA7133HL

Instruction	Description
BYPASS	this mandatory instruction provides a minimum length serial path (1 bit) between pins TDI and TDO when no test operation of the component is required
EXTEST	this mandatory instruction allows testing of off-chip circuitry and board level interconnections
SAMPLE	this mandatory instruction can be used to take a sample of the inputs during normal operation of the component; it can also be used to preload data values into the latched outputs of the boundary scan register
CLAMP	this optional instruction is useful for testing when not all ICs have BST; this instruction addresses the bypass register while the boundary scan register is in external test mode
IDCODE	this optional instruction will provide information on the components manufacturer, part number and version number

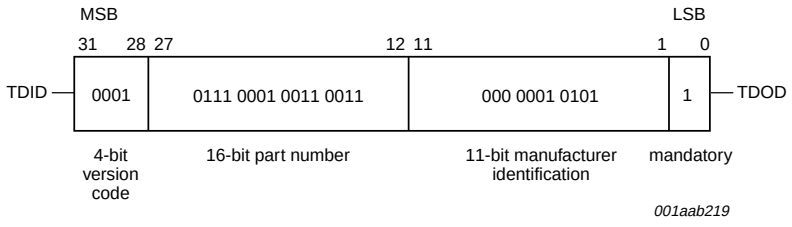
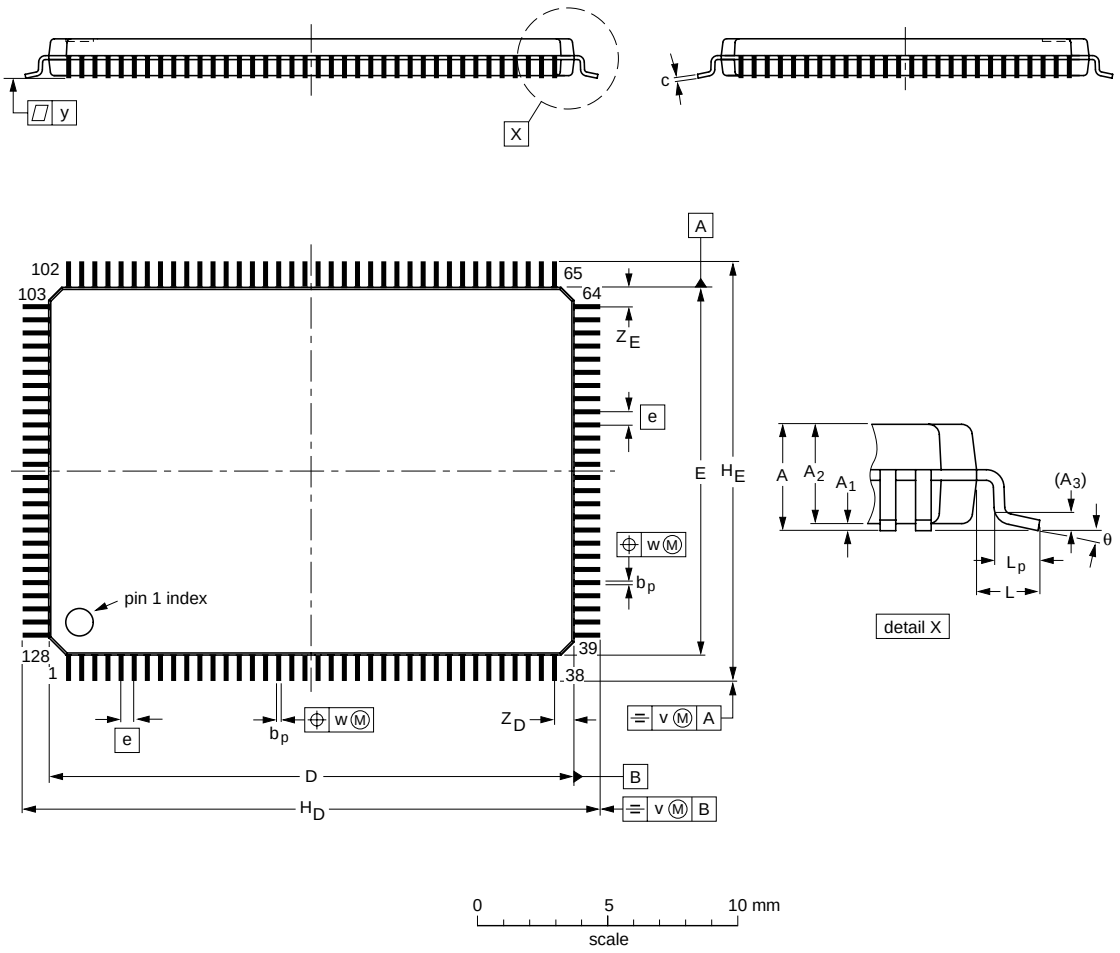


Fig 16. 32 bits of identification code

12. Package outline

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT425-1	136E28	MS-026				~~00-01-19~~ 03-02-20

Fig 17. Package outline SOT425-1 (LQFP128)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 25 and 26

Table 25. SnPb eutectic process (from J-STD-020C)

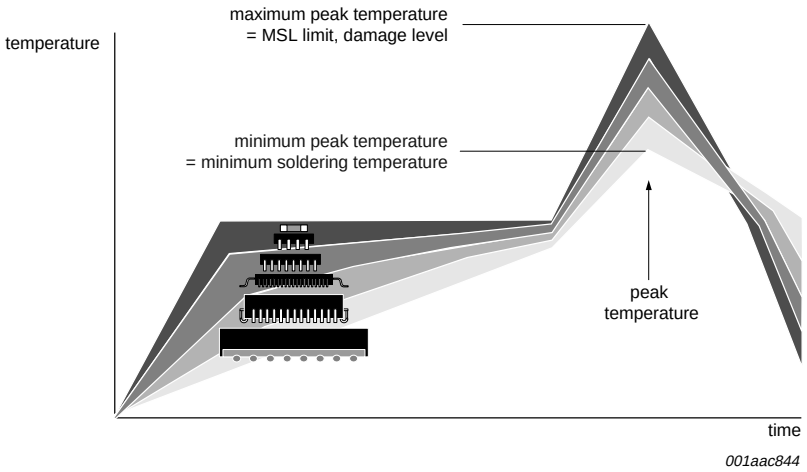
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 26. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 27. Abbreviations

Acronym	Description
AC-3	Audio Code 3 (Dolby Digital)
ACPI	Advanced Configuration and Power Interface
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AM	Amplitude Modulation
API	Application Programming Interface
ASD	Automatic Standard Detection
ATSC	Advanced Television Systems Committee
AVL	Automatic Volume Levelling
BDA	Broadcast Driver Architecture
BSDL	Boundary Scan Description Language
BST	Boundary Scan Test
BTSC	Broadcast Television Systems Committee
CC	Closed Captioning (in running text)
CD-ROM	Compact Disk Read Only Memory
CE	Chip-Enable
CGMS	Copy Guard Management System
CMOS	Complementary Metal-Oxide-Semiconductor
COM	Component Object Model

Table 27. Abbreviations *…continued*

Acronym	Description
CPU	Central Processing Unit
CVBS	Composite Video Blanking Sync (also known as “composite video signal”)
DAC	Digital-to-Analog Converter
DDEP	Demodulator and Decoder Easy Programming
DMA	Direct Memory Access
DMSD	Digital MultiStandard Decoder
DQPSK	Differential Quadrature Phase Shift Keying
DSP	Digital Signal Processor
DTV	Digital TeleVision
DVB	Digital Video Broadcasting
DVD	Digital Video Disc
EAV	End of Active Video
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
EIAJ	Electronic Industries Association of Japan
EIM	Effective Input Modulation
EPG	Electronic Program Guide
FID	Field-ID
FIFO	First-in First-Out
FIR	Finite-Impulse Response
FLC	Frame-Locked Clock
FM	Frequency Modulation
FS	Full-Scale
GPIO	General Purpose Input/Output
HAL	Hardware Abstraction Layer
I^2C	Inter-IC-Connection
I^2S	Inter-IC Sound
I/O	Input/Output
IC	Integrated Circuit
ID	IDentifier
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
INT	INTerrupt
IRE	Institute of Radio Engineers
ITU	International Telecommunication Union
ITU-R	ITU-Radio communication sector
ITU-T	International Telecommunication Union - Telecommunications sector
JTAG	Joint Test Action Group
JEDEC	Joint Electron Device Engineering Council
KS	Kernel Streaming
LLC	Line-Locked Clock

Table 27. Abbreviations *…continued*

Acronym	Description
MMU	Memory Management Unit
MPEG	Moving Picture Experts Group
NABTS	North American Broadcast Text System
NICAM	Near-Instantaneously Companded Audio Multiplex
NTSC	National Television Systems Committee
OS	Operating System
PAL	Phase Alternating Line
PC	Personal Computer (in running text)
	Picture Carrier (in Characteristics)
PCI	Peripheral Component Interconnect
PS	Program Stream
QAM	Quadrature Amplitude Modulation
QFDM	Quadrature Frequency Delta Modulation
RF	Radio Frequency
RGB	Red-Green-Blue (additive color space)
RMS	Root Mean Square
SAP	Secondary Audio Program
SAV	Start of Active Video
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs
SDK	Software Development Kit
SECAM	Systeme Electronique Couleur Avec Mémoire (French color TV standard)
SIF	Sound IF
SIG	Special Interest Group
SOP	Start Of Packet
S-video	Separated video
TAP	Test Access Port
THD	Total Harmonic Distortion
TS	Transport Stream
TV	TeleVision
UK	United Kingdom
UNIX	UNIpleXed information and computing system
USA	United States of America
VBI	Vertical Blanking Interval
VCR	Video Cassette Recorder
VfW	Video for Windows
VGA	Video Graphic Adapter
VIP	VESA video Interface Port
VMI	Video Module Interface
VPS	Video Programming System
VSB	Vestigal SideBand modulation
VTC	Video Time Codes

Table 27. Abbreviations *...continued*

Acronym	Description
VxD	Virtual device Driver
WSS	Wide Screen Signaling
WST	World System Teletext
WDM	Windows Driver Model
XTAL	Crystal
ZV	Zoom Video

15. Glossary

dbx — American company, which has invented the dbx-TV noise reduction system used within BTSC as based on dynamic compression.

Incredible Mono — An algorithm which adds stereo-like sound impression to mono audio signals.

Incredible Stereo — An algorithm which makes stereo sound impression wider. The distance between the two loudspeakers seems to become greater.

IRE — A unit of an arbitrary scale dividing the 1 V (p-p) video signal from the bottom of sync (−40 IRE) to the peak white level (+100 IRE) into 140 equal units. The active video range lasts from 0 IRE to 100 IRE.

MPEG-2 — Standard for A/V coding and data compression; successor of MPEG-1.

S-video — Separated video (signals for luminance Y and modulated chrominance C)

Tap — One or more extra access points in a digital filter to obtain useful information e.g. to enable a special display of a video signal.

YUV — Component video (signals for luminance Y and chrominance vectors U,V)

16. References

[1] BS.468 — ITU-R Recommendation concerning Broadcasting (Sound): “Measurement of audio-frequency noise voltage level in sound broadcasting”.

[2] BT.601 — ITU-R Recommendation concerning Broadcasting (Television): “Studio encoding parameters of digital television for standard 4 : 3 and wide-screen 16 : 9 aspect ratios”.

[3] BT.656-4:1994 — ITU-R Recommendation concerning Broadcasting service (Television): “Interfaces for digital component video signals in 525-line and 625-line television systems operating at the 4 : 2 : 2 level of ITU-R BT.601 (Part A)”.

[4] JESD22-A114E — JEDEC Standard 22, Test Method A114E: “Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)”.

[5] JESD22-A115-A — JEDEC Standard 22, Test Method A115-A: “Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)”.

[6] IEEE 1149.1 — IEEE “Standard Test Access Port and Boundary Scan Architecture” according to JTAG, issued in 1990, 1993, 1994 and 2001.

17. Revision history

Table 28. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAA7133HL_2	20080218	Product data sheet	-	SAA7133HL_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Reorganized data sheet to include Support information and Test information. • The EIA/JESD22 references have been updated throughout.			
SAA7133HL_1 (9397 750 10353)	20030204	Product specification	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Tables

continued >>

21. Figures

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22. Contents

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Document identifier: SAA7133HL_2