DDR SDRAM RDIMM

MT18VDDF6472D – 512MB[1]

MT18VDDF12872D – 1GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 184-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 512MB (64 Meg x 72) and 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DD}Q = +2.5V$ (-40B: $V_{DD} = V_{DD}Q = +2.6V$)
- $V_{DDSPD} = +2.3V$ to $+3.6V$
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) 2*n*-prefetch architecture
- Bidirectional data strobe (DQS) transmitted/ received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Dual rank
- Selectable burst lengths (BL): 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Gold edge contacts

184-Pin RDIMM (MO-206) Figures

Figure 1: R/C H (-40B)

PCB height: 28.58mm (1.125in)

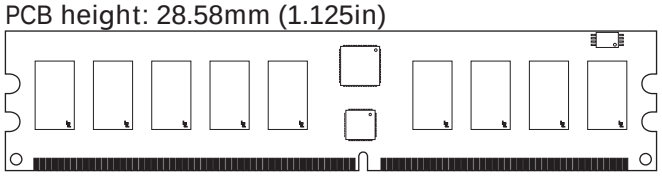
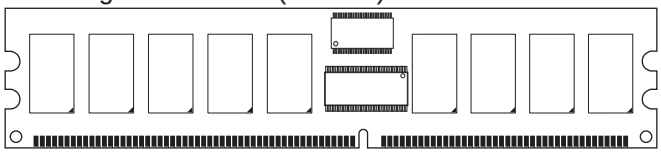


Figure 2: R/C B (-335, -262, -26A, -265)

PCB height: 28.58mm (1.125in)



Options — Marking

- Operating temperature[2]
  - Commercial ($0°C \le T_A \le +70°C$) — None
  - Industrial ($–40°C \le T_A \le +85°C$) — I
- Package
  - 184-pin DIMM (standard) — G
  - 184-pin DIMM (Pb-free) — Y
- Memory clock, speed, CAS latency[3]
  - 5.0ns (200 MHz), 400 MT/s, CL = 3 — -40B
  - 6.0ns (167 MHz), 333 MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2[1] — -262
  - 7.5ns (133 MHz), 266 MT/s, CL = 2[1] — -26A
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5[1] — -265

Notes: 1. Not recommended for new designs.
2. Contact Micron for industrial temperature module offerings.
3. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^tRCD (ns)	^tRP (ns)	^tRC (ns)	Notes
		CL = 3	CL = 2.5	CL = 2				
-40B	PC3200	400	333	266	15	15	55	
-335	PC2700	–	333	266	18	18	60	1
-262	PC2100	–	266	266	15	15	60	
-26A	PC2100	–	266	266	20	20	65	
-265	PC2100	–	266	200	20	20	65	

Notes: 1. The values of ^tRCD and ^tRP for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	8K (A0–A12)	8K (A0–A12)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column address	1K (A0–A9)	2K (A0–A9, A11)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT46V32M8,[1] 256Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^tRCD-^tRP)
MT18VDDF6472DG-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18VDDF6472DY-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18VDDF6472DG-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	3-3-3
MT18VDDF6472DY-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	3-3-3
MT18VDDF6472DG-265__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Notes: 1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
Example: MT18VDDF6472DY-335G2.

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT46V64M8,[1] 512Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT18VDDF12872DG-40B__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18VDDF12872DY-40B__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18VDDF12872DG-335__	1GB	128 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	3-3-3
MT18VDDF12872DY-335__	1GB	128 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	3-3-3
MT18VDDF12872DY-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT18VDDF12872DG-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT18VDDF12872DG-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18VDDF12872DY-335F1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

184-Pin DDR RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	24	DQ17	47	DQS8	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	CB2	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	CB3	74	VSS
6	DQ2	29	A7	52	BA1	75	NC
7	VDD	30	VDDQ	53	DQ32	76	NC
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQS6
10	RESET#	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	NC	39	DQ26	62	VDDQ	85	VDD
17	NC	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	CB0	67	DQS5	90	NC
22	VDDQ	45	CB1	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

184-Pin DDR RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DM8	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DM2	142	CB6	165	DQ52
97	DM0	120	VDD	143	VDDQ	166	DQ53
98	DQ6	121	DQ22	144	CB7	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DM4	172	VDDQ
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DM3	152	VSS	175	DQ61
107	DM1	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DM7
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	CKE1	134	CB4	157	S0#	180	VDDQ
112	VDDQ	135	CB5	158	S1#	181	SA0
113	NC	136	VDDQ	159	DM5	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	A12	138	CK0#	161	DQ46	184	VDDSPD

Table 6: Pin Descriptions

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0 and BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command
BA0, BA1	Input	**Bank address:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) the internal clock, input buffers, and output drivers.
DM0–DM8	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S0#, S1#	Input	**Chip selects:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize the presence-detect data transfer to and from the module.
CB0–CB7	I/O	Check bits.
DQ0–DQ63	I/O	**Data input/output:** Data bus.
DQS0–DQS8	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}/$V_{DD}Q$	Supply	**Power supply:** +2.5V ±0.2V (-40B: +2.6V ±0.1V).
V_{DDSPD}	Supply	**Serial EEPROM power supply:** +2.3V to +3.6V.
V_{REF}	Supply	SSTL_2 reference voltage (V_{DD}/2).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Functional Block Diagrams

Figure 3: Functional Block Diagram R/C H (-40B)

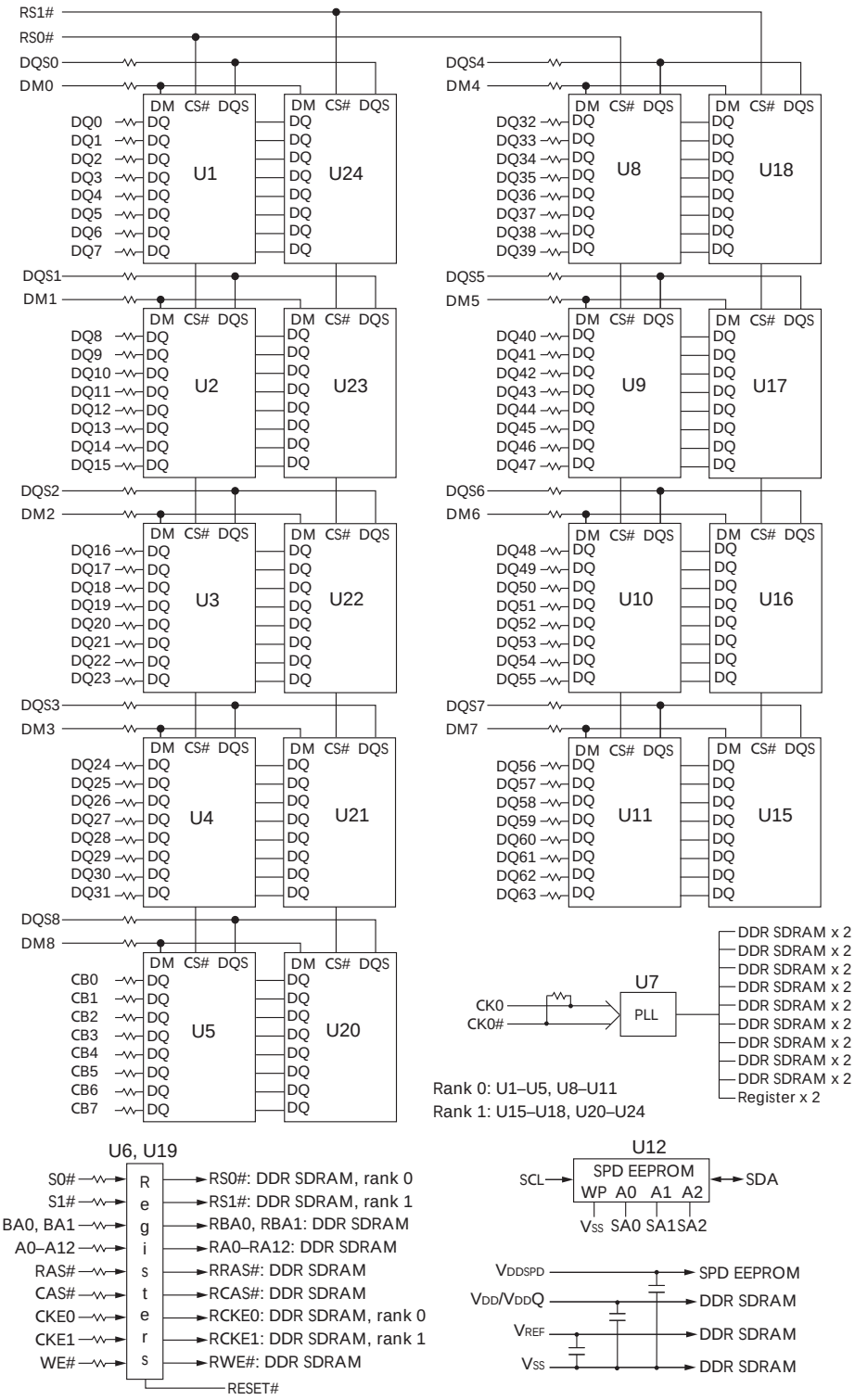
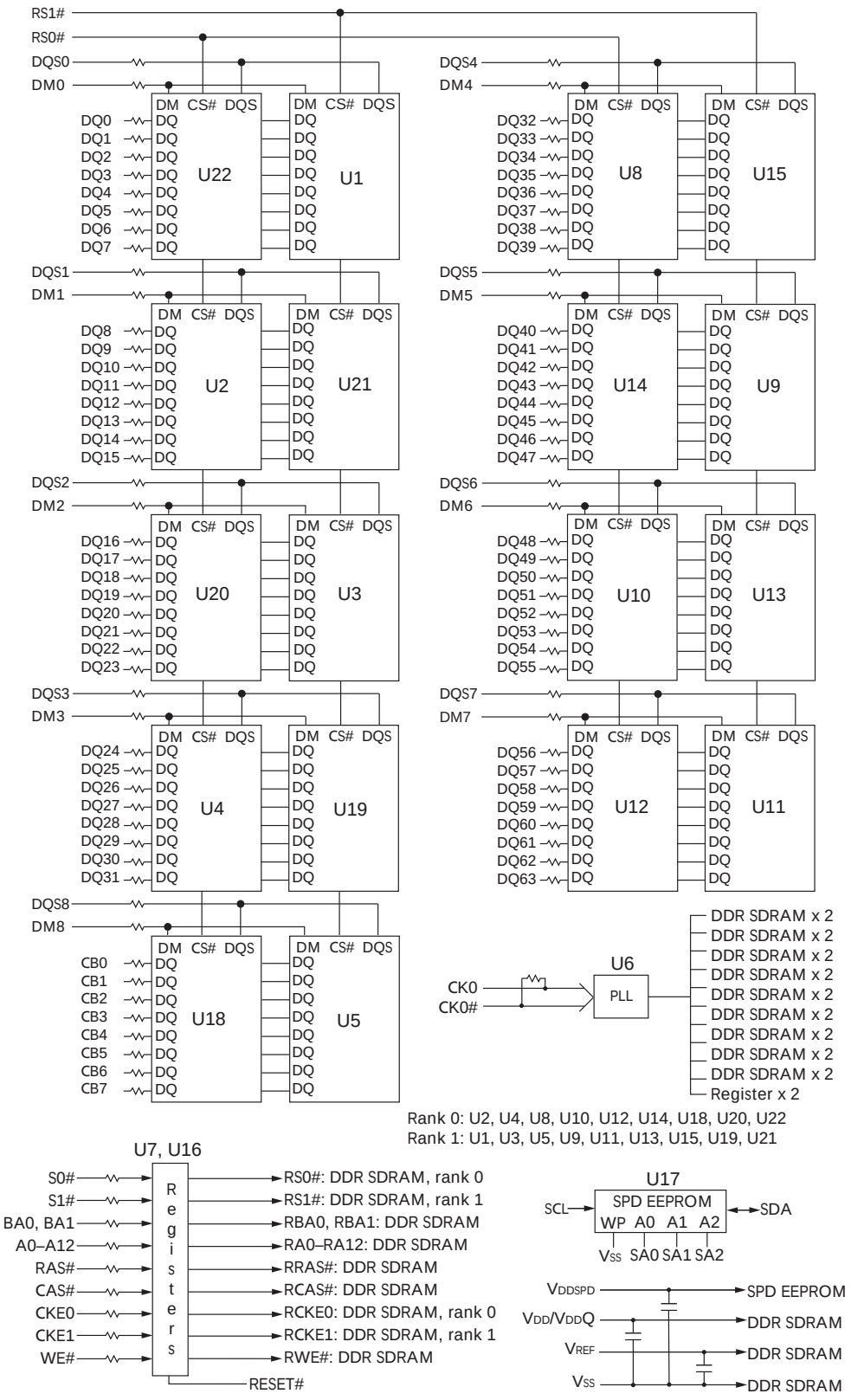


Figure 4: Functional Block Diagram R/C B (-335, -262, -26A, -265)



General Description

The MT18VDDF6472D and MT18VDDF12872D are high-speed, CMOS dynamic random access 512MB and 1GB memory modules organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

These DDR SDRAM modules operate in registered mode, where the control, command, and address input signals are latched in the registers on the rising clock edge and sent to the DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR SDRAM devices. The register(s) and PLL reduce control, command, address, and clock signals loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various DDR SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}/V_{DDQ}	V_{DD}/V_{DDQ} supply voltage relative to V_{SS}		–1.0	+3.6	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+3.2	V
I_I	Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; V_{REF} input $0V \le V_{IN} \le 1.35V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE	–5	+5	µA
		CK, CK#	–10	+10	
		DM	–4	+4	
I_{OZ}	Output leakage current; $0V \le V_{OUT} \le V_{DDQ}$; DQ are disabled	DQ, DQS	–10	+10	µA
T_A	DRAM ambient operating temperature[1]	Commercial	0	+70	°C
		Industrial	–40	+85	°C

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades
DDR components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-40B	-5B
-335	-6
-262	-75E
-26A	-75Z
-265	-75

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

IDD Specifications

Table 9: IDD Specifications and Conditions – 512MB (Die Revision K)
Values are for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one bank active-precharge current: ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0[1]	936	846	mA
Operating one bank active-read-precharge current: BL = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1[1]	1,116	1,071	mA
Precharge power-down standby current: All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW		IDD2P[2]	72	72	mA
Idle standby current: CS# = HIGH; All device banks idle; ^{t}CK = ^{t}CK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DM, and DQS		IDD2F[2]	900	900	mA
Active power-down standby current: One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW		IDD3P[2]	630	540	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N[2]	1,080	990	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA		IDD4R[1]	1,656	1,476	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W[1]	1,656	1,476	mA
Auto refresh current	^{t}RFC = ^{t}RFC (MIN)	IDD5[2]	2,880	2,880	mA
	^{t}RFC = 7.8125µs	IDD5A[2]	108	108	mA
Self refresh current: CKE ≤ 0.2V		IDD6[2]	72	72	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); Address and control inputs change only during active READ or WRITE commands		IDD7[1]	2,646	2,466	mA

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Table 10: IDD Specifications and Conditions – 512MB (All Other Die Revisions)
Values are for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	-265	Units
Operating one bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		$I_{DD}0$[1]	1,251	1,161	1,116	mA
Operating one bank active-read-precharge current: BL = 2; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		$I_{DD}1$[1]	1,566	1,566	1,341	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		$I_{DD}2P$[2]	72	72	72	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		$I_{DD}2F$[2]	1,080	900	810	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		$I_{DD}3P$[2]	720	540	540	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		$I_{DD}3N$[2]	1,260	1,080	900	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); I_{OUT} = 0mA		$I_{DD}4R$[1]	1,836	1,611	1,386	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		$I_{DD}4W$[1]	1,791	1,611	1,386	mA
Auto refresh current	$^{t}RFC = {}^{t}RFC$ (MIN)	$I_{DD}5$[2]	4,680	4,590	4,410	mA
	^{t}RFC = 7.8125µs	$I_{DD}5A$[2]	108	108	108	mA
Self refresh current: CKE ≤ 0.2V		$I_{DD}6$[2]	72	72	72	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		$I_{DD}7$[1]	4,266	3,726	3,321	mA

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Table 11: IDD Specifications and Conditions – 1GB

Values are for the MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	-262	-26A/ -265	Units
Operating one bank active-precharge current: tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0[1]	1,440	1,215	1,215	1,080	mA
Operating one bank active-read-precharge current: BL = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1[1]	1,710	1,485	1,485	1,350	mA
Precharge power-down standby current: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD2P[2]	90	90	90	90	mA
Idle standby current: CS# = HIGH; All device banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DM, and DQS		IDD2F[2]	990	810	810	720	mA
Active power-down standby current: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P[2]	810	630	630	540	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N[2]	1,080	900	800	810	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R[1]	1,755	1,530	1,530	1,350	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W[1]	1,800	1,620	1,440	1,260	mA
Auto refresh current	tRFC = tRFC (MIN)	IDD5[2]	6,210	5,220	5,220	5,040	mA
	tRFC = 7.8125µs	IDD5A[2]	198	180	180	180	mA
Self refresh current: CKE ≤ 0.2V		IDD6[2]	90	90	90	90	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; tRC = tRC (MIN); tCK = tCK (MIN); Address and control inputs change only during active READ or WRITE commands		IDD7[1]	4,095	3,690	3,645	3,195	mA

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Register and PLL Specifications

Table 12: Register Specifications
SSTV16859 devices or equivalent JESD82-4B

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	SSTL_25	$V_{REF(DC)}$ + 150	–	mV
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	SSTL_25	–	$V_{REF(DC)}$ - 150	mV
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	SSTL_25	$V_{REF(DC)}$ + 310	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	SSTL_25	–	$V_{REF(DC)}$ - 310	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	V_{DD} - 0.2	–	V
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.2	V
Input current	I_I	All pins	V_I = V_{DDQ} or V_{SSQ}	–5.0	+5.0	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I_O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	–	Varies by manufacturer	mA
Dynamic operating (clock tree)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	V_I = V_{REF} ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_I	RESET#	V_I = V_{DDQ} or V_{SSQ}	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR SDRAM RDIMM devices. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.

Table 13: PLL Specifications
CVF857 device or equivalent JESD82-1A

Parameter	Symbol	Min	Max	Units
DC high-level input voltage	V_{IH}	1.7	$V_{DD}Q$ + 0.3	V
DC low-level input voltage	V_{IL}	–0.3	0.7	V
Input voltage (limits)	V_{IN}	–0.3	$V_{DD}Q$ + 0.3	V
Input differential-pair cross voltage	V_{IX}	($V_{DD}Q$/2) - 0.2	($V_{DD}Q$/2) + 0.2	V
Input differential voltage	$V_{ID(DC)}$	0.36	$V_{DD}Q$ + 0.6	V
Input differential voltage	$V_{ID(AC)}$	0.70	$V_{DD}Q$ + 0.6	V
Input current	I_I	–10	+10	µA
Dynamic supply current	I_{DDPD}	–	200	µA
Dynamic supply current	I_{DDQ}	–	300	µA
Dynamic supply current	I_{ADD}	–	12	mA
Input capacitance	C_{IN}	2.0	3.5	pF

Table 14: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^{t}L	–	100	µs
Input clock slew rate	$^{t}slr(i)$	1.0	4.0	V/ns
SSC modulation frequency	–	30	50	kHz
SSC clock input frequency deviation	–	0	–0.50	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82-1A.

Serial Presence-Detect

Table 15: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–1.0	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 kHz	I_{CC}	–	2.0	mA

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	$^{t}HD:DAT$	200	–	ns	
SDA fall time	^{t}F	–	300	ns	2
SDA rise time	^{t}R	–	300	ns	2
Data-in hold time	$^{t}HD:DI$	0	–	µs	
Start condition hold time	$^{t}HD:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	5	ms	4

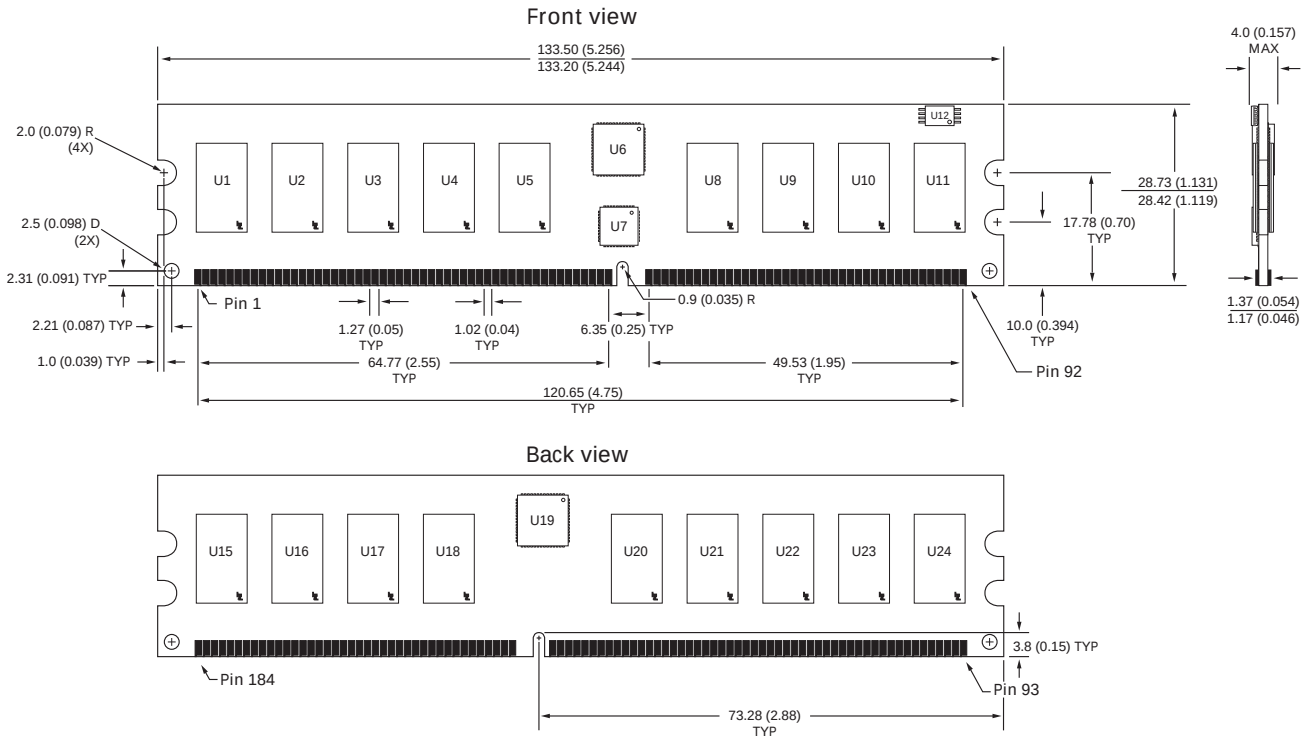
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

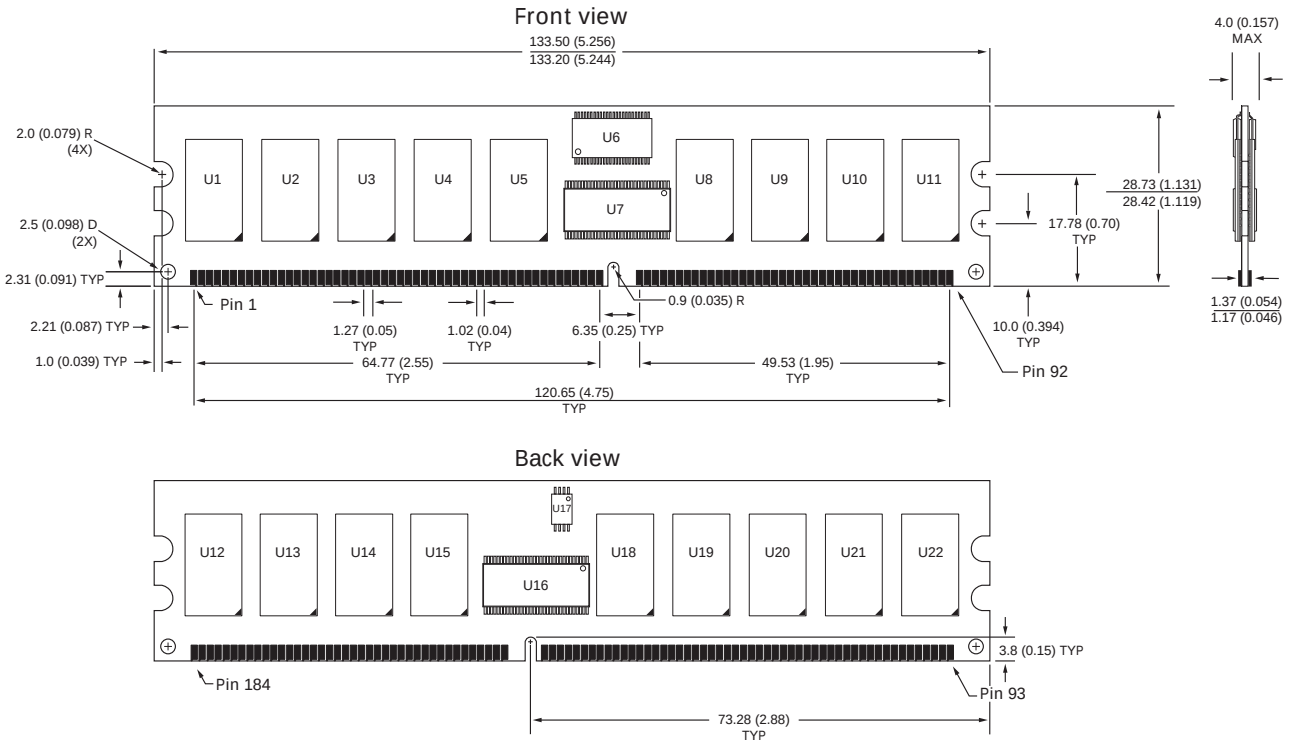
Module Dimensions

Figure 5: 184-Pin DDR RDIMM (-40B)



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

Figure 6: 184-Pin DDR RDIMM (-335, -262, -26A, -265)



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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