ASYMMETRICAL BIDIRECTIONAL THYRISTOR SPD

TISP4A265H3BJ LCAS R_{LINE} Protector

RING Line Protection for:
-LCAS (Line Card Access Switch)
-ADSL Interfaces

Voltages Optimized for:
-Battery-Backed Ringing Circuits
Maximum Ringing a.c. ..... 90 V rms
Maximum Battery Voltage ..... -52 V
-ADSL Voltage ..... ±23 V peak
-Minimum Ambient Temperature ..... 0 °C

Device	V_{DRM} V	$V_{(BO)}$ V
'4A265	+100	+125
	-200	-265

Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	300
10/160 µs	TIA/EIA-IS-968	250
10/700 µs	ITU-T K.20/45/21	200
10/560 µs	TIA/EIA-IS-968	160
10/1000 µs	GR-1089-CORE	100

SMB Package (Top View)

MD4A265

Device Symbol

SD4XAN

..... **UL Recognized Component**

Description

The TISP4A265H3BJ is an asymmetrical bidirectional overvoltage protector. It is designed to limit the peak voltages on the ring line terminal of the '7581/2/3 LCAS (Line Card Access Switches). The TISP4A265H3BJ must be connected with bar-indexed terminal 1, MT1, to the protective ground and terminal 2, MT2, to the ring conductor.

The TISP4A265H3BJ voltages are chosen to give adequate LCAS ring line terminal protection for all switch conditions. The most potentially stressful condition is low level power cross when the LCAS switches are closed. Under this condition, the TISP4A265H3BJ limits the voltage and corresponding LCAS dissipation until the LCAS thermal trip operates and opens the switches.

Under open-circuit ringing conditions, the line ring conductor will have high peak voltages. For battery backed ringing, the ring conductor will have a larger peak negative voltage than positive, i.e. the peak voltages are asymmetric. The TISP4A265H3BJ has a similar voltage asymmetry and will allow the maximum possible ringing voltage, while giving the most effective protection. On a connected line, the tip conductor will have much smaller voltage levels than the open-circuit ring conductor values. Here a TISP4xxxH3BJ series, symmetrical voltage protector gives adequate protection.

Overvoltages are initially clipped by breakdown clamping. If sufficient current is available from the overvoltage, the breakdown voltage will rise to the breakover level, which causes the device to switch into a low-voltage on-state condition. This switching action removes the high voltage stress from the following circuitry and causes the current resulting from the overvoltage to be safely diverted through the protector. The high holding (switch off) current prevents d.c. latchup as the diverted current subsides.

How to Order

Device	Package	Carrier	Order As
TISP4A265H3BJ	BJ (J-Bend DO-214AA/SMB)	R (Embossed Tape Reeled)	TISP4A265H3BJR-S

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
JANUARY 2002 - REVISED MAY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Description (Continued)

The TISP4A265H3BJ is guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. This high (H) current protection device is in a plastic SMBJ package (JEDEC DO-214AA with J-bend leads) and supplied in embossed carrier reel pack. For alternative voltage and holding current values, consult the factory.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	V_{DRM}	+100 -200	V
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)	I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)		500	
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 current combination wave generator)		300	
10/160 µs (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/160 µs voltage wave shape)		250	
5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/45/21)		200	
5/320 µs (TIA/EIA-IS-968 (Replaces FCC Part 68), 9/720 µs voltage wave shape)		200	
10/560 µs (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/560 µs voltage wave shape)		160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)		100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)	I_{TSM}		A
20 ms (50 Hz) full sine wave		55	
16.7 ms (60 Hz) full sine wave		60	
1000 s 50 Hz/60 Hz a.c.		2.2	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A	di_T/dt	400	A/µs
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. See Figure 7 for voltage values at other temperatures.
2. Initially, the TISP4A265H3BJ must be in thermal equilibrium with T_J = 25 °C.
3. The surge may be repeated after the TISP4A265H3BJ returns to its initial conditions.
4. See Figure 8 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 6 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

Overload Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Maximum overload on-state current without open circuit, 50 Hz/60 Hz a.c. (see Note 6)	$I_{T(OV)M}$		A rms
0.03 s		60	
0.07 s		40	
1.6 s		8	
5.0 s		7	
1000 s		2.2	

NOTE 6: Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A265H3BJ silicon chip. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short circuit fault mode. In the short circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open circuit fault mode developed.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = +100 V and -200 V	T_A = 25 °C			±5	µA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				+125 -265	V
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	µA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, (see Note 7)	V_D = 98 V		25	30	pF
			V_D = 50 V		30	36	
			V_D = 10 V		45	54	
			V_D = 5 V		52	62	
			V_D = 2 V		60	72	
			V_D = 1 V		65	79	
			V_D = 0		71	86	
			V_D = -1 V		65	79	
			V_D = -2 V		58	69	
			V_D = -5 V		48	57	
			V_D = -10 V		40	48	
			V_D = -50 V		26	31	
			V_D = -100 V		20	24	

NOTE 7: To avoid possible voltage clipping, the TISP4A265H3BJ is tested with V_D = +98 V in the positive polarity.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\Theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C, (see Note 8)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C		50		

NOTE 8: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

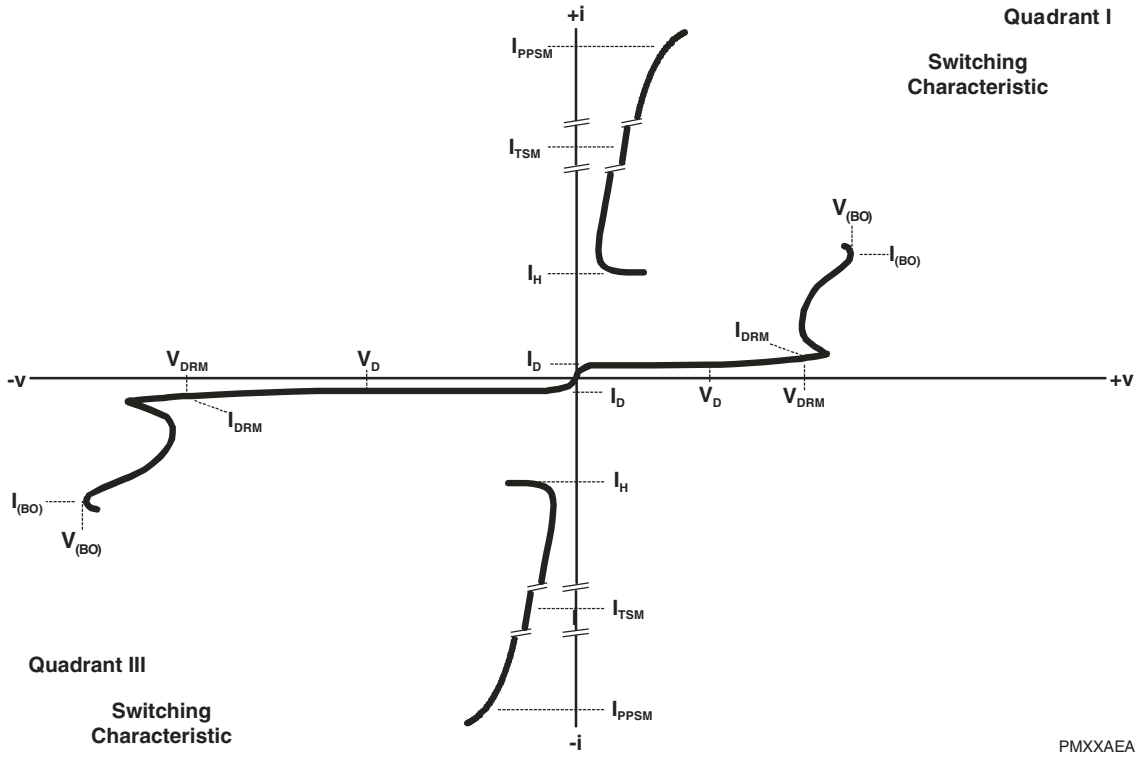


Figure 1. Voltage-Current Characteristic for MT1 and MT2 Terminals
All Measurements are Referenced to the MT1 Terminal

Typical Characteristics

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

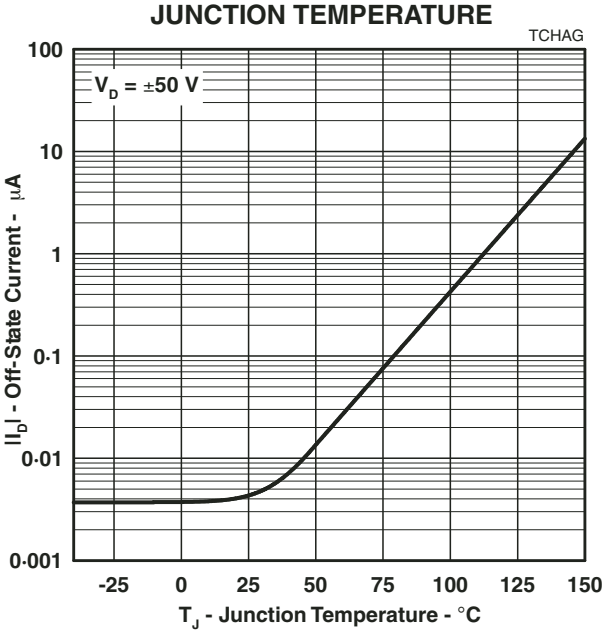


Figure 2.

NORMALIZED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

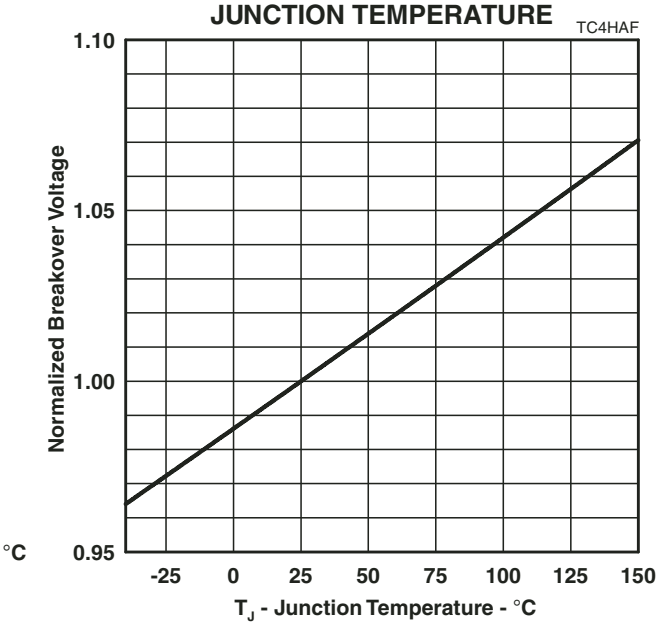


Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

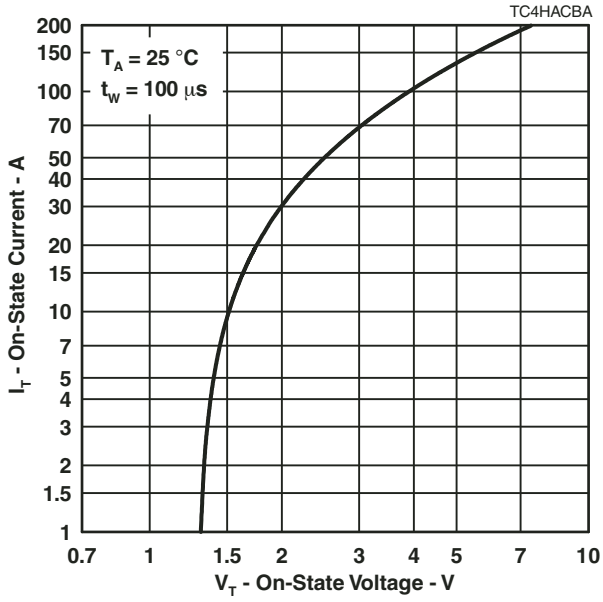


Figure 4.

NORMALIZED HOLDING CURRENT vs JUNCTION TEMPERATURE

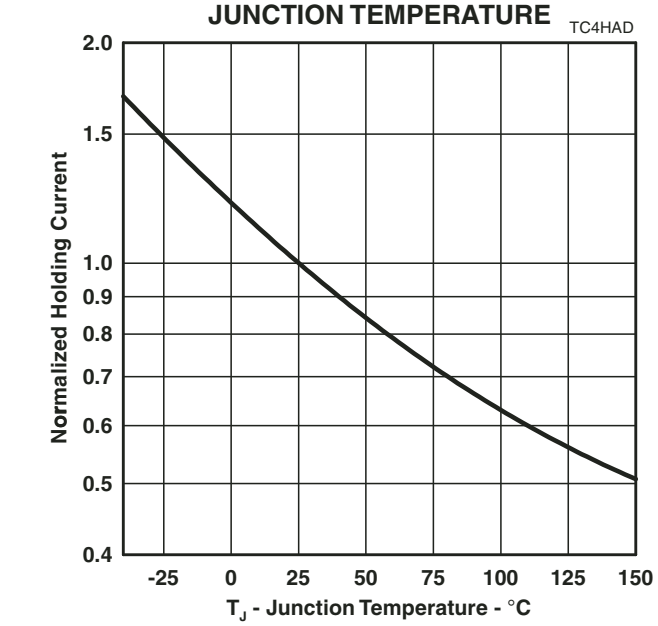


Figure 5.

Rating and Thermal Information

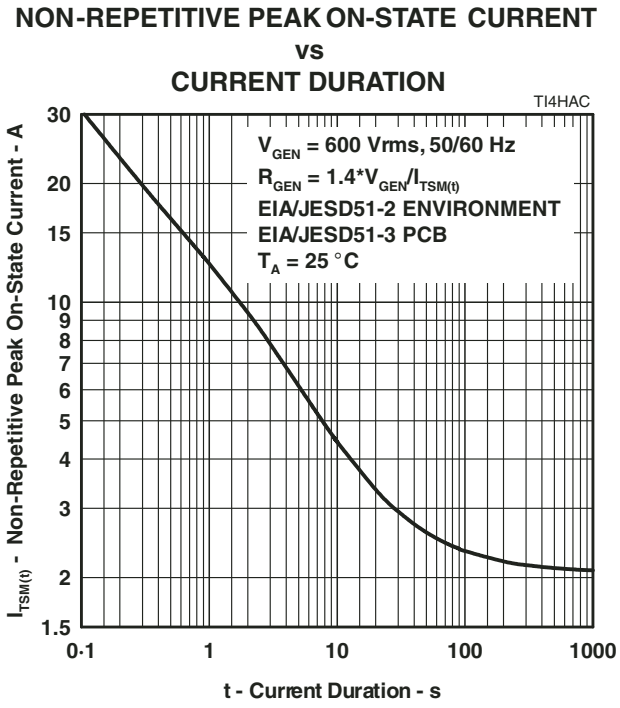


Figure 6.

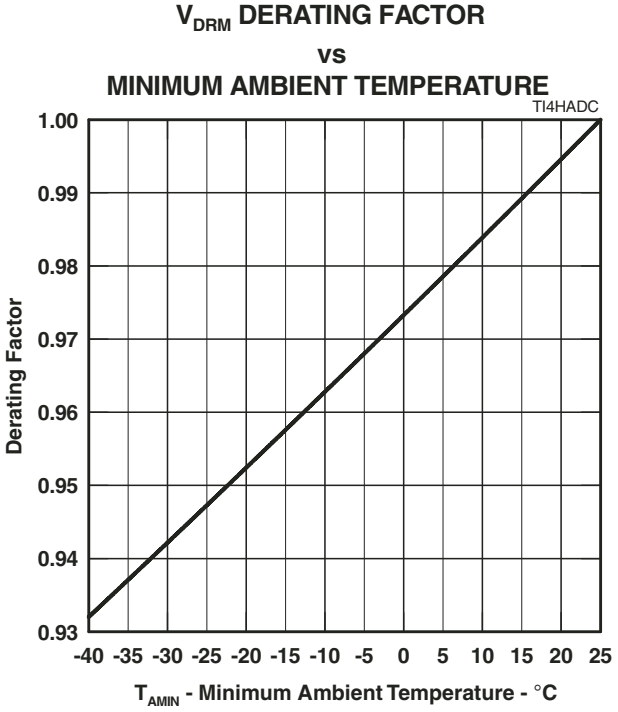


Figure 7.

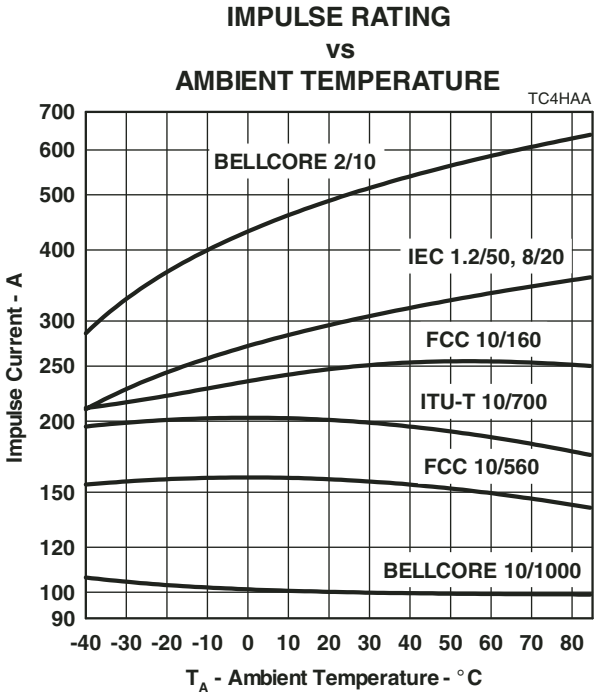


Figure 8.

Typical Circuits

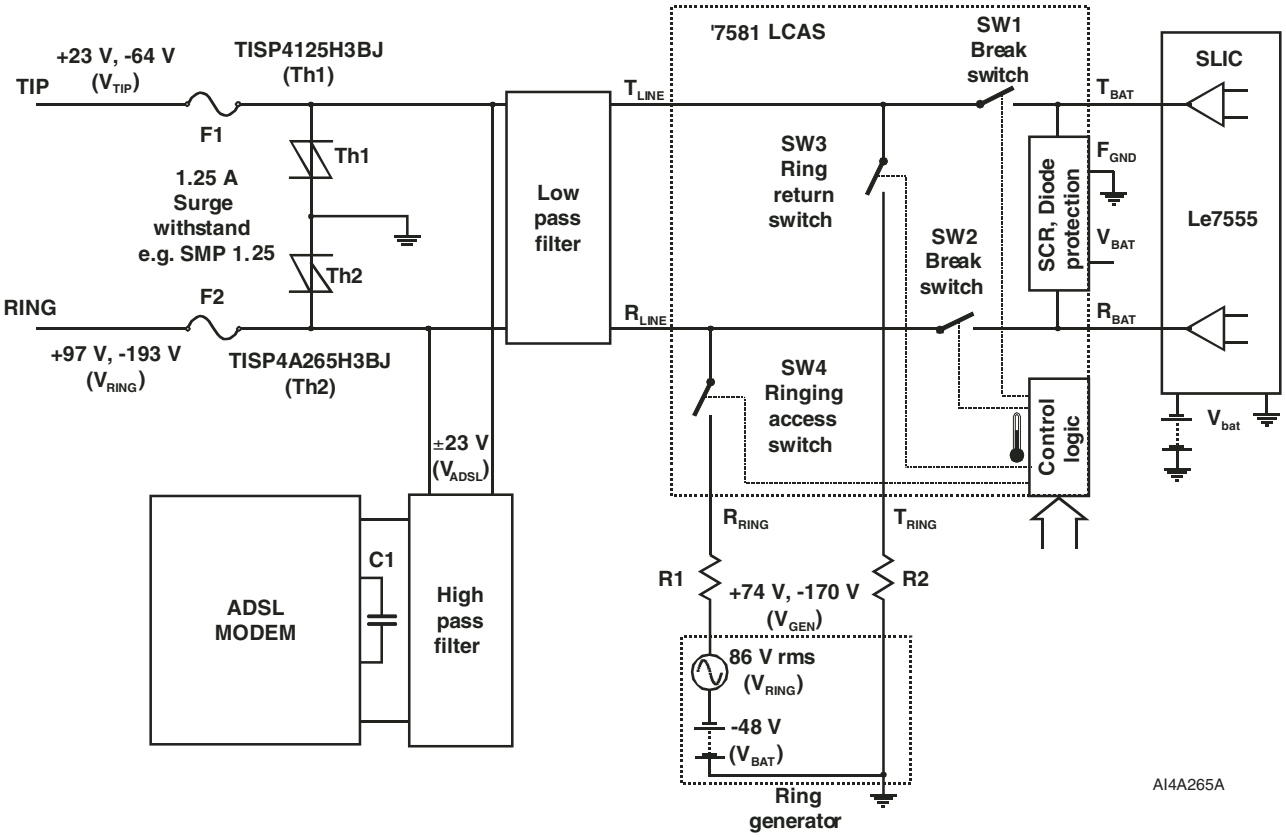
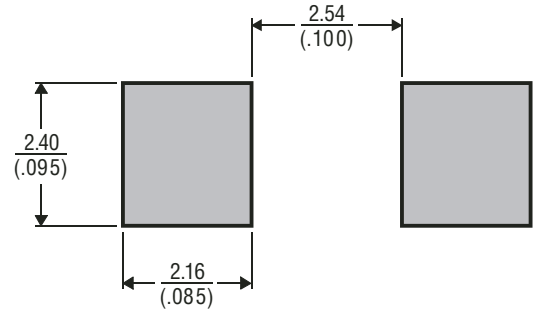


Figure 9. Integrated Voice Data (IVD) System with Typical Operating Voltage Levels Indicated

MECHANICAL DATA

Recommended Printed Wiring Land Pattern Dimensions

SMB Land Pattern



DIMENSIONS ARE: MILLIMETERS / (INCHES)

MDXX BID

Device Symbolization Code

Devices will be coded as below. Terminal 1 is indicated by an adjacent bar marked on the package body.

Device	Symbolization Code
TISP4A265H3BJ	4A265H

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

Package	Carrier	Standard Quantity
SMB	Embossed Tape Reel Pack	3000

JANUARY 2002 - REVISED MAY 2007