

## 16K/32K x 9 Deep Sync FIFOs

### Features

- High speed, low power, first-in first-out (FIFO) memories
- 16K x 9 (CY7C4261)
- 32K x 9 (CY7C4271)
- 0.5 micron CMOS for optimum speed and power
- High speed 100 MHz operation (10 ns read/write cycle times)
- Low power —  $I_{CC} = 35$  mA
- Fully asynchronous and simultaneous read and write operation
- Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags
- TTL compatible
- Output Enable ( $\overline{OE}$ ) pins
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- Supports free running 50% duty cycle clock inputs
- Width Expansion Capability
- Military temp SMD Offering – CY7C4271-15LMB
- 32-pin PLCC/LCC and 32-pin TQFP
- Pin compatible density upgrade to CY7C42X1 family
- Pin compatible density upgrade to IDT72201/11/21/31/41/51
- Pb-Free Packages Available

### Selection Guide

Parameter		7C4261/71-10	7C4261/71-15	7C4261/71-25	7C4261/71-35	Unit
Maximum Frequency		100	66.7	40	28.6	MHz
Maximum Access Time		8	10	15	20	ns
Minimum Cycle Time		10	15	25	35	ns
Minimum Data or Enable Setup		3	4	6	7	ns
Minimum Data or Enable Hold		0.5	1	1	2	ns
Maximum Flag Delay		8	10	15	20	ns
Active Power Supply Current ( $I_{CC1}$ )	Commercial	35	35	35	35	mA
	Industrial/Military	40	40	40	40	

Parameter	CY7C4261	CY7C4271
Density	16K x 9	32K x 9
Package	32-pin PLCC, TQFP	32-pin LCC, PLCC, TQFP

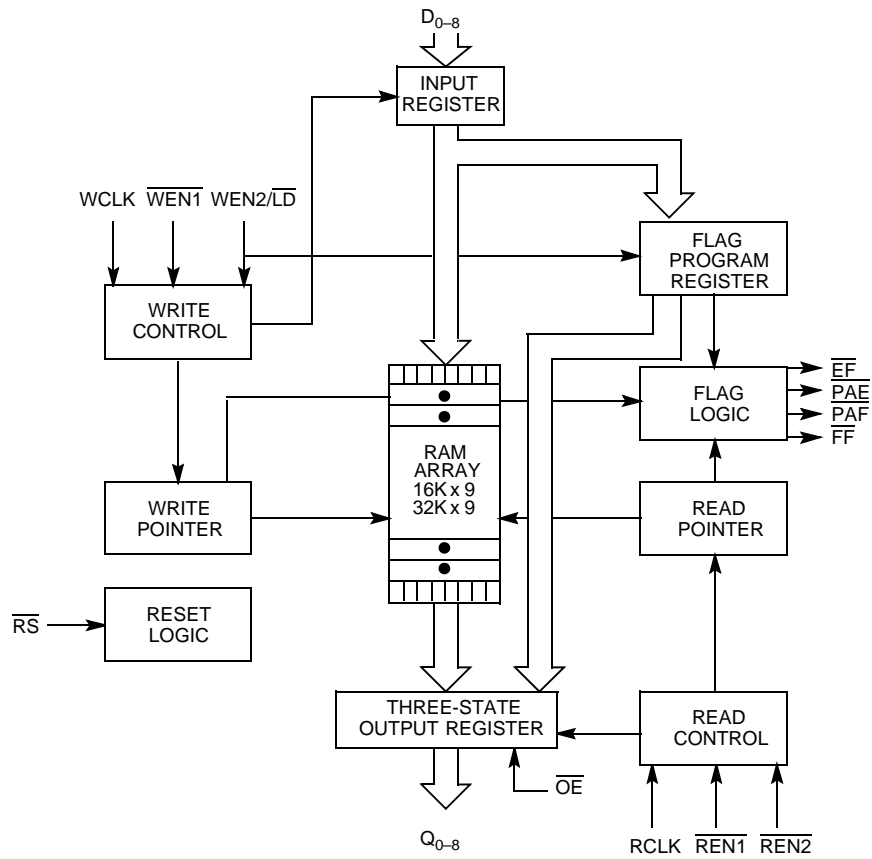
### Functional Description

The CY7C4261/71 are high speed, low power FIFO memories with clocked read and write interfaces. All are nine bits wide. The CY7C4261/71 are pin compatible to the CY7C42X1 Synchronous FIFO family. The CY7C4261/71 can be cascaded to increase FIFO width. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ( $\overline{WEN1}$ ,  $\overline{WEN2/LD}$ ).

When  $\overline{WEN1}$  is LOW and  $\overline{WEN2/LD}$  is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While  $\overline{WEN1}$ ,  $\overline{WEN2/LD}$  is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free running read clock (RCLK) and two read enable pins ( $\overline{REN1}$ ,  $\overline{REN2}$ ). In addition, the CY7C4261/71 has an output enable pin ( $\overline{OE}$ ). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable. Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 32-Pin PLCC/LCC (Top View)

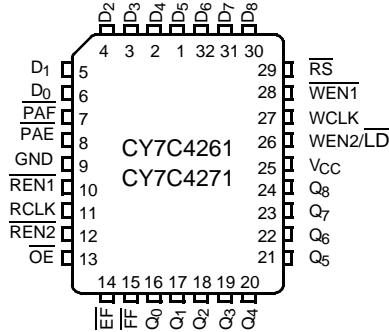


Figure 2. Pin Diagram - 32-Pin TQFP (Top View)

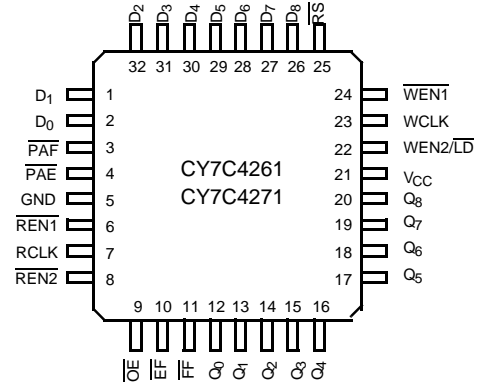


Table 1. Pin Definitions - 32-Pin Device

Signal Name	Description	IO	Description
D <sub>0-8</sub>	Data Inputs	I	Data Inputs for 9-bit bus.
Q <sub>0-8</sub>	Data Outputs	O	Data Outputs for 9-bit bus.
WEN1	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when WEN1 is asserted and FF is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when WEN1 is LOW and WEN2/LD and FF are HIGH.
WEN2/LD Dual Mode Pin	Write Enable 2 Load	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data is not written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
REN1, REN2	Read Enable Inputs	I	Enables the device for Read operation. Both REN1 and REN2 must be asserted to allow a read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when WEN1 is LOW and WEN2/LD is HIGH and the FIFO is not Full. When LD is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when REN1 and REN2 are LOW and the FIFO is not Empty. When WEN2/LD is LOW, RCLK reads data out of the programmable flag-offset register.
EF	Empty Flag	O	When EF is LOW, the FIFO is empty. EF is synchronized to RCLK.
FF	Full Flag	O	When FF is LOW, the FIFO is full. FF is synchronized to WCLK.
PAE	Programmable Almost Empty	O	When PAE is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. PAE is synchronized to RCLK.
PAF	Programmable Almost Full	O	When PAF is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. PAF is synchronized to WCLK.
RS	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power up.
OE	Output Enable	I	When OE is LOW, the FIFO's data outputs drive the bus to which they are connected. If OE is HIGH, the FIFO's outputs are in High Z (high impedance) state.

## Functional Description

The CY7C4261/71 provides four status pins: Empty, Full, Programmable Almost Empty, and Programmable Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty + 7 and Full – 7.

The flags are synchronous, that is, they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle.

All configurations are fabricated using an advanced 0.5µ CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

## Architecture

The CY7C4261/71 consists of an array of 16K to 32K words of nine bits each (implemented by a dual port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN1, REN2, WEN1, WEN2, RS), and flags (EF, PAE, PAF, FF).

## Resetting the FIFO

Upon power up, the FIFO must be reset with a Reset ( $\overline{RS}$ ) cycle. This causes the FIFO to enter the Empty condition signified by EF being LOW. All data outputs ( $Q_{0-8}$ ) go LOW  $t_{RSF}$  after the rising edge of RS. For the FIFO to reset to its default state, a falling edge must occur on  $\overline{RS}$  and the user must not read or write while RS is LOW. All flags are guaranteed to be valid  $t_{RSF}$  after RS is taken LOW.

## FIFO Operation

When the  $\overline{WEN1}$  signal is active LOW, WEN2 is active HIGH, and FF is active HIGH, data present on the  $D_{0-8}$  pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the REN1 and REN2 signals are active LOW and EF is active HIGH, data in the FIFO memory is presented on the  $Q_{0-8}$  outputs. New data is presented on each rising edge of RCLK while REN1 and REN2 are active. REN1 and REN2 must set up  $t_{ENS}$  before RCLK for it to be a valid read function. WEN1 and WEN2 must occur  $t_{ENS}$  before WCLK for it to be a valid write function.

An output enable ( $\overline{OE}$ ) pin is provided to three-state the  $Q_{0-8}$  outputs when OE is asserted. When OE is enabled (LOW), data in the output register is available to the  $Q_{0-8}$  outputs after  $t_{OE}$ . If devices are cascaded, the OE function only outputs data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its  $Q_{0-8}$  outputs even after additional reads occur.

**Write Enable 1 ( $\overline{WEN1}$ ).** If the FIFO is configured for programmable flags, Write Enable 1 ( $\overline{WEN1}$ ) is the only write enable control pin. In this configuration, when Write Enable 1 ( $\overline{WEN1}$ ) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

**Write Enable 2/Load ( $\overline{WEN2/LD}$ ).** This is a dual purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load ( $\overline{WEN2/LD}$ ) is set active HIGH at Reset ( $RS = LOW$ ), this pin operates as a second write enable pin.

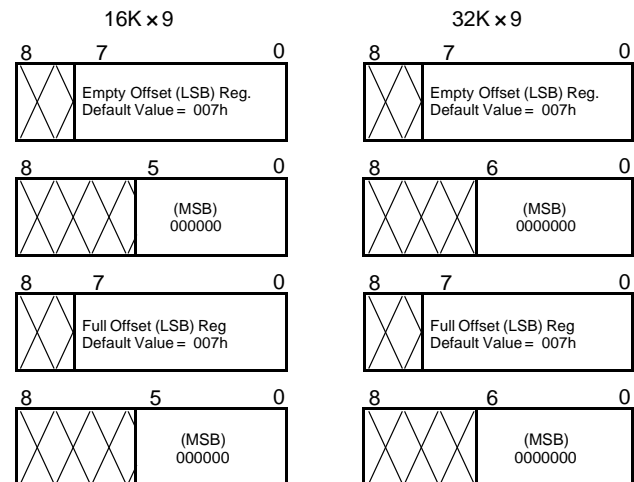
If the FIFO is configured to have two write enables, when Write Enable ( $\overline{WEN1}$ ) is LOW and Write Enable 2/Load ( $\overline{WEN2/LD}$ ) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

## Programming

When  $\overline{WEN2/LD}$  is held LOW during Reset, this pin is the load ( $\overline{LD}$ ) enable for flag offset programming. In this configuration,  $\overline{WEN2/LD}$  can be used to access the four 8-bit offset registers contained in the CY7C4261/71 for writing or reading data to these registers.

When the device is configured for programmable flags and both  $\overline{WEN2/LD}$  and  $\overline{WEN1}$  are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when  $\overline{WEN2/LD}$  and  $\overline{WEN1}$  are LOW. The fifth LOW-to-HIGH transition of WCLK while  $\overline{WEN2/LD}$  and  $\overline{WEN1}$  are LOW writes data to the empty LSB register again. Figure 3 shows the register sizes and default values for the various device types.

Figure 3. Offset Register Location and Default Values



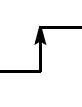



It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written, and then by bringing the WEN2/LD input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/LD is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/LD is LOW and both REN1 and REN2 are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads must not be performed simultaneously on the offset registers.

**Programmable Flag (PAE, PAF) Operation**

Whether the flag offset registers are programmed as described in Table 2 or the default values are used, the programmable almost-empty flag (PAE) (PAF) states are determined by their corresponding offset registers and the difference between the read and write pointers.

**Table 2. Writing the Offset Registers**

LD	WEN	WCLK <sup>[1]</sup>	Selection
0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as *n* and determines the operation of PAE. PAF is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains *n* or fewer unread words. PAE is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (*n*+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of PAF. PAE is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4261 (16K-*m*) and CY7C4271 (32K-*m*). PAF is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than *m*.

**Table 3. Status Flags**

Number of Words in FIFO		FF	PAF	PAE	EF
CY7C4261	CY7C4271				
0	0	H	H	L	L
1 to <i>n</i> <sup>[2]</sup>	1 to <i>n</i> <sup>[2]</sup>	H	H	L	H
( <i>n</i> + 1) to (16384 - ( <i>m</i> + 1))	( <i>n</i> + 1) to (32768 - ( <i>m</i> + 1))	H	H	H	H
(16384 - <i>m</i> ) <sup>[3]</sup> to 16383	(32768 - <i>m</i> ) <sup>[3]</sup> to 32767	H	L	H	H
16384	32768	L	L	H	H

**Width Expansion Configuration**

Word width may be increased by simply connecting the corresponding input controls signals of multiple devices. A composite flag must be created for each of the end-point status flags (EF and FF). The partial status flags (PAE and PAF) can be detected from any one device. Figure 4 on page 6 demonstrates a 18-bit word width by using two CY7C4261/71s. Any word width can be attained by adding additional CY7C4261/71s.

When the CY7C4261/71 is in a Width Expansion Configuration, the Read Enable (REN2) control input can be grounded (see Figure 4 on page 6). In this configuration, the Write Enable 2/Load (WEN2/LD) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

**Flag Operation**

The CY7C4261/71 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, PAE, and PAF are synchronous.

**Full Flag**

The Full Flag (FF) goes LOW when the device is full. Write operations are inhibited whenever FF is LOW regardless of the state of WEN1 and WEN2/LD. FF is synchronized to WCLK, that is, it is exclusively updated by each rising edge of WCLK.

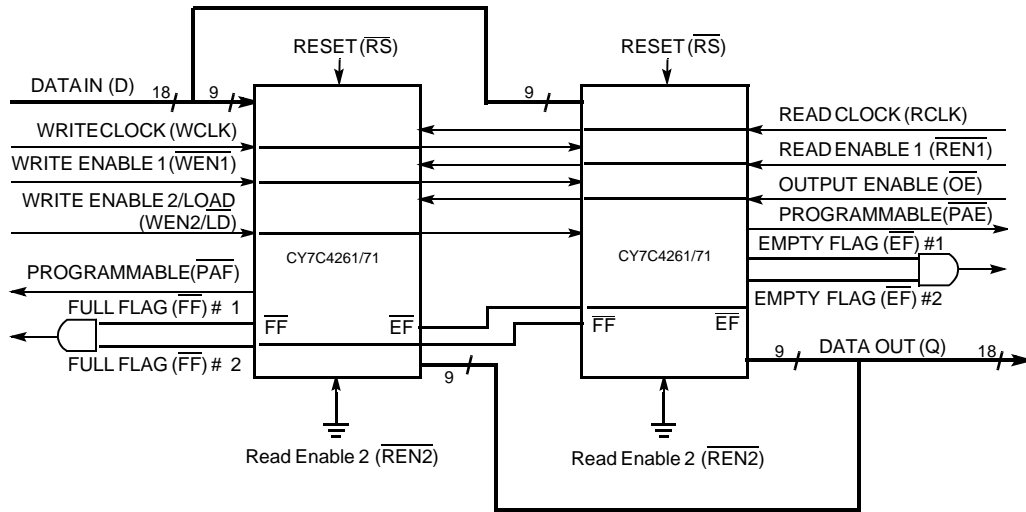
**Empty Flag**

The Empty Flag (EF) goes LOW when the device is empty. Read operations are inhibited whenever EF is LOW, regardless of the state of REN1 and REN2. EF is synchronized to RCLK, that is, it is exclusively updated by each rising edge of RCLK.

**Notes**

1. The same selection sequence applies to reading from the registers. REN1 and REN2 are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
2. *n* = Empty Offset (*n* = 7 default value).
3. *m* = Full Offset (*m* = 7 default value).

Figure 4. Block Diagram of 16K x 18/32K x 18 Deep Sync FIFO Memory Used in a Width Expansion Configuration



**Maximum Ratings**

Exceeding maximum ratings<sup>[4]</sup> may impair the useful life of the device. These user guidelines are not tested.

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High-Z State ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage ..... -0.5V to V<sub>CC</sub> + 0.5V
- Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial <sup>[5]</sup>	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

**Electrical Characteristics**

Over the Operating Range <sup>[6]</sup>

Parameter	Description	Test Conditions	7C4261/71-10		7C4261/71-15		7C4261/71-25		7C4261/71-35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -2.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage (Commercial/Industrial)		2.0	V <sub>CC</sub>	2.0	V <sub>CC</sub>	2.0	V <sub>CC</sub>	2.0	V <sub>CC</sub>	V
V <sub>IH</sub>	Input HIGH Voltage (Military)		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	V <sub>CC</sub> = Max.	-10	+10	-10	+10	-10	+10	-10	+10	µA
I <sub>OZL</sub> I <sub>OZH</sub>	Output OFF, High Z Current	OE ≥ V <sub>IH</sub> , V <sub>SS</sub> < V <sub>O</sub> < V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	-10	+10	µA
I <sub>CC1</sub> <sup>[7]</sup>	Active Power Supply Current	Com'l		35		35		35		35	mA
		Ind/Mil		40		40		40		40	mA
I <sub>SB</sub> <sup>[8]</sup>	Average Standby Current	Com'l		10		10		10		10	mA
		Ind/Mil		15		15		15		15	mA

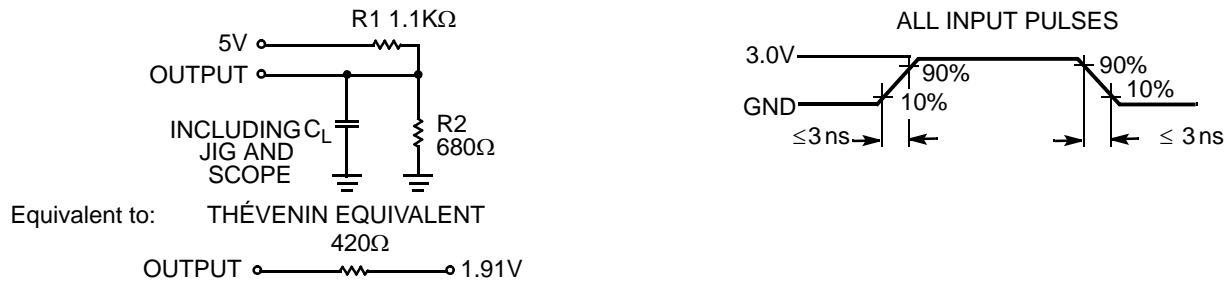
**Capacitance**

Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	5	pF
C <sub>OUT</sub>	Output Capacitance		7	pF

**Notes**

4. The voltage on any input or IO pin cannot exceed the power pin during power up.
5. T<sub>A</sub> is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.
7. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded. I<sub>CC1</sub>(typical) = (20 mA + (freq - 20 MHz) \* (0.7 mA/MHz)).
8. All inputs = V<sub>CC</sub> - 0.2V, except WCLK and RCLK (which are switching at frequency = 20 MHz). All outputs are unloaded.
9. Tested initially and after any design or process changes that may affect these parameters.



**Figure 5. AC Test Loads and Waveforms** <sup>[10, 11]</sup>


## Switching Characteristics

Over the Operating Range

Parameter	Description	7C4261/71-10		7C4261/71-15		7C4261/71-25		7C4261/71-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_S$	Clock Cycle Frequency		100		66.7		40		28.6	MHz
$t_A$	Data Access Time	2	8	2	10	2	15	2	20	ns
$t_{CLK}$	Clock Cycle Time	10		15		25		35		ns
$t_{CLKH}$	Clock HIGH Time	4.5		6		10		14		ns
$t_{CLKL}$	Clock LOW Time	4.5		6		10		14		ns
$t_{DS}$	Data Setup Time	3		4		6		7		ns
$t_{DH}$	Data Hold Time	0.5		1		1		2		ns
$t_{ENS}$	Enable Setup Time	3		4		6		7		ns
$t_{ENH}$	Enable Hold Time	0.5		1		1		2		ns
$t_{RS}$	Reset Pulse Width <sup>[12]</sup>	10		15		25		35		ns
$t_{RSS}$	Reset Setup Time	8		10		15		20		ns
$t_{RSR}$	Reset Recovery Time	8		10		15		20		ns
$t_{RSF}$	Reset to Flag and Output Time		10		15		25		35	ns
$t_{OLZ}$	Output Enable to Output in Low Z <sup>[13]</sup>	0		0		0		0		ns
$t_{OE}$	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
$t_{OHZ}$	Output Enable to Output in High Z <sup>[13]</sup>	3	7	3	8	3	12	3	15	ns
$t_{WFF}$	Write Clock to Full Flag		8		10		15		20	ns
$t_{REF}$	Read Clock to Empty Flag		8		10		15		20	ns
$t_{PAF}$	Clock to Programmable Almost Full Flag		8		10		15		20	ns
$t_{PAE}$	Clock to Programmable Almost Full Flag		8		10		15		20	ns
$t_{SKEW1}$	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		12		ns
$t_{SKEW2}$	Skew Time between Read Clock and Write Clock for Almost Empty Flag and Almost Full Flag	10		15		18		20		ns

### Notes

10.  $5C_L = 30$  pF for all AC parameters except for  $t_{OHZ}$ .
11.  $5C_L = 5$  pF for  $t_{OHZ}$ .
12. Pulse widths less than minimum values are not allowed.
13. Values guaranteed by design, not currently tested.



Switching Waveforms

Figure 6. Write Cycle Timing

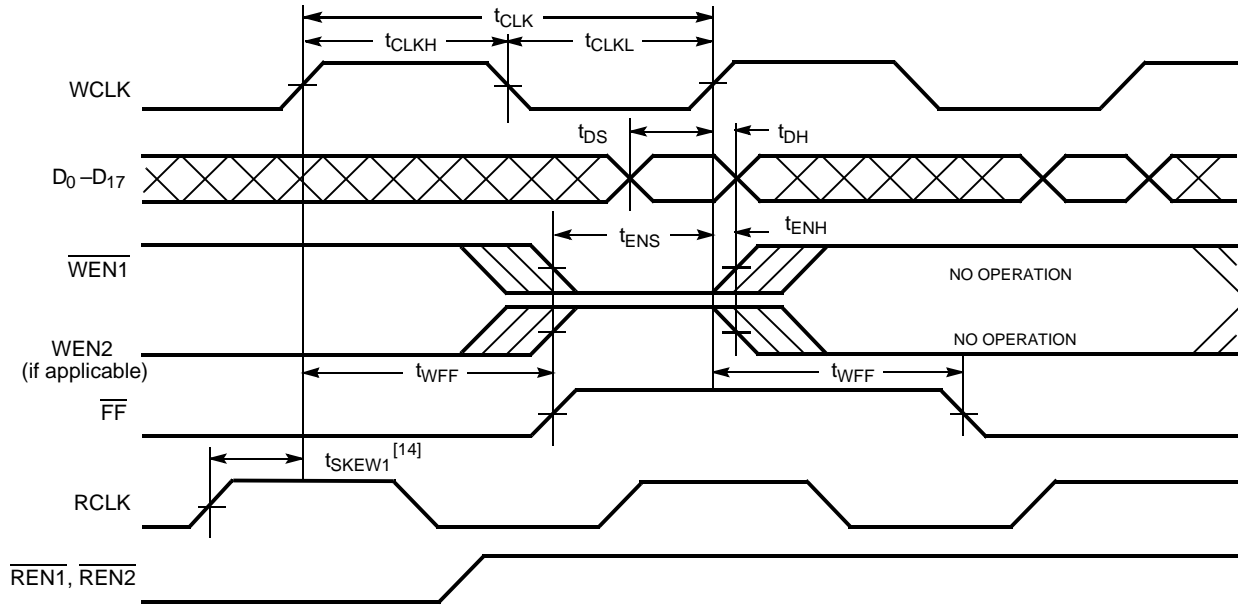
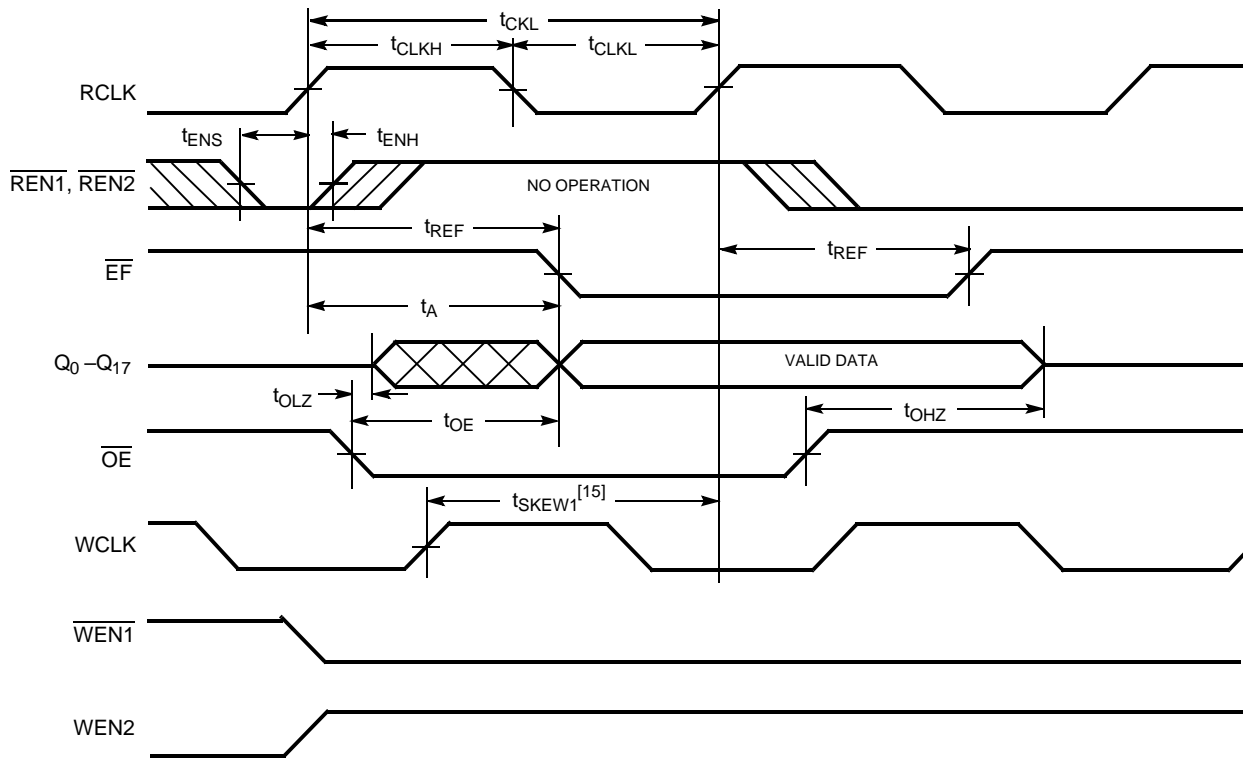


Figure 7. Read Cycle Timing



Notes

- 14.  $t_{SKEW1}$  is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that  $\overline{FF}$  goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $t_{SKEW1}$ , then  $\overline{FF}$  may not change state until the next WCLK rising edge.
- 15.  $t_{SKEW1}$  is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  goes HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than  $t_{SKEW2}$ , then  $\overline{EF}$  may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Figure 8. Reset Timing [16]

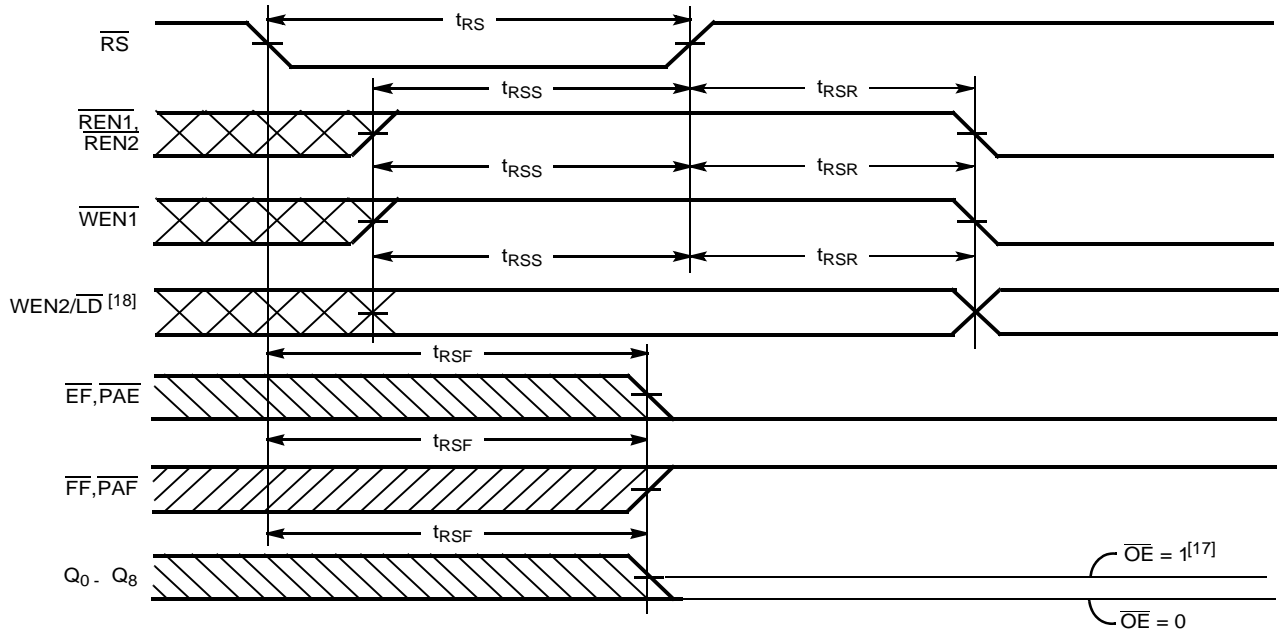
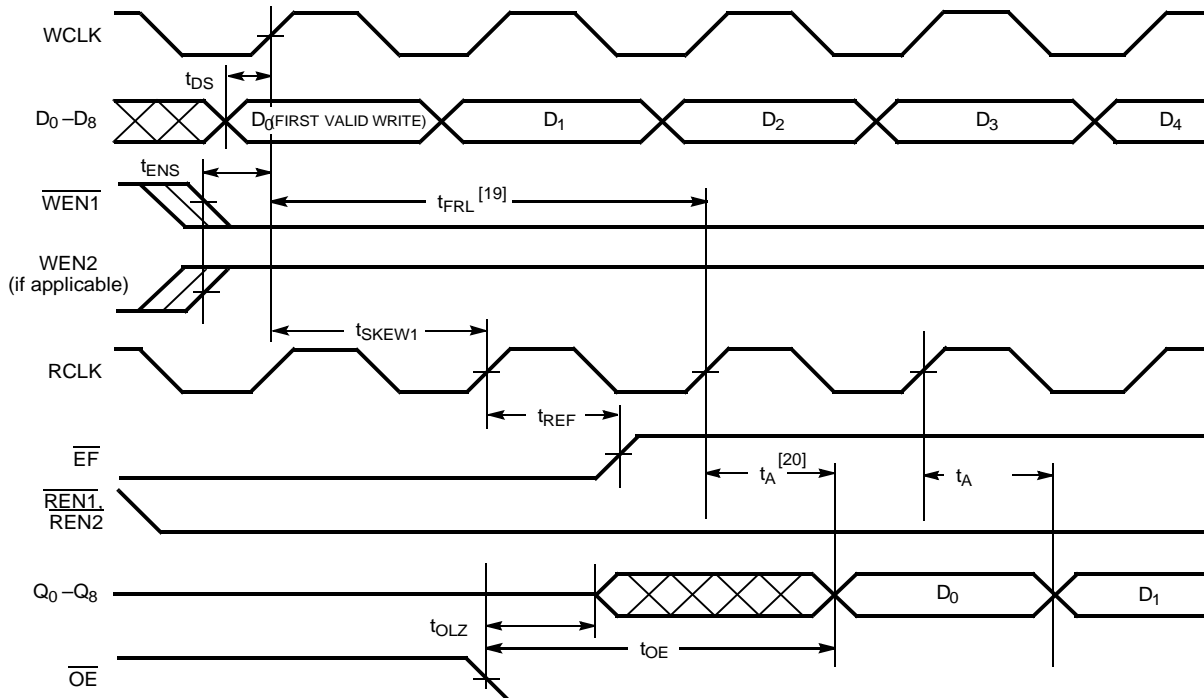


Figure 9. First Data Word Latency after Reset with Read and Write



Notes

- 16. The clocks (RCLK, WCLK) can be free running during reset.
- 17. After reset, the outputs are LOW if OE = 0 and three-state if OE = 1.
- 18. Holding WEN2/LD HIGH during reset makes the pin act as a second enable pin. Holding WEN2/LD LOW during reset makes the pin act as a load enable for the programmable flag offset registers.
- 19. When  $t_{SKEW1} \geq$  minimum specification,  $t_{FRL}$  (maximum) =  $t_{CLK} + t_{SKEW2}$ . When  $t_{SKEW1} <$  minimum specification,  $t_{FRL}$  (maximum) = either  $2 * t_{CLK} + t_{SKEW1}$  or  $t_{CLK} + t_{SKEW1}$ . The Latency Timing applies only at the Empty Boundary (EF = LOW).
- 20. The first word is available the cycle after EF goes HIGH, always.

Switching Waveforms (continued)

Figure 10. Empty Flag Timing

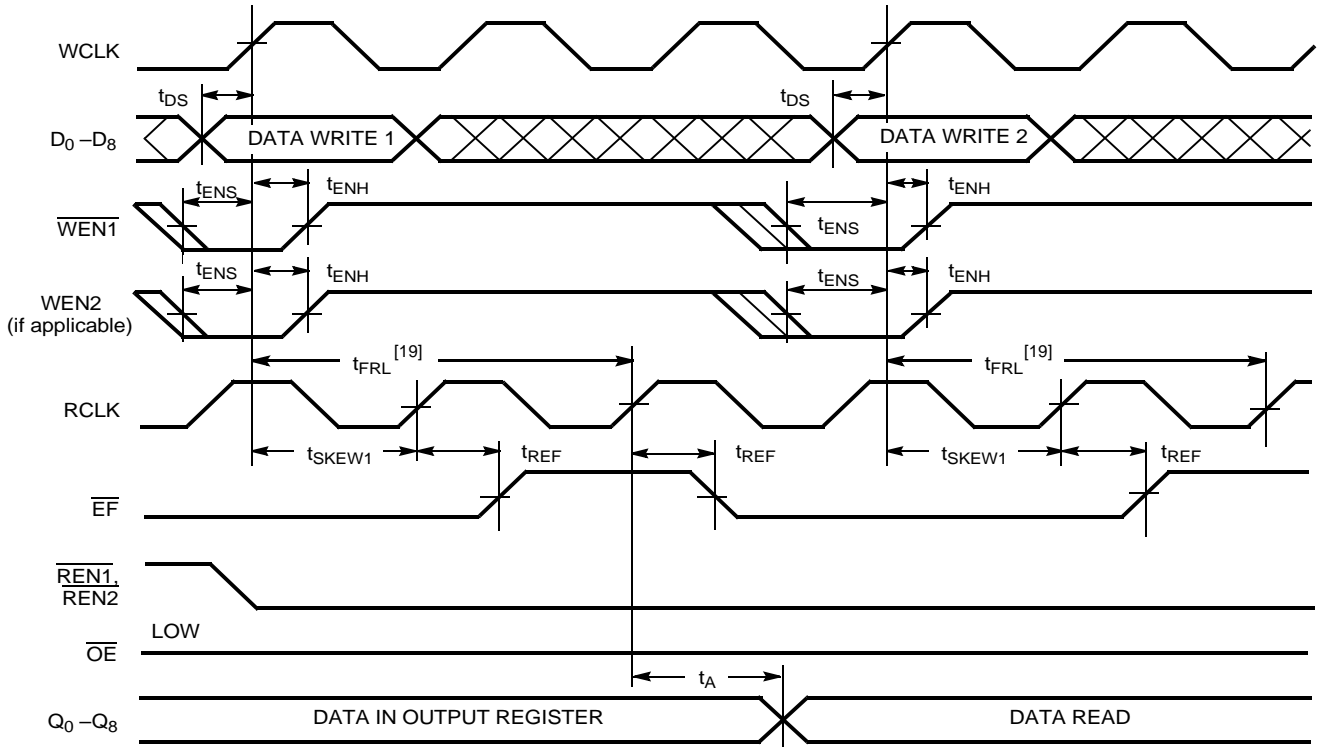
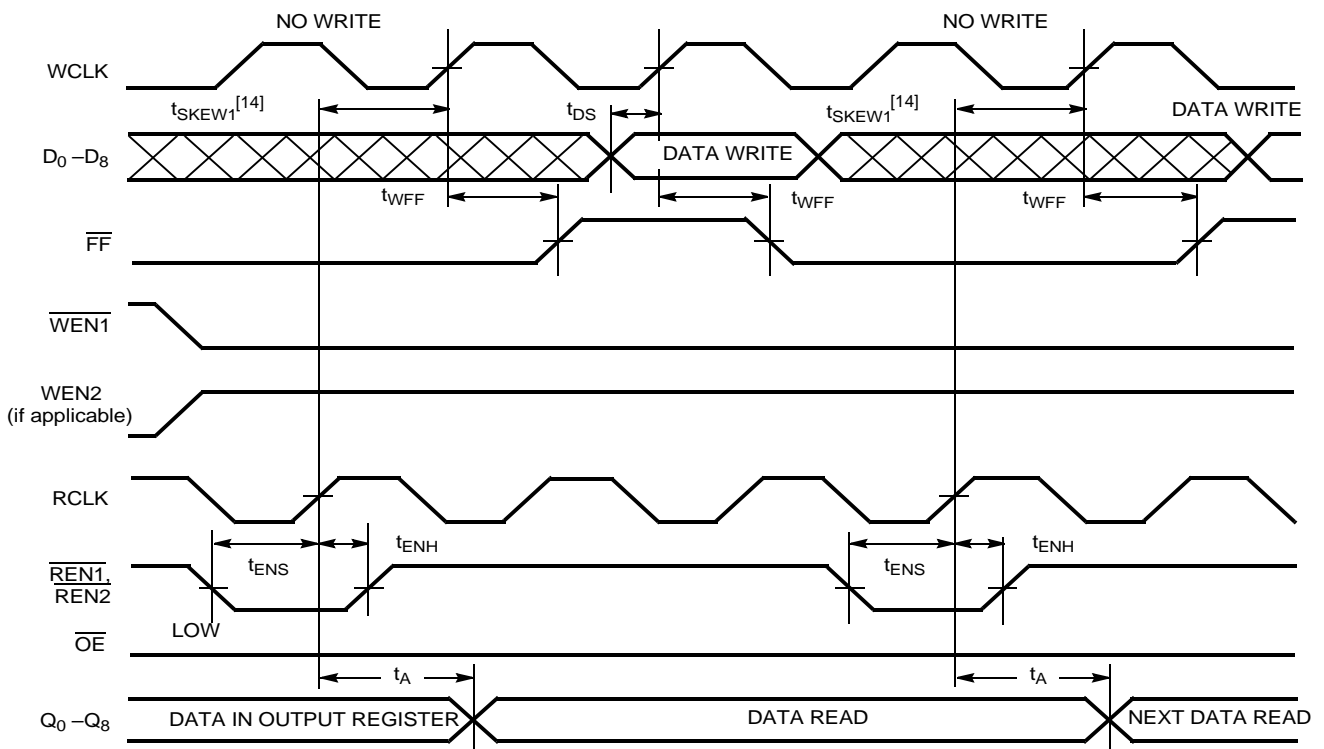


Figure 11. Full Flag Timing



Switching Waveforms (continued)

Figure 12. Programmable Almost Empty Flag Timing

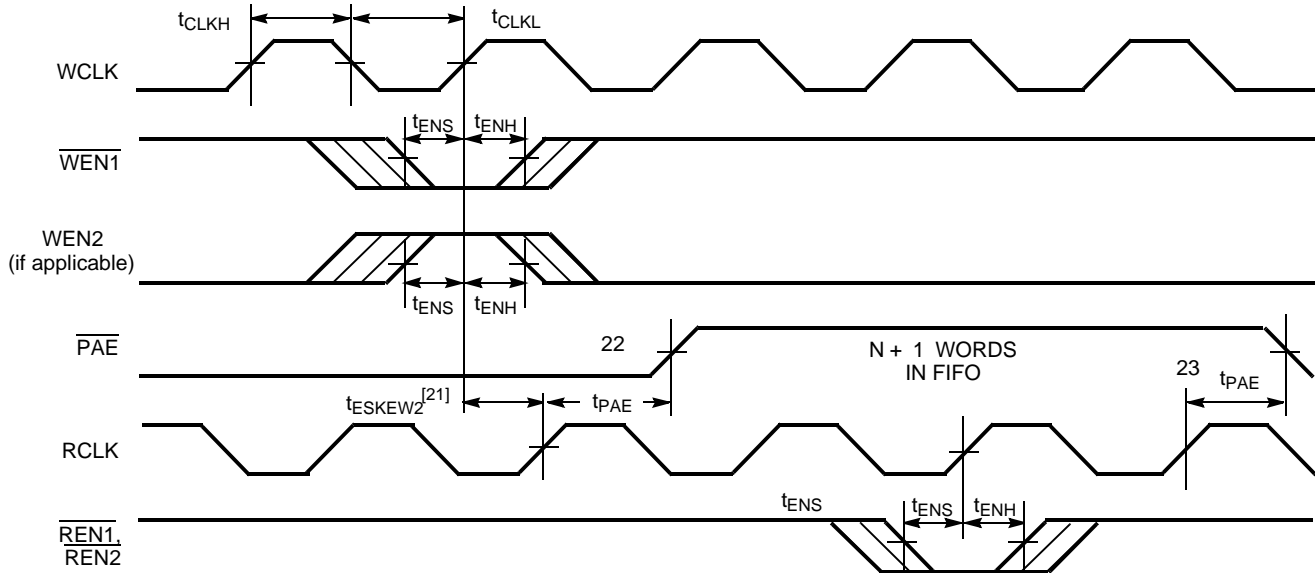
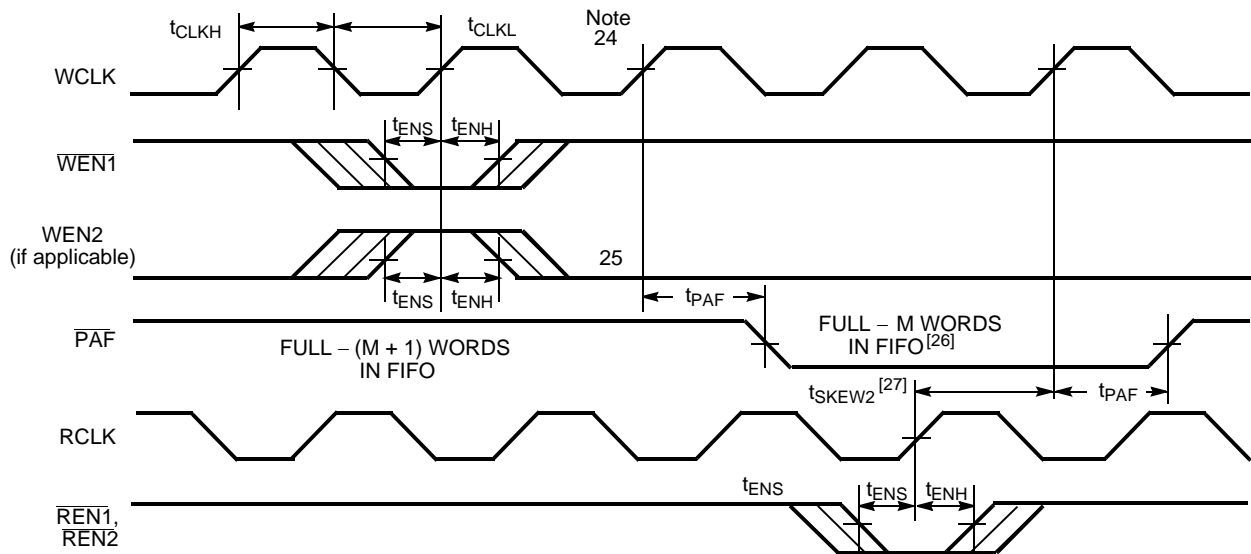


Figure 13. Programmable Almost Full Flag Timing



Notes

- 21.  $t_{SKEW2}$  is the minimum time between a rising WCLK and a rising RCLK edge for  $\overline{PAE}$  to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than  $t_{SKEW2}$ , then PAE may not change state until the next RCLK.
- 22. PAE offset = n.
- 23. If a read is performed on this rising edge of the read clock, there are Empty + (n-1) words in the FIFO when  $\overline{PAE}$  goes LOW.
- 24. If a write is performed on this rising edge of the write clock, there are Full - (m-1) words of the FIFO when  $\overline{PAF}$  goes LOW.
- 25. PAF offset = m.
- 26. 16,384 - m words for CY7C4261, 32,768 - m words for CY7C4271.
- 27.  $t_{SKEW2}$  is the minimum time between a rising RCLK edge and a rising WCLK edge for  $\overline{PAF}$  to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $t_{SKEW2}$ , then  $\overline{PAF}$  may not change state until the next WCLK.

Switching Waveforms (continued)

Figure 14. Write Programmable Registers

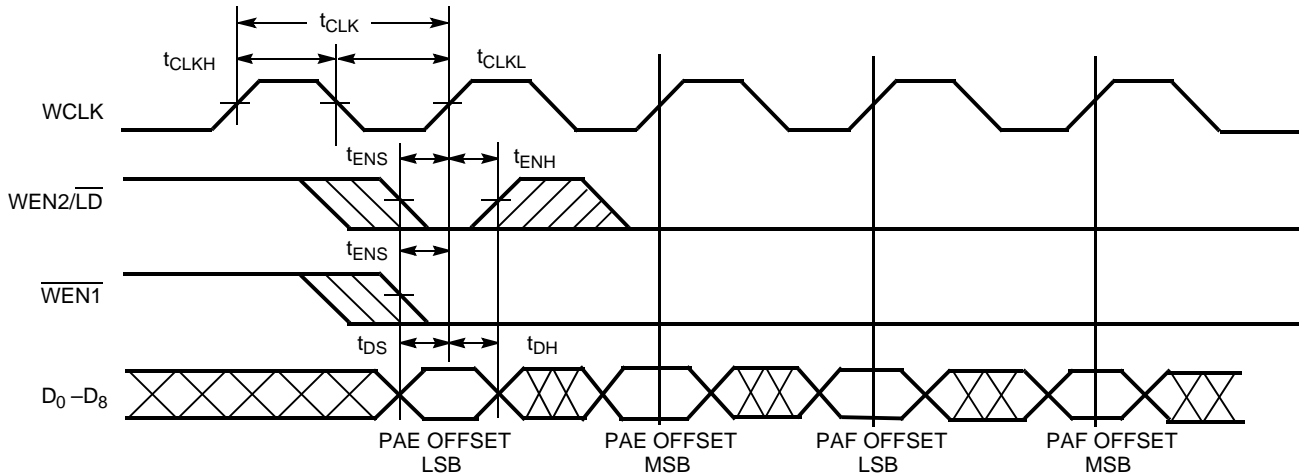


Figure 15. Read Programmable Registers

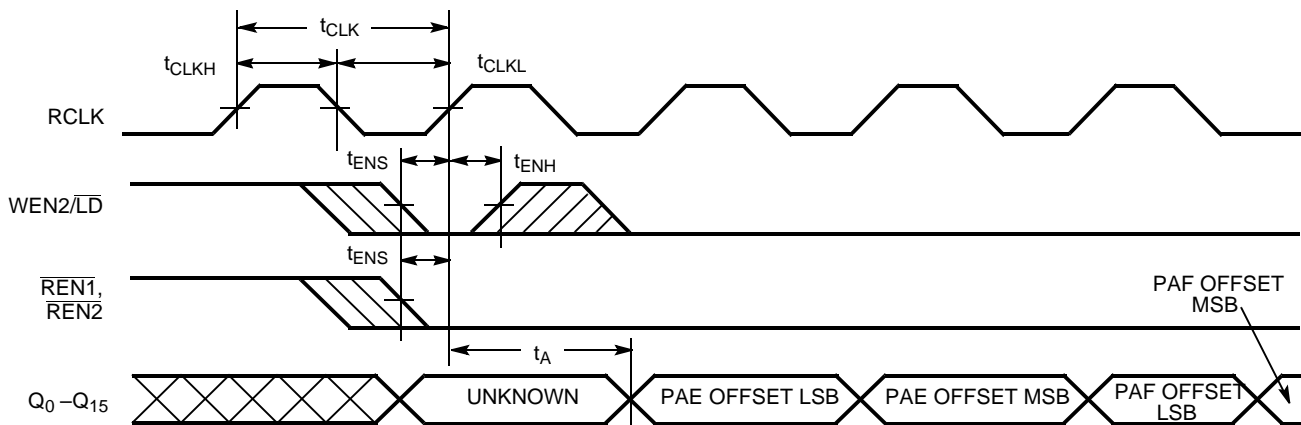
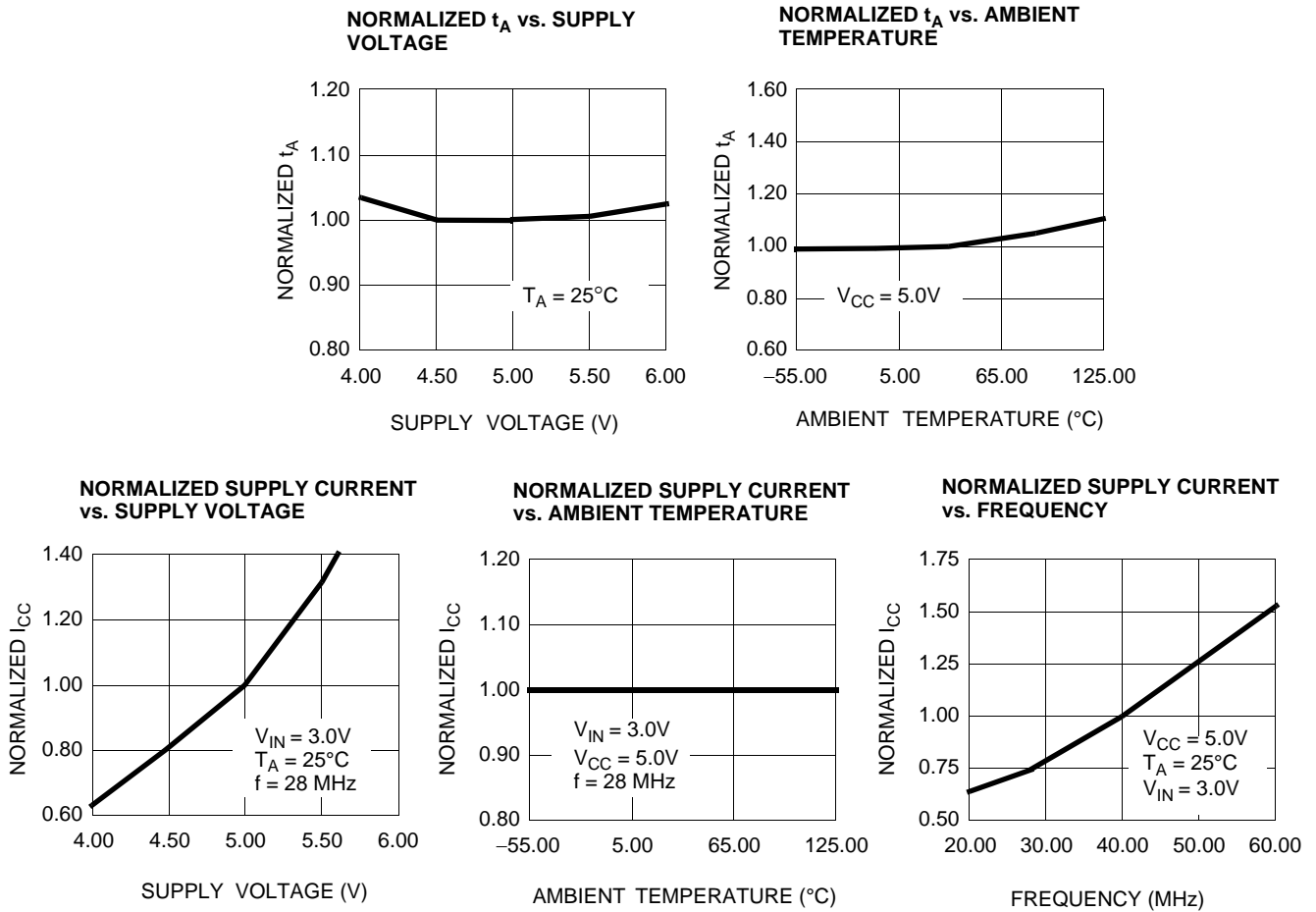


Figure 16. Typical AC and DC Characteristics



**Ordering Information**
**16Kx9 Deep Sync FIFO**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C4261-10AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4261-10JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4261-10AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4261-10JI	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4261-10JXI		32-Pin Plastic Leaded Chip Carrier (Pb-Free)	
15	CY7C4261-15AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4261-15JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4261-15JXC		32-Pin Plastic Leaded Chip Carrier (Pb-Free)	
	CY7C4261-15AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4261-15JI	51-85002	32-Pin Plastic Leaded Chip Carrier	
25	CY7C4261-25AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4261-25JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4261-25AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4261-25JI	51-85002	32-Pin Plastic Leaded Chip Carrier	
35	CY7C4261-35AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4261-35JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4261-35AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4261-35JI	51-85002	32-Pin Plastic Leaded Chip Carrier	

**32Kx9 Deep Sync FIFO**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C4271-10AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4271-10JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4271-10AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4271-10JI	51-85002	32-Pin Plastic Leaded Chip Carrier	
15	CY7C4271-15AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4271-15AXC		32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm) (Pb-Free)	
	CY7C4271-15JC	51-85002	32-Pin Plastic Leaded Chip Carrier	Industrial
	CY7C4271-15AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	
	CY7C4271-15JI	51-85002	32-Pin Plastic Leaded Chip Carrier	
		CY7C4271-15LMB	51-80068	32-Pin Rectangular Leadless Chip Carrier
5962-9736101QYA				
25	CY7C4271-25AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4271-25JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4271-25AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4271-25JI	51-85002	32-Pin Plastic Leaded Chip Carrier	
35	CY7C4271-35AC	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Commercial
	CY7C4271-35JC	51-85002	32-Pin Plastic Leaded Chip Carrier	
	CY7C4271-35AI	51-85063	32-Pin Thin Quad Flat Pack (7 x 7 x 1.0 mm)	Industrial
	CY7C4271-35JI	51-85002	32-Pin Plastic Leaded Chip Carrier	



Table 4. DC Characteristics

Parameters	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub> Max.	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>CC1</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3
I <sub>OS</sub>	1, 2, 3

Table 5. Switching Characteristics (continued)

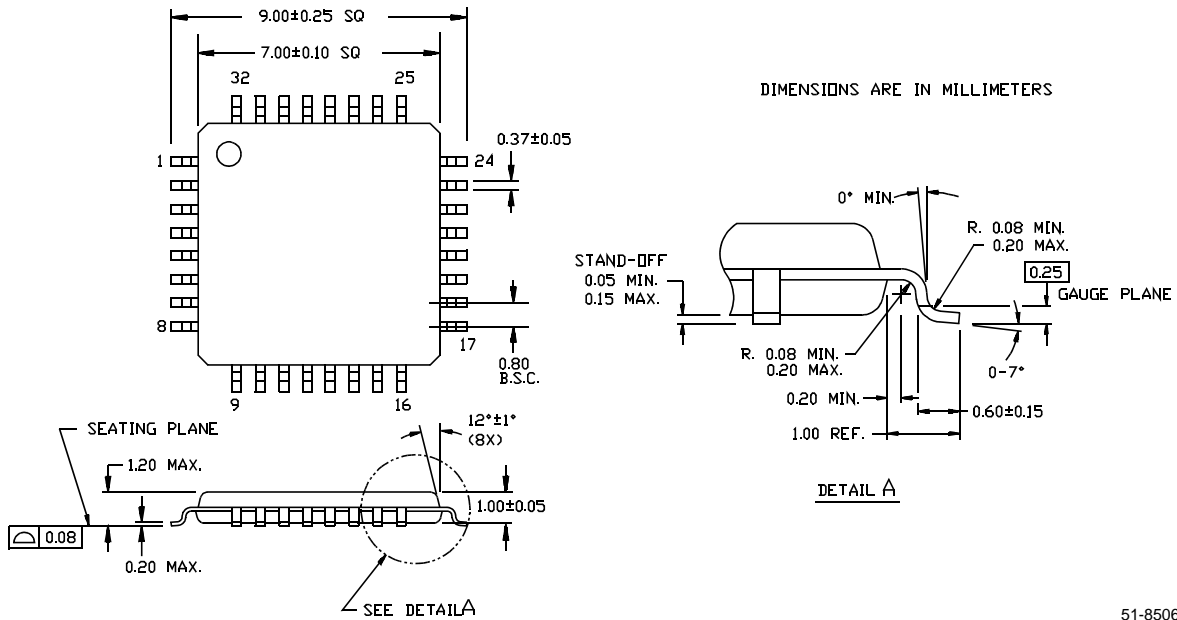
Parameters	Subgroups
t <sub>RFF</sub>	9, 10, 11
t <sub>WEF</sub>	9, 10, 11
t <sub>WFF</sub>	9, 10, 11
t <sub>WHF</sub>	9, 10, 11
t <sub>RHF</sub>	9, 10, 11
t <sub>RAE</sub>	9, 10, 11
t <sub>RPE</sub>	9, 10, 11
t <sub>WAF</sub>	9, 10, 11
t <sub>WPF</sub>	9, 10, 11
t <sub>XOL</sub>	9, 10, 11
t <sub>XOH</sub>	9, 10, 11

Table 5. Switching Characteristics

Parameters	Subgroups
t <sub>RC</sub>	9, 10, 11
t <sub>A</sub>	9, 10, 11
t <sub>RR</sub>	9, 10, 11
t <sub>PR</sub>	9, 10, 11
t <sub>DVR</sub>	9, 10, 11
t <sub>WC</sub>	9, 10, 11
t <sub>PW</sub>	9, 10, 11
t <sub>WR</sub>	9, 10, 11
t <sub>SD</sub>	9, 10, 11
t <sub>HD</sub>	9, 10, 11
t <sub>MRSC</sub>	9, 10, 11
t <sub>PMR</sub>	9, 10, 11
t <sub>RMR</sub>	9, 10, 11
t <sub>RPW</sub>	9, 10, 11
t <sub>WPW</sub>	9, 10, 11
t <sub>RTC</sub>	9, 10, 11
t <sub>PRT</sub>	9, 10, 11
t <sub>RTR</sub>	9, 10, 11
t <sub>EFL</sub>	9, 10, 11
t <sub>HFH</sub>	9, 10, 11
t <sub>FFH</sub>	9, 10, 11
t <sub>REF</sub>	9, 10, 11

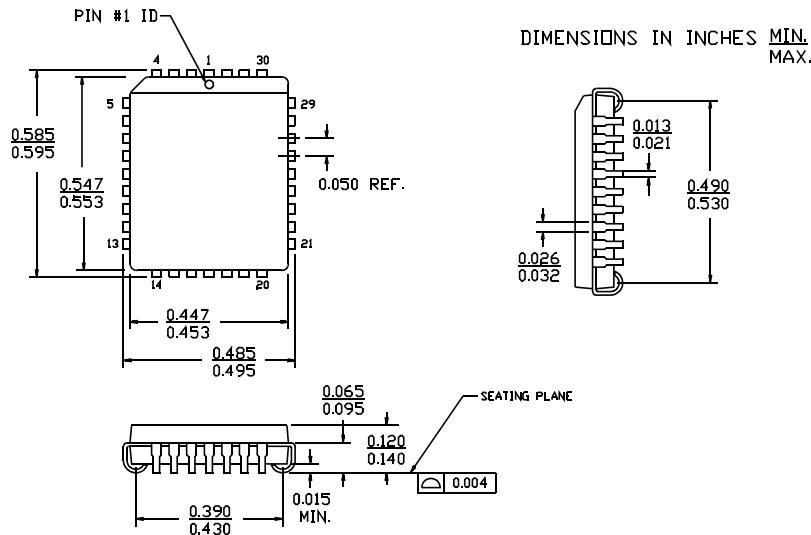
Package Diagrams

Figure 17. 32-Pin Thin Plastic Quad Flatpack (7 x 7 x 1.0 mm)



51-85063 \*B

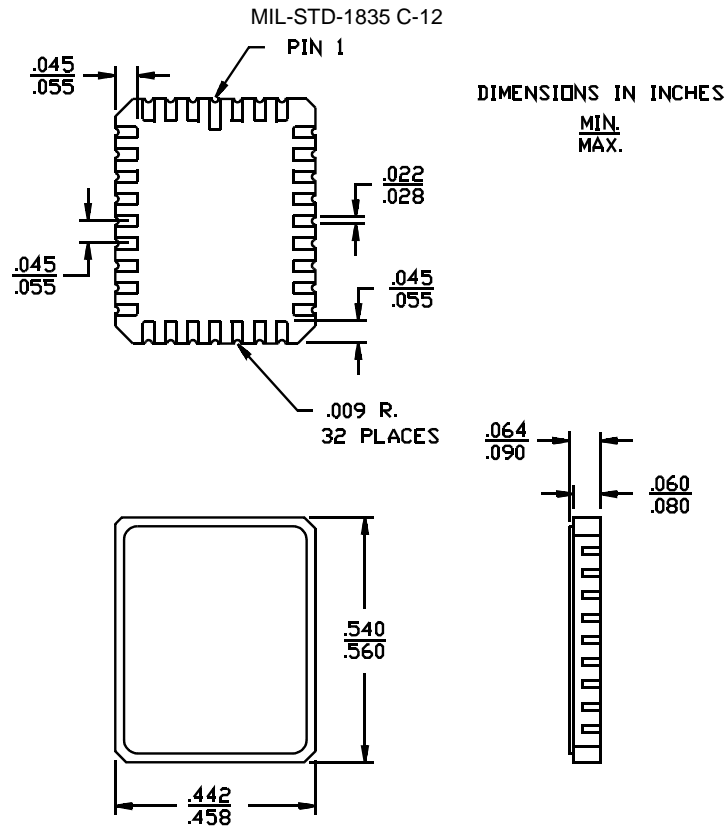
Figure 18. 32-Pin Plastic Leaded Chip Carrier



51-85002 \*B

Package Diagrams (continued)

Figure 19. 32-Pin Rectangular Leadless Chip Carrier



51-80068-\*\*

**Document History Page**

Document Title: CY7C4261/CY7C4271, 16K/32K x 9 Deep Sync FIFOs				
Document Number: 38-06015				
REV.	ECN	Orig. of Change	Submission Date	Description of Change
**	106476	SZV	09/10/01	Changed from Spec number: 38-00658 to 38-06015
*A	122267	RBI	12/26/02	Added power up requirements Maximum Ratings Information
*B	127853	FSG	08/22/03	Switching Waveforms section: fixed misplaced footnote in $t_A$ in "First Data Word Latency after Reset with Read and Write" drawing Switching Waveforms section: changed $t_{SKEW2}$ to $t_{SKEW1}$ (typo) in "Empty Flag Timing" drawing
*C	393437	ESH	See ECN	Added Pb-Free Logo to top of front page Added CY7C4261-10JXI, CY7C4261-15JXC to ordering information
*D	2556036	VKN/AESA	08/22/2008	Updated ordering information and data sheet template. Removed Pb-Free Logo.

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