INCH-POUND

MIL-M-38510/206D
25 April 2005
SUPERSEDING
MIL-M-38510/206C
10 September 1986

MILITARY SPECIFICATION

MICROCIRCUIT, DIGITAL, 4096-BIT SCHOTTKY, BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM),

Inactive for new design after 24 July 1995

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, programmable read-only memory (PROM) microcircuits which employ thin film nichrome (NiCr) resistors, tungsten (W) or titanium tungsten (TiW) as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. A special test requirement is included in this specification to screen against devices which may contain excess moisture in the package materials or internal atmosphere (see freeze-out test of 4.2d). For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit	Access times (ns)
01	1024 word/4 bits per word PROM with open collector.	85
02, 04	1024 word/4 bits per word PROM with three-state output.	85, 55
03	1024 word/4 bits per word PROM with active pull-up	85

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
Y	See figure 1	24	Square chip carrier
Z	See figure 1	18	Flat pack
U	GDFP2-F18	18	Flat pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 Ma to +5.5 V dc
Storage temperature range	-65° to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC}) 1/:	
Cases E, F, V, and U	See MIL-STD-1835
Case Y	30° C/W 2/
Case Z	0.08° C/W
Output voltage applied	-0.5 C dc to +V_{CC}
Output sink current	100 mA
Maximum power dissipation (P_D) 3/	794 mW dc
Maximum,unction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Normalized fanout (each output)	16 mA
Case operating temperature range (T_C)	-55 °C to +125 °C

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outline

1/ Heat sinking is recommended to reduce the junction temperature.
2/ When a thermal resistance value is included in, MIL-PRF-38535 it shall supersede the value stated herein.
3/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per MIL-PRF-38535.

(Copies of these documents are available online at *http://assist.daps.dla.mil/quicksearch/* or *http://assist.daps.dla.mil* or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figures 2.

3.3.2 Truth table

3.3.2.1 Unprogrammed devices. The truth table for unp;rogrammed devices for contracts involving no altered itme drawing shall be as specified on figure 3. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3 Functional block diagram. The functional block diagram shall be as specified on figure 4. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define the row address inputs and the column address inputs.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table II, and where applicable, the altered item drawing. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless other wise specified	Device Type	Limits		Units
				Min	Max	
High-level output voltage	V_{OH}	V_{CC}=4.5 V I_{OH} = -2 mA V_{IL} = 0.8 V; V_{IH} = 2.0 V	02, 03, 04	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL}=16 mA 2/ V_{IL} = 0.8 V; V_{IH} = 2.0 V	01, 02, 03, 04		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_{OL}= -12 mA; T_C = +25ºC	01, 02, 03, 04		-1.5	V
Maximum collector cut-off current	I_{CEX}	V_{CC} = 5.5 V V_{OH} = 5.2 V	01		100	µA
High-impedence (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V V_{IN} = 5.2 V	02, 04		100	µA
High-impedence (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V V_{OL} = 0.5 V	02, 04		-100	µA
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 5.5 V	01, 02, 03, 04		50	µA
High level input current	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 4.5 V Special program pin	01, 02, 04		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	01, 02, 03, 04	-1.0	-250	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V V_0 = 0.0 V 3/	02, 03, 04	-10	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V V_{IN} = 0 V Outputs open	01, 02, 03, 04,		140	mA
Propagation delay time, high to low level logic, address to output	t_{PHL1}	V_{CC} = 5.5 V and 4.5 V C_L = 30 pF See figure 5	01, 02, 03		85	ns
			04		55	
Propagation delay time, low to high level logic, address to output	t_{PLH1}		01, 02, 03		85	ns
			04		55	
Propagation delay time, high to low level logic, enable to output	t_{PHL2}		01, 02, 03		40	ns
			04		35	
Propagation delay time, low to high level logic, enable to output	t_{PLH2}		01, 02		40	ns
			04		35	

1/ Complete terminal conditions shall be specified In table III.
2/ I_{OL} = 8 mA for circuit A only.
3/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III) 1/, 2/, 3/	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters for unprogrammed devices	1*, 2, 3, 7, *8	1*, 2, 3, 7, *8
Final electrical test parameters for programmed devices	1*, 2, 3, 7* 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9,
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8 9, 10, 11
Group B end-point electrical parameters subgroup 5	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8
Group D test requirements	1, 2, 3, 7, 8	1, 2, 3, 7, 8

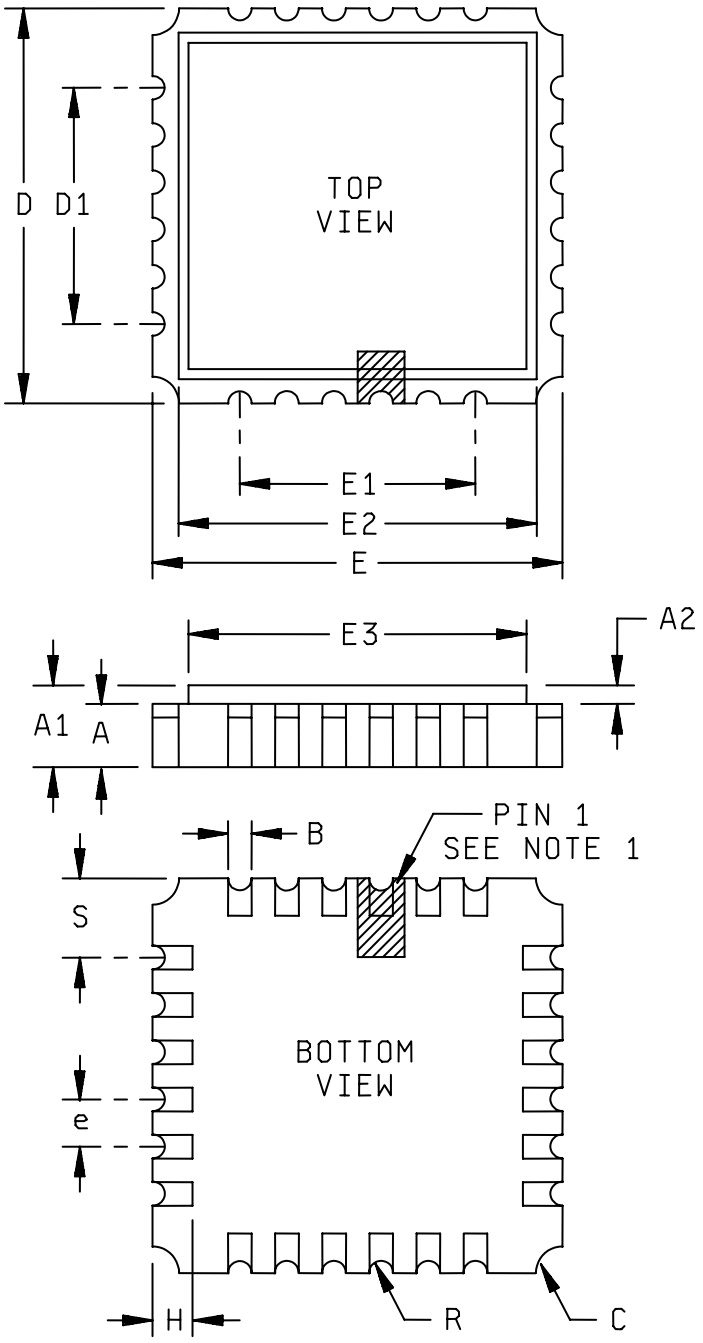
1/ * indicates PDA applies to subgroups 1 and 7 (see 4.2c).
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

3.8 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.3.2.1, table II, and table III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2 Maunufacture-programmed PROM delivered to the user. All testing requirements and quality assureance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

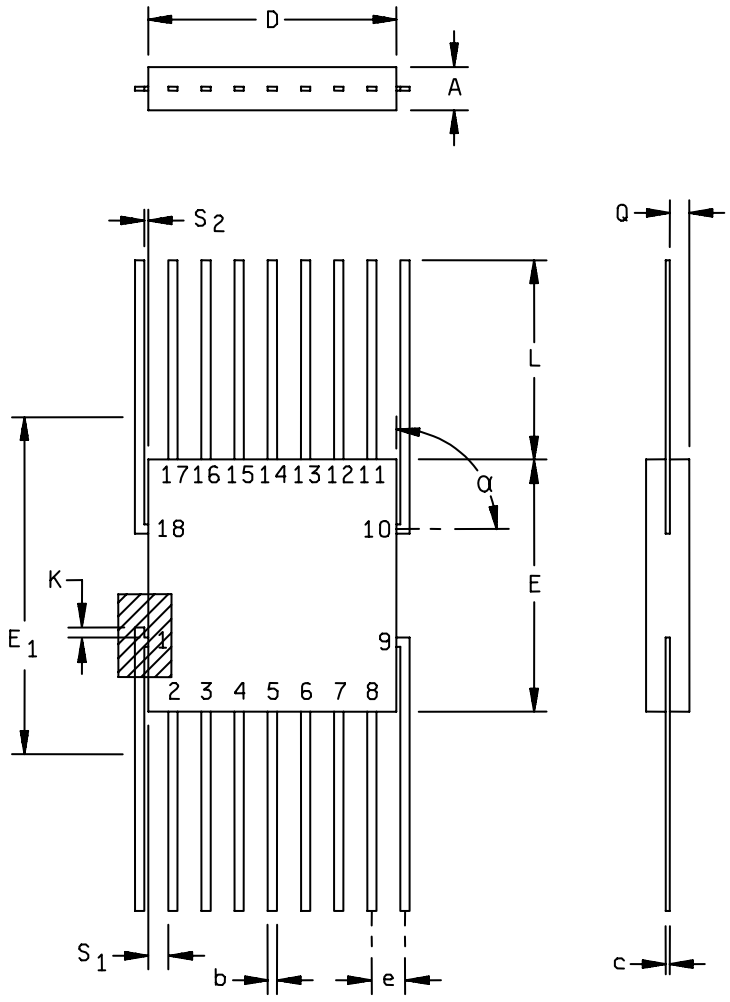
3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see Appendix A MIL-PRF-38535.)



Symbol	Dimension				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	1, 5
A	.053	.088	1.35	2.24	
A_1	.064	.100	1.63	2.54	
A_2	.010	.022	0.25	0.56	
B	.018	.028	0.46	0.71	3, 4
C	.012R	---	0.30R	---	2
D	.395	.410	10.03	10.41	
D_1	.250		6.35		7
E	.395	.410	10.03	10.41	
E_1	.250		6.35		7
E_2	.372	.388	9.45	9.86	6
E_3	.352	.358	8.94	9.09	
e	.050 BSC		1.27 BSC		7
H	.030	.035	0.76	0.89	
R	.008R	---	0.20R	---	4
S	.065	.085	1.65	2.16	

NOTES:
1. Index area: A notch, indentification mark or elongation shall be used to identify pin 1.
2. Applies to all four corners. Corners may also be chamfered.
3. Shaded areas are metallized.
4. 24 Locations.
5. No organic or polymeric materials shall be molded to the package.
6. Sealing metallization.
7. Dimensions vary in direct proportion to feature size of D and E.

FIGURE 1. Case outline Y (24 terminal, 0.40” x 0.40”, chip carrier).



Dimension					
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.085	1.14	2.16	
b	.014	.017	0.36	0.43	5
c	.003	.006	0.08	0.15	5
D		.380		9.65	3
E	.340	.380	8.64	9.65	
E_1		.400		10.16	3
e	.050 BSC		1.27 BSC		4,6
K	.008	.015	0.20	0.38	9
L	.250	.370	6.35	9.40	
Q	.010	.040	0.25	1.02	2
S_2	.004		0.10		10
S_1	.005		0.13		7, 8
α	30°	90°	30°	90°	11

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dim K) may be used to identify pin one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. Ths dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 (0.13 mm) of its exact longitudinal position relative to pins relative to pins 1 and 18.
5. All leads – increase maximum limit by .003 (0.08mm) measured at the center of the flat, when lead finish A is applied.
6. Sixteen spaces.
7. Applies to all four corners (leads number 2, 8, 11, and 17).
8. Dimension S_1 may be .000 (0.00 mm) if leads number 2, 8, 11, and 17 bend toward the cavity of the package within one lead width from the point of entry of the lead, into the body or if the leads are brazed to the metallized ceramic body (see MIL-STD-1835) .
9. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension K does not apply.
10. Applies to leads number 1, 9, 10, and 18.
11. Lead configuration is optional within dimension E except dimensions b and c apply (see MIL-STD-1835).

FIGURE 1. Case outline Z (18-lead, 3/8" x 3/8") – Continued.

	Device type 01, 02, and 04		Device type 03
	Cases		
Pin number	V, Z, and U	Y	E and F
1	A6	N/C	A6
2	A5	A6	A5
3	A4	A5	A4
4	A3	A4	A3
5	A0	A3	A0
6	A1	A0	A1
7	A2	A1	A2
8	$\overline{CE1}$	A2	GND
9	GND	NC	O4
10	$\overline{CE2}$	NC	O3
11	O4	$\overline{CE1}$	O2
12	O3	GND	O1
13	O2	$\overline{CE2}$	A9
14	O1	O4	A8
15	A9	O3	A7
16	A8	O2	V_{CC}
17	A7	O1	
18	V_{CC}	NC	
19		NC	
20		NC	
21		A9	
22		A8	
23		A7	
24		V_{CC}	

FIGURE 2. Terminal connections.

Word no.	Enable		Address										Data			
	$\overline{CE1}$	$\overline{CE2}$	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	01	02	03	04
NA	L	L	X	X	X	X	X	X	X	X	X	X	5/	5/	5/	5/
NA	L	H	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC
NA	H	L	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC
NA	H	H	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC

NOTES:
1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with both enable inputs at low level.
5. The outputs for an unprogrammed device shall be high for circuits A, and D, and shall be low for circuit B, C, and G.

FIGURE 3. Truth table (unprogrammed).

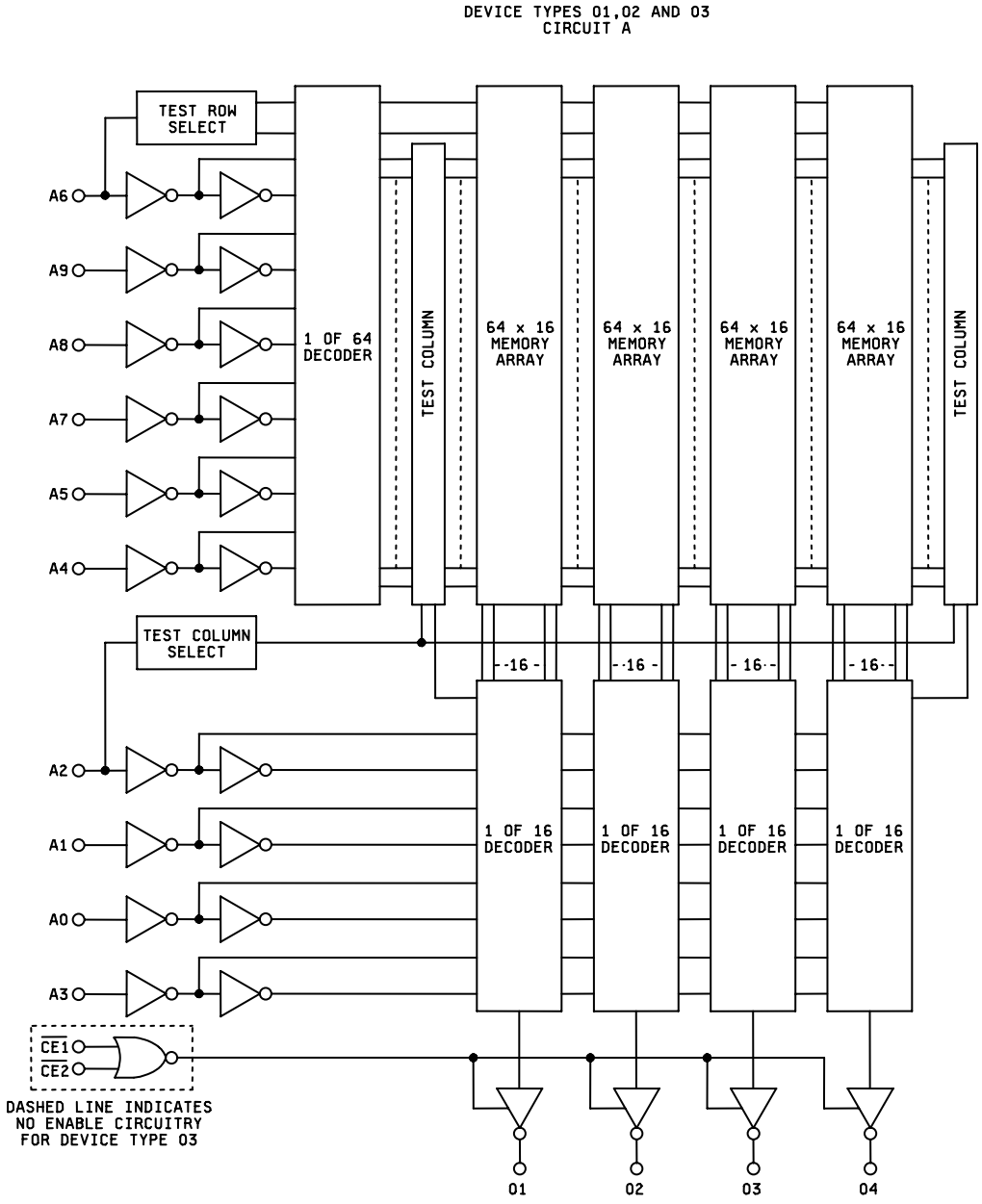


FIGURE 4. Functional block diagram.

CIRCUIT B

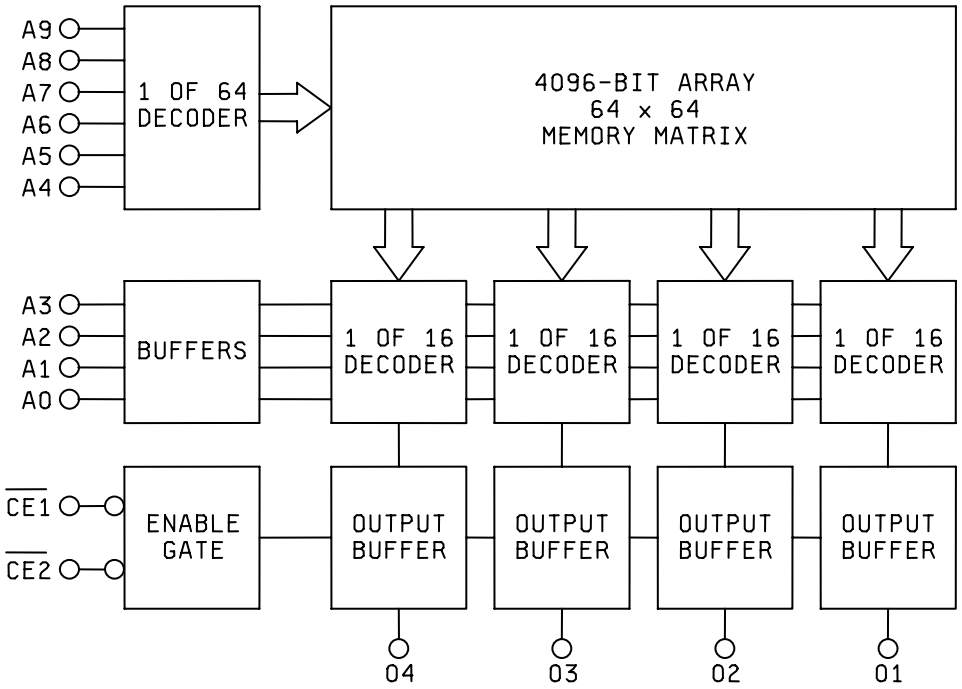


FIGURE 4. Functional block diagram – Continued.

CIRCUIT C

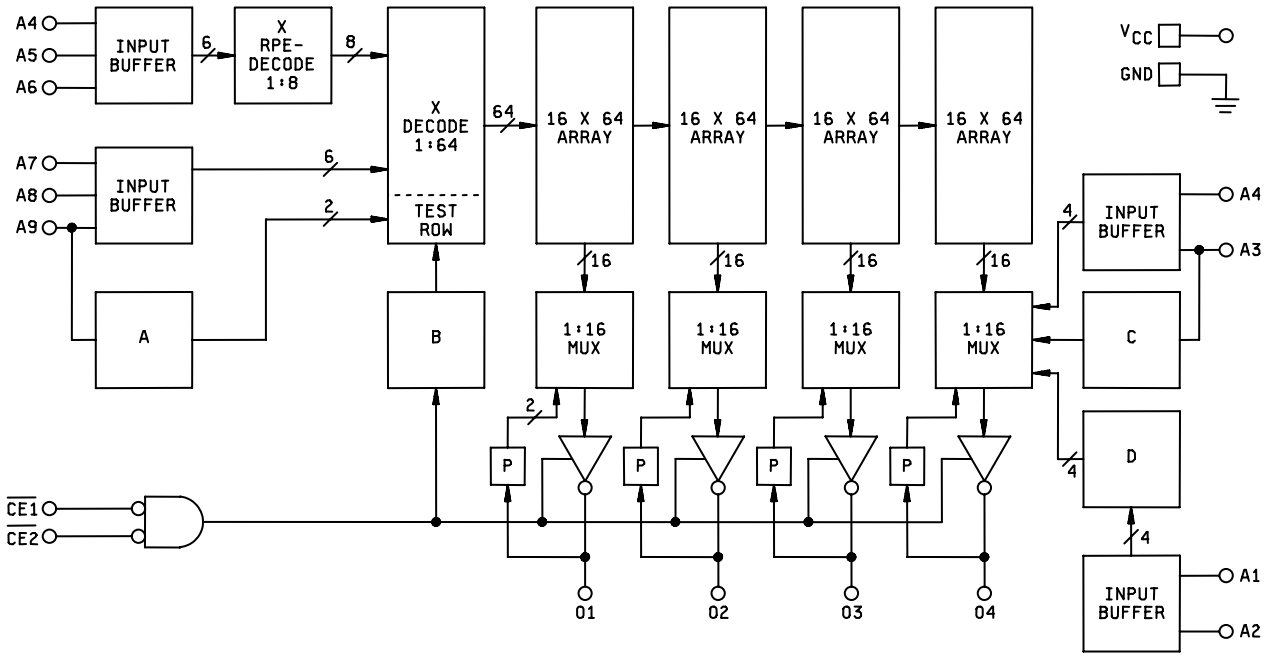


FIGURE 4. Functional block diagram – Continued.

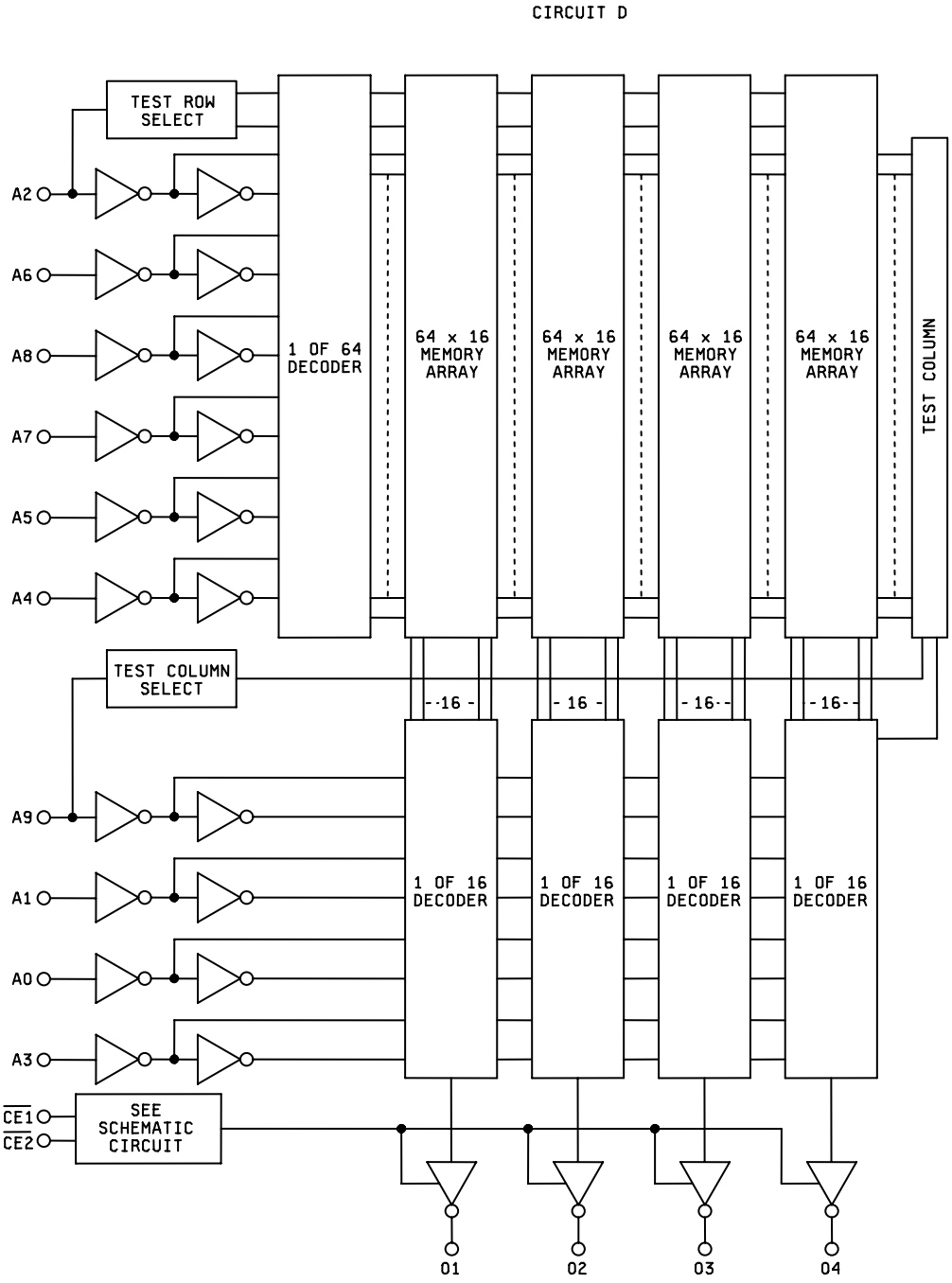


FIGURE 4. Functional block diagram - Continued

DEVICE TYPE 01
CIRCUIT G

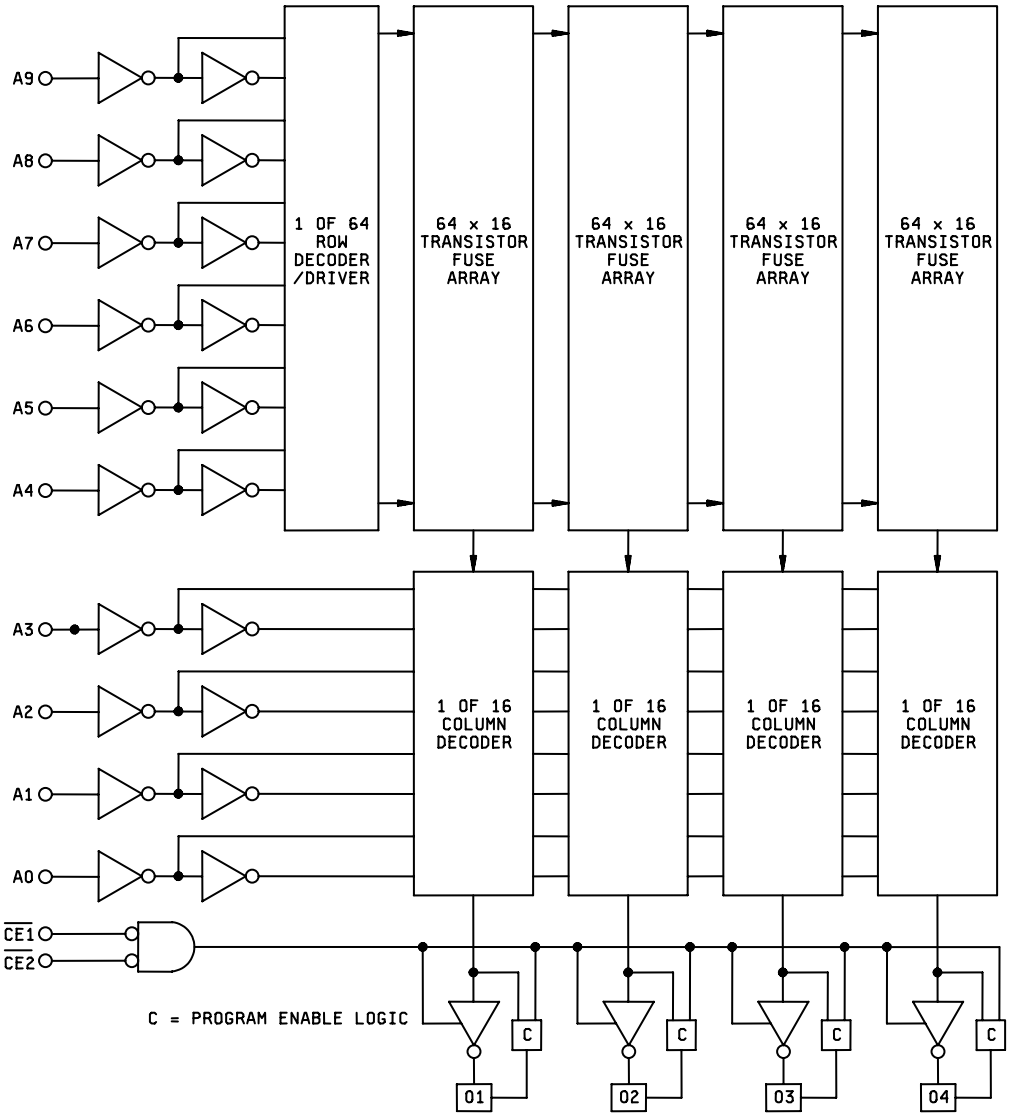


FIGURE 4. Functional block diagram - Continued

DEVICE TYPE 02
CIRCUIT G

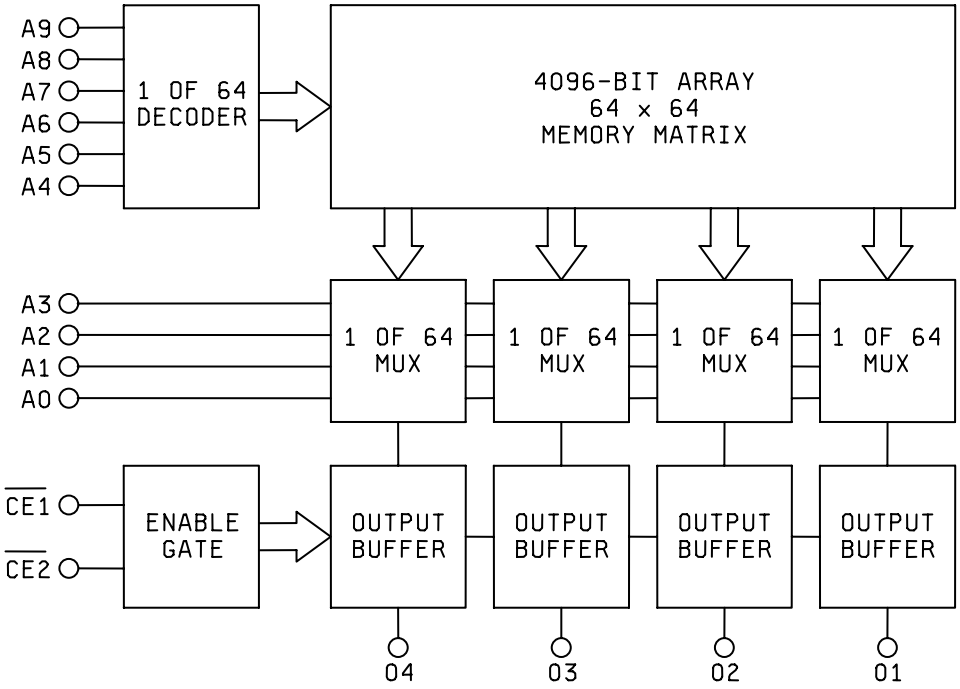
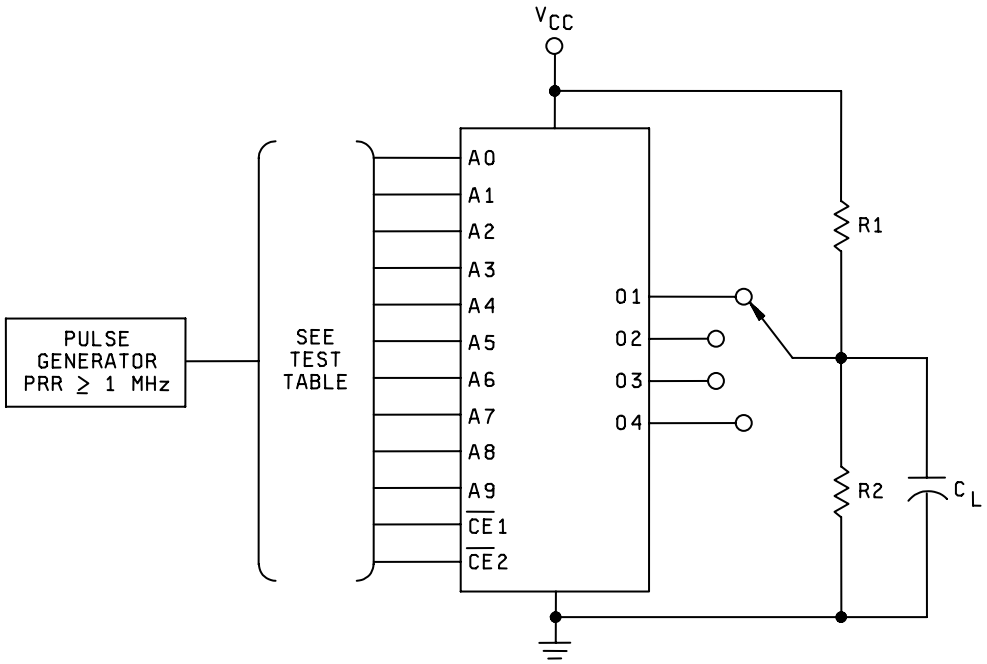
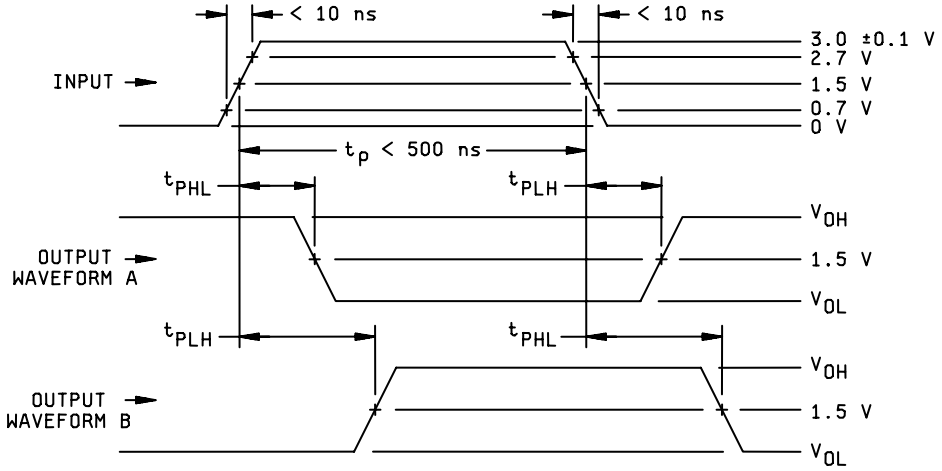


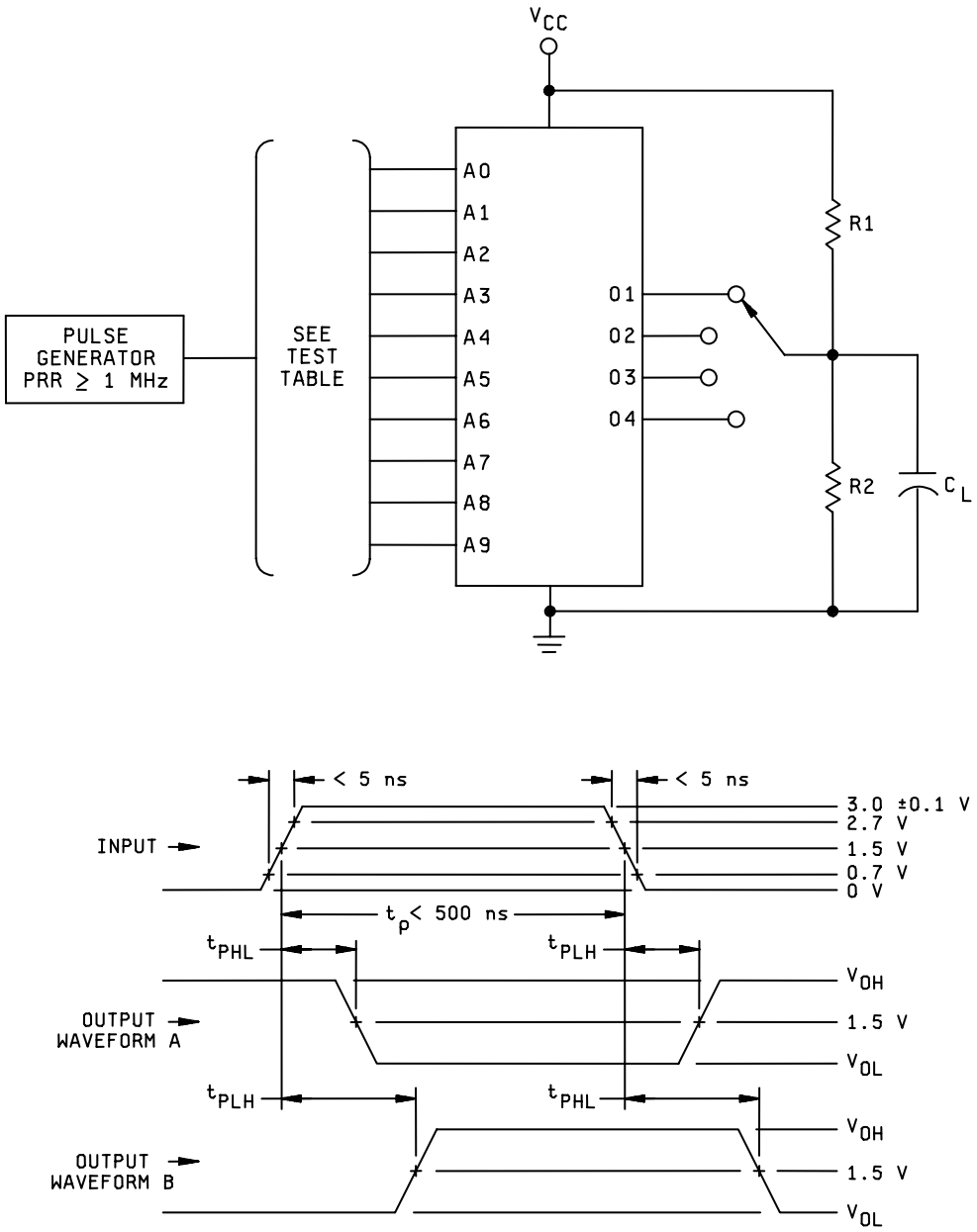
FIGURE 4. Functional block diagram – Continued.





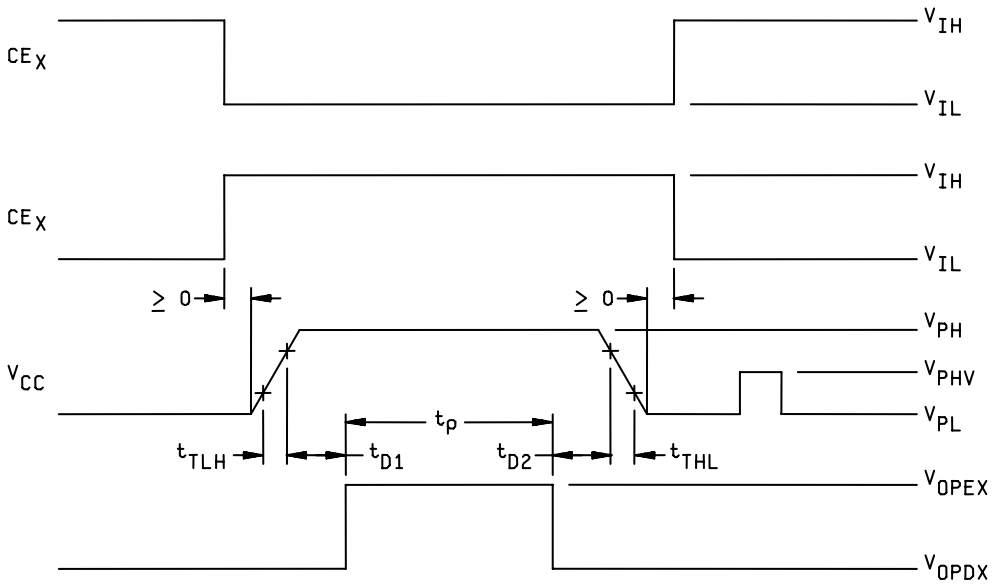
NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330Ω ±25%, and R_2 = 680Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 5 Switching time test circuit, device types 01, 02, and 04.



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330Ω ±25%, and R_2 = 680Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 5 Switching time test circuit, device types 03.



NOTE: All other waveform characteristics shall be as specified in table IVA.

FIGURE 6A. Programming voltage waveforms during programming for circuit A.

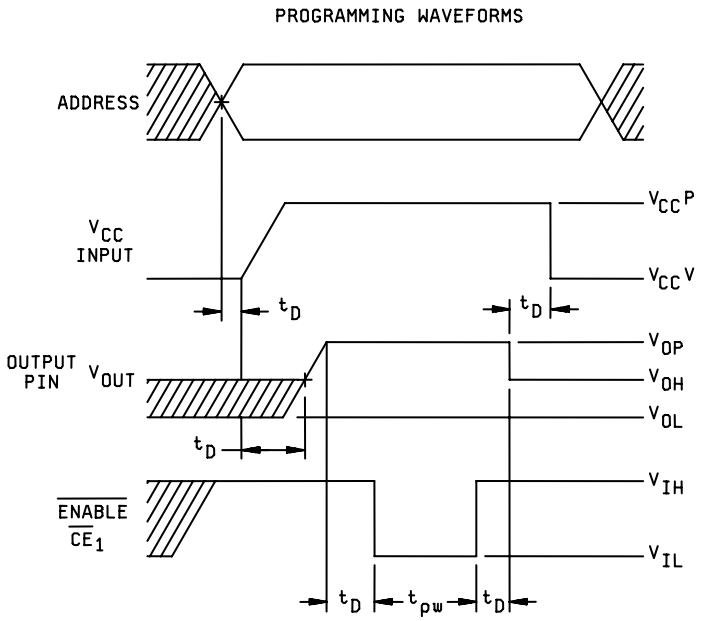
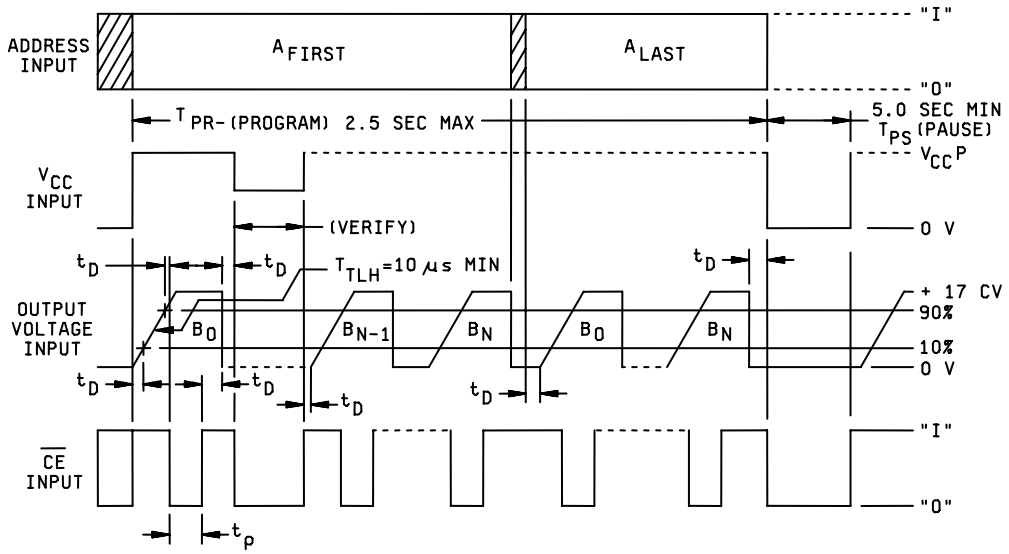


FIGURE 6B. Typical programming voltage waveforms during programming for circuit B.



NOTE: All other waveform characteristics shall be as specified in table IV C.

FIGURE 6C. Typical programming voltage waveforms during programming for circuit C.

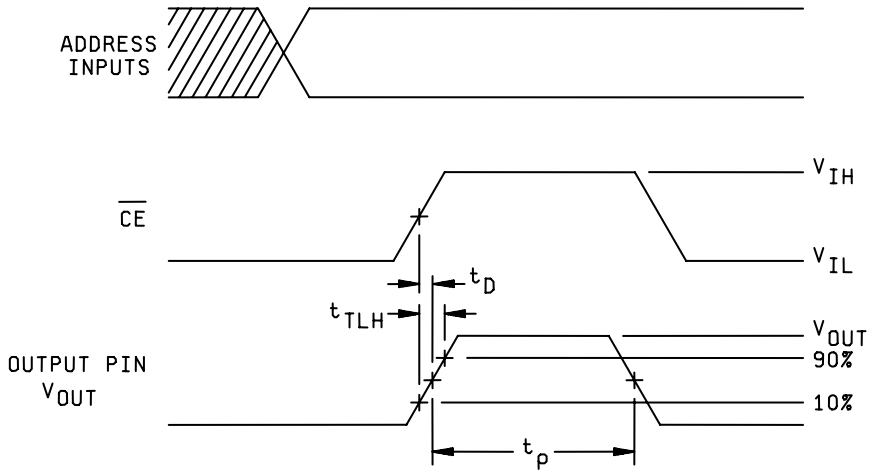


FIGURE 6D Programming voltage waveforms during programming for circuit D.

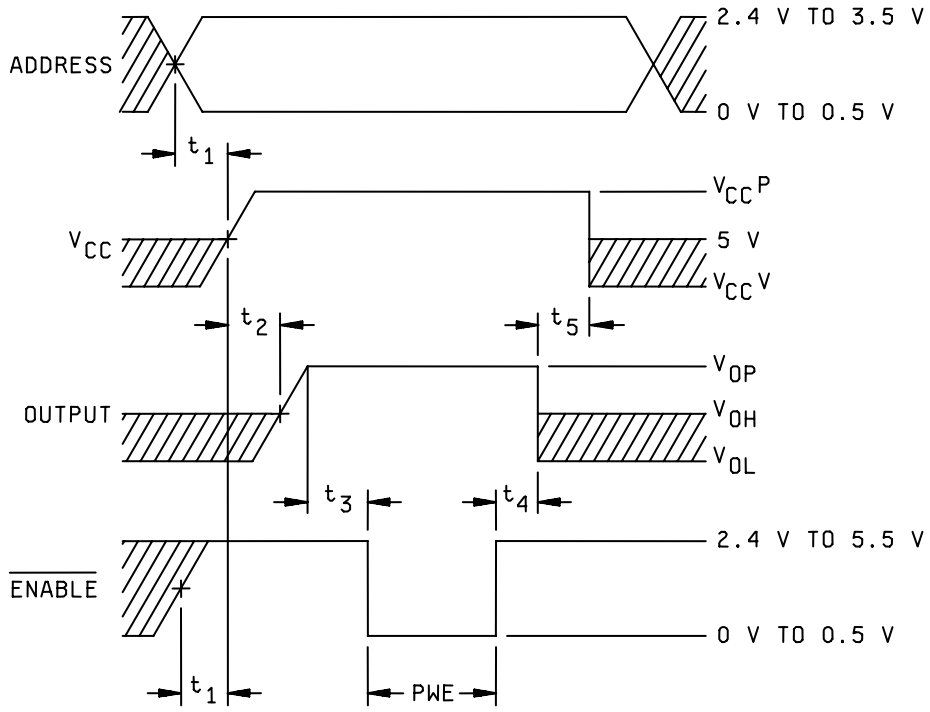
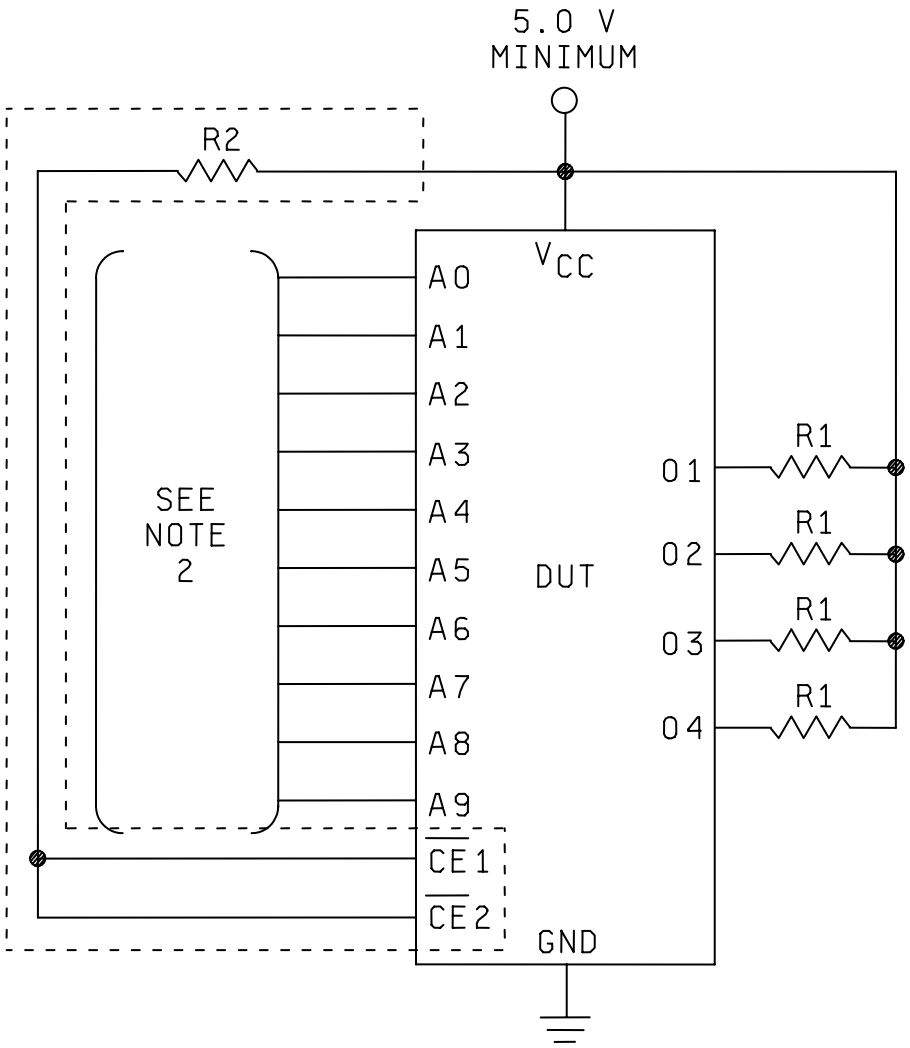


FIGURE 6G. Programming voltage waveforms during programming for circuit G.



NOTES:
1. R_1 = 4.7Ω ±5%. All bit outputs shall have separate identical loads.
2. All Addresses inputs shall be either high, low, or open.
3. R_2 = 1 kΩ ±5%.
4. Burn-in circuit may be used to perform this test . All Address inputs shall be either high, low, or open.
5. For device type 03, the circuitry within the dashed lines is not present.

FIGURE 7. Freeze-out test bias configuration.

4. *VERIFICATION*

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

d. Freeze-out test: This test shall be conducted as a 100 percent screen on all class S devices having nichrome as the fusing link. Within no more that 24 hours after completion of burn-in and prior to final electrical test, all devices containing nichrome resistors (see 3.8.1 and 3.8.2) shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the +125°C burn-in exposure, devices shall be conditioned with at least +125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is peformed the +25°C final electrical test parameters shall be completed 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:

(1) Connect devices in the electrical configuration of figures 7 or in the burn-in configuration with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.

(2) Reduce device temperature to T_C = -10° ±2°C with bias cycled and maintain at that temperature for a minimum of 5 hours duration.

(3) With the cycled bias maintained, allow T_C to go to room temperature (by removal from cold chamber or termination of forced cooling but with no forced heating (and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_C shall not exceed = +35°C during this period.

(4) Remove bias and subject all devices to subgroup 1 final electrical test to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to PDA requirements.

e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer’s discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically to other device types on this specification, then the other device types may be qualified by conducting only group A electrical tests and submitting data in accordance with MIL-PRF-38535 (i.e.,groups B, C, and D tests are not required).

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Electrical test requirements shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. For unprogrammed devices, a sample shall be be selected to satisfy programmability requirements prior to performing subgroups 9. 10, and 11. Twelve devices shall be submitted to programming (see 3.3.2.1). If more than 2 devices fail to program, the lot shall be rejected, At the manufacturer's option, the sample may be increased to 24 total devices with no more thatn 4 total device failures allowable.

d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more that 4 total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.

(a) Electrical test requirements shall be as specified in table II herein.

(b) For qualification, at least 50 percent of the sample selected for testing in subgroup 5 shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 5 tests.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator.

4.7 Programming procedure for circuit A. The programming characteristics in table IVA and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 6A and the programming characteristics in table IVA shall apply to these procedures.

b. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.

c. Apply V_{PL} voltage to V_{CC}.

d. Bring the $\overline{CE}_X$ inputs high and the $\overline{CE}_X$ inputs low to disable the device. The chip enables are TTL compatable. An open circuit shall not be used to disable the devices.

e. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.

f. Raise V_{CC} to V_{PH} with rise time less than or equal to t_{TLH}.

g. After a delay equal to or greater than t_{D1} apply only one pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.

h. Lower V_{CC} to V_{PL} following a delay to t_{D2} from programming enable pulse applied to an output.

i. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ and V_{IH} to $\overline{CE}_X$.

j. Apply V_{PHV} to V_{CC} and verify bit is programmed.

k. Repeat steps a through j for all other bits to be programmed in the PROM.

l. If any bit does not veify as programmed, it shall be considered a programming reject.

TABLE III. Group A inspection for device types 01.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
Inputs not designed are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case V, Z, U	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Meas. terminal	Test limits		
			Case Y	2	3	4	5	6	7	8	11	12	13	14	15	16	17	21	22	23	24		Min	Max	Unit
			Test No.	A6	A5	A4	A3	A0	A1	A2	$\overline{CE}_1$	GND	$\overline{CE}_2$	O4	O3	O2	O1	A9	A8	A7	V_{CC}				
1 T_C = 25°C	V_{IC}		1	-12 mA								"									4.5 V	A6		-1.5	V
			2		-12 mA							"									"	A5		"	"
			3			-12 mA						"									"	A4		"	"
			4				-12 mA					"									"	A3		"	"
			5					-12 mA				"									"	A0		"	"
			6						-12 mA			"									"	A1		"	"
			7							-12 mA		"									"	A2		"	"
			8								-12 mA	"									"	$\overline{CE}_1$		"	"
			9									"	-12 mA								"	$\overline{CE}_2$		"	"
			10									"						-12 mA			"	A9		"	"
			11									"							-12 mA		"	A8		"	"
			12									"								-12 mA	"	A7		"	"
	V_{OL}	3007	13	5/, 9/	9/	9/	9/	9/	9/	8/, 9/	0.8 V	"	0.8 V	16 mA	18/	18/	18/	8/, 9/	9/	9/	"	O4		0.5	"
			14	"	"	"	"	"	"	"	"	"	"	18/	16 mA			"	"	"	"	O3		"	"
			15	"	"	"	"	"	"	"	"	"	"			16 mA		"	"	"	"	O2		"	"
			16	"	"	"	"	"	"	"	"	"	"				16 mA	"	"	"	"	O1		"	"
	I_{IL}	3009	17	0.5 V								"									5.5 V	A6	-1.0	-250	µA
			18		0.5 V							"									"	A5	"	"	"
			19			0.5 V						"									"	A4	"	"	"
			20				0.5 V					"									"	A3	"	"	"
			21					0.5 V				"									"	A0	"	"	"
			22						0.5 V			"									"	A1	"	"	"
			23							0.5 V		"									"	A2	"	"	"
			24								0.5 V	"									"	$\overline{CE}_1$	"	"	"
			25									"	0.5 V								"	$\overline{CE}_2$	"	"	"
			26									"						0.5 V			"	A9	"	"	"
			27									"							0.5 V		"	A8	"	"	"
			28									"								0.5 V	"	A7	"	"	"
	I_{IH1}	3010	29	5.5 V								"									"	A6		50	"
			30		5.5 V							"									"	A5		"	"
			31			5.5 V						"									"	A4		"	"
			32				5.5 V					"									"	A3		"	"
			33					5.5 V				"									"	A0		"	"
			34						5.5 V			"									"	A1		"	"
			35							5.5 V		"									"	A2		"	"
			36								5.5 V	"									"	$\overline{CE}_1$		"	"
			37									"						5.5 V			"	A9		"	"
			38									"							5.5 V		"	A8		"	"
			39									"								5.5 V	"	A7		"	"
	I_{IH2} 16/		40									"	4.5 V								"	$\overline{CE}_2$		100	"
	I_{CEX}		41								5.5 V	"	5.5 V	5.2 V							"	O4		"	"
			42								"	"	"		5.2 V						"	O3		"	"
			43								"	"	"			5.2 V					"	O2		"	"
			44								"	"	"				5.2 V				"	O1		"	"
	I_{CC}	3005	45	GND	GND	GND	GND	GND	GND	GND	GND	"	GND					GND	GND	GND	"	V_{CC}		140	mA
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																								
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																								
7 T_C = +25°C	Func-tional tests		1/ 46	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	O4		1/	
"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	O3		"	
"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	O2		"	
"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	O1		"	

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 – Continued.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
Inputs not designed are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case V, Z, U	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Meas. terminal	Test limits		
			Case Y	2	3	4	5	6	7	8	11	12	13	14	15	16	17	21	22	23	24				
			Test No.	A6	A5	A4	A3	A0	A1	A2	$\overline{CE}_1$	GND	$\overline{CE}_2$	O4	O3	O2	O1	A9	A8	A7	V_{CC}		Min	Max	Unit
8	Same tests, terminal conditions, and limits as subgroup 7, except T_C = +125ºC and -55ºC.																								
9 T_C = +25°C	t_{PLH1}	GALPAT Fig. 5	47	2/	2/	2/	2/	2/	2/	2/	GND	GND	GND	4/	4/	4/	4/	2/	2/	2/	2/	Outputs		85	17/ ns
"	t_{PHL1}	GALPAT Fig. 5	48	2/	2/	2/	2/	2/	2/	2/	GND	"	GND	"	"	"	"	2/	2/	2/	2/	"		85	" "
"	t_{PLH2}	Sequential Fig. 5	49	3/	3/	3/	3/	3/	3/	3/	3/	"	3/	"	"	"	"	3/	3/	3/	3/	"		40	" "
"	t_{PHL2}	Sequential Fig. 5	50	3/	3/	3/	3/	3/	3/	3/	3/	"	3/	"	"	"	"	3/	3/	3/	3/	"		40	" "
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = +125°C.																								
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																								

See footnotes at end of table.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
Inputs not designed are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case V, Z, U	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Meas. terminal	Test limits		
			Case Y	2	3	4	5	6	7	8	11	12	13	14	15	16	17	21	22	23	24		Min	Max	Unit
			Test No.	A6	A5	A4	A3	A0	A1	A2	$\overline{CE}_1$	GND	$\overline{CE}_2$	O4	O3	O2	O1	A9	A8	A7	V_{CC}				
1 T_C = 25°C	V_{IC}		1	-12 mA								"									4.5 V	A6		-1.5	V
			2		-12 mA							"									"	A5		"	"
			3			-12 mA						"									"	A4		"	"
			4				-12 mA					"									"	A3		"	"
			5					-12 mA				"									"	A0		"	"
			6						-12 mA			"									"	A1		"	"
			7							-12 mA		"									"	A2		"	"
			8								-12 mA	"									"	$\overline{CE}_1$		"	"
			9									"	-12 mA								"	$\overline{CE}_2$		"	"
			10									"						-12 mA			"	A9		"	"
			11									"							-12 mA		"	A8		"	"
			12									"								-12 mA	"	A7		"	"
	V_{OL}	3007	13	5/, 9/, 14/	9/, 14/	9/, 14/	9/, 14/	9/, 14/	5/, 9/, 14/	8/, 9/, 14/	0.8 V	"	0.8 V	16 mA 18/	18/	18/	18/	8/, 9/, 14/	9/, 14/	9/, 14/	"	O4		0.5	"
			14								"	"	"		16 mA			"	"	"	"	O3		"	"
			15								"	"	"			16 mA		"	"	"	"	O2		"	"
			16								"	"	"				16 mA	"	"	"	"	O1		"	"
	V_{OH}	3006	17	9/, 12/	9/, 10/	12/	9/, 12/	9/, 12/	9/, 12/	9/, 10/	"	"	"	-2 mA				7/, 9/, 12/	9/, 12/	6/, 9/, 12/	"	O4	2.4		"
			18			11/					"	"	"		-2 mA			"	"	"	"	O3	"		"
			19			12/					"	"	"			-2 mA		"	"	"	"	O2	"		"
			20			11/					"	"	"				-2 mA	"	"	"	"	O1	"		"
	I_{IL}	3009	21	0.5 V								"									5.5 V	A6	-1.0	-250	µA
			22		0.5 V							"									"	A5	"	"	"
			23			0.5 V						"									"	A4	"	"	"
			24				0.5 V					"									"	A3	"	"	"
			25					0.5 V				"									"	A0	"	"	"
			26						0.5 V			"									"	A1	"	"	"
			27							0.5 V		"									"	A2	"	"	"
			28								0.5 V	"									"	$\overline{CE}_1$	"	"	"
			29									"	0.5 V								"	$\overline{CE}_2$	"	"	"
			30									"						0.5 V			"	A9	"	"	"
			31									"							0.5 V		"	A8	"	"	"
			32									"								0.5 V	"	A7	"	"	"
	I_{IH1}	3010	33	5.5 V								"									"	A6		50	"
			34		5.5 V							"									"	A5		"	"
			35			5.5 V						"									"	A4		"	"
			36				5.5 V					"									"	A3		"	"
			37					5.5 V				"									"	A0		"	"
			38						5.5 V			"									"	A1		"	"
			39							5.5 V		"									"	A2		"	"
			40								5.5 V	"									"	$\overline{CE}_1$		"	"
			41									"						5.5 V			"	A9		"	"
			42									"							5.5 V		"	A8		"	"
			43									"								5.5 V	"	A7		"	"
	I_{IH2} 13/		44									"	4.5 V								"	$\overline{CE}_2$		100	"
	I_{OLZ}		45								5.5 V 16/	"	5.5 V 16/	0.5 V							"	O4		-100	"
			46								"	"	"		0.5 V						"	O3		"	"
			47								"	"	"			0.5 V					"	O2		"	"
			48								"	"	"				0.5 V				"	O1		"	"
	I_{OHZ}		49								"	"	"	5.2 V							"	O4		100	"
			50								"	"	"		5.2 V						"	O3		"	"
			51								"	"	"			5.2 V					"	O2		"	"
			52								"	"	"				5.2 V				"	O1		"	"
	I_{CC}	3005	53	GND	GND	GND	GND	GND	GND	GND	GND	"	GND					GND	GND	GND	"	V_{CC}		140	mA

See footnotes at end of table.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
Inputs not designed are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case V, Z, U	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Meas. terminal	Test limits		
			Case Y	2	3	4	5	6	7	8	11	12	13	14	15	16	17	21	22	23	24				
			Test No.	A6	A5	A4	A3	A0	A1	A2	$\overline{CE}_1$	GND	$\overline{CE}_2$	O4	O3	O2	O1	A9	A8	A7	V_{CC}		Min	Max	Unit
1 T_C = 25°C	I_{OS}	3011	54	9/, 12/	9/, 10/	9/, 12/	9/, 12/	9/, 12/	9/, 12/	9/, 10/	0.5 V	GND	0.5 V	GND				7/, 9/	9/, 12/	6/, 9/	"	O4	-10	-100	mA
			55	"	"	11/	"	"	"	"	"	"	"		GND			12/		12/	"	O3	"	"	"
			56	"	"	12/	"	"	"	"	"	"	"			GND					"	O2	"	"	"
			57	"	"	11/	"	"	"	"	"	"	"				GND				"	O1	"	"	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125ºC and V_{IC} tests are omitted.																								
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																								
7 T_C = +25°C	Func-tional tests	1/	58	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	Outputs		1/	ns
8	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55ºC.																								
9 T_C = +25°C	t_{PLH1}	GALPAT Fig. 5	59	2/	2/	2/	2/	2/	2/	2/	GND	GND	GND	4/	4/	4/	4/	2/	2/	2/	2/	Outputs		15/ 17/	ns
	t_{PHL1}	GALPAT Fig. 5	60	2/	2/	2/	2/	2/	2/	2/	GND	"	GND	"	"	"	"	2/	2/	2/	2/	"		"	"
	t_{PLH2}	Sequential Fig. 5	61	3/	3/	3/	3/	3/	3/	3/	3/	"	3/	"	"	"	"	3/	3/	3/	3/	"		"	"
	t_{PHL2}	Sequential Fig. 5	62	3/	3/	3/	3/	3/	3/	3/	3/	"	3/	"	"	"	"	3/	3/	3/	3/	"		"	"
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = +125°C.																								
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																								

See footnotes at end of table.

TABLE III. Group A inspection for device types 03.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
Inputs not designed are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 A6	2 A5	3 A4	4 A3	5 A0	6 A1	7 A2	8 GND	9 O4	10 O3	11 O2	12 O1	13 A9	14 A8	15 A7	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 T_C = +25°C	V_{IC}		1	-12 mA							GND								4.5 V	A6		-1.5	V
			2		-12 mA						"								"	A5		"	"
			3			-12 mA					"								"	A4		"	"
			4				-12 mA				"								"	A3		"	"
			5					-12 mA			"								"	A0		"	"
			6						-12 mA		"								"	A1		"	"
			7							-12 mA	"								"	A2		"	"
			8								"					-12 mA			"	A9		"	"
			9								"						-12 mA		"	A8		"	"
			10								"							-12 mA	"	A7		"	"
	V_{OL}	3007	11	5/, 9/	9/	9/	9/	9/	9/	9/	"	16 mA	18/	18/	18/	9/	9/	9/	"	O4		0.5	"
			12	"	"	"	"	"	"	"	"	18/	16 mA			"	"	"	"	O3		"	"
			13	"	"	"	"	"	"	"	"			16 mA		"	"	"	"	O2		"	"
			14	"	"	"	"	"	"	"	"				16 mA	"	"	"	"	O1		"	"
	V_{OH}	3006	15	9	"	"	"	"	"	"	"	-2 mA				"	"	"	"	O4	2.4		"
			16	"	"	"	"	"	"	"	"		-2 mA			"	"	"	"	O3	"		"
			17	"	"	"	"	"	"	"	"			-2 mA		"	"	"	"	O2	"		"
			18	"	"	"	"	"	"	"	"				-2 mA	"	"	"	"	O1	"		"
	V_{IL}	3009	19	0.5 V							"								5.5 V	A6	-1.0	-250	µA
			20		0.5 V						"								"	A5	"	"	"
			21			0.5 V					"								"	A4	"	"	"
			22				0.5 V				"								"	A3	"	"	"
			23					0.5 V			"								"	A0	"	"	"
			24						0.5 V		"								"	A1	"	"	"
			25							0.5 V	"								"	A2	"	"	"
			26								"					0.5 V			"	A9	"	"	"
			27								"						0.5 V		"	A8	"	"	"
			28								"							0.5 V	"	A7	"	"	"
	I_{IH}	3010	29	5.5 V							"								"	A6		50	"
			30		5.5 V						"								"	A5		"	"
			31			5.5 V					"								"	A4		"	"
			32				5.5 V				"								"	A3		"	"
			33					5.5 V			"								"	A0		"	"
			34						5.5 V		"								"	A1		"	"
			35							5.5 V	"								"	A2		"	"
			36								"					5.5 V			"	A9		"	"
			37								"						5.5 V		"	A8		"	"
			38								"							5.5 V	"	A7		"	"
	I_{CC}	3005	39	GND	GND	GND	GND	GND	GND	GND	"					GND	GND	GND		V_{CC}		140	mA
	I_{OS}	3011	40	9/	9/	9/	9/	9/	9/	9/	"	GND				9/	9/	9/		O4	-10	-100	"
			41	"	"	"	"	"	"	"	"		GND			"	"	"		O3	"	"	"
			42	"	"	"	"	"	"	"	"			GND		"	"	"		O2	"	"	"
			43	"	"	"	"	"	"	"	"				GND	"	"	"		O1	"	"	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125ºC and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																						
7 T_C = 25°C	Functional tests	1/	44	1/	1/	1/	1/	1/	1/	1/	GND	GND	1/	1/	1/	1/	1/	1/	1/	Outputs		1/	

See footnotes at end of table.

TABLE III. Group A inspection for device types 03 - Continued.
Terminal conditions (outputs not designated are open or resistive, coupled to GND or voltage;
Inputs not designed are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 A6	2 A5	3 A4	4 A3	5 A0	6 A1	7 A2	8 GND	9 O4	10 O3	11 O2	12 O1	13 A9	14 A8	15 A7	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
8	Same tests, terminal conditions and limits as for subgroup 7, except T_C = +125ºC and -55ºC.																						
9 T_C = +25°C	t_{PLH1}	See Fig 5	45	2/	2/	2/	2/	2/	2/	2/	GND	4/	4/	4/	4/	2/	2/	2/	2/	Outputs		85	ns
	t_{PHL2}	See Fig 5	46	2/	2/	2/	2/	2/	2/	2/	GND	4/	4/	4/	4/	2/	2/	2/	2/	Outputs		85	ns
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = +125°C.																						
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																						

See footnotes at end of table.

1/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the truth table specified in the altered item drawing exists for programmed devices (see 3.3.2). All bits shall be tested. Terminal conditions shall be as follows:

a. Inputs: H = 3.0 V, L = 0.0 V.
b. Outputs:
   H ≥ 1.0 V and L ≤ 1.0 V.
c. The functional tests shall be performed with V_{CC} = 4.5 and V_{CC} = 5.5 V.

2/ GALPAT (PROGRAMMED PROM)

This program will test all bits in the array, the addressing and interaction between bits for ac performance t_{PLH1}. Each bit in the pattern is fixed by being programmed with a “H” and “L”.

Description:

1. Word 0 is read.
2. Word 1 is read.
3. Word 0 is read
4. Word 2 is read.
5. Word 0 is read.
6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 1023 is reached, then increments to the next word and reads back and forth as in steps 1 through 6 shall include all words.
7. Pass execution time = $(n^2 + n)$ x cycle time. N = 1024.
8. The GALPAT tests shall be performed with V_{CC} = 4.5 and 5.5 V.

3/ SEQUENTIAL TEST (PROGRAMMED PROM)

This program will test all bits in the array for t_{PHL2} and t_{PLH2}.

Description

1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
2. Each 0 is addressed. Enable line is pulled HI to LO and LO to HI. t_{PHL2} and t_{PLH2} are read.
3. Word 1 is addressed. Same enable sequence as above.
4. The reading procedure continues until word 1023 is reached.
5. Pass execution time = 1024 x cycle time.
6. The sequential tests shall be performed with V_{CC} = 4.5 and 5.5 V.

4/ The outputs are loaded per figure 6.

5/ For unprogrammed devices (circuit A), apply 11.0 V on pin 1 (A_6) for device types 01 and 03. Apply 11.0 V on pin 1 (A_6) for device type 02 with date codes prior to 8225, and apply 13.0 V on pin 1 (A_6) for device type 02 with date codes after and including 8226.

6/ For unprogrammed devices, apply 12.0 V on pin 17 (A_7) for circuit B devices.

7/ For unprogrammed 02 devices, apply 10.0 V on pin 17 (A_7), apply 0.5 V on pins 3, 2, 1, 16, 15 (A_4, A_5, A_6, A_8, A_9) and 5.0 V on all other addresses for circuit C.

8/ For unprogrammed devices, apply 12.0 V on terminals A_2 and A_9 for circuit D devices.

9/ For programmed devices, select an appropriate address to acquire the desired output state. V_{IH} = 2.0 V, V_{IL} = 0.8 V.

10/ For uprogrammed devices, apply 10.5 V on A_2 and A_5 for circuit G devices.

11/ For unprogrammed devices, apply 0 V on this pin for circuit G devices.

12/ For unprogrammed devices, apply 3 V on this pin for circuit G devices.

13/ At the manufacturer's option, this may be performed with V_{IH} = 5.5 and test limits of 50 μA maximum.

14/ For unprogramed 04 devices, apply 10.0 V on pin 17 (A_7), apply 0.5 V on pins 1, 2, 3, 15, 16, (A_4, A_5, A_6, A_8, A_9) and 5.0 V on all other addresses for circuit C.

15/ The limits shall be as follows:

Device	02 (ns)	04 (ns)
t_{PLH1}	85	55
t_{PHL1}	85	55
t_{PLH2}	40	35
t_{PHL2}	40	35

16/ For circuit B devices apply 2.4 V.

17/ For circuit B devices, type 01 and 02, t_{PHL1}, t_{PLH1} = 70 ns and t_{PHL2}, t_{PLH2} = 30 ns.

18/ I_{OL} = 8 mA for circuit A only.

TABLE IVA. Programming characteristics for circuit A.

Parameter	Symbol	Limits 1/			Unit
		Min	Rec	Max	
Address input voltage 2/	V_{IH} V_{IL}	2.4 0.0	5.0 0.4	5.0 0.5	V V
Programing Voltage to V_{CC} low Program verify Verify voltage	V_{PH} 3/ V_{PL} V_{PHV} V_R 4/	10.75 0.0 --- 4.5	11.0 0.0 5.5 ---	11.25 1.5 --- 5.5	“ “ “ “
Programming input low current at V_{PH}	I_{ILP}	---	-300	-600	µA
Programmed voltage (V_{CC}) transition time	t_{TLH} t_{THL}	1 1	5 5	10 10	µs “
Programming delay	t_{D1} t_{D2}	10 1	10 5	20 5	“
Programming pulse width	t_P 5/	90	100	110	“
Programming duty cycle	PDC	---	30	60	%
Output voltage Enable Disable	 V_{OPE} 6/ V_{OPD}	 10.5 0.0	 10.5 5.0	 11.0 5.5	 V V

During the programming the chip must be disabled for proper operation.

1/ T_C = +25°C.

2/ No inputs should be left open for V_{IH}.

3/ V_{PH} source must be capable of supplying one ampere.

4/ It is recommended that post programming dual verification be made at V_R minimum and V_R maximum.

5/ Note setup j in programming procedure.

6/ V_{OPE} source must be capable of supplying 10 mA minimum.

TABLE IVB. Programming characteristics for circuit B.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Rec	Max	
V_{CC} required during programming	V_{CCP}		11.5	11.75	12.0	V
V_{OUT} current limit during programming	I_{OP}		20	25	30	mA
Output programming voltage	V_{OUT}		10.5	11.0	11.5	V
Pulse width of programming voltage	t_P		9	10	11	µs
Programming delay	t_D		0	1	10	µs
V_{CCP} or V_{OUT} transition time	t_{TLH}	Rise time of V_{CC} or V_{OUT}	1	5	10	v/µs
V_{CCP} current	I_{CCP}		800	1200		mA
Low V_{CC} for verification	V_{CCL}		4.2	4.3	4.4	V
High V_{CC} for verification	V_{CCH}		5.8	6.0	6.2	V
Address input voltage	V_{IH}		2.4	3.0	5.5	V
	V_{IL}		0.0	0.0	0.5	V
Maximum duty cycle during automatic programming of program pin and output pin	D. C.	t_P/ t_C	---	25	25	%

1/ T_A = +25°C.

TABLE IVC. Programming characteristics for circuit C.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Rec	Max	
Programming voltage	V_{CCP} 1/	I_{CCP} = 375 ±75 mA Transient or steady-state	8.5	8.75	9.0	V
Verificaiton upper limit	V_{CCH}		5.3	5.5	5.7	V
Verificaiton lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S 2/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	V_{CCP} = +8.75 ±.25 V	300	375	450	mA
Input voltage high level "1"	V_{IH}		2.4		5.5	V
Input voltage low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	V_{IH} = +5.5 V			50	µA
Input current	I_{IL}	V_{IL} = +0.4 V			-500	µA
Output programming voltage	V_{OUT} 3/	I_{OUT} = 200 ±20 mA Transient or steady-state	16	17	18	V
Output programming current	I_{OUT}	V_{OUT} = +17 ±1 V	180	200	220	mA
Output pulse transition	t_{TLH}		10		50	µs
CE programming pulse width	t_P		0.3	0.4	0.5	ms
Pulse sequence delay	t_D		10			µs

1/ Bypass V_{CC} to GND with a 0.01 µF capacitor to reduce voltage spikes.

2/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 ±1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

TABLE IVD. Programming characteristics for circuit D.

Parameter	Symbol	Conditions 1/	Limits 1/			Unit
			Min	Rec	Max	
V_{CC} required during programming	V_{CCP}		4.75	5.0	5.25	V
Verification V_{CC} read	V_{CCL}	Programming read verify	4.2	4.4	5.0	V
Input voltage high level "1"	V_{IH}	Do not leave inputs open	2.4	5.0	5.0	V
Input voltage low level "0"	V_{IL}	Do not leave inputs open	0	0	0.4	V
Chip enable	CE1, CE2	Pin 8 or 10 or both	2.4	5.0	5.0	V
Output programming voltage	V_{OUT}	Applied to ouput to be programmed	20	20.5	21	V
Output programming current	I_{OUT}	If pulse generator is used, set current limit to the max value			100	mA
Programming voltage transition time	t_{TLH}		0.5	1.0	3.0	µs
Programming pulse width	t_P		50	100	180	µs
Programming duty cycle	D. C.	Maximum duty cycle to maintain T_C < +85°C		20	20	%
Required delay between disabling memory output and application of output programming pulse	t_D		30			ns

1/ Recommended T_C = +25°C; maximum T_C = +85°C.

4.8 Programming procedure for circuit B. The programming characteristics in table IVB and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 6B and the programming characteristics of table IVB shall apply to these procedures.

b. Apply V_{IH} to $\overline{CE}_1$ and the binary address of the PROM word to be programmed. Raise V_{CC} to V_{CCP}.

c. After a t_D delay, apply only one V_{OP} to the output to be programmed high. Apply V_{op} to one output at a time.

d. After a t_D delay, a pulse $\overline{CE}_1$ to a V_{IL} level for a duration of t_P.

e. After t_P and a t_D delay, remove V_{OP} from the programmed output.

f. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OP} pulses to each output to be programmed and pulsing $\overline{CE}_1$ to the V_{IL} level, allowing for proper delays between V_{OP} and $\overline{CE}_1$.

g. Repeat 4.8b through 4.8e for all bits to be programmed.

h. To verify programming, lower V_{CCP} to V_{CC}. Connect a 10 kΩ resistor between each output and V_{CC}. Apply V_{IL} to $\overline{CE}_1$ inputs. The programmed outputs should remain in the high state and the unprogrammed outputs should go to the low level.

i. If any bit does not verify as programmed, it shall be considered a programming reject.

4.9 Programming procedures for circuit C. The programming characteristics in table IVC and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms on the figure 6C and the programming characteristics of table IVC shall apply to these procedures.

b. Terminate all device outputs with a 10 kΩ resistor to V_{CC}.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a t_D delay (10μs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.

e. After a t_D delay (10μs), pulse both CE inputs to "0" for a duration of t_P.

f. After a t_D delay (10μs), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 6C.

h. Repeat steps b through g for all other bits to be programmed.

i. To verify programming, after t_D (10 μs) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to both CE inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.

j. If any bit does not veify as programmed it shall be considered a programming reject.

4.10 Programming procedure for circuit D. The programming characteristics in table IVD and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 6D and the programming characteristics in table IVD shall apply to these procedures.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

c. Disable the chip by applying V_{IH} to the CE inputs. The CE inputs are TTL compatible.

d. After a delay of t_D, apply only one V_{OUT} pulse with a duration of t_p to the ouput selected for programming. The other outputs may be left open or tied to V_{IH}. The outputs shall be programmed one output at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

e. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

f. Repeat steps b through e for all other bits to be programmed.

g. Enable the chip by applying V_{IL} to the CE inputs and verify the program.

h. If any bit does not verify as programmed, it shall be considered a programming reject.

4.11 Programming procedure for circuit G. The programming characteristics on table IVG and the following procedures shall be used for programming.

a. Connect the device in the electrical configuration of programming. The waveforms on figure 6G and the programming characteristics of table IVG shall apply to these procedures.

b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and Enable inputs must be driven with TTL logic levels during programming and verification.

c. Increase V_{CC} from nominal to V_{CCP} (10.5 ±0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.

d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ±0.5 V). Limit the slew rate to I_{RR} (1.0 to 10.0 V/μs). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP}, but must precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum (remember that the outputs of the device are disabled at this time).

e. Enable the device by taking the chip enable(s) to a low level. This is done with a pulse PWE for 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 V (±0.25 V). The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.

g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of step f is to be performed at a V_{CC} level of 4.0 volt (±0.2 V). V_{OH}, during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.

h. Repeat steps 4.11b through 4.11f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

i. If any bit does not verify as programmed it shall be considered a programming reject.

TABLE IVG. Programming characteristics for circuit G.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Rec	Max	
V_{CC} required during programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	V_{CC} = 11 V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	V_{OUT} = 11 V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/µs
Programming pulse width (Enabled)	PWE		9	10	11	µs
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address set-up time	T_1		100			ns
V_{CCP} set-up time	T_2	2/	5			ns
V_{CCP} hold time	T_5		100			ns
V_{OP} set-up time	T_3		100			ns
V_{OP} hold time	T_4		100			ns

1/ T_A = +25°C.

2/ V_{CCP} set-up time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP}.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirement for programming the device, including processing option. The device may be programmed pre- or post-burn-in, if applicable.

j. Requirements for "JAN" marking.

k. Packaging Requirements (see 5.1)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND ..... Ground zero voltage potential.
V_{IN} ..... Voltage level at an input terminal
V_{IC} ..... Input clamp voltage
I_{IN} ..... Current flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.4). Longer length leads and lead forming should not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry Type	Circuit Designator	Fusible Links
01	54S572 / National Semiconductor	G	TiW
01 1/	7642 / Harris Semiconductor	A	NiCr
01	53S440 / Monolithic Memories	B	TiW
01 1/	82S136 / Signetics Corporation	C	NiCr
01	93452 / Fairchild Semiconductor	D	NiCr
02	7643 / Harris Semiconductor	A	NiCr
02	53S441 / Monolithic Memories	B	TiW
02, 04	82S137A / Signetics Corporation	C	NiCr
02	93453 / Fairchild Semiconductor	D	NiCr
02	54S573 / National Semiconductor	G	TiW / W
03 1/	7644 / Harris Semiconductor	A	NiCr

1/ This generic-industry type is no longer manufactured.

6.8 Change from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

Review activities:
Army – SM, MI
Navy - AS, CG, MC, SH TD
Air Force – 03, 19, 99

(Project 5962-2108)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.