

DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks

MT41J256M8 – 32 Meg x 8 x 8 Banks

MT41J128M16 – 16 Meg x 16 x 8 Banks

Features

- $V_{DD} = V_{DDQ} = +1.5V \pm 0.075V$
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- CAS (READ) latency (CL): 5, 6, 7, 8, 9, 10, or 11
- POSTED CAS ADDITIVE latency (AL): 0, CL - 1, CL - 2
- CAS (WRITE) latency (CWL): 5, 6, 7, 8, based on t_{CK}
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
 - 64ms, 8,192 cycle refresh at 0°C to 85°C
 - 32ms at 85°C to 95°C
- Clock frequency range of 300–800 MHz
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options¹

- Configuration
 - 512 Meg x 4
 - 256 Meg x 8
 - 128 Meg x 16
- FBGA package (Pb-free) - x4, x8
 - 78-ball (9mm x 11.5mm) Rev. D, F
 - 82-ball (12.5mm x 15.5mm) Rev. A
- FBGA package (Pb-free) - x16
 - 96-ball (9mm x 14mm) Rev. D
- Timing - cycle time
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.25ns @ CL = 10 (DDR3-1600)
 - 1.5ns @ CL = 10 (DDR3-1333)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.87ns @ CL = 8 (DDR3-1066)
 - 1.87ns @ CL = 7 (DDR3-1066)
- Operating temperature
 - Commercial (0°C ≤ T_C ≤ 95°C)
 - Industrial (-40°C ≤ T_C ≤ 95°C)
- Revision

Marking

512M4
256M8
128M16

HX
JE

HA

-125
-125E
-15
-15E
-187
-187E

None
IT

:A/:D/:F

Notes: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for available offerings.

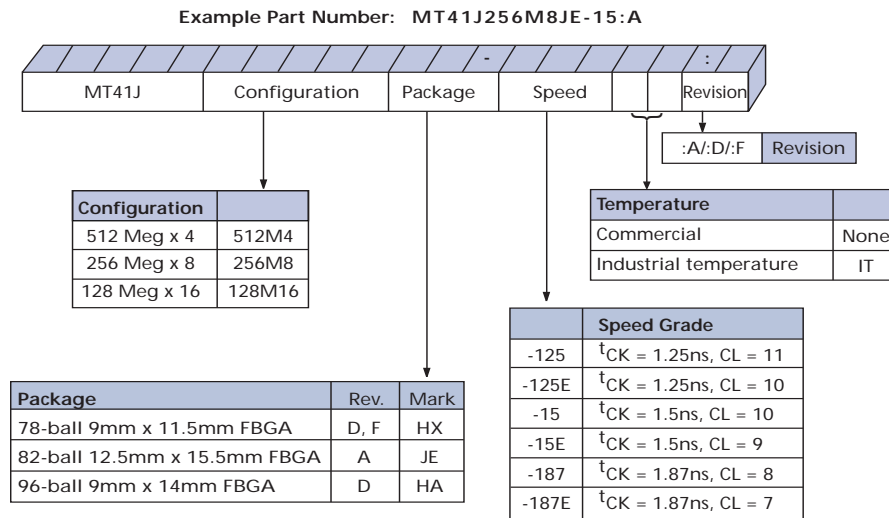
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target t_{RCD} - t_{RP} -CL	t_{RCD} (ns)	t_{RP} (ns)	CL (ns)
-125	1600	11-11-11	13.75	13.75	13.75
-125E	1600	10-10-10	12.5	12.5	12.5
-15	1333	10-10-10	15	15	15
-15E	1333	9-9-9	13.5	13.5	13.5
-187	1066	8-8-8	15	15	15
-187E	1066	7-7-7	13.1	13.1	13.1

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	32K (A[14:0])	32K (A[14:0])	16K (A[13:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])

Figure 1: 2Gb DDR3 Part Numbers



Notes: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: www.micron.com.

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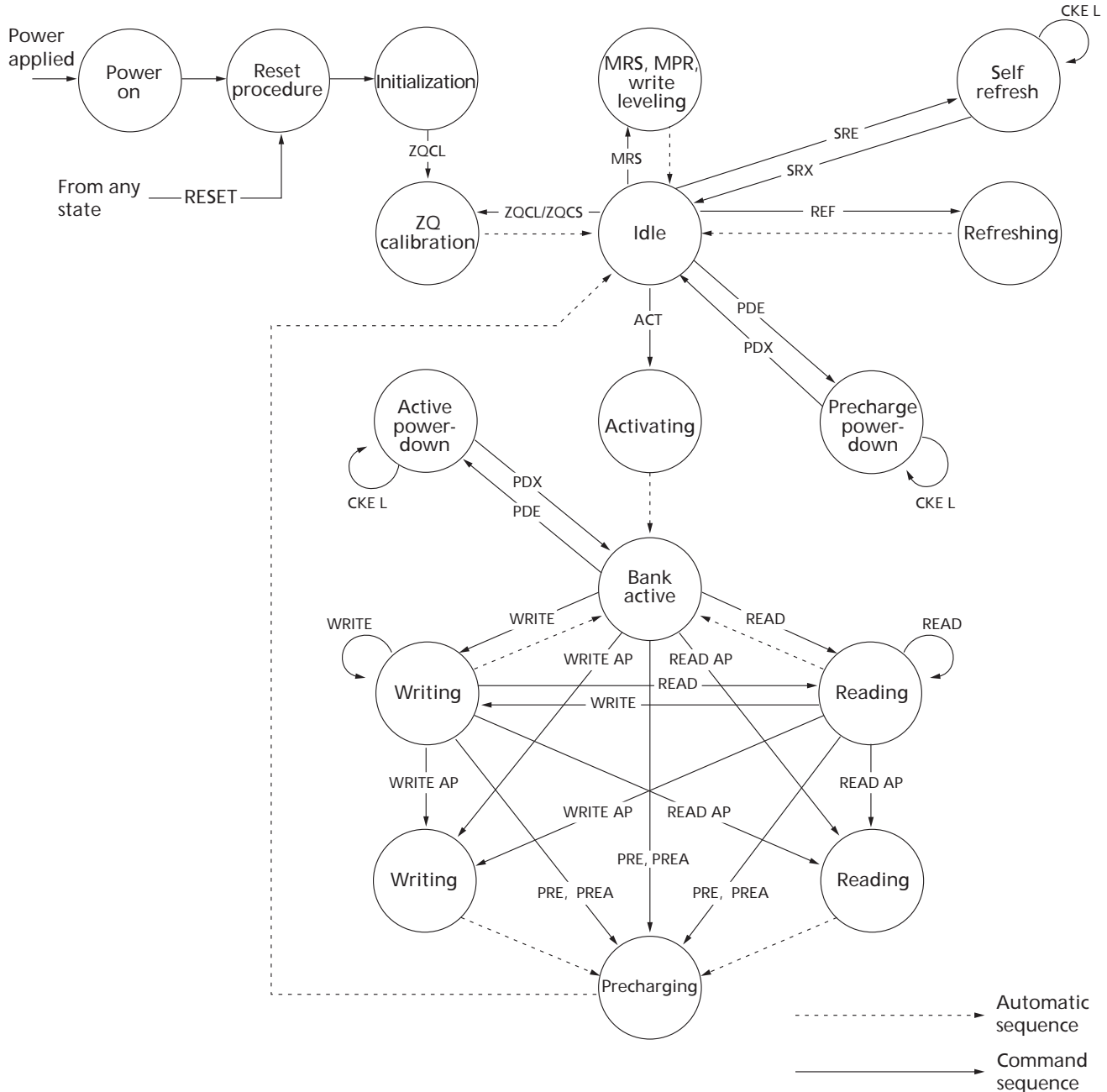
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State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVATE
 MPR = Multipurpose register
 MRS = Mode register set
 PDE = Power-down entry
 PDX = Power-down exit
 PRE = PRECHARGE

PREA = PRECHARGE ALL
 READ = RD, RDS4, RDS8
 READ AP = RDAP, RDAPS4, RDAPS8
 REF = REFRESH
 RESET = START RESET PROCEDURE
 SRE = Self refresh entry

SRX = Self refresh exit
 WRITE = WR, WRS4, WRS8
 WRITE AP = WRAP, WRAPS4, WRAPS8
 ZQCL = ZQ LONG CALIBRATION
 ZQCS = ZQ SHORT CALIBRATION

Functional Description

The DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITES. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM use READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

Industrial Temperature

The industrial temperature (IT) device requires the case temperature not exceed -40°C or $+95^{\circ}\text{C}$. JEDEC specifications require the refresh rate to double when T_C exceeds $+85^{\circ}\text{C}$; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when the T_C is $< 0^{\circ}\text{C}$ or $> +95^{\circ}\text{C}$.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms “DQS” and “CK” found throughout the data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated herewithin is considered undefined, illegal, and not supported and can result in unknown operation.
- Row addressing is denoted as $A[n:0]$ (2Gb: $n = 13$ [x16] and 2Gb: $n = 14$ [x4, x8]).

Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3: 512 Meg x 4 Functional Block Diagram

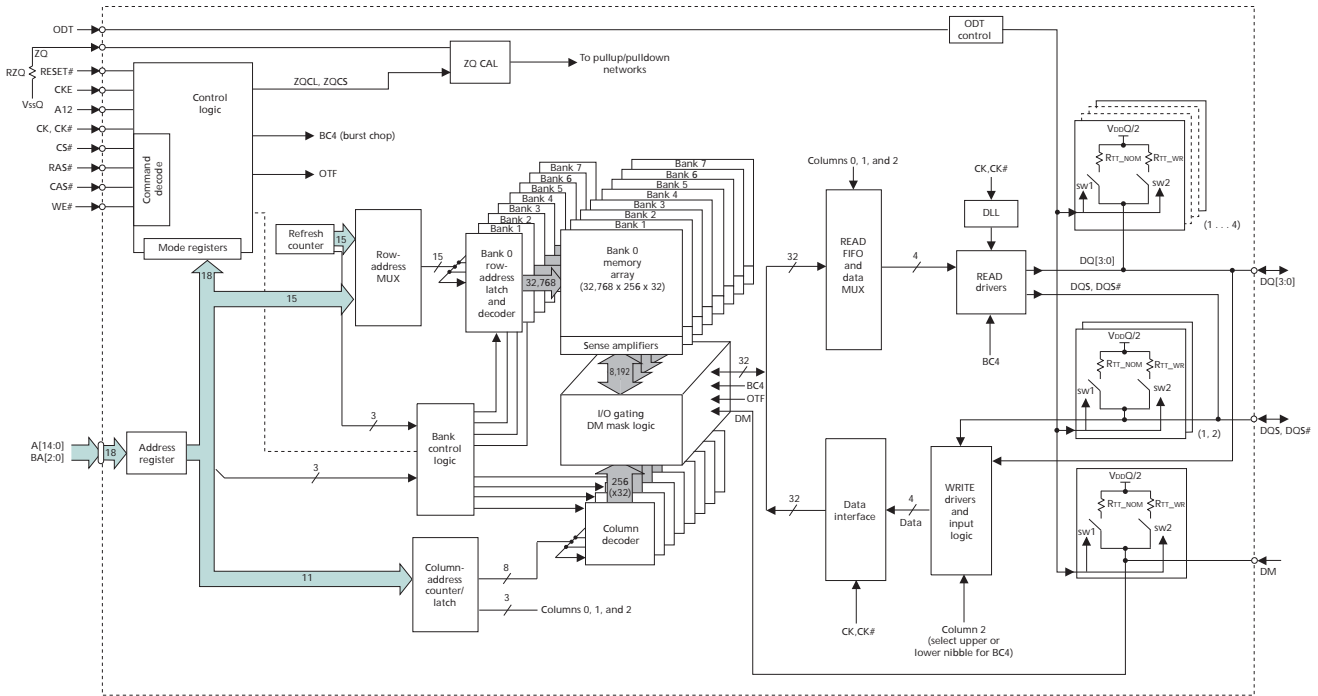


Figure 4: 256 Meg x 8 Functional Block Diagram

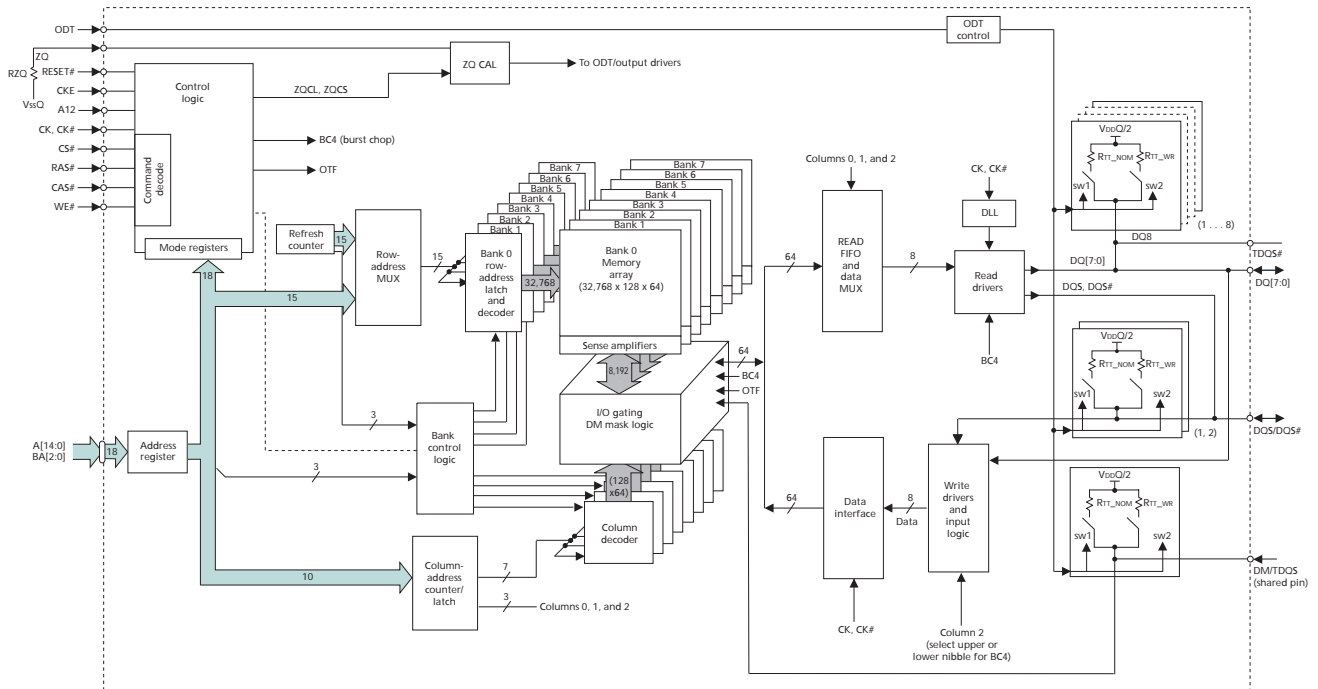
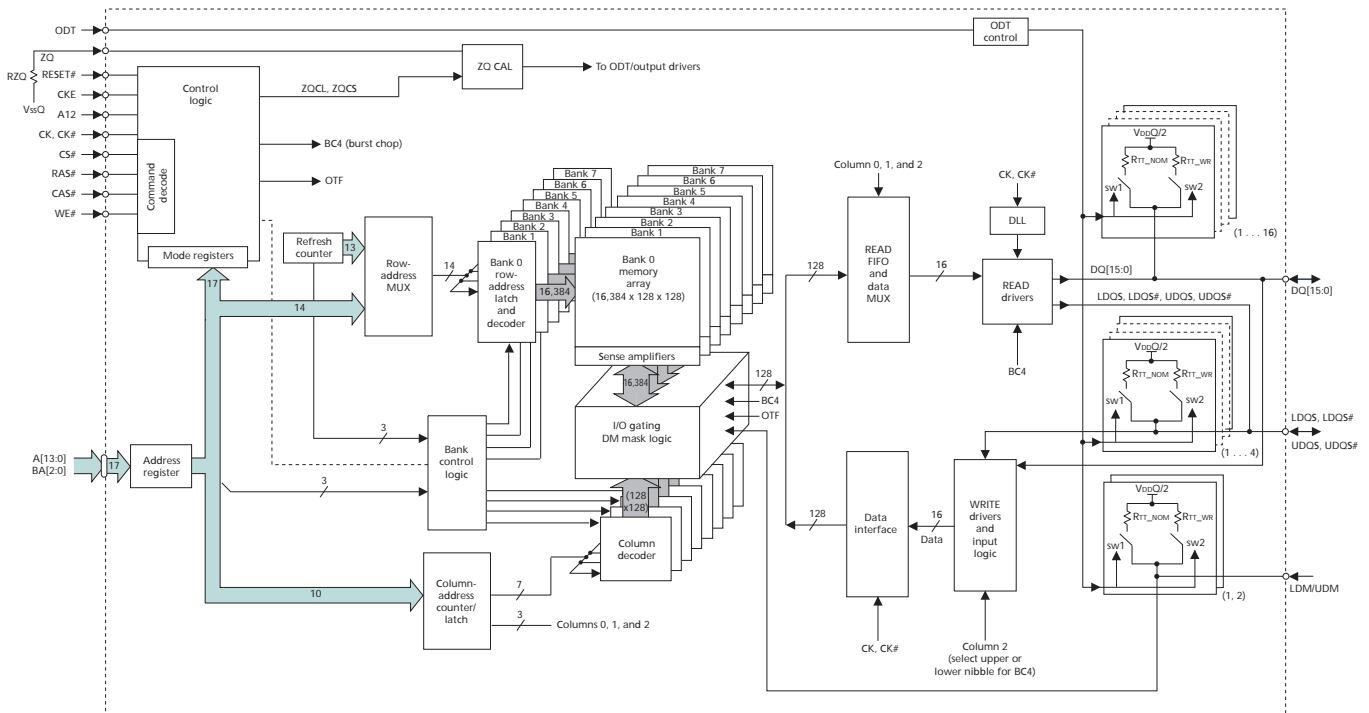


Figure 5: 128 Meg x 16 Functional Block Diagram



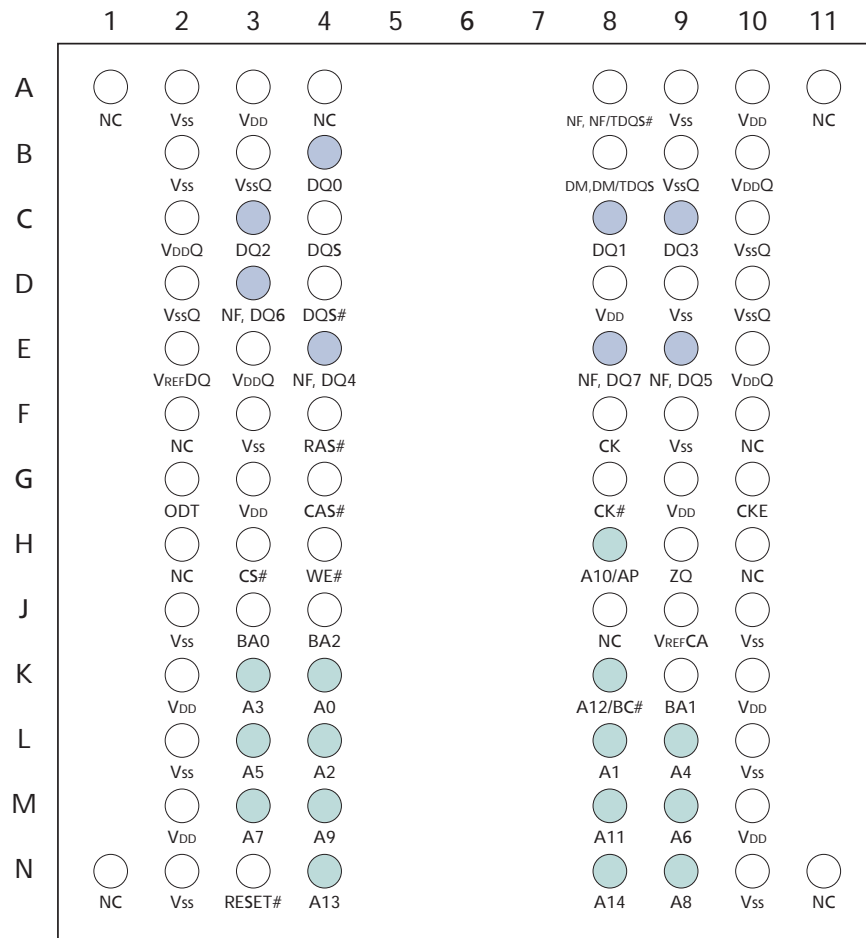
Ball Assignments and Descriptions

Figure 6: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	V _{SS}	V _{DD}	NC				NF, NF/TDQS#	V _{SS}	V _{DD}
B	V _{SS}	V _{SS} Q	DQ0				DM, DM/TDQS	V _{SS} Q	V _{DD} Q
C	V _{DD} Q	DQ2	DQ5				DQ1	DQ3	V _{SS} Q
D	V _{SS} Q	NF, DQ6	DQS#				V _{DD}	V _{SS}	V _{SS} Q
E	V _{REF} DQ	V _{DD} Q	NF, DQ4				NF, DQ7	NF, DQ5	V _{DD} Q
F	NC	V _{SS}	RAS#				CK	V _{SS}	NC
G	ODT	V _{DD}	CAS#				CK#	V _{DD}	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	V _{SS}	BA0	BA2				NC	V _{REF} CA	V _{SS}
K	V _{DD}	A3	A0				A12/BC#	BA1	V _{DD}
L	V _{SS}	A5	A2				A1	A4	V _{SS}
M	V _{DD}	A7	A9				A11	A6	V _{DD}
N	V _{SS}	RESET#	A13				A14	A8	V _{SS}

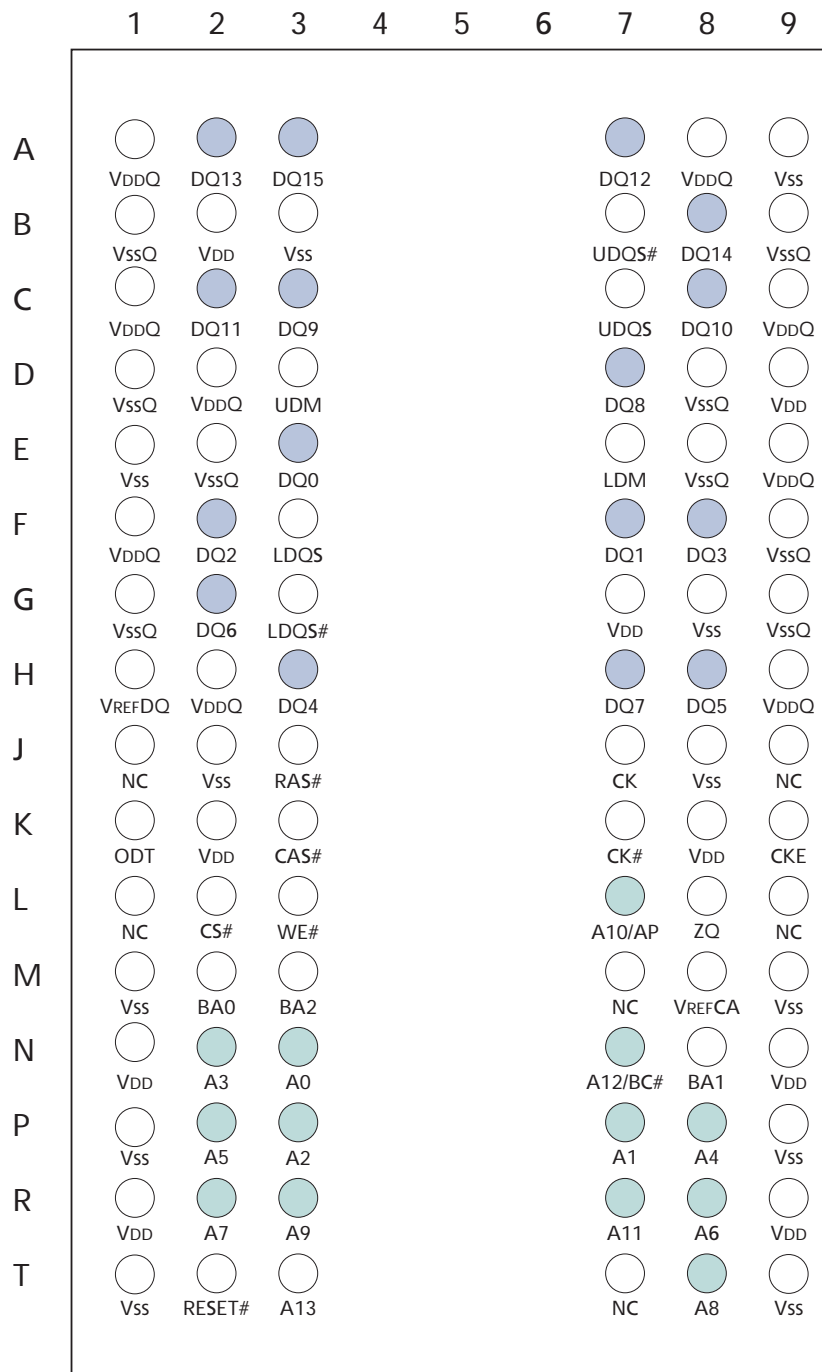
- Notes:
- Ball descriptions listed in Table 3 on page 18 are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
 - A comma separates the configuration; a slash defines a selectable function.
Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3 on page 18).

Figure 7: 82-Ball FBGA – x4, x8 Pin Assignments (Top View)



- Notes:
- Ball descriptions are listed Table 4 on page 20 as “x4, x8” if unique, otherwise x4, x8 are the same.
 - A comma separates the configuration, a slash defines a selectable function.
Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 4 on page 20).

Figure 8: 96-Ball FBGA – x16 Ball Assignments (Top View)



- Notes:
- Ball descriptions listed in Table 5 on page 22 are listed as "x4, x8" if unique; otherwise, x4 and x8 are the same.
 - A comma separates the configuration; a slash defines a selectable function.
Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 5 on page 22).

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Ball Assignments	Symbol	Type	Description
K3, L7, L3, K2, L8, L2, M8, M2, N8, M3, H7, M7, K7, N3, N7	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC#, A13, A14	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Table 65 on page 93.
J2, K8, J3	BA0, BA1, BA2	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
F7, G7	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
G9	CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
H2	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
B7	DM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use as TDQS on the x8.
G1	ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
F3, G3, H3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (continued)

Ball Assignments	Symbol	Type	Description
N2	RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$. RESET# assertion and desertion are asynchronous.
B3, C7, C2, C8	DQ0, DQ1, DQ2, DQ3	I/O	Data input/output: Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to VREFDQ.
B3, C7, C2, C8, E3, E8, D2, E7	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	Data input/output: Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to VREFDQ.
C3, D3	DQS, DQS#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
B7, A7	TDQS, TDQS#	Output	Termination data strobe: Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
A2, A9, D7, G2, G8, K1, K9, M1, M9	VDD	Supply	Power supply: 1.5V $\pm 0.075V$.
B9, C1, E2, E9	VDDQ	Supply	DQ power supply: 1.5V $\pm 0.075V$. Isolated on the device for improved noise immunity.
J8	VREFCA	Supply	Reference voltage for control, command, and address: VREFCA must be maintained at all times (including self refresh) for proper device operation.
E1	VREFDQ	Supply	Reference voltage for data: VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
A1, A8, B1, D8, F2, F8, J1, J9, L1, L9, N1, N9	Vss	Supply	Ground.
B2, B8, C9, D1, D9	VssQ	Supply	DQ ground: Isolated on the device for improved noise immunity.
H8	ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240 Ω resistor (RZQ), which is tied to VssQ.
A3, J7, F9, H1, F1, H9	NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
A7, D2, E3, E7, E8	NF	–	No function: When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Table 4: 82-Ball FBGA (x4, x8)

Ball Number	Symbol	Type	Description
K4, L8, L4, K3, L9, L3, M9, M3, N9, M4, H8, M8, K8, N4, N8	A0, A1, A2, A3 A4, A5, A6, A7 A8, A9, A10/AP, A11, A12/BC# A13, A14	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Table 65 on page 93.
J3, K9, J4	BA0, BA1, BA2	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
F8, G8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
G10	CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
H3	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
B8	DM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use as TDQS on the x8.
G2	ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
F4, G4, H4	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

Table 4: 82-Ball FBGA (x4, x8) (continued)

Ball Number	Symbol	Type	Description
N3	RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$. RESET# assertion and desertion are asynchronous.
B4, C8, C3, C9	DQ0, DQ1, DQ2, DQ3	I/O	Data input/output: Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to VREFDQ.
B4, C8, C3, C9, E4, E9, D3, E8	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	Data input/output: Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to VREFDQ.
C4, D4	DQS, DQS#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
B8, A8	TDQS, TDQS#	Output	Termination data strobe: Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
A3, A10, D8, G3, G9, K2, K10, M2, M10	VDD	Supply	Power supply: 1.5V $\pm 0.075V$.
B10, C2, E3, E10	VDDQ	Supply	DQ power supply: 1.5V $\pm 0.075V$. Isolated on the device for improved noise immunity.
J9	VREFCA	Supply	Reference voltage for control, command, and address: VREFCA must be maintained at all times (including self refresh) for proper device operation.
E2	VREFDQ	Supply	Reference voltage for data: VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
A2, A9, B2, D9, F3, F9, J2, J10, L2, L10, N2, N10	Vss	Supply	Ground.
B3, B9, C10, D2, D10	VssQ	Supply	DQ ground: Isolated on the device for improved noise immunity.
H9	ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240 Ω resistor (RZQ), which is tied to VssQ.
A1, A4, A11, F2, F10, H2, H10, J8, N1, N11	NC	-	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
A8, D3, E4, E8, E9	NF	-	No function: When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Table 5: 96-Ball FBGA – x16 Ball Descriptions

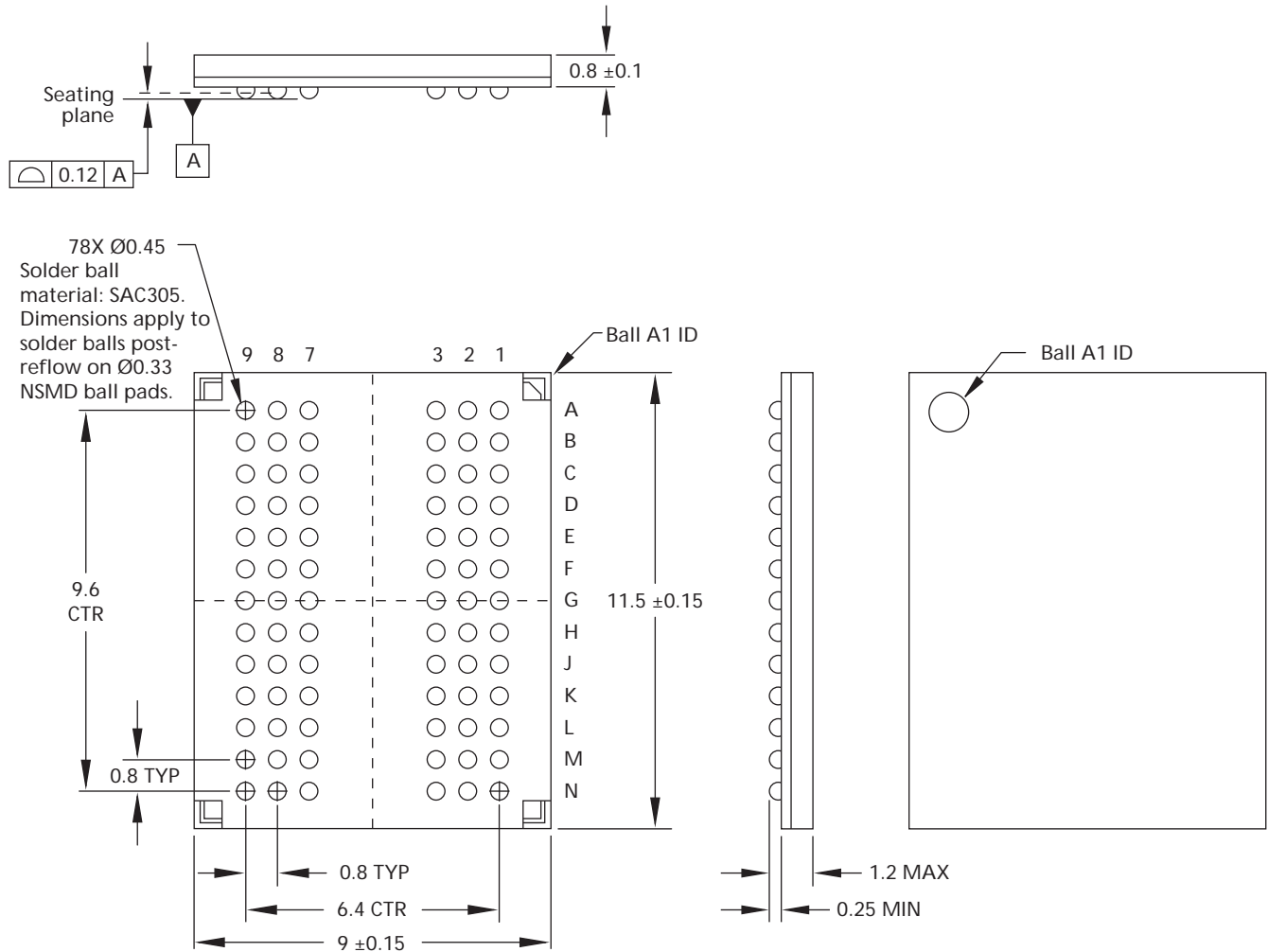
Ball Assignments	Symbol	Type	Description
N3, P7, P3, N2, P8, P2, R8, R2, T8, R3, L7, R7, N7 T3	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9 A10/AP, A11, A12/BC#, A13	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Table 65 on page 93.
M2, N8, M3	BA0, BA1, BA2	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
J7, K7	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
K9	CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
L2	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
E7	LDM	Input	Input data mask: LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to VREFDQ.
K1	ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
J3, K3, L3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

Table 5: 96-Ball FBGA – x16 Ball Descriptions (continued)

Ball Assignments	Symbol	Type	Description
T2	RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$. RESET# assertion and desertion are asynchronous.
D3	UDM	Input	Input data mask: UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to VREFDQ.
E3, F7, F2, F8, H3, H8, G2, H7	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	Data input/output: Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to VREFDQ.
D7, C3, C8, C2, A7, A2, B8, A3	DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, DQ15	I/O	Data input/output: Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to VREFDQ.
F3, G3	LDQS, LDQS#	I/O	Lower byte data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
C7, B7	UDQS, UDQS#	I/O	Upper byte data strobe: Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
B2, D9, G7, K2, K8, N1, N9, R1, R9	VDD	Supply	Power supply: 1.5V $\pm 0.075V$.
A1, A8, C1, C9, D2, E9, F1, H2, H9	VDDQ	Supply	DQ power supply: 1.5V $\pm 0.075V$. Isolated on the device for improved noise immunity.
M8	VREFCA	Supply	Reference voltage for control, command, and address: VREFCA must be maintained at all times (including self refresh) for proper device operation.
H1	VREFDQ	Supply	Reference voltage for data: VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Supply	Ground.
B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Supply	DQ ground: Isolated on the device for improved noise immunity.
L8	ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240 Ω resistor (RZQ), which is tied to VssQ.
J1, J9, L1, L9, M7, T7	NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

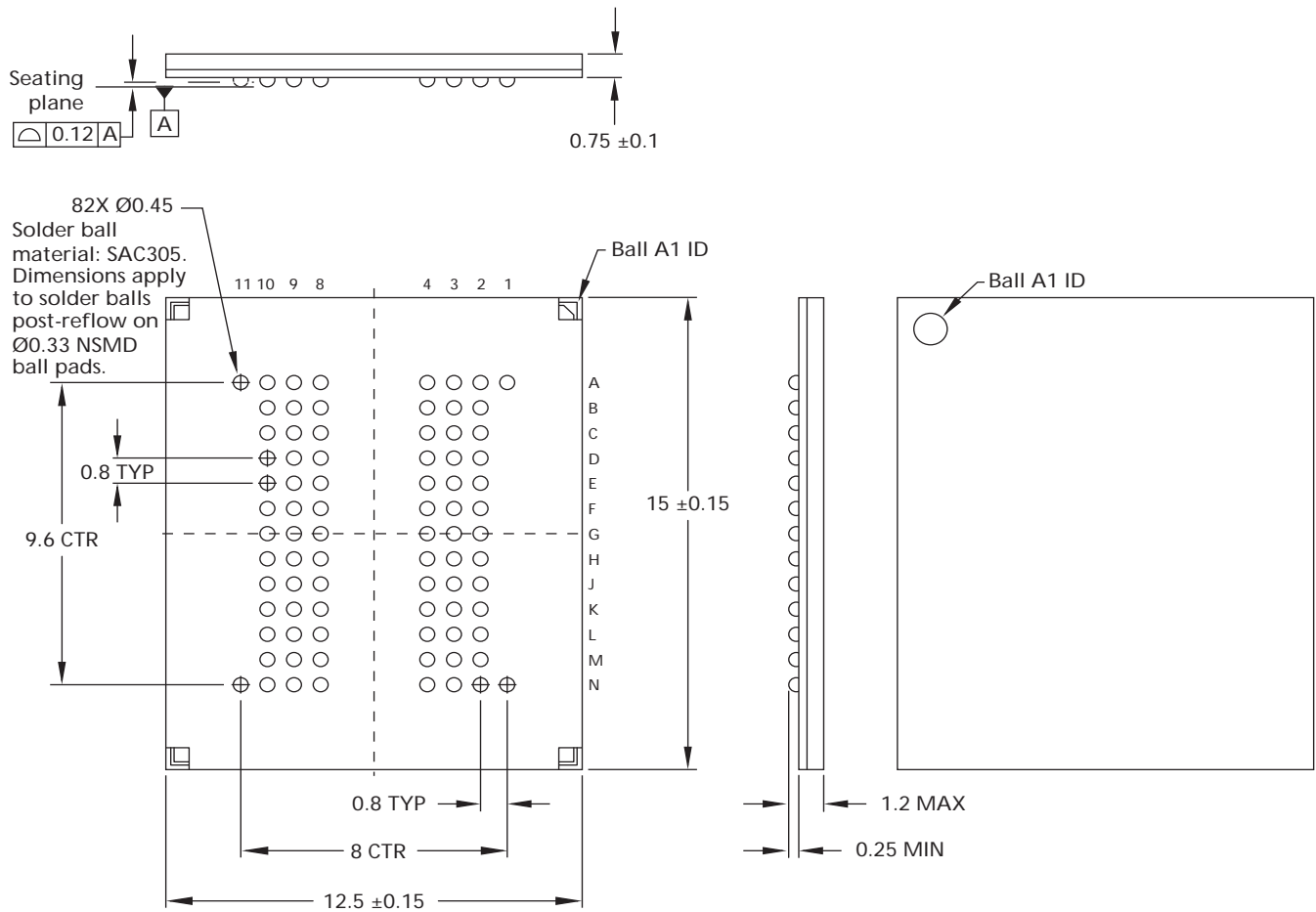
Package Dimensions

Figure 9: 78-Ball FBGA – x4, x8; “HX”



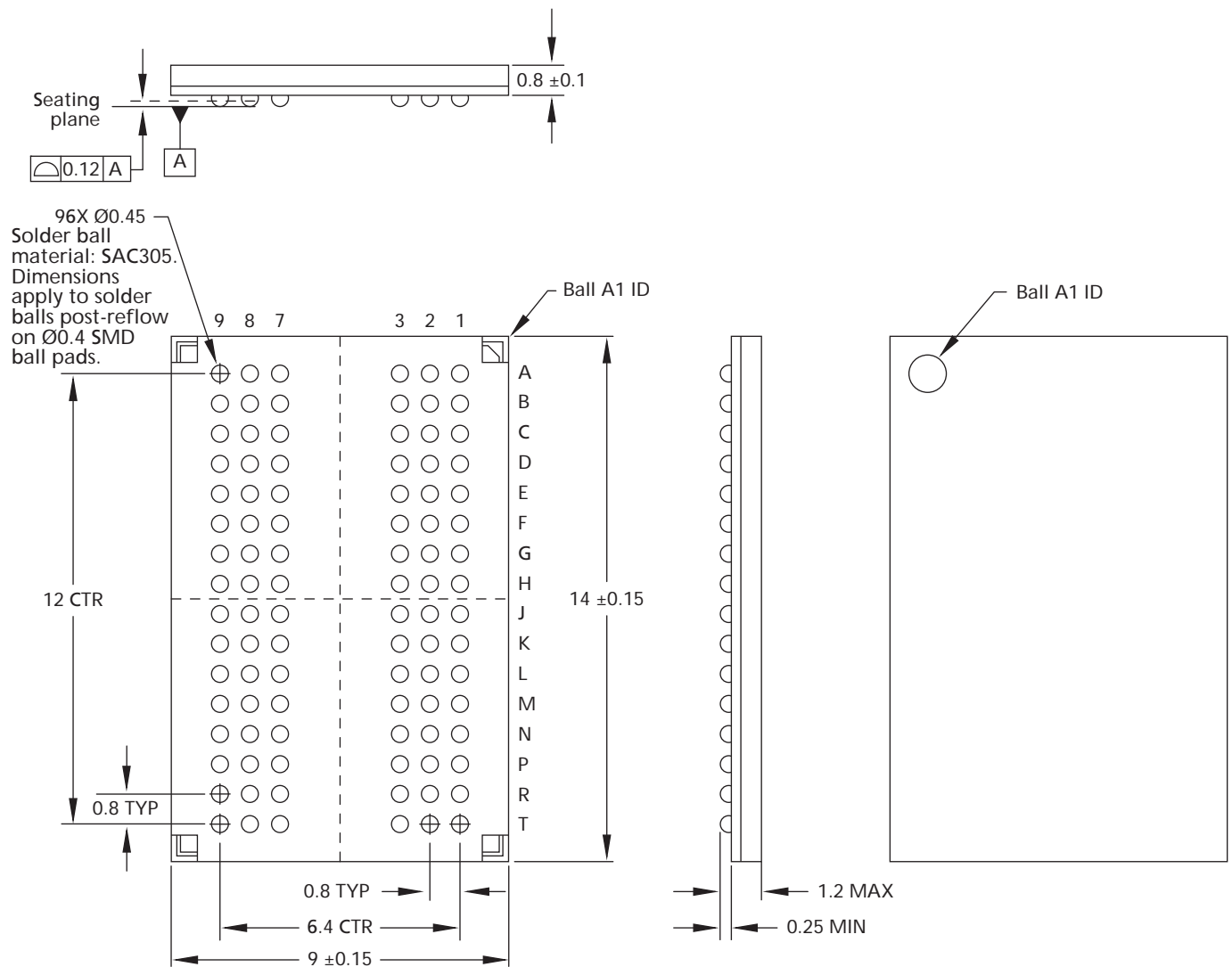
Notes: 1. All dimensions are in millimeters.

Figure 10: 82-Ball FBGA – x4, x8; “JE”



Notes: 1. All dimensions are in millimeters.

Figure 11: 96-Ball FBGA - x16; "HA"



Notes: 1. All dimensions are in millimeters.

Electrical Specifications

Absolute Ratings

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V _{DD}	V _{DD} supply voltage relative to V _{SS}	-0.4	1.975	V	1
V _{DDQ}	V _{DDQ} supply voltage relative to V _{SSQ}	-0.4	1.975	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.4	1.975	V	
T _C	Operating case temperature	0	95	°C	2, 3
T _{STG}	Storage temperature	-55	150	°C	

- Notes:
- V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500mV, V_{REF} may be ≤300mV.
 - MAX operating case temperature. T_C is measured in the center of the package (see Figure 12 on page 28).
 - Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Input/Output Capacitance

Table 7: Input/Output Capacitance

Note 1 applies to the entire table

Capacitance Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CK and CK#	C _{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	
ΔC: CK to CK#	C _{DCCK}	0	0.15	0	0.15	0	0.15	0	0.15	pF	
Single-end I/O: DQ, DM	C _{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	pF	2
Differential I/O: DQS, DQS#, TDQS, TDQS#	C _{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	pF	3
ΔC: DQS to DQS#, TDQS, TDQS#	C _{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	pF	3
ΔC: DQ to DQS	C _{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	C _I	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	pF	5
ΔC: CTRL to CK	C _{DI_CTRL}	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	C _{DI_CMD_ADDR}	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	7

- Notes:
- V_{DD} = +1.5V ±0.075mV, V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C.
V_{OUT(DC)} = 0.5 × V_{DDQ}, V_{OUT} (peak-to-peak) = 0.1V.
 - DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
 - Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.
 - C_{DIO} = C_{IO} (DQ) - 0.5 × (C_{IO} [DQS] + C_{IO} [DQS#]).
 - Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[n:0], BA[2:0].
 - C_{DI_CTRL} = C_I (CTRL) - 0.5 × (C_{CK} [CK] + C_{CK} [CK#]).
 - C_{DI_CMD_ADDR} = C_I (CMD_ADDR) - 0.5 × (C_{CK} [CK] + C_{CK} [CK#]).

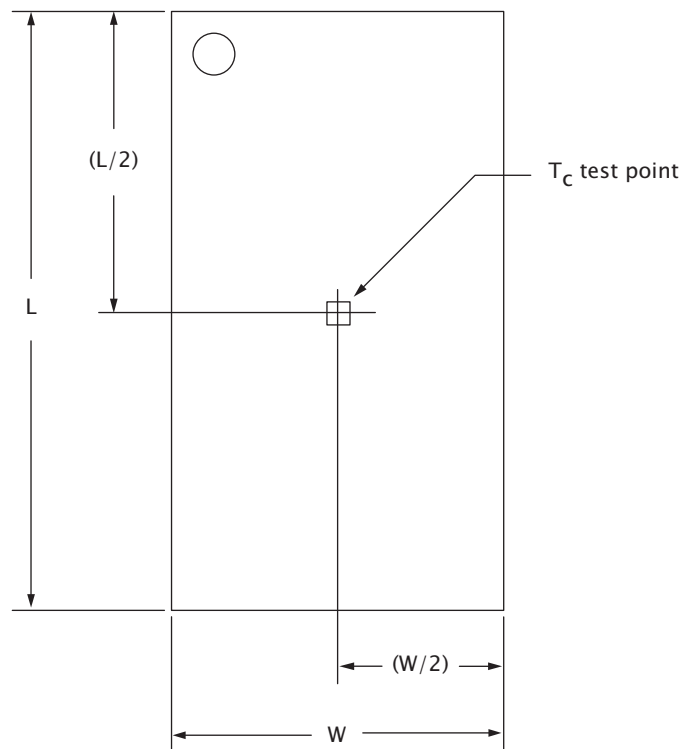
Thermal Characteristics

Table 8: Thermal Characteristics

Parameter/Condition		Value	Units	Symbol	Notes
Operating case temperature		0 to 85	°C	T_C	1, 2, 3
		0 to 95	°C	T_C	1, 2, 3, 4
Junction-to-case (TOP)	78-ball "HX"	TBD	°C/W	Θ_{JC}	5
	82-ball "JE"	1.6			
	96-ball "HA"	TBD			

- Notes:
1. MAX operating case temperature. T_C is measured in the center of the package (see Figure 12).
 2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
 3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
 4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate. The use of SRT or ASR (if available) must be enabled.
 5. The thermal resistance data is based off of a number of samples from multiple lots and should be viewed as a typical number.

Figure 12: Thermal Measurement Point



Electrical Specifications – IDD Specifications and Conditions

Within the following Idd measurement tables (Table 9 through Table 19), the following definitions and conditions are used, unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(AC) MAX}$; HIGH: $V_{IN} \geq V_{IH(AC) MIN}$
- Mid-level: Inputs are $V_{REF} = V_{DD}/2$
- R_{ON} set to $RZQ/7$, that is, 34Ω
- R_{TT_NOM} set to $RZQ/6$, that is, 40Ω
- R_{TT_WR} set to $RZQ/2$, that is, 120Ω
- QOFF is enabled in MR1
- ODT is enabled in MR1 (R_{TT_NOM}) and MR2 (R_{TT_WR})
- TDQS is disabled in MR1
- External DQ/DQS/DM load resistor is 25Ω to $V_{DDQ}/2$
- Burst lengths are BL8 fixed
- AL equals 0 (except in IDD7)
- IDD specifications are tested after the device is properly initialized
- Input slew rate is specified by AC parametric test conditions
- Optional ASR is disabled
- READ burst type uses nibble sequential (MR0 [3] 0)
- Loop patterns must be executed at least once prior to current measurements begin

Table 9: Timing Parameters used for IDD Measurements – Clock Units

IDD Parameter	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
	-25E	-25	-187E	-187	-15E	-15	-125E	-125	
	5-5-5	6-6-6	7-7-7	8-8-8	9-9-9	10-10-10	10-10-10	11-11-11	
$t_{CK} (MIN)_{IDD}$	2.5		1.875		1.5		1.25		ns
CL _{IDD}	5	6	7	8	9	10	10	11	CK
$t_{RCD} (MIN)_{IDD}$	5	6	7	8	9	10	10	11	CK
$t_{RC} (MIN)_{IDD}$	20	21	27	28	33	34	38	39	CK
$t_{RAS} (MIN)_{IDD}$	15	15	20	20	24	24	28	28	CK
$t_{RP} (MIN)$	5	6	7	8	9	10	10	11	CK
t_{FAW}	x4, x8	16	16	20	20	20	24	24	CK
	x16	20	20	27	27	30	30	32	CK
t_{RRD}_{IDD}	x4, x8	4	4	4	4	4	5	5	CK
	x16	4	4	6	6	5	5	6	CK
t_{RFC}	2Gb	64	64	86	86	107	107	128	CK

Table 10: IDD0 Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data			
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-			
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3	D#	1	1	1	1	0	0	0	0	0	0	0	0	0	-	
			4	D#	1	1	1	1	0	0	0	0	0	0	0	0	0	-	
			Repeat cycles 1 through 4 until $nRAS - 1$, truncate if needed																
			$nRAS$	PRE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			Repeat cycles 1 through 4 until $nRC - 1$, truncate if needed																
			nRC	ACT	0	0	1	1	0	0	0	0	0	0	0	F	0	0	-
			$nRC + 1$	D	1	0	0	0	0	0	0	0	0	0	0	F	0	0	-
			$nRC + 2$	D	1	0	0	0	0	0	0	0	0	0	0	F	0	0	-
			$nRC + 3$	D#	1	1	1	1	0	0	0	0	0	0	0	F	0	0	-
			$nRC + 4$	D#	1	1	1	1	0	0	0	0	0	0	0	F	0	0	-
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $nRC - 1 + nRAS - 1$, truncate if needed																
			$nRC + nRAS$	PRE	0	0	1	0	0	0	0	0	0	0	0	F	0	0	-
		Repeat cycles $nRC + 1$ through $nRC + 4$ until $2 \times RC - 1$, truncate if needed																	
		1	$2 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 1															
		2	$4 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 2															
		3	$6 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 3															
		4	$8 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 4															
		5	$10 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 5															
6	$12 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 6																	
7	$14 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 7																	

- Notes:
1. DQs, DQS, DQS# are mid-level.
 2. DM is LOW.
 3. Only selected bank (single) active.

Table 11: IDD1 Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³			
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-			
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	-		
			3	D#	1	1	1	1	1	0	0	0	0	0	0	0	-		
			4	D#	1	1	1	1	1	0	0	0	0	0	0	0	-		
			Repeat cycles 1 through 4 until $nRCD - 1$, truncate if needed																
			$nRCD$	RD	0	1	0	1	0	0	0	0	0	0	0	0	0	0	00000000
			Repeat cycles 1 through 4 until $nRAS - 1$, truncate if needed																
			$nRAS$	PRE	0	0	1	0	0	0	0	0	0	0	0	0	0	-	
			Repeat cycles 1 through 4 until $nRC - 1$, truncate if needed																
			nRC	ACT	0	0	1	1	0	0	0	0	0	0	F	0	-		
			$nRC + 1$	D	1	0	0	0	0	0	0	0	0	0	F	0	-		
			$nRC + 2$	D	1	0	0	0	0	0	0	0	0	0	F	0	-		
			$nRC + 3$	D#	1	1	1	1	0	0	0	0	0	0	F	0	-		
			$nRC + 4$	D#	1	1	1	1	0	0	0	0	0	0	F	0	-		
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $nRC + nRCD - 1$, truncate if needed																
			$nRC + nRCD$	RD	0	1	0	1	0	0	0	0	0	0	F	0	00110011		
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $nRC + nRAS - 1$, truncate if needed																
		$nRC + nRAS$	PRE	0	0	1	0	0	0	0	0	0	0	F	0	-			
		Repeat cycle $nRC + 1$ through $nRC + 4$ until $2 \times nRC - 1$, truncate if needed																	
		1	$2 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 1															
		2	$4 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 2															
		3	$6 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 3															
		4	$8 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 4															
		5	$10 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 5															
		6	$12 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 6															
		7	$14 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 7															

- Notes:
1. DQs, DQS, DQS# are mid-level unless driven as required by the READ (RD) command.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the RD command.
 4. Only selected bank (single) active.

Table 12: IDD Measurement Conditions for Power-Down Currents

Name	IDD2P0 Precharge Power-Down Current (Slow Exit) ¹	IDD2P1 Precharge Power-Down Current (Fast Exit) ¹	IDD2Q Precharge Quiet Standby Current	IDD3P Active Power-Down Current
Timing pattern	n/a	n/a	n/a	n/a
CKE	LOW	LOW	HIGH	LOW
External clock	Toggling	Toggling	Toggling	Toggling
^t CK	^t CK (MIN) IDD	^t CK(MIN) IDD	^t CK(MIN) IDD	^t CK (MIN) IDD
^t RC	n/a	n/a	n/a	n/a
^t RAS	n/a	n/a	n/a	n/a
^t RCD	n/a	n/a	n/a	n/a
^t RRD	n/a	n/a	n/a	n/a
^t RC	n/a	n/a	n/a	n/a
CL	n/a	n/a	n/a	n/a
AL	n/a	n/a	n/a	n/a
CS#	HIGH	HIGH	HIGH	HIGH
Command inputs	LOW	LOW	LOW	LOW
Row/column addr	LOW	LOW	LOW	LOW
Bank addresses	LOW	LOW	LOW	LOW
DM	LOW	LOW	LOW	LOW
Data I/O	Mid-level	Mid-level	Mid-level	Mid-level
Output buffer DQ, DQS	Enabled	Enabled	Enabled	Enabled
ODT ²	Enabled, off	Enabled, off	Enabled, off	Enabled, off
Burst length	8	8	8	8
Active banks	None	None	None	All
Idle banks	All	All	All	None
Special notes	n/a	n/a	n/a	n/a

- Notes: 1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).
2. "Enabled, off" means the MR bits are enabled, but the signal is LOW.

Table 13: IDD2N and IDD3N Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data		
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-	
			2	D#	1	1	1	1	0	0	0	0	0	0	F	0	-	
			3	D#	1	1	1	1	0	0	0	0	0	0	F	0	-	
		1	4-7	Repeat sub-loop 0, use BA[2:0] = 1														
		2	8-11	Repeat sub-loop 0, use BA[2:0] = 2														
		3	12-15	Repeat sub-loop 0, use BA[2:0] = 3														
		4	16-19	Repeat sub-loop 0, use BA[2:0] = 4														
		5	20-23	Repeat sub-loop 0, use BA[2:0] = 5														
		6	24-27	Repeat sub-loop 0, use BA[2:0] = 6														
7	28-31	Repeat sub-loop 0, use BA[2:0] = 7																

- Notes: 1. DQs, DQS, DQS# are mid-level.
2. DM is LOW.
3. All banks closed during IDD2N, all banks open during IDD3N.

Table 14: IDD2NT Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data		
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-	
			2	D#	1	1	1	1	0	0	0	0	0	0	F	0	-	
			3	D#	1	1	1	1	0	0	0	0	0	0	F	0	-	
		1	4-7	Repeat sub-loop 0, use BA[2:0] = 1; ODT = 0														
		2	8-11	Repeat sub-loop 0, use BA[2:0] = 2; ODT = 1														
		3	12-15	Repeat sub-loop 0, use BA[2:0] = 3; ODT = 1														
		4	16-19	Repeat sub-loop 0, use BA[2:0] = 4; ODT = 0														
		5	20-23	Repeat sub-loop 0, use BA[2:0] = 5; ODT = 0														
		6	24-27	Repeat sub-loop 0, use BA[2:0] = 6; ODT = 1														
7	28-31	Repeat sub-loop 0, use BA[2:0] = 7; ODT = 1																

- Notes: 1. DQs, DQS, DQS# are mid-level.
2. DM is LOW.
3. All banks closed.

Table 15: IDD4R Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³		
Toggling	Static HIGH	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	-	
			2	D#	1	1	1	1	0	0	0	0	0	0	0	0	-	
			3	D#	1	1	1	1	0	0	0	0	0	0	0	0	-	
			4	RD	0	1	0	1	0	0	0	0	0	0	F	0	00110011	
			5	D	1	0	0	0	0	0	0	0	0	0	F	0	-	
			6	D#	1	1	1	1	0	0	0	0	0	0	F	0	-	
			7	D#	1	1	1	1	0	0	0	0	0	0	F	0	-	
		1	8-15	Repeat sub-loop 0, use BA[2:0] = 1														
		2	16-23	Repeat sub-loop 0, use BA[2:0] = 2														
		3	24-31	Repeat sub-loop 0, use BA[2:0] = 3														
		4	32-39	Repeat sub-loop 0, use BA[2:0] = 4														
		5	40-47	Repeat sub-loop 0, use BA[2:0] = 5														
		6	48-55	Repeat sub-loop 0, use BA[2:0] = 6														
		7	56-63	Repeat sub-loop 0, use BA[2:0] = 7														

- Notes:
1. DQs, DQS, DQS# are mid-level when not driving in burst sequence.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the RD command.
 4. All banks open.

Table 16: IDD4W Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³		
Toggling	Static HIGH	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000		
			1	D	1	0	0	0	1	0	0	0	0	0	0	0	-	
			2	D#	1	1	1	1	1	1	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	1	0	0	0	0	0	0	0	-
			4	WR	0	1	0	0	0	1	0	0	0	0	F	0	00110011	
			5	D	1	0	0	0	0	1	0	0	0	0	F	0	-	
			6	D#	1	1	1	1	1	1	0	0	0	0	F	0	-	
			7	D#	1	1	1	1	1	1	0	0	0	0	F	0	-	
		1	8-15	Repeat sub-loop 0, use BA[2:0] = 1														
		2	16-23	Repeat sub-loop 0, use BA[2:0] = 2														
		3	24-31	Repeat sub-loop 0, use BA[2:0] = 3														
		4	32-39	Repeat sub-loop 0, use BA[2:0] = 4														
		5	40-47	Repeat sub-loop 0, use BA[2:0] = 5														
		6	48-55	Repeat sub-loop 0, use BA[2:0] = 6														
		7	56-63	Repeat sub-loop 0, use BA[2:0] = 7														

- Notes:
1. DQs, DQS, DQS# are mid-level when not driving in burst sequence.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the WRITE (WR) command.
 4. All banks open.

Table 17: IDD5B Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data	
Toggling	Static HIGH	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-	
		1a	1	D	1	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	0	0	0	F	0	-
			4	D#	1	1	1	1	1	0	0	0	0	0	F	0	-
		1b	5-8	Repeat sub-loop 1a, use BA[2:0] = 1													
		1c	9-12	Repeat sub-loop 1a, use BA[2:0] = 2													
		1d	13-16	Repeat sub-loop 1a, use BA[2:0] = 3													
		1e	17-20	Repeat sub-loop 1a, use BA[2:0] = 4													
		1f	21-24	Repeat sub-loop 1a, use BA[2:0] = 5													
		1g	25-28	Repeat sub-loop 1a, use BA[2:0] = 6													
		1h	29-32	Repeat sub-loop 1a, use BA[2:0] = 7													
2	33-nRFC - 1	Repeat sub-loop 1a through 1h until nRFC - 1, truncate if needed															

Notes: 1. DQs, DQS, DQS# are mid-level.
2. DM is LOW.

Table 18: IDD Measurement Conditions for IDD6, IDD6ET, and IDD8

IDD Test	IDD6: Self Refresh Current Normal Temperature Range T _C = 0°C to 85°C	IDD6ET: Self Refresh Current Extended Temperature Range T _C = 0°C to 95°C	IDD8: Reset ²
CKE	LOW	LOW	Mid-level
External clock	Off, CK and CK# = LOW	Off, CK and CK# = LOW	Mid-level
^t CK	n/a	n/a	n/a
^t RC	n/a	n/a	n/a
^t RAS	n/a	n/a	n/a
^t RCD	n/a	n/a	n/a
^t RRD	n/a	n/a	n/a
^t RC	n/a	n/a	n/a
CL	n/a	n/a	n/a
AL	n/a	n/a	n/a
CS#	Mid-level	Mid-level	Mid-level
Command inputs	Mid-level	Mid-level	Mid-level
Row/column addresses	Mid-level	Mid-level	Mid-level
Bank addresses	Mid-level	Mid-level	Mid-level
Data I/O	Mid-level	Mid-level	Mid-level
Output buffer DQ, DQS	Enabled	Enabled	Mid-level
ODT ¹	Enabled, mid-level	Enabled, mid-level	Mid-level
Burst length	n/a	n/a	n/a

Table 18: IDD Measurement Conditions for IDD6, IDD6ET, and IDD8

IDD Test	IDD6: Self Refresh Current Normal Temperature Range $T_C = 0^{\circ}\text{C to } 85^{\circ}\text{C}$	IDD6ET: Self Refresh Current Extended Temperature Range $T_C = 0^{\circ}\text{C to } 95^{\circ}\text{C}$	IDD8: Reset ²
Active banks	n/a	n/a	None
Idle banks	n/a	n/a	All
SRT	disabled (normal)	enabled (extended)	n/a
ASR	disabled	disabled	n/a

- Notes:
1. Enabled, mid-level“ means the MR command is enabled, but the signal is mid-level.
 2. During a cold boot RESET (initialization), the current reading is valid once power is stable and RESET has been LOW for 1ms; during a warm boot RESET (while operating), the current reading is valid after RESET has been LOW for 200ns + ^tRFC.

Table 19: IDD7 Measurement Loop

CK, CK#	CKE	Sub-loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³		
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-		
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	-	
			3	Repeat cycle 2 until $nRRD - 1$														
		1	$nRRD$	ACT	0	0	1	1	0	1	0	1	0	0	F	0	-	
			$nRRD + 1$	RDA	0	1	0	1	0	1	0	1	0	1	0	F	0	00110011
			$nRRD + 2$	D	1	0	0	0	0	0	0	1	0	0	0	F	0	-
			$nRRD + 3$	Repeat cycle $nRRD + 2$ until $2 \times nRRD - 1$														
		2	$2 \times nRRD$	Repeat sub-loop 0, use BA[2:0] = 2														
		3	$3 \times nRRD$	Repeat sub-loop 1, use BA[2:0] = 3														
		4	$4 \times nRRD$	D	1	0	0	0	0	0	0	3	0	0	0	F	0	-
			$4 \times nRRD + 1$	Repeat cycle $4 \times nRRD$ until $nFAW - 1$, if needed														
		5	$nFAW$	Repeat sub-loop 0, use BA[2:0] = 4														
		6	$nFAW + nRRD$	Repeat sub-loop 1 use BA[2:0] = 5														
		7	$nFAW + 2 \times nRRD$	Repeat sub-loop 0, use BA[2:0] = 6														
		8	$nFAW + 3 \times nRRD$	Repeat sub-loop 1 use BA[2:0] = 7														
		9	$nFAW + 4 \times nRRD$	D	1	0	0	0	0	0	0	7	0	0	0	F	0	-
			$nFAW + 4 \times nRRD + 1$	Repeat cycle $nFAW + 4 \times nRRD$ until $2 \times nFAW - 1$, if needed														
		10	$2 \times nFAW$	ACT	0	0	1	1	0	0	0	0	0	0	F	0	-	
			$2 \times nFAW + 1$	RDA	0	1	0	1	0	0	0	0	1	0	F	0	00110011	
			$2 \times nFAW + 2$	D	1	0	0	0	0	0	0	0	0	0	0	F	0	-
			$2 \times nFAW + 3$	Repeat cycle $2 \times nFAW + 2$ until $2 \times nFAW + nRRD - 1$														
		11	$2 \times nFAW + nRRD$	ACT	0	0	1	1	0	1	0	1	0	0	0	0	-	
			$2 \times nFAW + nRRD + 1$	RDA	0	1	0	1	0	1	0	1	0	1	0	0	00000000	
			$2 \times nFAW + nRRD + 2$	D	1	0	0	0	0	0	1	0	0	0	0	0	-	
			$2 \times nFAW + nRRD + 3$	Repeat cycle $2 \times nFAW + nRRD + 2$ until $2 \times nFAW + 2 \times nRRD - 1$														
		12	$2 \times nFAW + 2 \times nRRD$	Repeat sub-loop 10, use BA[2:0] = 2														
		13	$2 \times nFAW + 3 \times nRRD$	Repeat sub-loop 11, use BA[2:0] = 3														
		14	$2 \times nFAW + 4 \times nRRD$	D	1	0	0	0	0	0	0	3	0	0	0	0	0	-
			$2 \times nFAW + 4 \times nRRD + 1$	Repeat cycle $2 \times nFAW + 4 \times nRRD$ until $3 \times nFAW - 1$, if needed														
		15	$3 \times nFAW$	Repeat sub-loop 10, use BA[2:0] = 4														
		16	$3 \times nFAW + nRRD$	Repeat sub-loop 11 use BA[2:0] = 5														
		17	$3 \times nFAW + 2 \times nRRD$	Repeat sub-loop 10, use BA[2:0] = 6														
		18	$3 \times nFAW + 3 \times nRRD$	Repeat sub-loop 11 use BA[2:0] = 7														
		19	$3 \times nFAW + 4 \times nRRD$	D	1	0	0	0	0	0	0	7	0	0	0	0	0	-
			$3 \times nFAW + 4 \times nRRD + 1$	Repeat cycle $3 \times nFAW + 4 \times nRRD$ until $4 \times nFAW - 1$, if needed														

- Notes: 1. DQs, DQS, DQS# are mid-level unless driven as required by the RD command.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the RD command.
 4. AL = CL - 1.

Electrical Characteristics – IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

Table 20: IDD Maximum Limits - Die Rev A

Speed Bin		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Notes
IDD	Width						
IDD0	x4	75	90	100	TBD	mA	1, 2
	x8	100	120	130	TBD	mA	1, 2
	x16	n/a	n/a	n/a	n/a	mA	1, 2
IDD1	x4	100	115	130	TBD	mA	1, 2
	x8	115	135	155	TBD	mA	1, 2
	x16	n/a	n/a	n/a	n/a	mA	1, 2
IDD2P0 (slow)	All	12	12	12	TBD	mA	1, 2
IDD2P1 (fast)	All	30	35	40	TBD	mA	1, 2
IDD2Q	All	55	65	75	TBD	mA	1, 2
IDD2N	All	60	70	80	TBD	mA	1, 2
IDD2NT	x4, x8	75	90	100	TBD	mA	1, 2
	x16	85	105	115	TBD	mA	1, 2
IDD3P	All	50	55	65	TBD	mA	1, 2
IDD3N	x4, x8	70	80	95	TBD	mA	1, 2
	x16	n/a	n/a	n/a	n/a	mA	1, 2
IDD4R	x4	175	200	230	TBD	mA	1, 2
	x8	195	225	255	TBD	mA	1, 2
	x16	n/a	n/a	n/a	n/a	mA	1, 2
IDD4W	x4	225	255	285	TBD	mA	1, 2
	x8	260	295	330	TBD	mA	1, 2
	x16	n/a	n/a	n/a	n/a	mA	1, 2
IDD5B	All	275	290	305	TBD	mA	1, 2
IDD6	All	9	9	9	TBD	mA	1, 2, 3
IDD6ET	All	12	12	12	TBD	mA	2, 4
IDD7	x4	320	345	415	TBD	mA	1, 2
	x8	400	430	460	TBD	mA	1, 2
	x16	n/a	n/a	n/a	n/a	mA	1, 2
IDD8	All	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	mA	1, 2

- Notes:
1. $T_C = 85^\circ\text{C}$; SRT and ASR are disabled.
 2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
 3. Restricted to $T_C (\text{MAX}) = 85^\circ\text{C}$.
 4. $T_C = 85^\circ\text{C}$; ASR and ODT are disabled; SRT is enabled.
 5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range $0^\circ\text{C} \leq T_C \leq 85^\circ\text{C}$:
 - 5a. When $T_C < 0^\circ\text{C}$: I_{DD2P} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD5W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%
 - 5b. When $T_C > 85^\circ\text{C}$: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5W} must be derated by 2%; I_{DD2Px} must be derated by 30%; and I_{DD6} must be derated by 80%.

Table 21: IDD Maximum Limits - Die Rev D

Speed Bin		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Notes
IDD	Width						
IDD0	x4	60	70	80	TBD	mA	1, 2
	x8	70	80	90	TBD	mA	1, 2
	x16	90	105	120	TBD	mA	1, 2
IDD1	x4	80	90	105	TBD	mA	1, 2
	x8	85	100	115	TBD	mA	1, 2
	x16	115	130	150	TBD	mA	1, 2
IDD2P0 (slow)	All	12	12	12	TBD	mA	1, 2
IDD2P1 (fast)	All	30	30	35	TBD	mA	1, 2
IDD2Q	All	45	55	65	TBD	mA	1, 2
IDD2N	All	45	55	65	TBD	mA	1, 2
IDD2NT	x4, x8	60	75	85	TBD	mA	1, 2
	x16	70	90	100	TBD	mA	1, 2
IDD3P	All	35	40	45	TBD	mA	1, 2
IDD3N	x4, x8	50	60	75	TBD	mA	1, 2
	x16	50	60	75	TBD	mA	1, 2
IDD4R	x4	115	150	190	TBD	mA	1, 2
	x8	125	160	200	TBD	mA	1, 2
	x16	180	245	290	TBD	mA	1, 2
IDD4W	x4	145	185	225	TBD	mA	1, 2
	x8	155	200	240	TBD	mA	1, 2
	x16	215	280	335	TBD	mA	1, 2
IDD5B	All	225	245	255	TBD	mA	1, 2
IDD6	All	9	9	9	TBD	mA	1, 2, 3
IDD6ET	All	12	12	12	TBD	mA	2, 4
IDD7	x4	260	290	350	TBD	mA	1, 2
	x8	290	320	365	TBD	mA	1, 2
	x16	340	390	445	TBD	mA	1, 2
IDD8	All	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	mA	1, 2

- Notes:
1. $T_C = 85^\circ\text{C}$; SRT and ASR are disabled.
 2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
 3. Restricted to $T_C (\text{MAX}) = 85^\circ\text{C}$.
 4. $T_C = 85^\circ\text{C}$; ASR and ODT are disabled; SRT is enabled.
 5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range $0^\circ\text{C} \leq T_C \leq 85^\circ\text{C}$:
 - 5a. When $T_C < 0^\circ\text{C}$: I_{DD2P} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD5W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%
 - 5b. When $T_C > 85^\circ\text{C}$: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5W} must be derated by 2%; I_{DD2Px} must be derated by 30%; and I_{DD6} must be derated by 80%.

Table 22: IDD Maximum Limits - Die Rev F

Speed Bin		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Notes
IDD	Width						
IDD0	x4	60	70	80	TBD	mA	1, 2
	x8	70	80	90	TBD	mA	1, 2
IDD1	x4	80	90	105	TBD	mA	1, 2
	x8	85	100	115	TBD	mA	1, 2
IDD2P0 (slow)	All	12	12	12	TBD	mA	1, 2
IDD2P1 (fast)	All	30	30	35	TBD	mA	1, 2
IDD2Q	All	45	55	65	TBD	mA	1, 2
IDD2N	All	45	55	65	TBD	mA	1, 2
IDD2NT	All	60	75	85	TBD	mA	1, 2
IDD3P	All	35	40	45	TBD	mA	1, 2
IDD3N	All	50	60	75	TBD	mA	1, 2
IDD4R	x4	115	150	190	TBD	mA	1, 2
	x8	125	160	200	TBD	mA	1, 2
IDD4W	x4	145	185	225	TBD	mA	1, 2
	x8	155	200	240	TBD	mA	1, 2
IDD5B	All	225	245	255	TBD	mA	1, 2
IDD6	All	9	9	9	TBD	mA	1, 2, 3
IDD6ET	All	12	12	12	TBD	mA	2, 4
IDD7	x4	260	290	350	TBD	mA	1, 2
	x8	290	320	365	TBD	mA	1, 2
IDD8	All	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	IDD2P + 2mA	mA	1, 2

- Notes:
1. $T_C = 85^\circ\text{C}$; SRT and ASR are disabled.
 2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
 3. Restricted to $T_C (\text{MAX}) = 85^\circ\text{C}$.
 4. $T_C = 85^\circ\text{C}$; ASR and ODT are disabled; SRT is enabled.
 5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range $0^\circ\text{C} \leq T_C \leq 85^\circ\text{C}$:
 - 5a. When $T_C < 0^\circ\text{C}$: I_{DD2P} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD5W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%
 - 5b. When $T_C > 85^\circ\text{C}$: I_{DD0} , I_{DD1} , I_{DD2N} , I_{DD2NT} , I_{DD2Q} , I_{DD3N} , I_{DD3P} , I_{DD4R} , I_{DD4W} , and I_{DD5W} must be derated by 2%; I_{DD2Px} must be derated by 30%; and I_{DD6} must be derated by 80%.

Electrical Specifications – DC and AC

DC Operating Conditions

Table 23: DC Electrical Characteristics and Operating Conditions

 All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V _{DD}	1.425	1.5	1.575	V	1, 2
I/O supply voltage	V _{DDQ}	1.425	1.5	1.575	V	1, 2
Input leakage current Any input 0V ≤ V _{IN} ≤ V _{DD} , V _{REF} pin 0V ≤ V _{IN} ≤ 1.1V (All other pins not under test = 0V)	I _I	-2	-	2	μA	
V _{REF} supply leakage current V _{REFDQ} = V _{DD} /2 or V _{REFCA} = V _{DD} /2 (All other pins not under test = 0V)	I _{VREF}	-1	-	1	μA	3, 4

- Notes:
1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
 2. V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
 3. V_{REF} (see Table 24).
 4. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.

Input Operating Conditions

Table 24: DC Electrical Characteristics and Input Conditions

 All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
V _{IN} low; DC/commands/address busses	V _{IL}	V _{SS}	n/a	See Table 23	V	
V _{IN} high; DC/commands/address busses	V _{IH}	See Table 23	n/a	V _{DD}	V	
Input reference voltage command/address bus	V _{REFCA} (DC)	0.49 × V _{DD}	0.5 × V _{DD}	0.51 × V _{DD}	V	1, 2
I/O reference voltage DQ bus	V _{REFDQ} (DC)	0.49 × V _{DD}	0.5 × V _{DD}	0.51 × V _{DD}	V	2, 3
I/O reference voltage DQ bus in SELF REFRESH	V _{REFDQ} (SR)	V _{SS}	0.5 × V _{DD}	V _{DD}	V	4
Command/address termination voltage (system level, not direct DRAM input)	V _{TT}	-	0.5 × V _{DDQ}	-	V	5

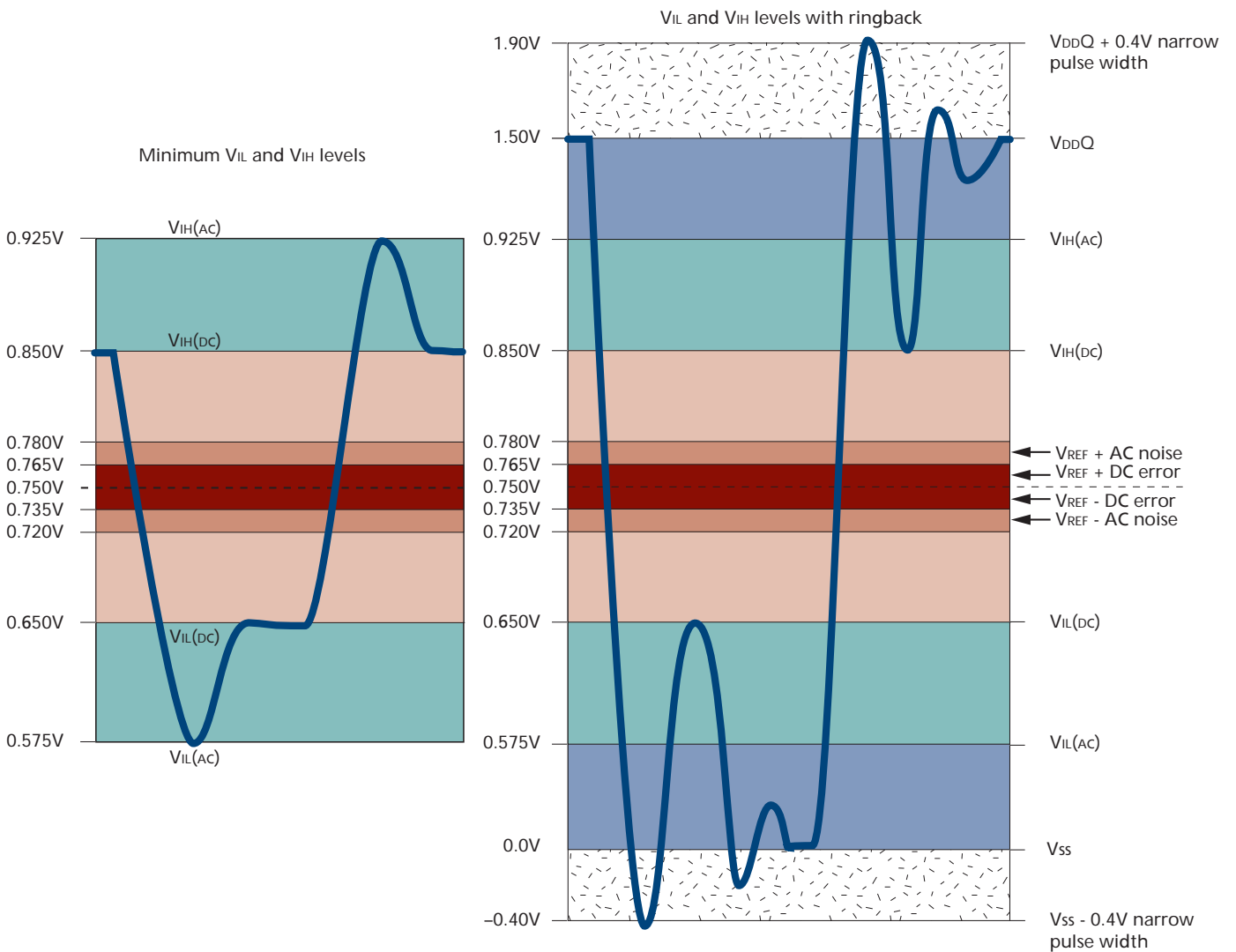
- Notes:
1. V_{REFCA}(DC) is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the V_{REFCA}(DC) value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of V_{REFCA}(DC).
 2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
 3. V_{REFDQ}(DC) is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the V_{REFDQ}(DC) value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of V_{REFDQ}(DC).
 4. V_{REFDQ}(DC) may transition to V_{REFDQ}(SR) and back to V_{REFDQ}(DC) when in SELF REFRESH, within restrictions outlined in the SELF REFRESH section.
 5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

Table 25: Input Switching Conditions

Parameter/Condition	Symbol	DDR3-800 DDR3-1066	DDR3-1333 DDR3-1600	Units
Command and Address				
Input high AC voltage: Logic 1	$V_{IH(AC175)}$ MIN	+175	175	mV
Input high AC voltage: Logic 1	$V_{IH(AC150)}$ MIN	+150	+150	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)}$ MIN	+100	+100	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)}$ MAX	-100	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)}$ MAX	-150	-150	mV
Input low AC voltage: Logic 0	$V_{IL(AC175)}$ MAX	-175	-175	mV
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC175)}$ MIN	+175	-	mV
Input high AC voltage: Logic 1	$V_{IH(AC150)}$ MIN	+150	+150	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)}$ MIN	+100	+100	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)}$ MAX	-100	-100	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)}$ MAX	-150	-150	mV
Input low AC voltage: Logic 0	$V_{IL(AC)175}$ MAX	-175	-	mV

- Notes:
1. All voltages are referenced to V_{REF} . V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
 2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
 3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
 4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Figure 13: Input Signal



Notes: 1. Numbers in diagrams reflect nominal values.

AC Overshoot/Undershoot Specification

Table 26: Control and Address Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure 14 on page 45)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 15 on page 45)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (see Figure 14 on page 45)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns
Maximum undershoot area below VSS (see Figure 15 on page 45)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns

Table 27: Clock, Data, Strobe, and Mask Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure 14 on page 45)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 15 on page 45)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}/V_{DDQ} (see Figure 14 on page 45)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns
Maximum undershoot area below V_{SS}/V_{SSQ} (see Figure 15 on page 45)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns

Figure 14: Overshoot

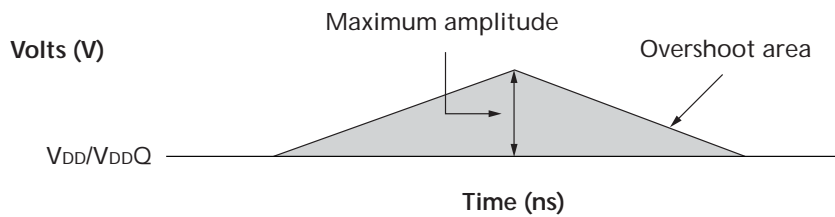


Figure 15: Undershoot

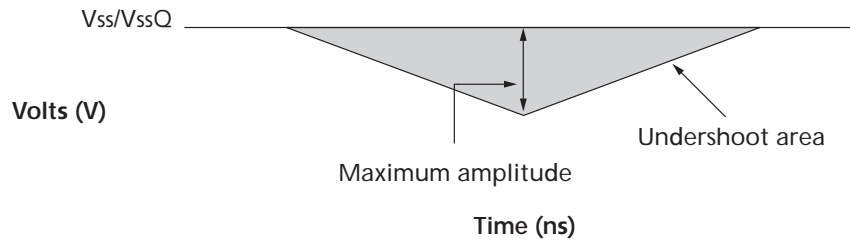


Table 28: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Differential input voltage logic high - slew	VIHDIFF(AC)slew	+200	n/a	mV	4
Differential input voltage logic low - slew	VILDIFF(AC)slew	n/a	-200	mV	4
Differential input voltage logic high	VIHDIFF(AC)	$2 \times (V_{IH(AC)} - V_{REF})$	VDD/VDDQ	mV	5
Differential input voltage logic low	VILDIFF(AC)	VSS/VSSQ	$2 \times (V_{REF} - V_{IL(AC)})$	mV	6
Differential input crossing voltage relative to VDD/2 for DQS, DQS#; CK, CK#	VIX	VREF(DC) - 150	VREF(DC) + 150	mV	7
Differential input crossing voltage relative to VDD/2 for CK, CK#	VIX (175)	VREF(DC) - 175	VREF(DC) + 175	mV	7, 8
Single-ended high level for strobes	VSHE	VDDQ/2 + VIH(AC)	VDDQ	mV	5
Single-ended high level for CK, CK#		VDD/2 + VIH(AC)	VDD	mV	5
Single-ended low level for strobes	VSEL	VSSQ	VDDQ/2 - VIL(AC)	mV	6
Single-ended low level for CK, CK#		VSS	VDD/2 - VIL(AC)	mV	6

- Notes:
1. Clock is referenced to VDD and VSS. Data strobe is referenced to VDDQ and VSSQ.
 2. Reference is VREFCA(DC) for clock and for VREFDQ(DC) for strobe.
 3. Differential input slew rate = 2 V/ns
 4. Defines slewrates reference points, relative to input crossing voltages.
 5. MAX limit is relative to single-ended signals, the overshoot specifications are applicable.
 6. MIN limit is relative to single-ended signals, the undershoot specifications are applicable.
 7. The typical value of VIX(AC) is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
 8. The VIX extended range ($\pm 175\text{mV}$) is allowed only for the clock, and this VIX extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing VSEL, VSEH of at least $V_{DD}/2 \pm 250\text{mV}$, and the differential slew rate of CK, CK# is greater than 3 V/ns.

Figure 16: Vix for Differential Signals

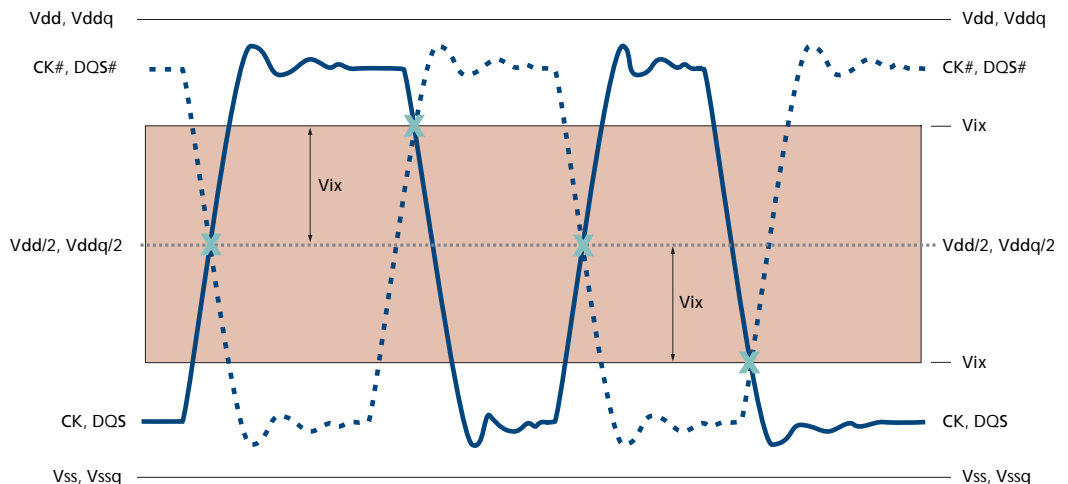


Figure 17: Single-Ended Requirements for Differential Signals

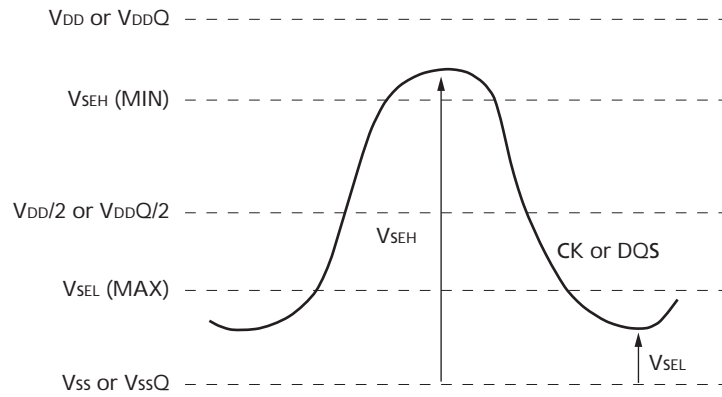


Figure 18: Definition of Differential AC-Swing and t_{DVAC}

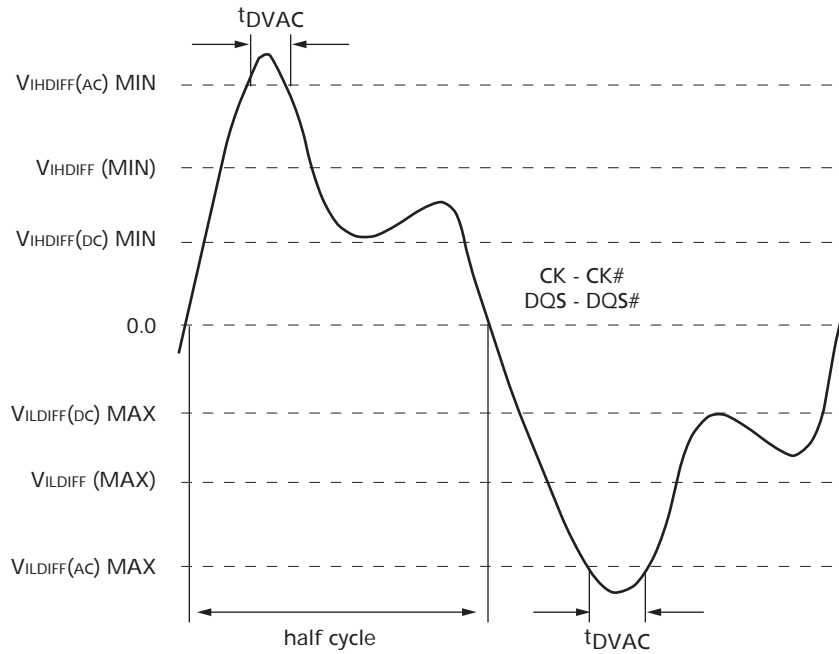


Table 29: Allowed Time Before Ringback (t_{DVAC}) for CK - CK# and DQS - DQS#
Below $V_{IL(AC)}$

Slew Rate (V/ns)	t_{DVAC} (ps) at $ V_{IHDIFF(AC)} \text{ to } V_{ILDIFF(AC)} $	
	350mV	300mV
>4.0	75	175
4.0	57	170
3.0	50	167
2.0	38	163
1.9	34	162
1.6	29	161
1.4	22	159
1.2	13	155
1.0	0	150
<1.0	0	150

Slew Rate Definitions for Single-Ended Input Signals

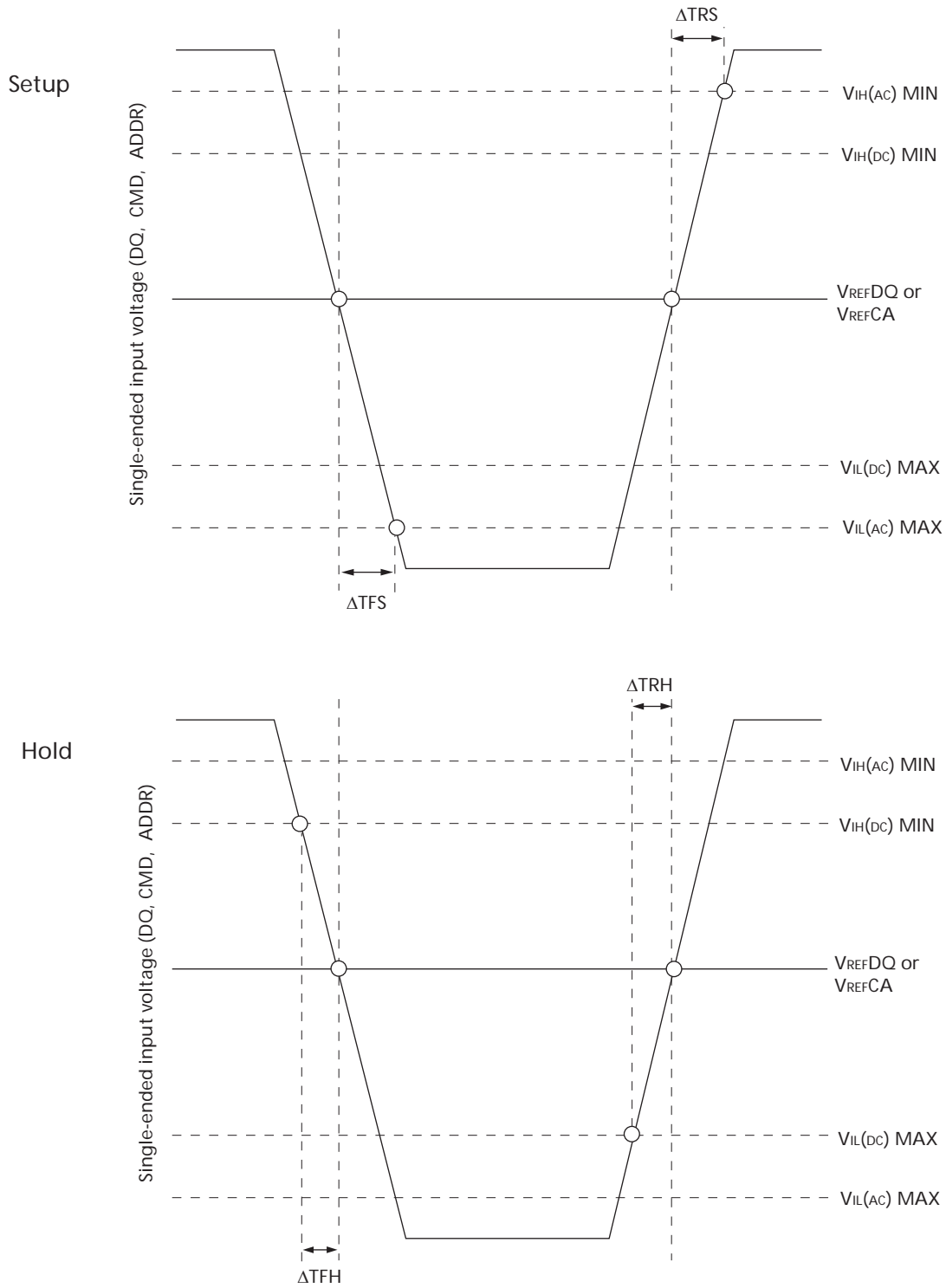
Setup (t_{IS} and t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC) MIN}$. Setup (t_{IS} and t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IL(AC) MAX}$ (see Figure 19 on page 50).

Hold (t_{IH} and t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC) MAX}$ and the first crossing of V_{REF} . Hold (t_{IH} and t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC) MIN}$ and the first crossing of V_{REF} (see Figure 19 on page 50).

Table 30: Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
Setup	Rising	V_{REF}	$V_{IH(AC) MIN}$	$\frac{V_{IH(AC) MIN} - V_{REF}}{\Delta TRS}$
	Falling	V_{REF}	$V_{IL(AC) MAX}$	$\frac{V_{REF} - V_{IL(AC) MAX}}{\Delta TFS}$
Hold	Rising	$V_{IL(DC) MAX}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC) MAX}}{\Delta TFH}$
	Falling	$V_{IH(DC) MIN}$	V_{REF}	$\frac{V_{IH(DC) MIN} - V_{REF}}{\Delta TRSH}$

Figure 19: Nominal Slew Rate Definition for Single-Ended Input Signals



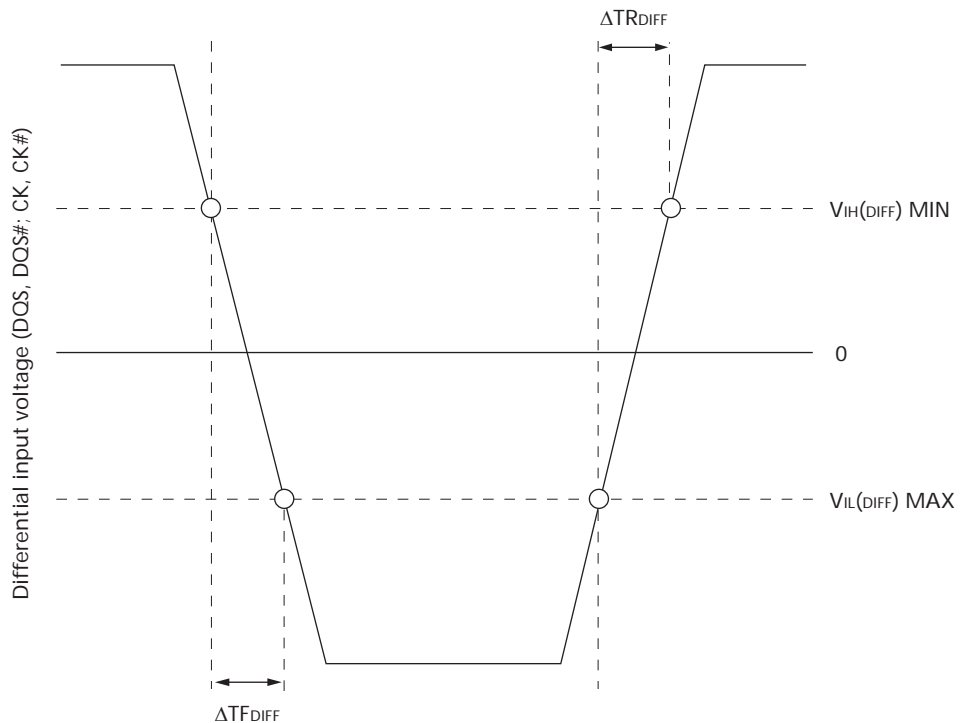
Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured, as shown in Table 31 and Figure 20. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL(DIFF) MAX}$ and $V_{IH(DIFF) MIN}$. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH(DIFF) MIN}$ and $V_{IL(DIFF) MAX}$.

Table 31: Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
CK and DQS reference	Rising	$V_{IL(DIFF) MAX}$	$V_{IH(DIFF) MIN}$	$\frac{V_{IH(DIFF) MIN} - V_{IL(DIFF) MAX}}{\Delta TR_{(DIFF)}}$
	Falling	$V_{IH(DIFF) MIN}$	$V_{IL(DIFF) MAX}$	$\frac{V_{IH(DIFF) MIN} - V_{IL(DIFF) MAX}}{\Delta TF_{(DIFF)}}$

Figure 20: Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#



ODT Characteristics

ODT effective resistance R_{TT} is defined by MR1 [9, 6, and 2]. ODT is applied to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls (x8 devices only). The ODT target values are listed in Table 32 and Table 33 on page 53. A functional representation of the ODT is shown in Figure 21. The individual pull-up and pull-down resistors ($R_{TT_{PU}}$ and $R_{TT_{PD}}$) are defined as follows:

- $R_{TT_{PU}} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$, under the condition that $R_{TT_{PD}}$ is turned off
- $R_{TT_{PD}} = (V_{OUT}) / |I_{OUT}|$, under the condition that $R_{TT_{PU}}$ is turned off

Figure 21: ODT Levels and I-V Characteristics

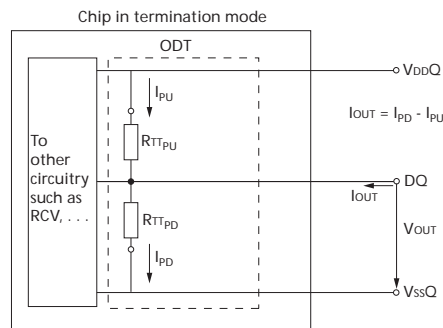


Table 32: On-Die Termination DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes	
R_{TT} effective impedance	R_{TT_EFF}	See Table 33 on page 53					1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	-5		+5	%	1, 2, 3	

- Notes:
1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$). Refer to "ODT Sensitivity" on page 53 if either the temperature or voltage changes after calibration.
 2. Measurement definition for R_{TT} : Apply $V_{IH(AC)}$ to pin under test and measure current $I[V_{IH(AC)}]$, then apply $V_{IL(AC)}$ to pin under test and measure current $I[V_{IL(AC)}]$:

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{|I(V_{IH(AC)}) - I(V_{IL(AC)})|}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1 \right) \times 100$$

4. For IT devices, the minimum values are derated by 6% when the device operates between -40°C and 0°C (T_C).

ODT Resistors

Table 33 on page 53 provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- $R_{TT} 120\Omega$ is made up of $R_{TT_{120PD240}}$ and $R_{TT_{120PU240}}$
- $R_{TT} 60\Omega$ is made up of $R_{TT_{60PD120}}$ and $R_{TT_{60PU120}}$
- $R_{TT} 40\Omega$ is made up of $R_{TT_{40PD80}}$ and $R_{TT_{40PU80}}$
- $R_{TT} 30\Omega$ is made up of $R_{TT_{30PD60}}$ and $R_{TT_{30PU60}}$
- $R_{TT} 20\Omega$ is made up of $R_{TT_{20PD40}}$ and $R_{TT_{20PU40}}$

Table 33: RTT Effective Impedances

MR1 [9, 6, 2]	RTT	Resistor	Vout	Min	Nom	Max	Units
0, 1, 0	120Ω	RTT _{120PD240}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/1
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/1
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/1
		RTT _{120PU240}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/1
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/1
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/1
	120Ω		VIL(AC) to VIH(AC)	0.9	1.0	1.6	RZQ/2
0, 0, 1	60Ω	RTT _{60PD120}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/2
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/2
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/2
		RTT _{60PU120}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/2
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/2
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/2
	60Ω		VIL(AC) to VIH(AC)	0.9	1.0	1.6	RZQ/4
0, 1, 1	40Ω	RTT _{40PD80}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/3
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/3
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/3
		RTT _{40PU80}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/3
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/3
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/3
	40Ω		VIL(AC) to VIH(AC)	0.9	1.0	1.6	RZQ/6
1, 0, 1	30Ω	RTT _{30PD60}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/4
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/4
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/4
		RTT _{30PU60}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/4
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/4
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/4
	30Ω		VIL(AC) to VIH(AC)	0.9	1.0	1.6	RZQ/8
1, 0, 0	20Ω	RTT _{20PD40}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/6
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/6
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/6
		RTT _{20PU40}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/6
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/6
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/6
	20Ω		VIL(AC) to VIH(AC)	0.9	1.0	1.6	RZQ/12

Notes: 1. Values assume an RZQ of 240Ω (±1%).

ODT Sensitivity

If either the temperature or voltage changes after I/O calibration, the tolerance limits listed in Table 32 on page 52 and Table 33 can be expected to widen according to Tables 34 and 35 on page 54.

Table 34: ODT Sensitivity Definition

Symbol	Min	Max	Units
RTT	$0.9 - dRTTdT \times DT - dRTTdV \times DV $	$1.6 + dRTTdT \times DT + dRTTdV \times DV $	RZO/(2, 4, 6, 8, 12)

Notes: 1. $\Delta T = T - T(@ \text{calibration})$, $\Delta V = V_{DDQ} - V_{DDQ}(@ \text{calibration})$ and $V_{DD} = V_{DDQ}$.

Table 35: ODT Temperature and Voltage Sensitivity

Change	Min	Max	Units
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

Notes: 1. $\Delta T = T - T(@ \text{calibration})$, $\Delta V = V_{DDQ} - V_{DDQ}(@ \text{calibration})$ and $V_{DD} = V_{DDQ}$.

ODT Timing Definitions

ODT loading differs from that used in AC timing measurements. The reference load for ODT timings is shown in Figure 22. Two parameters define when ODT turns on or off synchronously, two define when ODT turns on or off asynchronously, and another defines when ODT turns on or off dynamically. Table 36 outlines and provides definition and measurement reference settings for each parameter (see Figure 37 on page 55).

ODT turn-on time begins when the output leaves High-Z and ODT resistance begins to turn on. ODT turn-off time begins when the output leaves Low-Z and ODT resistance begins to turn off.

Figure 22: ODT Timing Reference Load

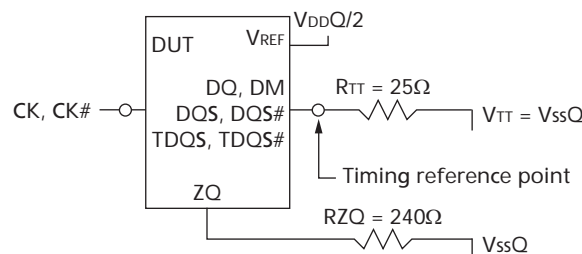


Table 36: ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - CK# defined by the end point of ODTL on	Extrapolated point at VssQ	Figure 23 on page 55
t_{AOF}	Rising edge of CK - CK# defined by the end point of ODTL off	Extrapolated point at VRTT_NOM	Figure 23 on page 55
t_{AONPD}	Rising edge of CK - CK# with ODT first being registered HIGH	Extrapolated point at VssQ	Figure 24 on page 56
t_{AOFPD}	Rising edge of CK - CK# with ODT first being registered LOW	Extrapolated point at VRTT_NOM	Figure 24 on page 56
t_{ADC}	Rising edge of CK - CK# defined by the end point of ODTLCNW, ODTLCWN4, or ODTLCWN8	Extrapolated points at VRTT_WR and VRTT_NOM	Figure 25 on page 56

Table 37: Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_NOM Setting	RTT_WR Setting	Vsw1	Vsw2
t_{AON}	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
t_{AOF}	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
t_{AONPD}	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
t_{AOFPD}	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
t_{ADC}	RZQ/12 (20Ω)	RZQ/2 (120Ω)	200mV	300mV

Notes: 1. Assume an RZQ of 240Ω (±1%) and that proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).

Figure 23: t_{AON} and t_{AOF} Definitions

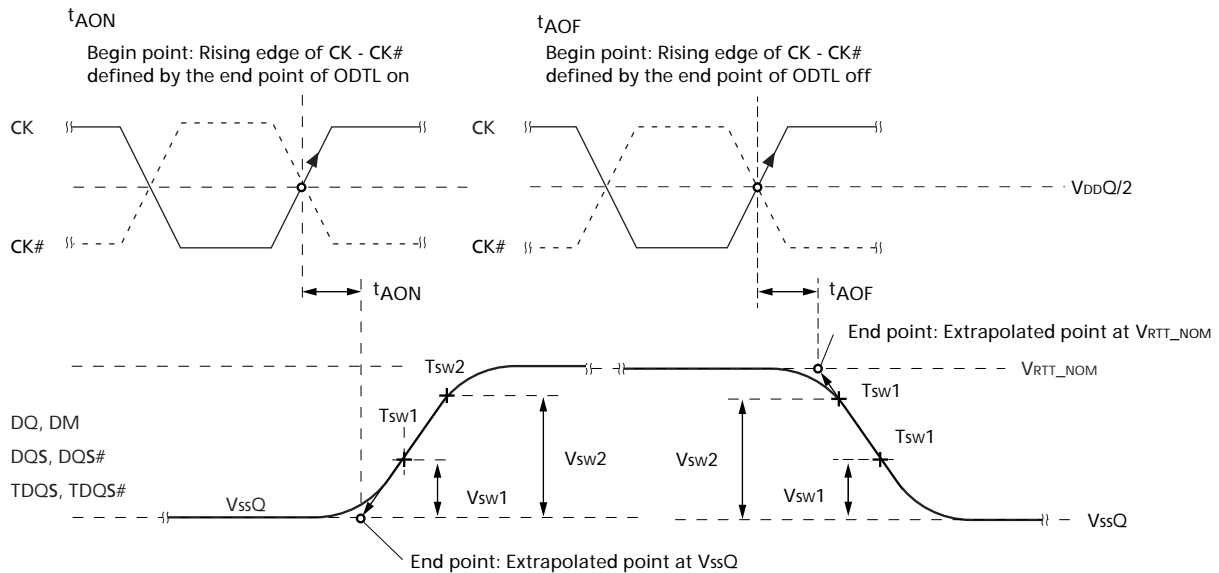


Figure 24: t_{AONPD} and t_{AOFPD} Definition

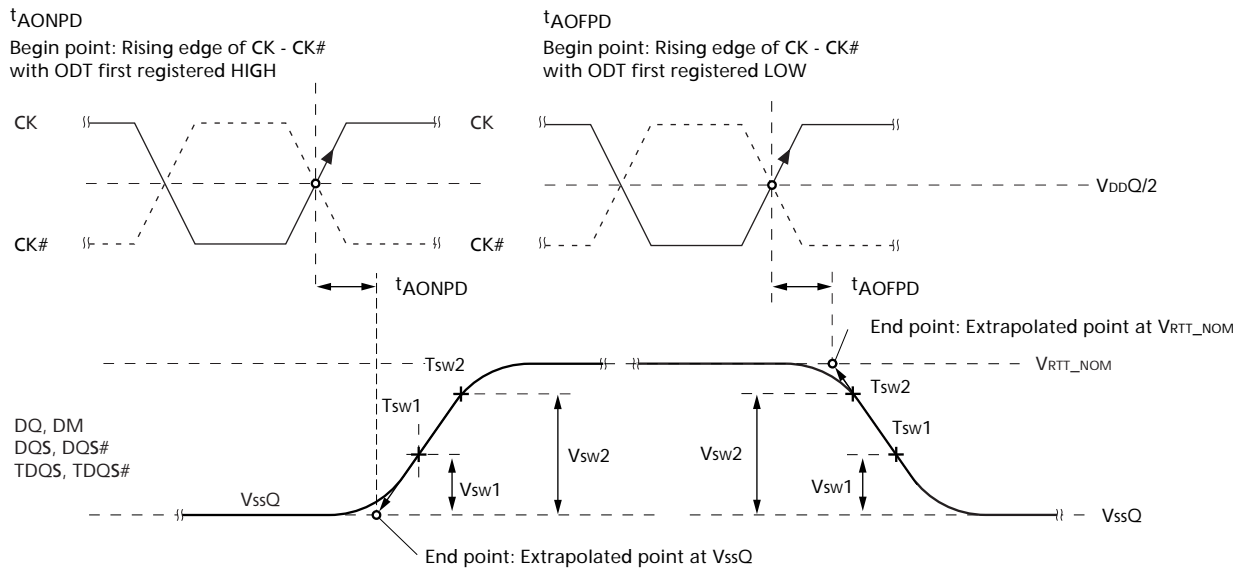
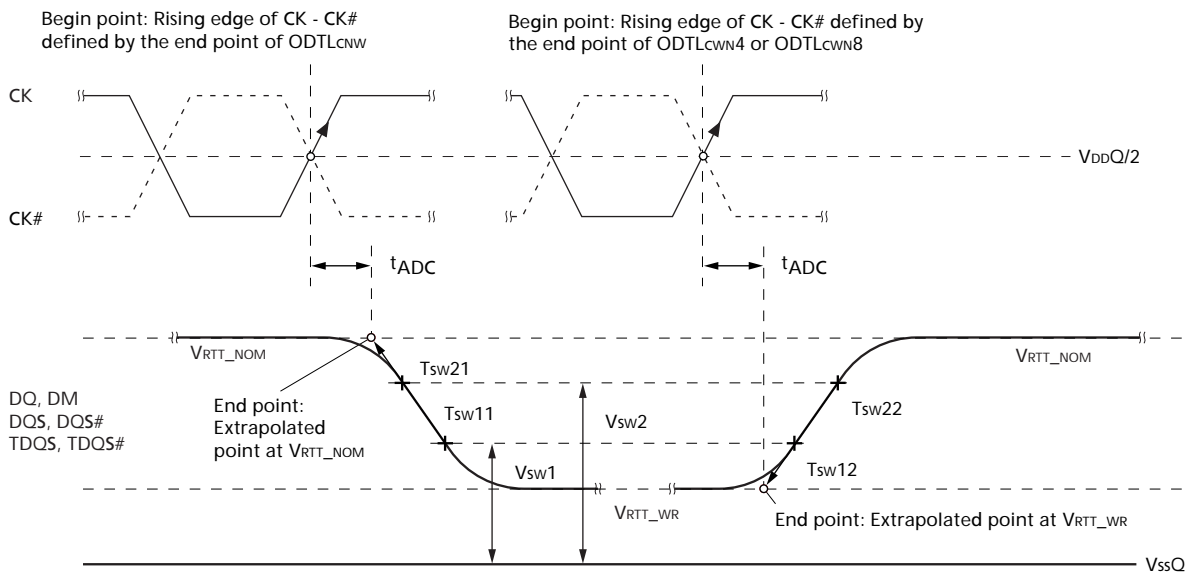


Figure 25: t_{ADC} Definition



Output Driver Impedance

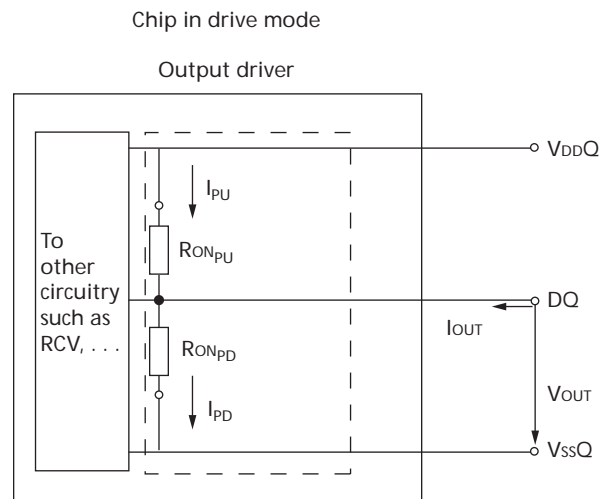
The output driver impedance is selected by MR1[5,1] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown in Figure 26 on page 57. The output driver impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows:

- $R_{ON_x} = RZQ/y$ (with $RZQ = 240\Omega \pm 1\%$; $x = 34\Omega$ or 40Ω with $y = 7$ or 6 , respectively)

The individual pull-up and pull-down resistors ($R_{ON_{PU}}$ and $R_{ON_{PD}}$) are defined as follows:

- $R_{ON_{PU}} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$, when $R_{ON_{PD}}$ is turned off
- $R_{ON_{PD}} = (V_{OUT})/|I_{OUT}|$, when $R_{ON_{PU}}$ is turned off

Figure 26: Output Driver



34 Ohm Output Driver Impedance

The 34Ω driver (MR1[5, 1] = 01) is the default driver. Unless otherwise stated, all timings and specifications listed herein apply to the 34Ω driver only. Its impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows: $R_{ON_{34}} = RZQ/7$ (with nominal $RZQ = 240\Omega \pm 1\%$) and is actually $34.3\Omega \pm 1\%$. The 34Ω output driver impedance characteristics are listed in Table 38 on page 58.

Table 38: 34Ω Driver Impedance Characteristics

MR1[5,1]	RON	Resistor	Vout	Min	Nom	Max	Units	Notes
0,1	34.3Ω	RON _{34PD}	0.2/VDDQ	0.6	1.0	1.1	RZQ/7	1
			0.5/VDDQ	0.9	1.0	1.1	RZQ/7	1
			0.8/VDDQ	0.9	1.0	1.4	RZQ/7	1
		RON _{34PU}	0.2/VDDQ	0.9	1.0	1.4	RZQ/7	1
			0.5/VDDQ	0.9	1.0	1.1	RZQ/7	1
			0.8/VDDQ	0.6	1.0	1.1	RZQ/7	1
Pull-up/pull-down mismatch (MM _{PUPD})			0.5/VDDQ	-10%	n/a	10	%	1, 2

- Notes:
1. Tolerance limits assume RZQ of 240Ω (±1%) and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS). Refer to “34 Ohm Driver Output Sensitivity” on page 59 if either the temperature or the voltage changes after calibration.
 2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both RON_{PU} and RON_{PD} at 0.5 × VDDQ:

$$MM_{PUPD} = \frac{RON_{PU} - RON_{PD}}{RON_{NOM}} \times 100$$

3. For IT devices, the minimum values are derated by 6% when the device operates between -40°C and 0°C (T_C).

34 Ohm Driver

The 34Ω driver’s current range has been calculated and summarized in Table 40 on page 59 for VDD = 1.5V, Table 41 on page 59 for VDD = 1.575V, and Table 42 on page 59 for VDD = 1.425V. The individual pull-up and pull-down resistors (RON_{34PD} and RON_{34PU}) are defined as follows:

- RON_{34PD} = (VOUT)/|IOUT|; RON_{34PU} is turned off
- RON_{34PU} = (VDDQ - VOUT)/|IOUT|; RON_{34PD} is turned off

Table 39: 34Ω Driver Pull-Up and Pull-Down Impedance Calculations

RON		Min	Nom	Max	Units		
RZQ = 240Ω ±1%		237.6	240	242.4	Ω		
RZQ/7 = (240Ω ±1%)/7		33.9	34.3	34.6	Ω		
MR1[5,1]	RON	Resistor	Vout	Min	Nom	Max	Units
0, 1	34.3Ω	RON _{34PD}	0.2 × VDDQ	20.4	34.3	38.1	Ω
			0.5 × VDDQ	30.5	34.3	38.1	Ω
			0.8 × VDDQ	30.5	34.3	48.5	Ω
		RON _{34PU}	0.2 × VDDQ	30.5	34.3	48.5	Ω
			0.5 × VDDQ	30.5	34.3	38.1	Ω
			0.8 × VDDQ	20.4	34.3	38.1	Ω

Table 40: 34Ω Driver IOH/IOL Characteristics: VDD = VDDQ = 1.5V

MR1[5,1]	RON	Resistor	VOUT	Max	Nom	Min	Units
0, 1	34.3Ω	RON _{34PD}	IOL @ 0.2 × VDDQ	14.7	8.8	7.9	mA
			IOL @ 0.5 × VDDQ	24.6	21.9	19.7	mA
			IOL @ 0.8 × VDDQ	39.3	35.0	24.8	mA
		RON _{34PU}	IOH @ 0.2 × VDDQ	39.3	35.0	24.8	mA
			IOH @ 0.5 × VDDQ	24.6	21.9	19.7	mA
			IOH @ 0.8 × VDDQ	14.7	8.8	7.9	mA

Table 41: 34Ω Driver IOH/IOL Characteristics: VDD = VDDQ = 1.575V

MR1[5,1]	RON	Resistor	VOUT	Max	Nom	Min	Units
0, 1	34.3Ω	RON _{34PD}	IOL @ 0.2 × VDDQ	15.5	9.2	8.3	mA
			IOL @ 0.5 × VDDQ	25.8	23	20.7	mA
			IOL @ 0.8 × VDDQ	41.2	36.8	26	mA
		RON _{34PU}	IOH @ 0.2 × VDDQ	41.2	36.8	26	mA
			IOH @ 0.5 × VDDQ	25.8	23	20.7	mA
			IOH @ 0.8 × VDDQ	15.5	9.2	8.3	mA

Table 42: 34Ω Driver IOH/IOL Characteristics: VDD = VDDQ = 1.425V

MR1[5,1]	RON	Resistor	VOUT	Max	Nom	Min	Units
0, 1	34.3Ω	RON _{34PD}	IOL @ 0.2 × VDDQ	14.0	8.3	7.5	mA
			IOL @ 0.5 × VDDQ	23.3	20.8	18.7	mA
			IOL @ 0.8 × VDDQ	37.3	33.3	23.5	mA
		RON _{34PU}	IOH @ 0.2 × VDDQ	37.3	33.3	23.5	mA
			IOH @ 0.5 × VDDQ	23.3	20.8	18.7	mA
			IOH @ 0.8 × VDDQ	14.0	8.3	7.5	mA

34 Ohm Driver Output Sensitivity

If either the temperature or the voltage changes after ZQ calibration, the tolerance limits listed in Table 38 on page 58 can be expected to widen according to Table 43 and Table 44 on page 60.

Table 43: 34Ω Output Driver Sensitivity Definition

Symbol	Min	Max	Units
RON @ 0.8 × VDDQ	0.9 - dRONdTH × ΔT - dRONdVH × ΔV	1.1 + dRONdTH × ΔT + dRONdVH × ΔV	RZQ/7
RON @ 0.5 × VDDQ	0.9 - dRONdTM × ΔT - dRONdVM × ΔV	1.1 + dRONdTM × ΔT + dRONdVM × ΔV	RZQ/7
RON @ 0.2 × VDDQ	0.9 - dRONdTL × ΔT - dRONdVL × ΔV	1.1 + dRONdTL × ΔT + dRONdVL × ΔV	RZQ/7

Notes: 1. ΔT = T - T(@ calibration), ΔV = VDDQ - VDDQ(@ calibration), and VDD = VDDQ.

Table 44: 34Ω Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Units
dRondTM	0	1.5	%/°C
dRondVM	0	0.13	%/mV
dRondTL	0	1.5	%/°C
dRondVL	0	0.13	%/mV
dRondTH	0	1.5	%/°C
dRondVH	0	0.13	%/mV

Alternative 40 Ohm Driver

Table 45: 40Ω Driver Impedance Characteristics

MR1[5,1]	RON	Resistor	Vout	Min	Nom	Max	Units	Notes
0,0	40Ω	RON _{40PD}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/6	1, 2
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/6	1, 2
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/6	1, 2
		RON _{40PU}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/6	1, 2
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/6	1, 2
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/6	1, 2
Pull-up/pull-down mismatch (MM _{PUPD})			0.5 × VDDQ	-10%	n/a	10	%	1, 2

- Notes:
1. Tolerance limits assume RZQ of 240Ω (±1%) and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS). Refer to “40 Ohm Driver Output Sensitivity” on page 60 if either the temperature or the voltage changes after calibration.
 2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both RON_{PU} and RON_{PD} at 0.5 × VDDQ:

$$MM_{PUPD} = \frac{RON_{PU} - RON_{PD}}{RON_{Nom}} \times 100$$

3. For IT devices, the minimum values are derated by six% when the device operates between -40°C and 0°C (T_C).

40 Ohm Driver Output Sensitivity

If either the temperature or the voltage changes after I/O calibration, the tolerance limits listed in Table 45 can be expected to widen according to Table 46 and Table 47 on page 61.

Table 46: 40Ω Output Driver Sensitivity Definition

Symbol	Min	Max	Units
RON @ 0.8 × VDDQ	0.9 - dRondTH × ΔT - dRondVH × ΔV	1.1 + dRondTH × ΔT + dRondVH × ΔV	RZQ/6
RON @ 0.5 × VDDQ	0.9 - dRondTM × ΔT - dRondVM × ΔV	1.1 + dRondTM × ΔT + dRondVM × ΔV	RZQ/6
RON @ 0.2 × VDDQ	0.9 - dRondTL × ΔT - dRondVL × ΔV	1.1 + dRondTL × ΔT + dRondVL × ΔV	RZQ/6

- Notes:
1. ΔT = T - T(@ calibration), ΔV = VDDQ - VDDQ(@ calibration), and VDD = VDDQ.

Table 47: 40Ω Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
dRondTM	0	1.5	%/°C
dRondVM	0	0.15	%/mV
dRondTL	0	1.5	%/°C
dRondVL	0	0.15	%/mV
dRondTH	0	1.5	%/°C
dRondVH	0	0.15	%/mV

Output Characteristics and Operating Conditions

The DRAM uses both single-ended and differential output drivers. The single-ended output driver is summarized in Table 48 while the differential output driver is summarized in Table 49 on page 62.

Table 48: Single-Ended Output Driver Characteristics

All voltages are referenced to Vss

Parameter/Condition	Symbol	Min	Max	Units	Notes
Output leakage current: DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$; ODT is disabled; ODT is HIGH	IOZ	-5	+5	μA	1
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 \times V_{DDQ}$	SRQSE	2.5	6	V/ns	1, 2, 3, 4
Single-ended DC high-level output voltage	VOH(DC)	$0.8 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC mid-point level output voltage	VOM(DC)	$0.5 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC low-level output voltage	VOL(DC)	$0.2 \times V_{DDQ}$		V	1, 2, 5
Single-ended AC high-level output voltage	VOH(AC)	$V_{TT} + 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Single-ended AC low-level output voltage	VOL(AC)	$V_{TT} - 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Delta RON between pull-up and pull-down for DQ/DQS	MM _{PUPD}	-10	+10	%	1, 7
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25Ω resistor				3

- Notes:
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$).
 2. $V_{TT} = V_{DDQ}/2$.
 3. See Figure 29 on page 63 for the test load configuration.
 4. The 6 V/ns maximum is applicable for a single DQ signal when it is switching from either HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5V/ns.
 5. See Table 38 on page 58 for IV curve linearity. Do not use AC test load.
 6. See Table 50 on page 64 for output slew rate.
 7. See Table 38 on page 58 for additional information.
 8. See Figure 27 on page 62 for an example of a single-ended output signal.

Table 49: Differential Output Driver Characteristics

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
Output leakage current: DQ are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ} ; ODT is disabled; ODT is HIGH	I _{OZ}	-5	+5	μA	1
Output slew rate: Differential; For rising and falling edges, measure between V _{OLDIFF(AC)} = -0.2 × V _{DDQ} and V _{OHDIFF(AC)} = +0.2 × V _{DDQ}	SR _{QDIFF}	5	12	V/ns	1
Output differential cross-point voltage	V _{OX(AC)}	V _{REF} - 150	V _{REF} + 150	mV	1, 2, 3
Differential high-level output voltage	V _{OHDIFF(AC)}	+0.2 × V _{DDQ}		V	1, 4
Differential low-level output voltage	V _{OLDIFF(AC)}	-0.2 × V _{DDQ}		V	1, 4
Delta RON between pull-up and pull-down for DQ/DQS	MM _{PUPD}	-10	+10	%	1, 5
Test load for AC timing and output slew rates	Output to V _{TT} (V _{DDQ} /2) via 25Ω resistor				3

- Notes:
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
 2. V_{REF} = V_{DDQ}/2.
 3. See Figure 29 on page 63 for the test load configuration.
 4. See Table 51 on page 65 for the output slew rate.
 5. See Table 38 on page 58 for additional information.
 6. See Figure 28 on page 63 for an example of a differential output signal.

Figure 27: DQ Output Signal

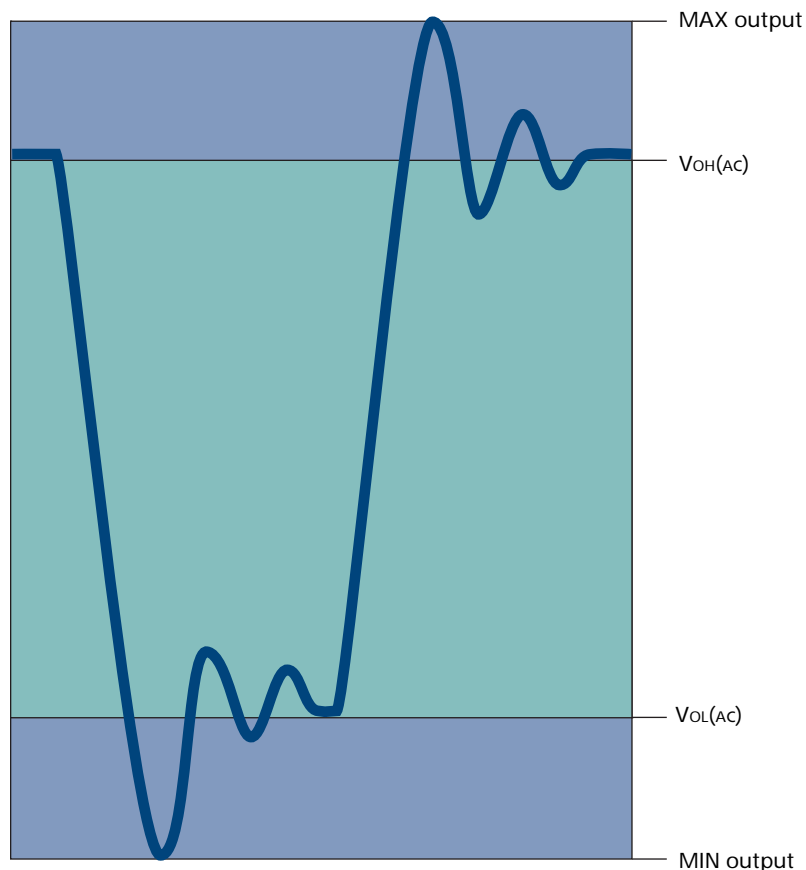
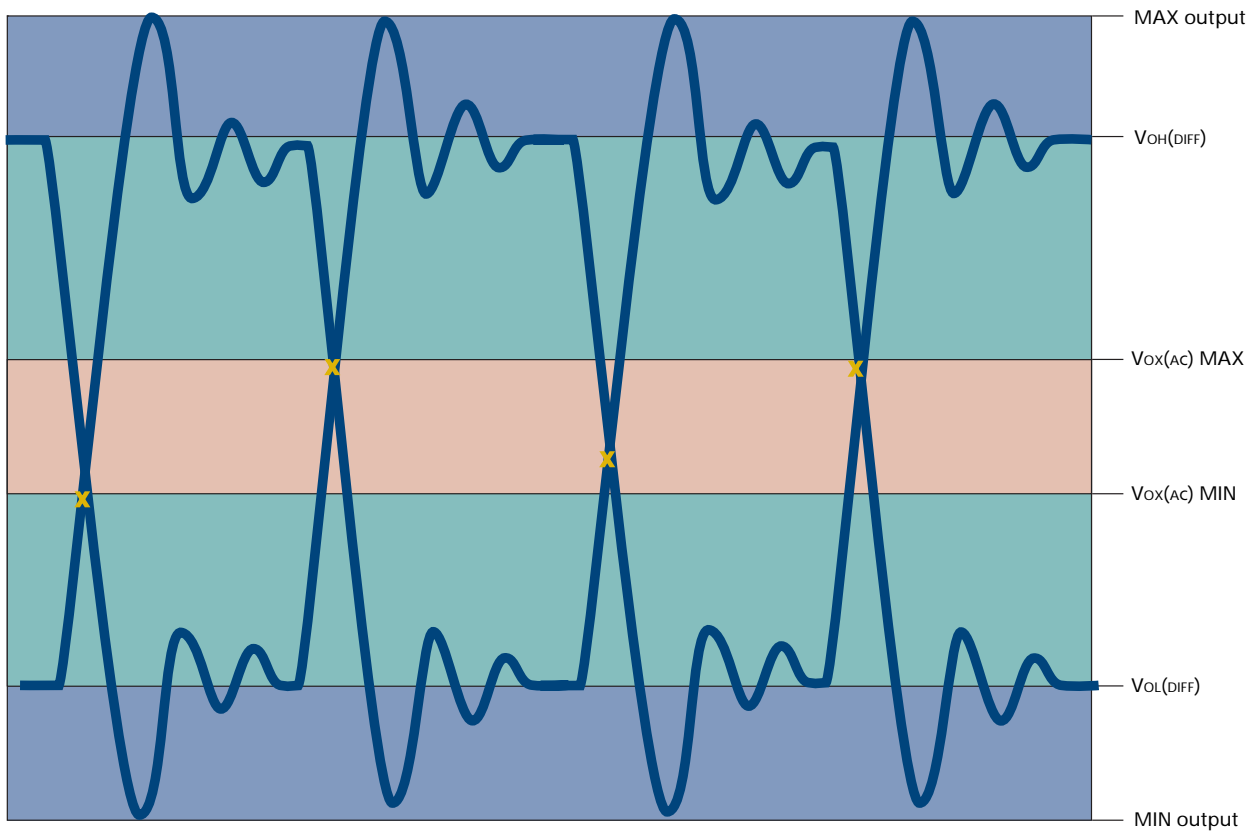


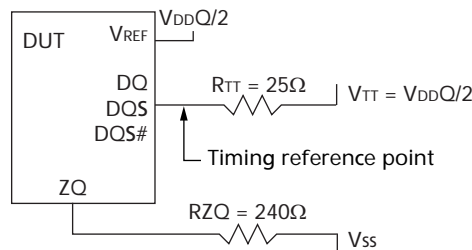
Figure 28: Differential Output Signal



Reference Output Load

Figure 29 represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODT reference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Figure 29: Reference Output Load for AC Timing and Output Slew Rate



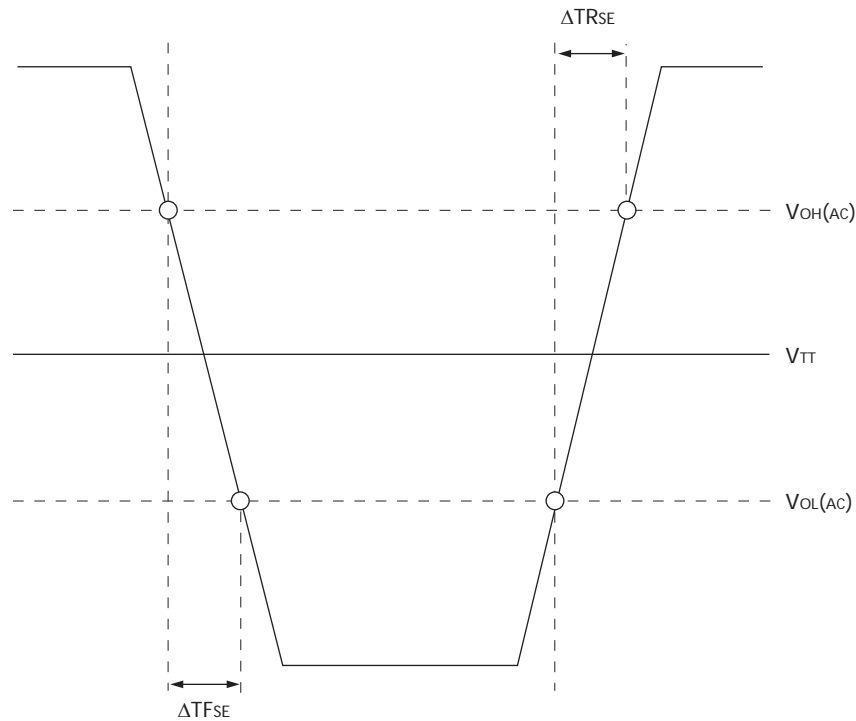
Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized in Table 48 on page 61. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals, as shown in Table 50 and Figure 30.

Table 50: Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQ	Rising	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR_{SE}}$
	Falling	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TF_{SE}}$

Figure 30: Nominal Slew Rate Definition for Single-Ended Output Signals



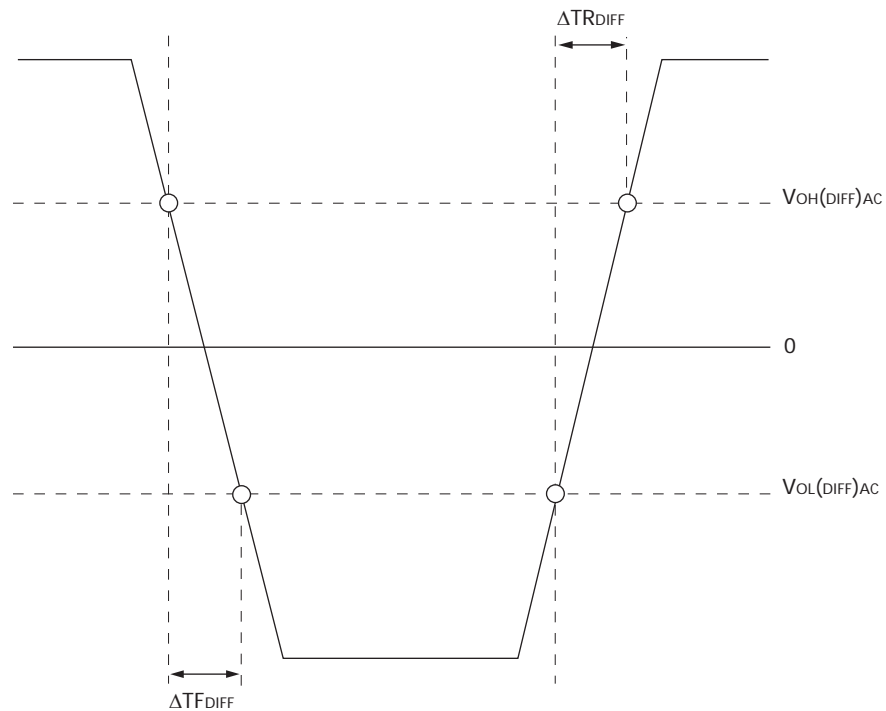
Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized in Table 49 on page 62. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for differential signals, as shown in Table 51 and Figure 31.

Table 51: Differential Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQS, DQS#	Rising	VOLDIFF(AC)	VOHDIFF(AC)	$\frac{VOHDIFF(AC) - VOLDIFF(AC)}{\Delta TR_{DIFF}}$
	Falling	VOHDIFF(AC)	VOLDIFF(AC)	$\frac{VOHDIFF(AC) - VOLDIFF(AC)}{\Delta TF_{DIFF}}$

Figure 31: Nominal Differential Output Slew Rate Definition for DQS, DQS#



Speed Bin Tables

Table 52: DDR3-800 Speed Bins

DDR3-800 Speed Bin			-25E		-25		Units	Notes
CL- ^t RCD- ^t RP			5-5-5		6-6-6			
Parameter	Symbol		Min	Max	Min	Max		
ACTIVATE to internal READ or WRITE delay time	^t RCD		12.5	–	15	–	ns	
PRECHARGE command period	^t RP		12.5	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC		50	–	52.5	–	ns	
ACTIVATE-to-PRECHARGE command period	^t RAS		37.5	60ms	37.5	60ms	ns	1
CL = 5	CWL = 5	^t CK (AVG)	2.5	3.3	3.0	3.3	ns	2, 3
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	2.5	3.3	ns	2
Supported CL settings			5, 6		5, 6		CK	
Supported CWL settings			5		5		CK	

- Notes:
- ^tREFI depends on T_{OPER}.
 - The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 - Reserved settings are not allowed.

Table 53: DDR3-1066 Speed Bins

DDR3-1066 Speed Bin			-187E		-187		Units	Notes
CL- ^t RCD- ^t RP			7-7-7		8-8-8			
Parameter	Symbol		Min	Max	Min	Max		
ACTIVATE to internal READ or WRITE delay time	^t RCD		13.125	-	15	-	ns	
PRECHARGE command period	^t RP		13.125	-	15	-	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC		50.625	-	52.5	-	ns	
ACTIVATE-to-PRECHARGE command period	^t RAS		37.5	60ms	37.5	60ms	ns	1
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	3.0	3.3	ns	2, 3
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	2, 3
CL = 7	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	Reserved		ns	2, 3
CL = 8	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2
Supported CL settings			5, 6, 7, 8		5, 6, 8		CK	
Supported CWL settings			5, 6		5, 6		CK	

- Notes:
- ^tREFI depends on T_{OPER}.
 - The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 - Reserved settings are not allowed.

Table 54: DDR3-1333 Speed Bins

DDR3-1333 Speed Bin			-15E		-15		Units	Notes
CL- ^t RCD- ^t RP			9-9-9		10-10-10			
Parameter	Symbol		Min	Max	Min	Max		
ACTIVATE to internal READ or WRITE delay time	^t RCD		13.125	–	15	–	ns	
PRECHARGE command period	^t RP		13.125	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC		49.5	–	51	–	ns	
ACTIVATE-to-PRECHARGE command period	^t RAS		36	60ms	36	60ms	ns	1
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	3.0	3.3	ns	2, 3
	CWL = 6, 7	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	2, 3
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 7	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	Reserved		ns	2, 3
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	2, 3
CL = 8	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	2, 3
CL = 9	CWL = 5, 6	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 7	^t CK (AVG)	1.5	<1.875	Reserved		ns	2, 3
CL = 10	CWL = 5, 6	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 7	^t CK (AVG)	1.5	<1.875	1.5	<1.875	ns	2
Supported CL settings			5, 6, 7, 8, 9, 10		5, 6, 8, 10		CK	
Supported CWL settings			5, 6, 7		5, 6, 7		CK	

- Notes:
- ^tREFI depends on T_{OPER}.
 - The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 - Reserved settings are not allowed.

Table 55: DDR3-1600 Speed Bins

DDR3-1600 Speed Bin			-125E		-125		Units	Notes
CL- ^t RCD- ^t RP			10-10-10		11-11-11			
Parameter	Symbol		Min	Max	Min	Max		
ACTIVATE to internal READ or WRITE delay time	^t RCD		12.5	–	13.125	–	ns	
PRECHARGE command period	^t RP		12.5	–	13.125	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC		47.5	–	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period	^t RAS		35	60ms	35	60ms	ns	1
CL = 5	CWL = 5	^t CK (AVG)	2.5	3.3	3.0	3.3	ns	2, 3
	CWL = 6, 7, 8	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	2, 3
	CWL = 7, 8	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 7	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2, 3
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	2, 3
	CWL = 8	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 8	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	2, 3
	CWL = 8	^t CK (AVG)	Reserved		Reserved		ns	2, 3
CL = 9	CWL = 5, 6	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 7	^t CK (AVG)	1.5	<1.875	1.5	<1.875	ns	2, 3
	CWL = 8	^t CK (AVG)	Reserved		Reserved		ns	2, 3
CL = 10	CWL = 5, 6	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 7	^t CK (AVG)	1.5	<1.875	1.5	<1.875	ns	2
	CWL = 8	^t CK (AVG)	1.25	<1.5	Reserved		ns	2, 3
CL = 11	CWL = 5, 6, 7	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 8	^t CK (AVG)	1.25	<1.5	1.25	<1.5	ns	2
Supported CL settings			5, 6, 7, 8, 9, 10, 11		5, 6, 7, 8, 9, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		5, 6, 7, 8		CK	

- Notes:
- ^tREFI depends on T_{OPER}.
 - The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 - Reserved settings are not allowed.

Table 56: Electrical Characteristics and AC Operating Conditions (Sheet 1 of 6)

Notes: 1-8 apply to the entire table; notes appear on page 76

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes		
		Min	Max	Min	Max	Min	Max	Min	Max				
Clock Timing													
Clock period average: DLL disable mode	$T_C = 0^\circ\text{C to } 85^\circ\text{C}$	t_{CKDLL_DIS}	8	7,800	8	7,800	8	7,800	8	7,800	ns	9, 42	
	$T_C = >85^\circ\text{C to } 95^\circ\text{C}$		8	3,900	8	3,900	8	3,900	8	3,900	ns	42	
Clock period average: DLL enable mode	$t_{CK (AVG)}$	See "Speed Bin Tables" on page 66 for t_{CK} range allowed									ns	10, 11	
High pulse width average	$t_{CH (AVG)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12		
Low pulse width average	$t_{CL (AVG)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12		
Clock period jitter	DLL locked	t_{JITPER}	-100	100	-90	90	-80	80	-70	70	ps	13	
	DLL locking	$t_{JITPER, LCK}$	-90	90	-80	80	-70	70	-60	60	ps	13	
Clock absolute period	$t_{CK(ABS)}$	MIN = $t_{CK (AVG) MIN} + t_{JITPER MIN}$; MAX = $t_{CK (AVG) MAX} + t_{JITPER MAX}$										ps	
Clock absolute high pulse width	$t_{CH (ABS)}$	0.43	-	0.43	-	0.43	-	0.43	-	$t_{CK (AVG)}$	14		
Clock absolute low pulse width	$t_{CL (ABS)}$	0.43	-	0.43	-	0.43	-	0.43	-	$t_{CK (AVG)}$	15		
Cycle-to-cycle jitter	DLL locked	t_{JITCC}	200		180		160		140		ps	16	
	DLL locking	$t_{JITCC, LCK}$	180		160		140		120		ps	16	
Cumulative error across	2 cycles	$t_{ERR_{2PER}}$	-147	147	-132	132	-118	118	-103	103	ps	17	
	3 cycles	$t_{ERR_{3PER}}$	-175	175	-157	157	-140	140	-122	122	ps	17	
	4 cycles	$t_{ERR_{4PER}}$	-194	194	-175	175	-155	155	-136	136	ps	17	
	5 cycles	$t_{ERR_{5PER}}$	-209	209	-188	188	-168	168	-147	147	ps	17	
	6 cycles	$t_{ERR_{6PER}}$	-222	222	-200	200	-177	177	-155	155	ps	17	
	7 cycles	$t_{ERR_{7PER}}$	-232	232	-209	209	-186	186	-163	163	ps	17	
	8 cycles	$t_{ERR_{8PER}}$	-241	241	-217	217	-193	193	-169	169	ps	17	
	9 cycles	$t_{ERR_{9PER}}$	-249	249	-224	224	-200	200	-175	175	ps	17	
	10 cycles	$t_{ERR_{10PER}}$	-257	257	-231	231	-205	205	-180	180	ps	17	
	11 cycles	$t_{ERR_{11PER}}$	-263	263	-237	237	-210	210	-184	184	ps	17	
	12 cycles	$t_{ERR_{12PER}}$	-269	269	-242	242	-215	215	-188	188	ps	17	
	$n = 13, 14 \dots 49, 50$ cycles	$t_{ERR_{nPER}}$	$t_{ERR_{nPER} MIN} = (1 + 0.68 \ln[n]) \times t_{JITPER MIN}$ $t_{ERR_{nPER} MAX} = (1 + 0.68 \ln[n]) \times t_{JITPER MAX}$									ps	17

Table 56: Electrical Characteristics and AC Operating Conditions (Sheet 2 of 6)

Notes: 1–8 apply to the entire table; notes appear on page 76

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes	
		Min	Max	Min	Max	Min	Max	Min	Max			
DQ Input Timing												
Data setup time to DQS, DQS#	Base (specification)	^t DS	75	–	25	–	–	–	–	–	ps	18, 19
	VREF @ 1 V/ns	AC175	250	–	200	–	–	–	–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	^t DS	125	–	75	–	30	–	10	–	ps	18, 19
	VREF @ 1 V/ns	AC150	275	–	250	–	180	–	160	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	^t DH	150	–	100	–	65	–	45	–	ps	18, 19
	VREF @ 1 V/ns	AC100	250	–	200	–	165	–	145	–	ps	19, 20
Minimum data pulse width		^t DIPW	600	–	490	–	400	–	360	–	ps	41
DQ Output Timing												
DQS, DQS# to DQ skew, per access		^t DQSQ	–	200	–	150	–	125	–	100	ps	
DQ output hold time from DQS, DQS#		^t QH	0.38	–	0.38	–	0.38	–	0.38	–	^t CK (AVG)	21
DQ Low-Z time from CK, CK#		^t LZ (DQ)	–800	400	–600	300	–500	250	–450	225	ps	22, 23
DQ High-Z time from CK, CK#		^t HZ (DQ)	–	400	–	300	–	250	–	225	ps	22, 23
DQ Strobe Input Timing												
DQS, DQS# rising to CK, CK# rising		^t DQSS	–0.25	0.25	–0.25	0.25	–0.25	0.25	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		^t DQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		^t DQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		^t DSS	0.2	–	0.2	–	0.2	–	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		^t DSH	0.2	–	0.2	–	0.2	–	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		^t WPRE	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		^t WPST	0.3	–	0.3	–	0.3	–	0.3	–	CK	
DQ Strobe Output Timing												
DQS, DQS# rising to/from rising CK, CK#		^t DQCK	–400	400	–300	300	–255	255	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		^t DQCK DLL_DIS	1	10	1	10	1	10	1	10	ns	26
DQS, DQS# differential output high time		^t QSH	0.38	–	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		^t QSL	0.38	–	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		^t LZ (DQS)	–800	400	–600	300	–500	250	–450	225	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		^t HZ (DQS)	–	400	–	300	–	250	–	225	ps	22, 23
DQS, DQS# differential READ preamble		^t RPRE	0.9	Note 24	0.9	Note 24	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		^t RPST	0.3	Note 27	0.3	Note 27	0.3	Note 27	0.3	Note 27	CK	23, 27

Table 56: Electrical Characteristics and AC Operating Conditions (Sheet 3 of 6)

Notes: 1-8 apply to the entire table; notes appear on page 76

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes	
		Min	Max	Min	Max	Min	Max	Min	Max			
Command and Address Timing												
DLL locking time	t_{DLLK}	512	-	512	-	512	-	512	-	CK	28	
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	t_{IS}	200	-	125	-	65	-	45	-	ps	29, 30
	VREF @ 1 V/ns	AC175	375	-	300	-	240	-	220	-	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	t_{IS}	350	-	275	-	190	-	170	-	ps	29, 30
	VREF @ 1 V/ns	AC150	500	-	425	-	340	-	320	-	ps	20, 30
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	t_{IH}	275	-	200	-	140	-	120	-	ps	29, 30
	VREF @ 1 V/ns	DC100	375	-	300	-	240	-	220	-	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width	t_{IPW}	900	-	780	-	620	-	560	-	ps	41	
ACTIVATE to internal READ or WRITE delay	t_{RCD}	See "Speed Bin Tables" on page 66 for t_{RCD}									ns	31
PRECHARGE command period	t_{RP}	See "Speed Bin Tables" on page 66 for t_{RP}									ns	31
ACTIVATE-to-PRECHARGE command period	t_{RAS}	See "Speed Bin Tables" on page 66 for t_{RAS}									ns	31, 32
ACTIVATE-to-ACTIVATE command period	t_{RC}	See "Speed Bin Tables" on page 66 for t_{RC}									ns	31
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	t_{RRD}	MIN = greater of 4CK or 10ns	MIN = greater of 4CK or 7.5ns	MIN = greater of 4CK or 6ns	MIN = greater of 4CK or 6ns					CK	31
	2KB page size		MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns						CK	31
Four ACTIVATE windows for 1KB page size	t_{FAW}	40	-	37.5	-	30	-	30	-	ns	31	
Four ACTIVATE windows for 2KB page size		50	-	50	-	45	-	40	-	ns	31	
Write recovery time	t_{WR}	MIN = 15ns; MAX = n/a									ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command	t_{WTR}	MIN = greater of 4CK or 7.5ns; MAX = n/a									CK	31, 34
READ-to-PRECHARGE time	t_{RTP}	MIN = greater of 4CK or 7.5ns; MAX = n/a									CK	31, 32
CAS#-to-CAS# command delay	t_{CCD}	MIN = 4CK; MAX = n/a									CK	
Auto precharge write recovery + precharge time	t_{DAL}	MIN = WR + t_{RP}/t_{CK} (AVG); MAX = n/a									CK	
MODE REGISTER SET command cycle time	t_{MRD}	MIN = 4CK; MAX = n/a									CK	
MODE REGISTER SET command update delay	t_{MOD}	MIN = greater of 12CK or 15ns; MAX = n/a									CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit	t_{MPRR}	MIN = 1CK; MAX = n/a									CK	

Table 56: Electrical Characteristics and AC Operating Conditions (Sheet 4 of 6)

Notes: 1–8 apply to the entire table; notes appear on page 76

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes	
		Min	Max	Min	Max	Min	Max	Min	Max			
Calibration Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	t_{ZQINIT}	512	–	512	–	512	–	512	–	CK	
	Normal operation	t_{ZQOPER}	256	–	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		t_{ZQCS}	64	–	64	–	64	–	64	–	CK	
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		t_{XPR}	MIN = greater of 5CK or $t_{RFC} + 10ns$; MAX = n/a								CK	
Begin power supply ramp to power supplies stable		t_{VDDPR}	MIN = n/a; MAX = 200								ms	
RESET# LOW to power supplies stable		t_{RPS}	MIN = 0; MAX = 200								ms	
RESET# LOW to I/O and RTT High-Z		t_{IOZ}	MIN = n/a; MAX = 20								ns	35
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period		t_{RFC}	MIN = 160; MAX = $9 \times t_{REFI}$ (REFRESH-to-REFRESH command period)								ns	
Maximum refresh period	$T_C \leq 85^\circ C$	–	64 (1X)								ms	36
	$T_C > 85^\circ C$	–	32 (2X)								ms	36
Maximum average periodic refresh	$T_C \leq 85^\circ C$	t_{REFI}	7.8 (64ms/8,192)								μs	36
	$T_C > 85^\circ C$	t_{REFI}	3.9 (32ms/8,192)								μs	36
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL		t_{XS}	MIN = greater of 5CK or $t_{RFC} + 10ns$; MAX = n/a								CK	
Exit self refresh to commands requiring a locked DLL		t_{XSDLL}	MIN = t_{DLLK} (MIN); MAX = n/a								CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		t_{CKESR}	MIN = t_{CKE} (MIN) + CK; MAX = n/a								CK	
Valid clocks after self refresh entry or power-down entry		t_{CKSRE}	MIN = greater of 5CK or 10ns; MAX = n/a								CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		t_{CKSRX}	MIN = greater of 5CK or 10ns; MAX = n/a								CK	

Table 56: Electrical Characteristics and AC Operating Conditions (Sheet 5 of 6)

Notes: 1–8 apply to the entire table; notes appear on page 76

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes		
		Min	Max	Min	Max	Min	Max	Min	Max				
Power-Down Timing													
CKE MIN pulse width	^t CKE (MIN)	Greater of 3CK or 7.5ns	Greater of 3CK or 5.625ns	Greater of 3CK or 5.625ns	Greater of 3CK or 5ns					CK			
Command pass disable delay	^t CPDED	MIN = 1; MAX = n/a								CK			
Power-down entry to power-down exit timing	^t PD	MIN = ^t CKE (MIN); MAX = 60ms								CK			
Begin power-down period prior to CKE registered HIGH	^t ANPD	WL - 1CK								CK			
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of ^t ANPD or ^t RFC - REFRESH command to CKE LOW time								CK			
Power-down exit period: ODT either synchronous or asynchronous	PDX	^t ANPD + ^t XPDLL								CK			
Power-Down Entry Minimum Timing													
ACTIVATE command to power-down entry	^t ACTPDEN	MIN = 1								CK			
PRECHARGE/PRECHARGE ALL command to power-down entry	^t PRPDEN	MIN = 1								CK			
REFRESH command to power-down entry	^t REFPDEN	MIN = 1								CK	37		
MRS command to power-down entry	^t MRS PDEN	MIN = ^t MOD (MIN)								CK			
READ/READ with auto precharge command to power-down entry	^t RDPDEN	MIN = RL + 4 + 1								CK			
WRITE command to power-down entry	BL8 (OTF, MRS)	^t WRPDEN								MIN = WL + 4 + ^t WR/ ^t CK (AVG)		CK	
	BC4OTF									MIN = WL + 2 + ^t WR/ ^t CK (AVG)		CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS)	^t WRAPDEN								MIN = WL + 4 + WR + 1		CK	
	BC4MRS									MIN = WL + 2 + WR + 1		CK	
Power-Down Exit Timing													
DLL on, any valid command, or DLL off to commands not requiring locked DLL	^t XP	MIN = greater of 3CK or 7.5ns; MAX = n/a				MIN = greater of 3CK or 6ns; MAX = n/a				CK			
Precharge power-down with DLL off to commands requiring a locked DLL	^t XPDLL	MIN = greater of 10CK or 24ns; MAX = n/a								CK	28		

Table 56: Electrical Characteristics and AC Operating Conditions (Sheet 6 of 6)

Notes: 1–8 apply to the entire table; notes appear on page 76

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
ODT Timing											
RTT synchronous turn-on delay	ODTL on	CWL + AL - 2CK								CK	38
RTT synchronous turn-off delay	ODTL off	CWL + AL - 2CK								CK	40
RTT turn-on from ODTL on reference	^t AON	-400	400	-300	300	-250	250	-225	225	ps	23, 38
RTT turn-off from ODTL off reference	^t AOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous RTT turn-on delay (power-down with DLL off)	^t AONPD	MIN = 2; MAX = 8.5								ns	38
Asynchronous RTT turn-off delay (power-down with DLL off)	^t AOPFD	MIN = 2; MAX = 8.5								ns	40
ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = n/a								CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = n/a								CK	
Dynamic ODT Timing											
RTT_NOM-to-RTT_WR change skew	ODTLCNW	WL - 2CK								CK	
RTT_WR-to-RTT_NOM change skew - BC4	ODTLCNW4	4CK + ODTL off								CK	
RTT_WR-to-RTT_NOM change skew - BL8	ODTLCNW8	6CK + ODTL off								CK	
RTT dynamic change skew	^t ADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing											
First DQS, DQS# rising edge	^t WLMRD	40	-	40	-	40	-	40	-	CK	
DQS, DQS# delay	^t WLDQSEN	25	-	25	-	25	-	25	-	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	^t WLS	325	-	245	-	195	-	165	-	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	^t WLH	325	-	245	-	195	-	165	-	ps	
Write leveling output delay	^t WLO	0	9	0	9	0	9	0	7.5	ns	
Write leveling output error	^t WLOE	0	2	0	2	0	2	0	2	ns	

Notes

1. Parameters are applicable with $0^{\circ}\text{C} \leq T_C \leq +95^{\circ}\text{C}$ and $V_{DD}/V_{DDQ} = +1.5\text{V} \pm 0.075\text{V}$.
2. All voltages are referenced to VSS.
3. Output timings are only valid for RON₃₄ output buffer selection.
4. Unit “t_{CK (AVG)}” represents the actual t_{CK (AVG)} of the input clock under operation. Unit “CK” represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 900mV in the test environment, but input timing is still referenced to VREF (except t_{IS}, t_{IH}, t_{DS}, and t_{DH} use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between VIL(AC) and VIH(AC).
6. All timings that use time-based values (ns, μs, ms) should use t_{CK (AVG)} to determine the correct number of clocks (Table 56 on page 70 uses “CK” or “t_{CK [AVG]}” interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. The use of “strobe” or “DQSDIFF” refers to the DQS and DQS# differential crossing point when DQS is the rising edge. The use of “clock” or “CK” refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is VDDQ/2 for single-ended signals and the crossing point for differential signals (see Figure 29 on page 63).
9. When operating in DLL disable mode, Micron does not warrant compliance with normal mode timings or functionality.
10. The clock’s t_{CK (AVG)} is the average clock over any 200 consecutive clocks and t_{CK(AVG) MIN} is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of t_{CK (AVG)} as a long-term jitter component; however, the spread-spectrum may not use a clock rate below t_{CK (AVG) MIN}.
12. The clock’s t_{CH (AVG)} and t_{CL (AVG)} are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (t_{JITPER}) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. t_{CH(ABS)} is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. t_{CL(ABS)} is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter (t_{JITCC}) is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.

17. The cumulative jitter error ($t_{ERRnPER}$), where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. t_{DS} (base) and t_{DH} (base) values are for a single-ended 1 V/ns DQ slew rate and 2 V/ns differential DQS, DQS# slew rate.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{JITPER} (larger of $t_{JITPER}(MIN)$ or $t_{JITPER}(MAX)$ of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting $t_{ERR10PER}(MAX)$: $t_{DQSCK}(MIN)$, $t_{LZ}(DQS) MIN$, $t_{LZ}(DQ) MIN$, and $t_{AON}(MIN)$. The following parameters are required to be derated by subtracting $t_{ERR10PER}(MIN)$: $t_{DQSCK}(MAX)$, $t_{HZ}(MAX)$, $t_{LZ}(DQS) MAX$, $t_{LZ}(DQ) MAX$, and $t_{AON}(MAX)$. The parameter $t_{RPRE}(MIN)$ is derated by subtracting $t_{JITPER}(MAX)$, while $t_{RPRE}(MAX)$ is derated by subtracting $t_{JITPER}(MIN)$.
24. The maximum preamble is bound by $t_{LZDQS}(MAX)$.
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The $t_{DQSCK} DLL_DIS$ parameter begins $CL + AL - 1$ cycles after the READ command.
27. The maximum postamble is bound by $t_{HZDQS}(MAX)$.
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency t_{XPDLL} , timing must be met.
29. t_{IS} (base) and t_{IH} (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports $t_{nPARAM}(nCK) = RU(t_{PARAM}[ns]/t_{CK}[AVG][ns])$, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP}(nCK) = RU(t_{RP}/t_{CK}[AVG])$ if all input clock jitter specifications are met. This means for DDR3-800 6-6-6, of which $t_{RP} = 15ns$, the device will support $t_{nRP} = RU(t_{RP}/t_{CK}[AVG]) = 6$ as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T_0 and the ACTIVATE command at $T_0 + 6$ are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until $t_{RAS}(MIN)$ has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for t_{WR} .

34. The start of the write recovery time is defined as follows:
 - For BL8 (fixed by MRS and OTF): Rising clock edge four clock cycles after WL
 - For BC4 (OTF): Rising clock edge four clock cycles after WL
 - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125 μ s. However, nine REFRESH commands should be asserted at least once every 70.3 μ s. When T_C is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when $t_{REFPDEN}$ (MIN) is satisfied, there are cases where additional time such as t_{XPDLL} (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 21 on page 52.
39. Half-clock output parameters must be derated by the actual $t_{ERR_{10PER}}$ and t_{JITDTY} when input clock jitter is present. This results in each parameter becoming larger. The parameters t_{ADC} (MIN) and t_{AOF} (MIN) are each required to be derated by subtracting both $t_{ERR_{10PER}}$ (MAX) and t_{JITDTY} (MAX). The parameters t_{ADC} (MAX) and t_{AOF} (MAX) are required to be derated by subtracting both $t_{ERR_{10PER}}$ (MAX) and t_{JITDTY} (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 22 on page 54. This output load is used for ODT timings (see Figure 29 on page 63).
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than t_{RFC} (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz) all REFRESH commands should be followed by a PRECHARGE All command.

Command and Address Setup, Hold, and Derating

The total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet t_{IS} (base) and t_{IH} (base) values (see Table 57; values come from Table 56 on page 70) to the Δt_{IS} and Δt_{IH} derating values (see Table 58 on page 80 and Table 59 on page 80), respectively. Example: t_{IS} (total setup time) = t_{IS} (base) + Δt_{IS} . For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time t_{VAC} (see Table 59 on page 80).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$ (see Figure 13 on page 44 for input signal requirements). For slew rates which fall between the values listed in Table 59 on page 80 and Table 60 on page 81, the derating values may be obtained by linear interpolation.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC) MIN}$. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC) MAX}$. If the actual signal is always earlier than the nominal slew rate line between the shaded “ $V_{REF(DC)}$ -to-AC region,” use the nominal slew rate for derating value (see Figure 32 on page 82). If the actual signal is later than the nominal slew rate line anywhere between the shaded “ $V_{REF(DC)}$ -to-AC region,” the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 34 on page 84).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC) MAX}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC) MIN}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded “DC-to- $V_{REF(DC)}$ region,” use the nominal slew rate for derating value (see Figure 33 on page 83). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded “DC-to- $V_{REF(DC)}$ region,” the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for derating value (see Figure 35 on page 85).

Table 57: Command and Address Setup and Hold Values Referenced at 1 V/ns – AC/DC-Based

Symbol	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Reference
t_{IS} (base) AC175	200	125	65	45	ps	$V_{IH(AC)}/V_{IL(AC)}$
t_{IS} (base) AC150	350	275	190	170	ps	$V_{IH(AC)}/V_{IL(AC)}$
t_{IH} (base) DC100	275	200	140	120	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 58: Derating Values for t_{IS}/t_{IH} - AC175/DC100-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) - AC/DC-Based AC175 Threshold: $V_{IH}(AC) = V_{REF}(DC) + 175mV, V_{IL}(AC) = V_{REF}(DC) - 175mV$																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

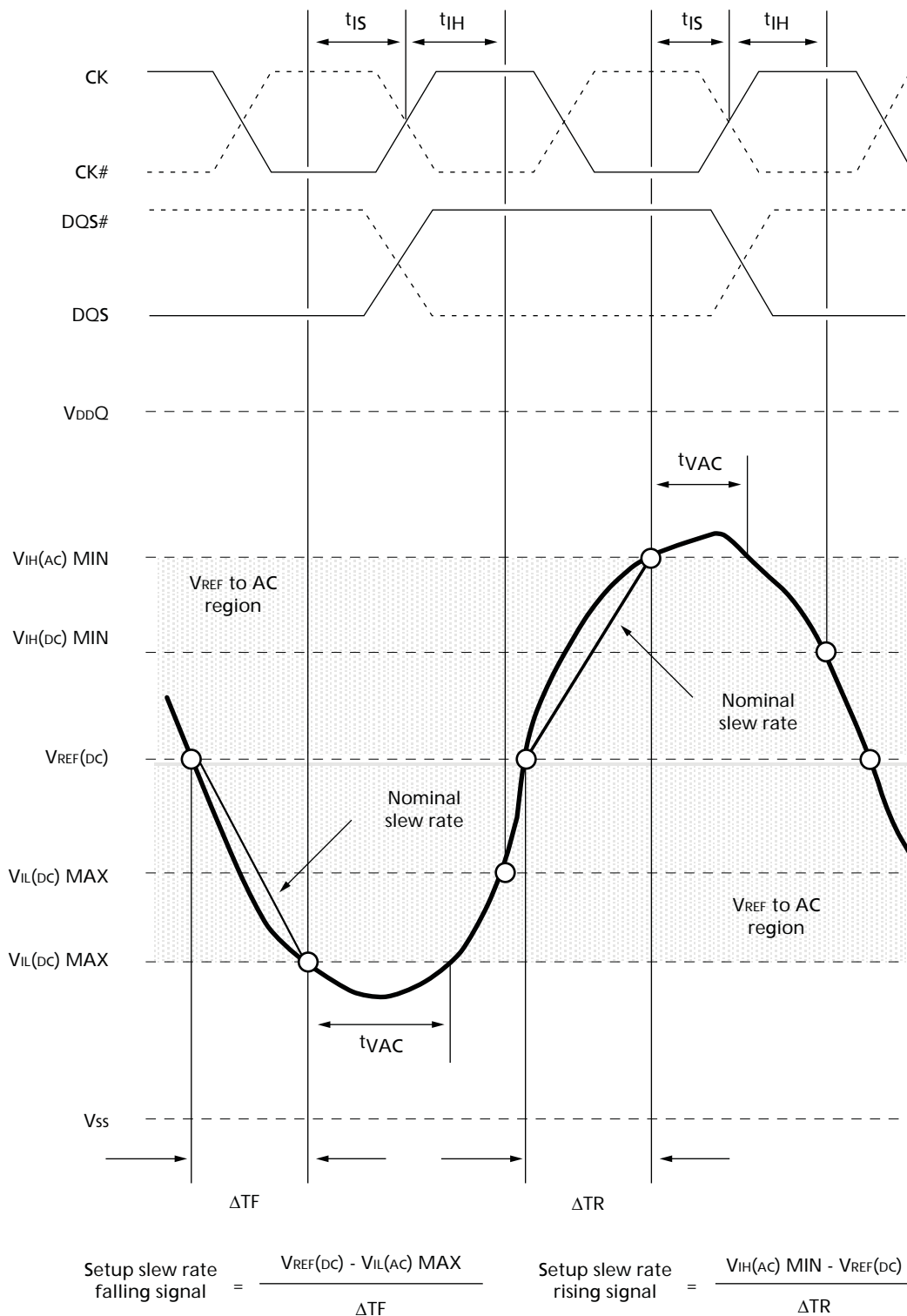
Table 59: Derating Values for t_{IS}/t_{IH} - AC150/DC100-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) - AC/DC-Based AC150 Threshold: $V_{IH}(AC) = V_{REF}(DC) + 150mV, V_{IL}(AC) = V_{REF}(DC) - 150mV$																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 60: Minimum Required Time t_{VAC} Above $V_{IH(AC)}$ for Valid Transition
Below $V_{IL(AC)}$

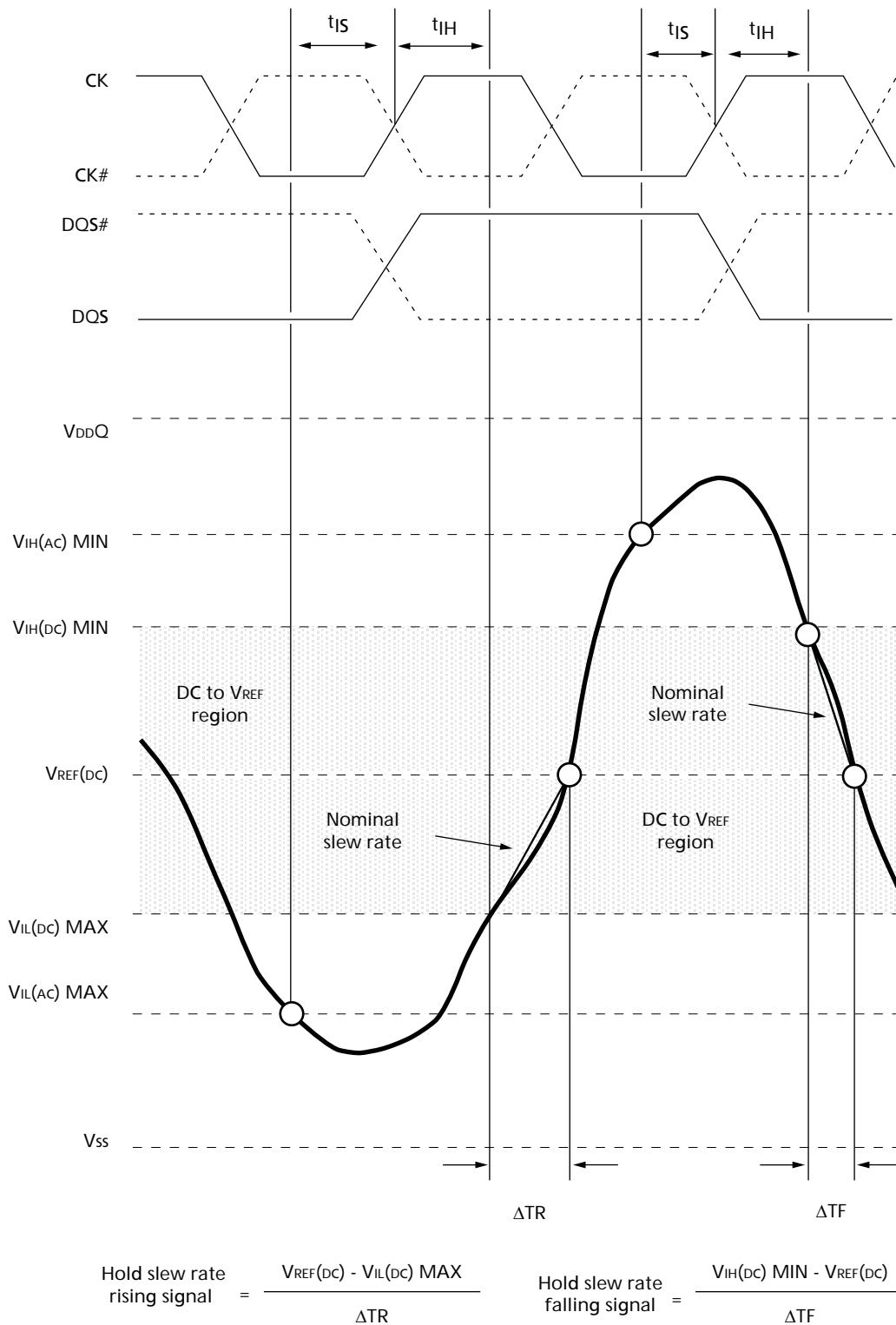
Slew Rate (V/ns)	t_{VAC} at 175mV (ps)	t_{VAC} at 150mV (ps)
>2.0	75	175
2.0	57	170
1.5	50	167
1.0	38	163
0.9	34	162
0.8	29	161
0.7	22	159
0.6	13	155
0.5	0	150
<0.5	0	150

Figure 32: Nominal Slew Rate and t_{VAC} for t_{IS} (Command and Address - Clock)



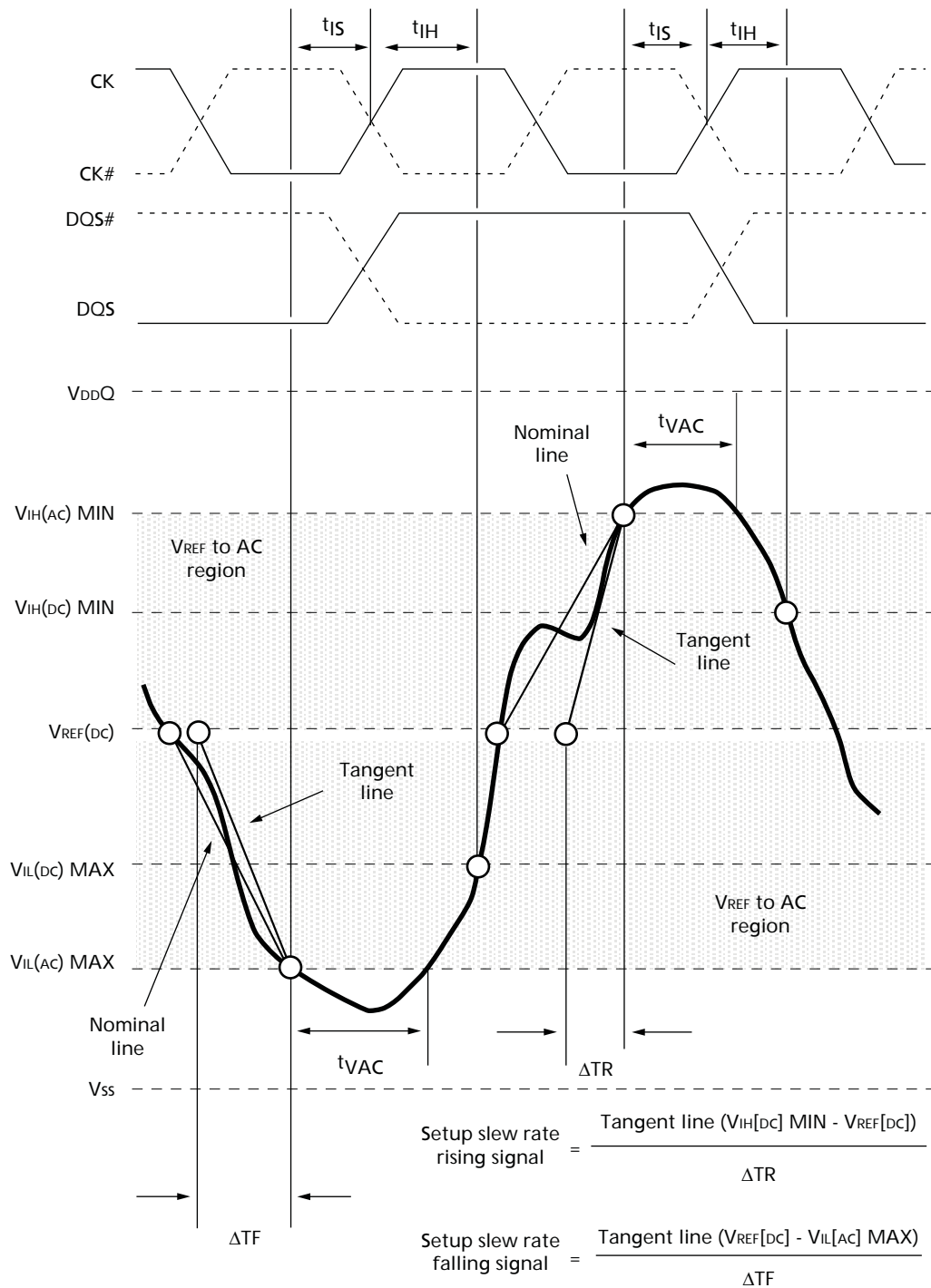
Notes: 1. Both the clock and the strobe are drawn on different time scales.

Figure 33: Nominal Slew Rate for t_{IH} (Command and Address - Clock)



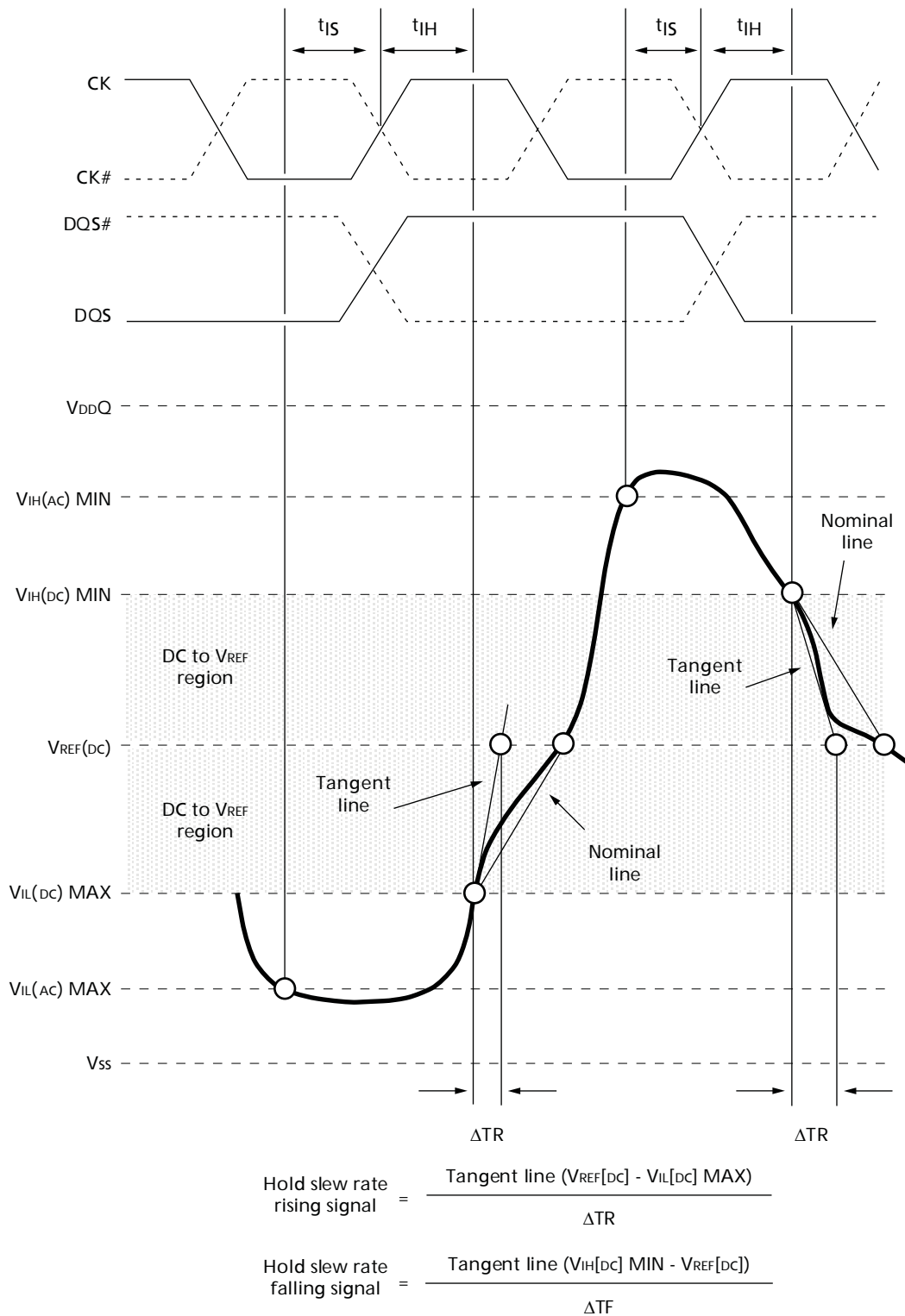
Notes: 1. Both the clock and the strobe are drawn on different time scales.

Figure 34: Tangent Line for t_{IS} (Command and Address - Clock)



Notes: 1. Both the clock and the strobe are drawn on different time scales.

Figure 35: Tangent Line for t_{IH} (Command and Address - Clock)



Notes: 1. Both the clock and the strobe are drawn on different time scales.

Data Setup, Hold, and Derating

The total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet t_{DS} (base) and t_{DH} (base) values (see Table 61; values come from Table 56 on page 70) to the Δt_{DS} and Δt_{DH} derating values (see Table 62 on page 87), respectively. Example: t_{DS} (total setup time) = t_{DS} (base) + Δt_{DS} . For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time t_{VAC} (see Table 64 on page 88).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH}/V_{IL(AC)}$. For slew rates which fall between the values listed in Table 63 on page 87, the derating values may be obtained by linear interpolation.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)}$ MIN. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)}$ MAX. If the actual signal is always earlier than the nominal slew rate line between the shaded “ $V_{REF(DC)}$ -to-AC region,” use the nominal slew rate for derating value (see Figure 36 on page 89). If the actual signal is later than the nominal slew rate line anywhere between the shaded “ $V_{REF(DC)}$ -to-AC region,” the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 38 on page 91).

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$ MAX and the first crossing of $V_{REF(DC)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$ MIN and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded “DC-to- $V_{REF(DC)}$ region,” use the nominal slew rate for derating value (see Figure 37 on page 90). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded “DC-to- $V_{REF(DC)}$ region,” the slew rate of a tangent line to the actual signal from the “DC-to- $V_{REF(DC)}$ region” is used for derating value (see Figure 39 on page 92).

Table 61: Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based

Symbol	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Reference
t_{DS} (base) AC175	75	25	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
t_{DS} (base) AC150	125	75	30	10	ps	$V_{IH(AC)}/V_{IL(AC)}$
t_{DH} (base) DC100	150	100	65	45	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 62: Derating Values for t_{DS}/t_{DH} - AC175/DC100-Based
Shaded cells indicate slew rate combinations not supported

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) - AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	88	50	88	50	88	50										
1.5	59	34	59	34	59	34	67	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			-2	-4	-2	-4	6	4	14	12	22	20				
0.8					-6	-10	2	-2	10	6	18	14	26	24		
0.7							-3	-8	5	0	13	8	21	18	29	34
0.6									-1	-10	7	-2	15	8	23	24
0.5											-11	-16	-2	-6	5	10
0.4													-30	-26	-22	-10

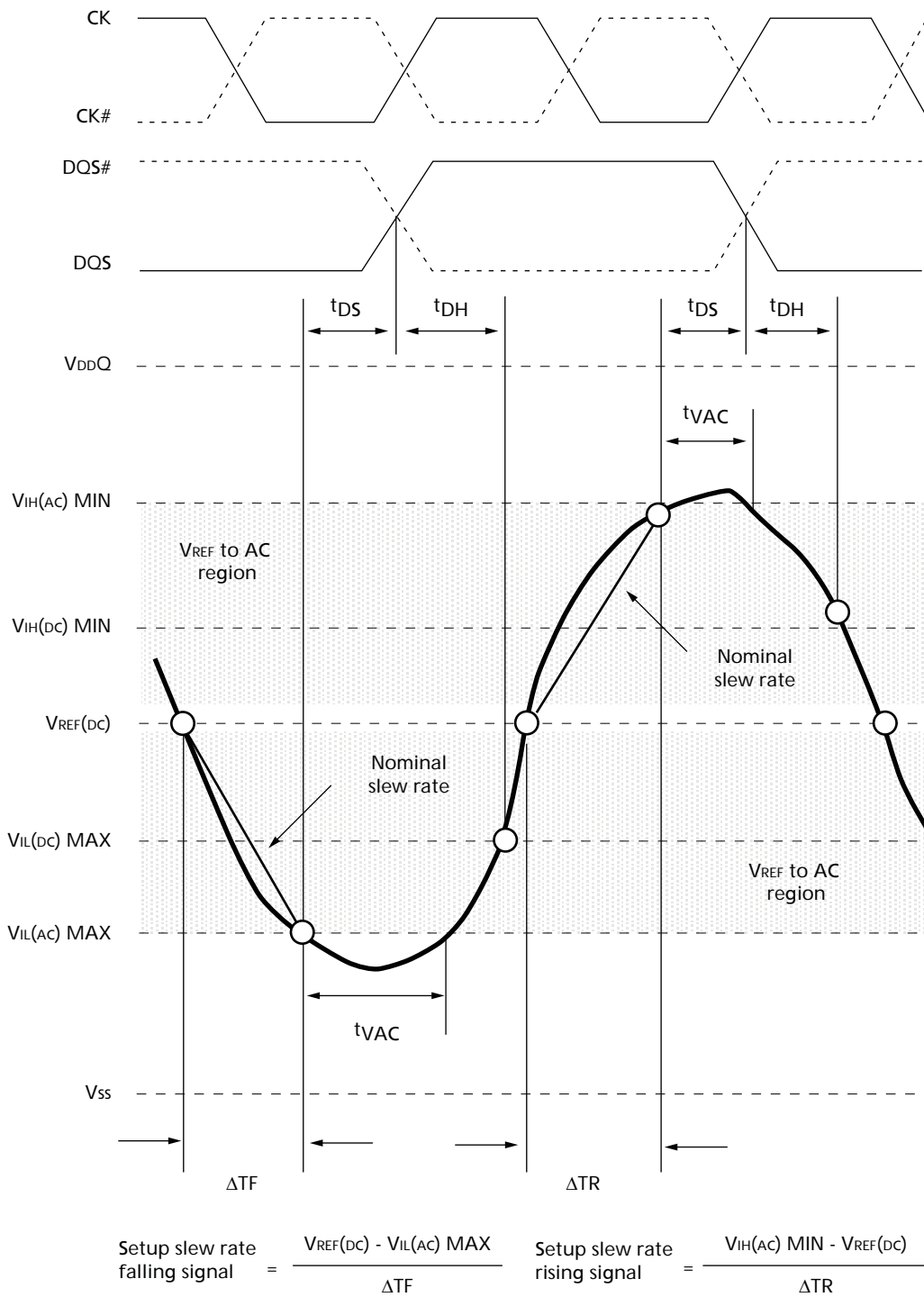
Table 63: Derating Values for t_{DS}/t_{DH} - AC150/DC100-Based
Shaded cells indicate slew rate combinations not supported

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) - AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	75	50	75	50	75	50										
1.5	50	34	50	34	50	34	58	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			0	-4	0	-4	8	4	16	12	24	20				
0.8					0	-10	8	-2	16	6	24	14	32	24		
0.7							8	-8	16	0	24	8	32	18	40	34
0.6									15	-10	23	-2	31	8	39	24
0.5											14	-16	22	-6	30	10
0.4													7	-26	15	-10

Table 64: Required Time t_{VAC} Above $V_{IH}(AC)$ (Below $V_{IL}(AC)$) for Valid Transition

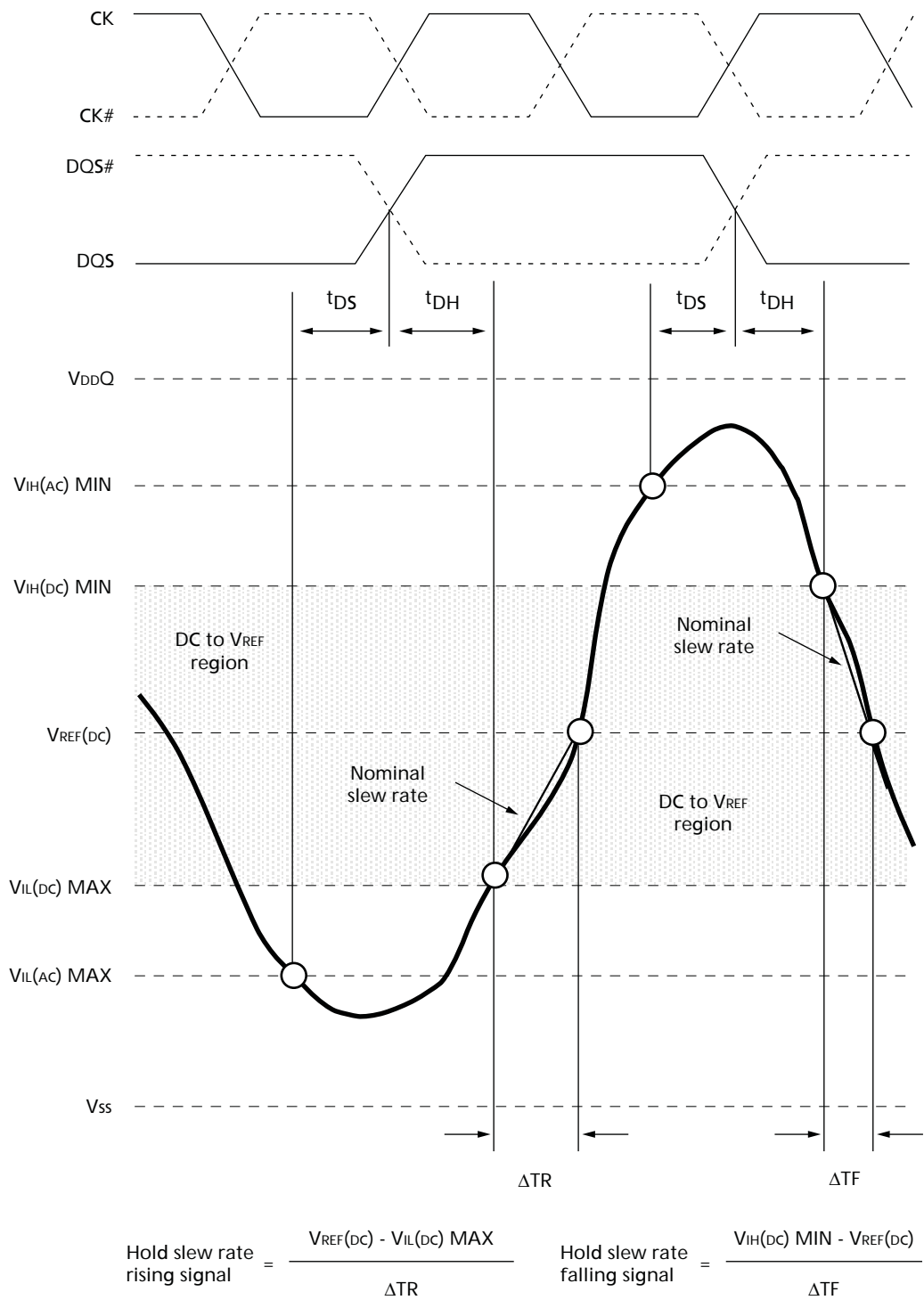
Slew Rate (V/ns)	t_{VAC} at 175mV (ps)	t_{VAC} at 150mV (ps)
	Min	Min
>2.0	75	175
2.0	57	170
1.5	50	167
1.0	38	163
0.9	34	162
0.8	29	161
0.7	22	159
0.6	13	155
0.5	0	150
<0.5	0	150

Figure 36: Nominal Slew Rate and t_{VAC} for t_{DS} (DQ - Strobe)



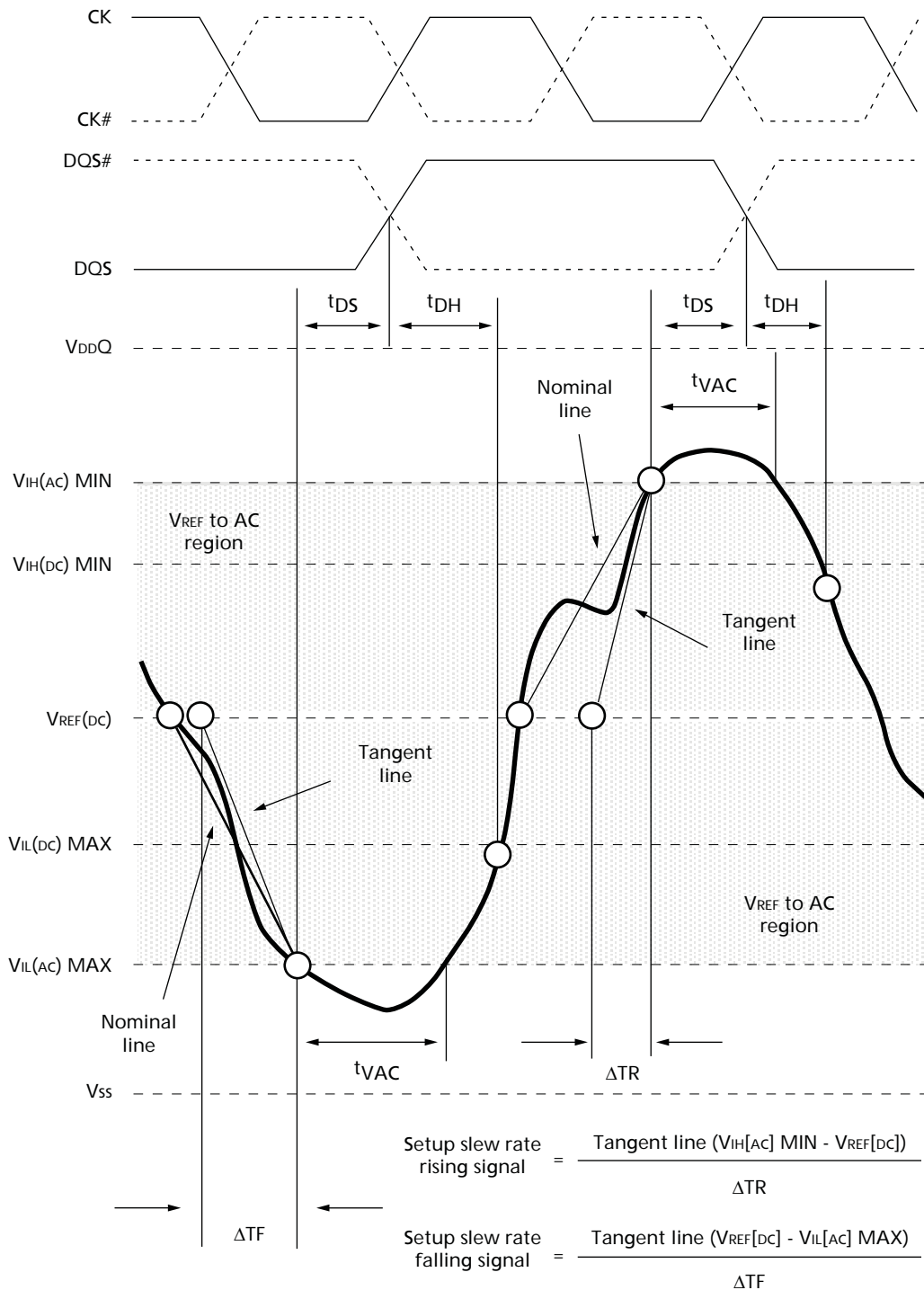
Notes: 1. Both the clock and the strobe are drawn on different time scales.

Figure 37: Nominal Slew Rate for t_{DH} (DQ - Strobe)



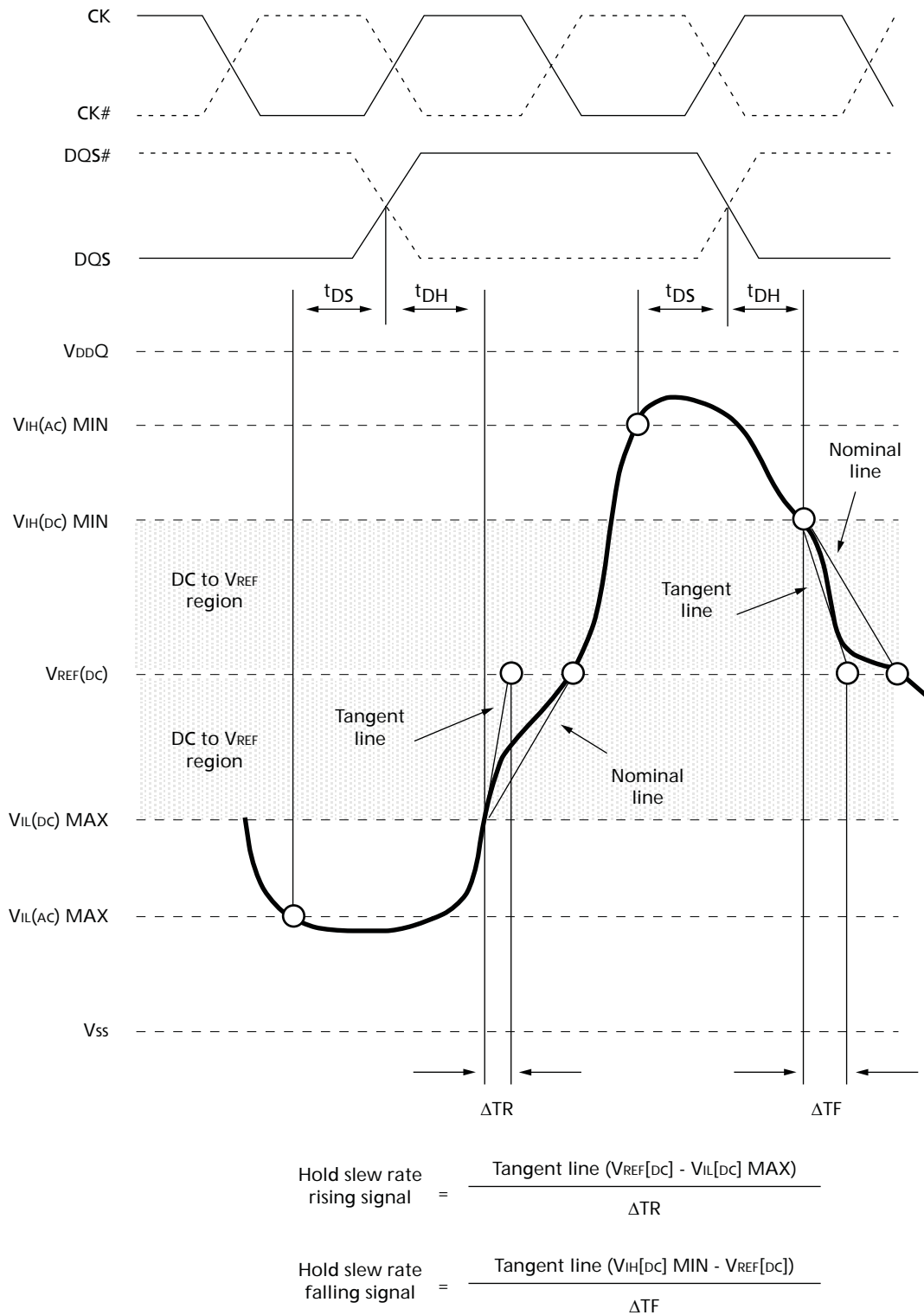
Notes: 1. Both the clock and the strobe are drawn on different time scales.

Figure 38: Tangent Line for t_{DS} (DQ - Strobe)



Notes: 1. Both the clock and the strobe are drawn on different time scales.

Figure 39: Tangent Line for t_{DH} (DQ - Strobe)



Notes: 1. Both the clock and the strobe are drawn on different time scales.

Commands

Truth Tables

Table 65: Truth Table – Command
Notes 1–5 apply to the entire table

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]	Notes
		Prev Cycle	Next Cycle										
MODE REGISTER SET	MRS	H	H	L	L	L	L	BA	OP code				
REFRESH	REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry	SRE	H	L	L	L	L	H	V	V	V	V	V	6
Self refresh exit	SRX	L	H	H	V	V	V	V	V	V	V	V	6, 7
				L	H	H	H						
Single-bank PRECHARGE	PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank ACTIVATE	ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	BA	RFU	H	L	CA	8
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	BA	RFU	H	H	CA	8
READ	BL8MRS, BC4MRS	RD	H	H	L	H	L	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	BA	RFU	H	L	CA	8
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H	H	L	H	L	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	BA	RFU	H	H	CA	8
NO OPERATION	NOP	H	H	L	H	H	H	V	V	V	V	V	9
Device DESELECTED	DES	H	H	H	X	X	X	X	X	X	X	X	10
Power-down entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6
				H	V	V	V						
Power-down exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6, 11
				H	V	V	V						
ZQ CALIBRATION LONG	ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ CALIBRATION SHORT	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

- Notes:
1. Commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-density and configuration-dependent.
 2. RESET# is LOW enabled and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.
 3. The state of ODT does not affect the states described in this table.

4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. "V" means "H" or "L" (a defined logic level), and "X" means "Don't Care."
6. See Table 66 for additional information on CKE transition.
7. Self refresh exit is asynchronous.
8. Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
10. The DES and NOP commands perform similarly.
11. The power-down mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQINIT (first ZQCL command during initialization) or ZQOPER (ZQCL command after initialization).

Table 66: Truth Table – CKE

Notes 1–2 apply to the entire table; see Table 65 on page 93 for additional command details

Current State ³	CKE		Command ⁵ (RAS#, CAS#, WE#, CS#)	Action ⁵	Notes
	Previous Cycle ⁴ (<i>n</i> - 1)	Present Cycle ⁴ (<i>n</i>)			
Power-down	L	L	"Don't Care"	Maintain power-down	
	L	H	DES or NOP	Power-down exit	
Self refresh	L	L	"Don't Care"	Maintain self refresh	
	L	H	DES or NOP	Self refresh exit	
Bank(s) active	H	L	DES or NOP	Active power-down entry	
Reading	H	L	DES or NOP	Power-down entry	
Writing	H	L	DES or NOP	Power-down entry	
Precharging	H	L	DES or NOP	Power-down entry	
Refreshing	H	L	DES or NOP	Precharge power-down entry	
All banks idle	H	L	DES or NOP	Precharge power-down entry	6
	H	L	REFRESH	Self refresh	

- Notes:
1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
 2. ^tCKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^tIS + ^tCKE (MIN) + ^tIH.
 3. Current state = The state of the DRAM immediately prior to clock edge *n*.
 4. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n* - 1) was the state of CKE at the previous clock edge.
 5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 65 on page 93). Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.
 6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All self refresh exit and power-down exit parameters are also satisfied.

DESELECT (DES)

The DES command (CS# HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

NO OPERATION (NOP)

The NOP command (CS# LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION

ZQ CALIBRATION LONG (ZQCL)

The ZQCL command is used to perform the initial calibration during a power-up initialization and reset sequence (see Figure 48 on page 109). This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated RON and ODT values.

The DRAM is allowed a timing window defined by either t_{ZQINIT} or t_{ZQOPER} to perform the full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter t_{ZQINIT} must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter t_{ZQOPER} to be satisfied.

ZQ CALIBRATION SHORT (ZQCS)

The ZQCS command is used to perform periodic calibrations to account for small voltage and temperature variations. The shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter t_{ZQCS} . A ZQCS command can effectively correct a minimum of 0.5% RON and RTT impedance error within 64 clock cycles, assuming the maximum sensitivities specified in Table 43 on page 59 and Table 44 on page 60.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[n:0] selects the row. This row remains open (or active) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address depending on the burst length and burst type selected (see Table 71 on page 113 for additional information). The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the mode register) when the READ command is issued determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted. A summary of READ commands is shown in Table 67 on page 96.

Table 67: READ Command Summary

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [3:0]	An	A12	A10	A[11, 9:0]
			Previous Cycle	Next Cycle									
READ	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H		L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H		L	H	L	H	BA	RFU	H	L	CA
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H		L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAPS4	H		L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAPS8	H		L	H	L	H	BA	RFU	H	H	CA

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether or not auto precharge is used. The value on input A12 (if enabled in the MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used. The WRITE command summary is shown in Table 68.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

Table 68: WRITE Command Summary

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [3:0]	An	A12	A10	A[11, 9:0]
			Prev Cycle	Next Cycle									
WRITE	BL8MRS, BC4MRS	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H		L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H		L	H	L	L	BA	RFU	H	L	CA
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H		L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAPS4	H		L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAPS8	H		L	H	L	L	BA	RFU	H	H	CA

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access a specified time (RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. A READ or WRITE command to a different bank is allowed during concurrent auto precharge as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is precharged, inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as "Don't Care." After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if

there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period is determined by the last PRECHARGE command issued to the bank.

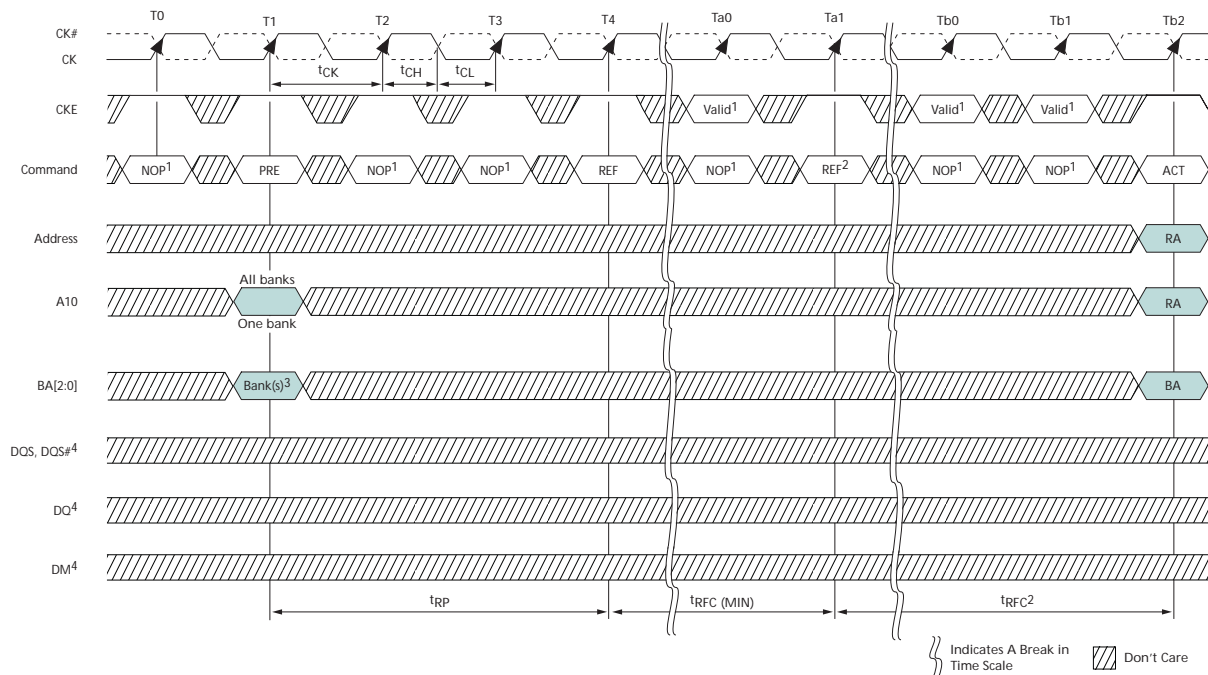
REFRESH

REFRESH is used during normal operation of the DRAM and is analogous to CAS#-before-RAS# (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command. The DRAM requires REFRESH cycles at an average interval of 7.8µs (maximum when $T_C \leq 85^\circ\text{C}$ or 3.9µs MAX when $T_C \leq 95^\circ\text{C}$). The REFRESH period begins when the REFRESH command is registered and ends t_{RFC} (MIN) later.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. Self refresh may be entered with up to eight REFRESH commands being posted. After exiting self refresh (when entered with posted REFRESH commands) additional posting of REFRESH commands is allowed to the extent the maximum number of cumulative posted REFRESH commands (both pre and post self refresh) does not exceed eight REFRESH commands.

The posting limit of eight REFRESH commands is a JEDEC specification; however, as long as all the required number of REFRESH commands are issued within the refresh period (64ms), exceeding the eight posted REFRESH commands is allowed.

Figure 40: Refresh Mode



- Notes: 1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times (see “Power-Down Mode” on page 153).

2. The second REFRESH is not required but depicts two back-to-back REFRESH commands.
3. “Don’t Care” if A10 is HIGH at this point; however, A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. For operations shown, DM, DQ, and DQS signals are all “Don’t Care”/High-Z.

SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in the self refresh mode, the DRAM retains data without external clocking. The self refresh mode is also a convenient method used to enable/disable the DLL (see “DLL Disable Mode” on page 98) as well as to change the clock frequency within the allowed synchronous operating range (see “Input Clock Frequency Change” on page 101). All power supply inputs (including VREFCA and VREFDQ) must be maintained at valid levels upon entry/exit and during self refresh mode operation. All power supply inputs (including VREFCA and VREFDQ) must be maintained at valid levels upon entry/exit and during self refresh mode operation. VREFDQ may float or not drive $V_{DDQ}/2$ while in the self refresh mode under certain conditions:

- $V_{SS} < V_{REFDQ} < V_{DD}$ is maintained
- VREFDQ is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after VREFDQ is valid
- All other self refresh mode exit timing requirements are met.

DLL Disable Mode

If the DLL is disabled by the mode register (MR1[0] can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode with a few notable exceptions:

- The DRAM supports only one value of CAS latency (CL = 6) and one value of CAS WRITE latency (CWL = 6).
- DLL disable mode affects the read data clock-to-data strobe relationship (t_{DQSCK}), but not the read data-to-data strobe relationship (t_{DQSQ} , t_{QH}). Special attention is needed to line the read data up with the controller time domain when the DLL is disabled.
- In normal operation (DLL on), t_{DQSCK} starts from the rising clock edge AL + CL cycles after the READ command. In DLL disable mode, t_{DQSCK} starts AL + CL - 1 cycles after the READ command. Additionally, with the DLL disabled, the value of t_{DQSCK} could be larger than t_{CK} .

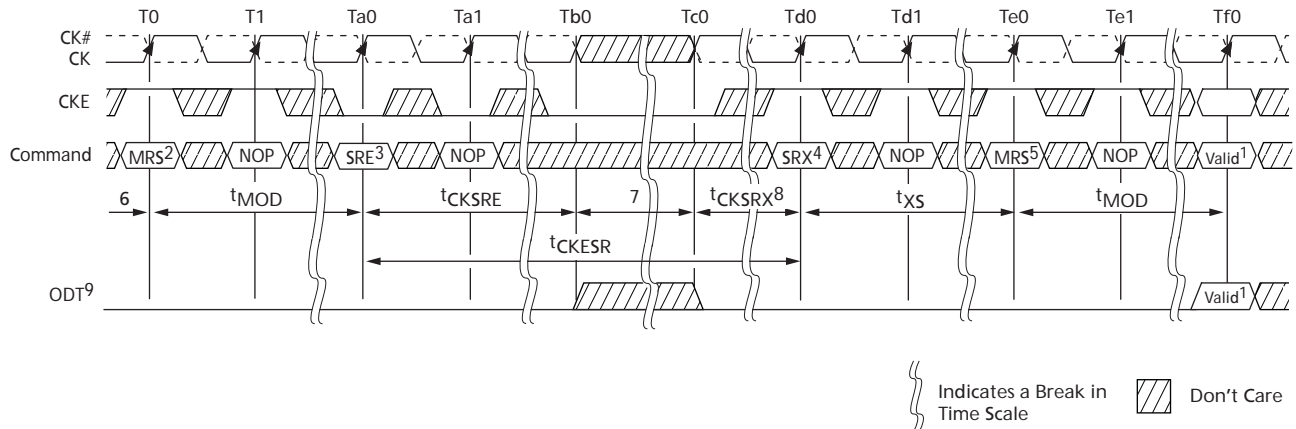
The ODT feature is not supported during DLL disable mode (including dynamic ODT). The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming RTT_NOM MR1[9, 6, 2] and RTT_WR MR2[10, 9] to “0” while in the DLL disable mode.

Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes ($t_{CK} [AVG] MAX$ and $t_{CK} [DLL \text{ disable}] MIN$, respectively). The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh (see Figure 41 on page 99):

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), set MR1[0] to “1” to disable the DLL.
2. Enter self refresh mode after t_{MOD} has been satisfied.

3. After t_{CKSRE} is satisfied, change the frequency to the desired clock rate.
4. Self refresh may be exited when the clock is stable with the new frequency for t_{CKSRX} . After t_{XS} is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of t_{MRD} or t_{MOD} has been satisfied. A ZQCL command should be issued with appropriate timings met as well.

Figure 41: DLL Enable Mode to DLL Disable Mode

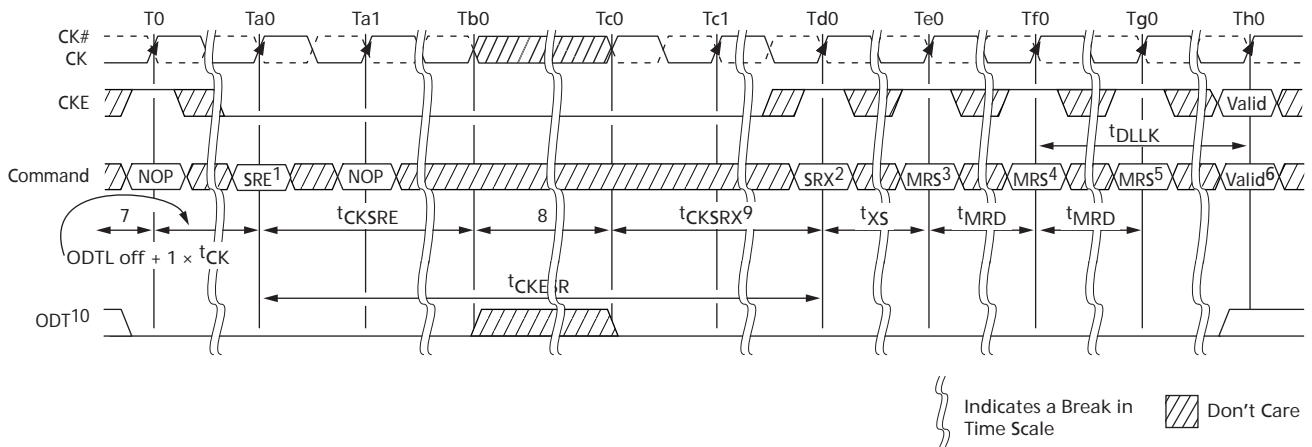


- Notes:
1. Any valid command.
 2. Disable DLL by setting MR1[0] to "1."
 3. Enter SELF REFRESH.
 4. Exit SELF REFRESH.
 5. Update the mode registers with the DLL disable parameters setting.
 6. Starting with the idle state, RTT is in the High-Z state.
 7. Change frequency.
 8. Clock must be stable t_{CKSRX} .
 9. Static LOW in case RTT_NOM or RTT_WR is enabled; otherwise, static LOW or HIGH.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode (see Figure 42 on page 100).

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), enter self refresh mode.
2. After t_{CKSRE} is satisfied, change the frequency to the new clock rate.
3. Self refresh may be exited when the clock is stable with the new frequency for t_{CKSRX} . After t_{XS} is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to "0" to enable the DLL. Wait t_{MRD} , then set MR0[8] to "1" to enable DLL RESET.
4. After another t_{MRD} delay is satisfied, then update the remaining mode registers with the appropriate values.
5. The DRAM will be ready for its next command in the DLL enable mode after the greater of t_{MRD} or t_{MOD} has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of t_{DLLK} after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met as well.

Figure 42: DLL Disable Mode to DLL Enable Mode



- Notes:
1. Enter SELF REFRESH.
 2. Exit SELF REFRESH.
 3. Wait t_{XS} , then set MR1[0] to "0" to enable DLL.
 4. Wait t_{MRD} , then set MR0[8] to "1" to begin DLL RESET.
 5. Wait t_{MRD} , update registers (CL, CWL, and write recovery may be necessary).
 6. Wait t_{MOD} , any valid command.
 7. Starting with the idle state.
 8. Change frequency.
 9. Clock must be stable at least t_{CKSRX} .
 10. Static LOW in case RTT_NOM or RTT_WR is enabled; otherwise, static LOW or HIGH.

The clock frequency range for the DLL disable mode is specified by the parameter t_{CKDLL_DIS} . Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (t_{DQSCK}) but not the data strobe to data relationship (t_{DQSQ} , t_{QH}). Special attention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where t_{DQSCK} starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode t_{DQSCK} starts AL + CL - 1 cycles after the READ command (see Figure 43 on page 101).

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

Figure 43: DLL Disable t_{DQSK} Timing

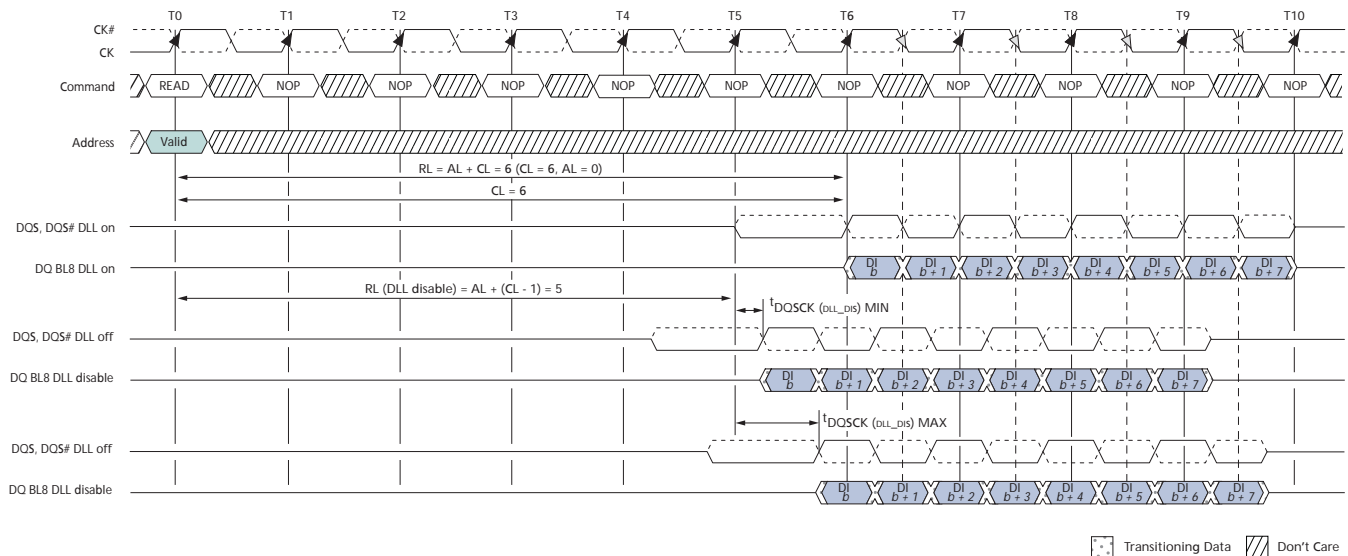


Table 69: READ Electrical Characteristics, DLL Disable Mode

Parameter	Symbol	Min	Max	Units
Access window of DQS from CK, CK#	$t_{DQSK} (DLL_DIS)$	1	10	ns

Input Clock Frequency Change

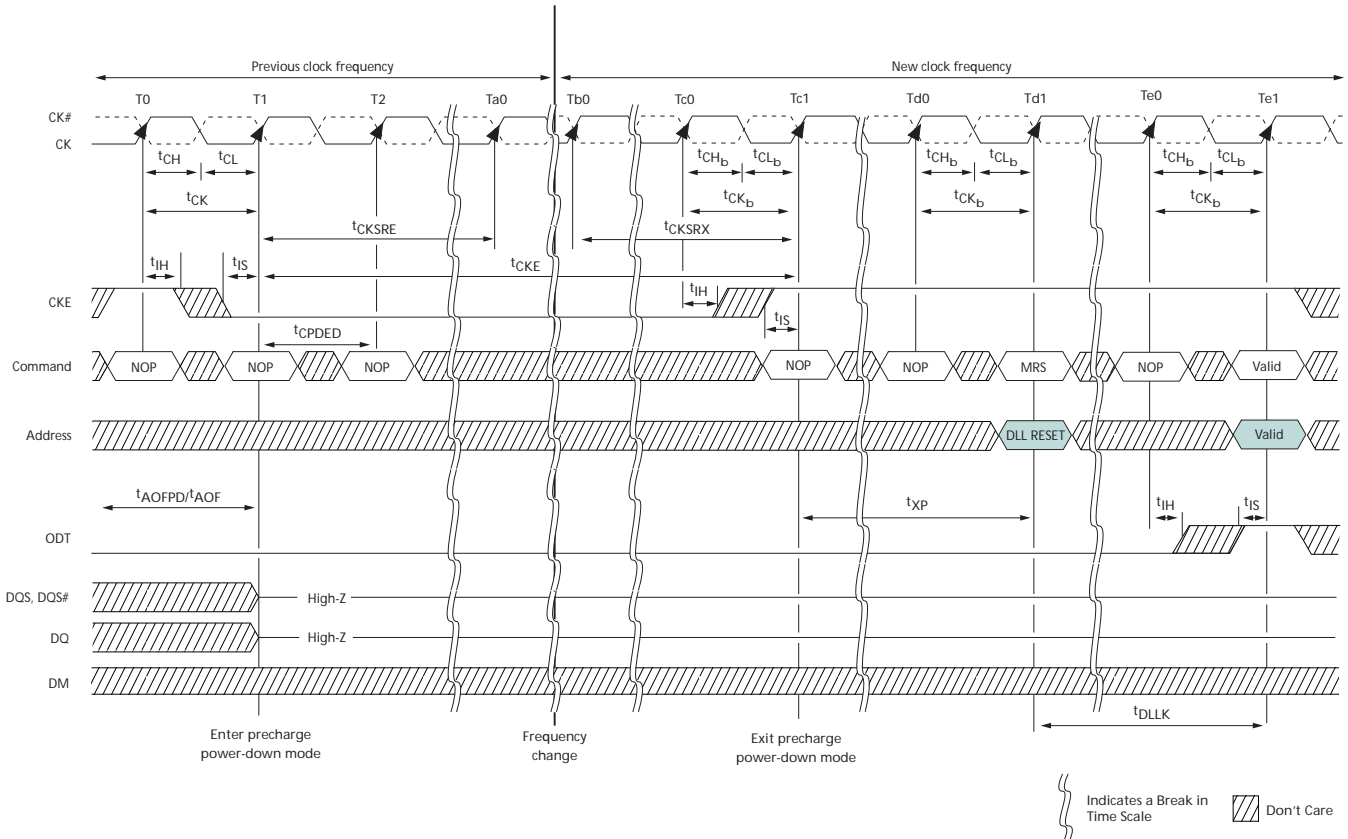
When the DDR3 SDRAM is initialized, it requires the clock to be stable during most normal states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate except what is allowed for by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: self refresh mode and precharge power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the self refresh mode condition, when the DDR3 SDRAM has been successfully placed into self refresh mode and t_{CKSRE} has been satisfied, the state of the clock becomes a “Don’t Care.” When the clock becomes a “Don’t Care,” changing the clock frequency is permissible, provided the new clock frequency is stable prior to t_{CKSRX} . When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met.

The precharge power-down mode condition is when the DDR3 SDRAM is in precharge power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or R_{TT_NOM} and R_{TT_WR} must be disabled via MR1 and MR2. This ensures R_{TT_NOM} and R_{TT_WR} are in an off state prior to entering precharge power-down mode, and CKE must be at a logic LOW. A minimum of t_{CKSRE} must occur after CKE goes LOW before the clock frequency can change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade ($t_{CK [AVG] MIN}$ to $t_{CK [AVG] MAX}$). During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the DRAM t_{CKSRX} before precharge power-down may be exited. After precharge power-down is exited and t_{XP} has

been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, RTT_NOM and RTT_WR must remain in an off state. After the DLL lock time, the DRAM is ready to operate with a new clock frequency. This process is depicted in Figure 44.

Figure 44: Change Frequency During Precharge Power-Down



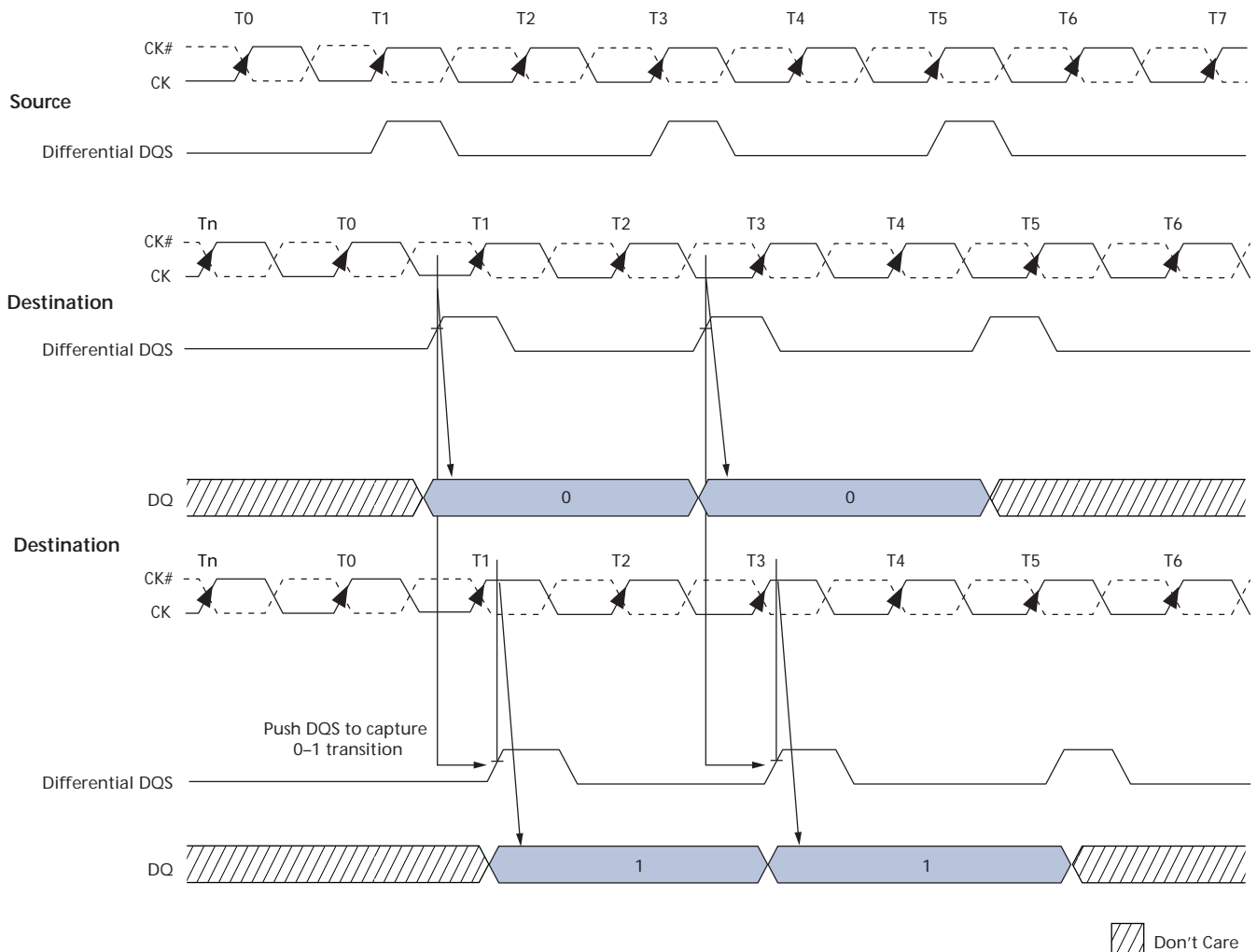
- Notes:
1. Applicable for both slow-exit and fast-exit precharge power-down modes.
 2. t_{AOPFD} and t_{AOF} must be satisfied and outputs High-Z prior to T1 (see "On-Die Termination (ODT)" on page 161 for exact requirements).
 3. If the RTT_NOM feature was enabled in the mode register prior to entering precharge power-down mode, the ODT signal must be continuously registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering precharge power-down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Write Leveling

For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks. Write leveling is a scheme for the memory controller to adjust or deskew the DQS strobe (DQS, DQS#) to CK relationship at the DRAM with a simple feedback feature provided by the DRAM. Write leveling is generally used as part of the initialization process, if required. For normal DRAM operation, this feature must be disabled. This is the only DRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQ function as outputs (to report the state of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the write leveling procedure must have adjustable delay settings on its DQS strobe to align the rising edge of DQS to the clock at the DRAM pins. This is accomplished when the DRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from “0” to “1” is detected. The DQS delay established through this procedure helps ensure t_{DQSS} , t_{DSS} , and t_{DSH} specifications in systems that use fly-by topology by deskewing the trace length mismatch. A conceptual timing of this procedure is shown in Figure 45.

Figure 45: Write Leveling Concept



When write leveling is enabled, the rising edge of DQS samples CK, and the prime DQ outputs the sampled CK's status. The prime DQ for a x4 or x8 configuration is DQ0 with all other DQ (DQ[7:1]) driving LOW. The prime DQ for a x16 configuration is DQ0 for the lower byte and DQ8 for the upper byte. It outputs the status of CK sampled by LDQS and UDQS. All other DQ (DQ[7:1], DQ[15:9]) continue to drive LOW. Two prime DQ on a x16 enable each byte lane to be leveled independently.

The write leveling mode register interacts with other mode registers to correctly configure the write leveling functionality. Besides using MR1[7] to disable/enable write leveling, MR1[12] must be used to enable/disable the output buffers. The ODT value, burst length, and so forth need to be selected as well. This interaction is shown in Table 70. It should also be noted that when the outputs are enabled during write leveling mode, the DQS buffers are set as inputs, and the DQ are set as outputs. Additionally, during write leveling mode, only the DQS strobe terminations are activated and deactivated via the ODT ball. The DQ remain disabled and are not affected by the ODT ball (see Table 70).

Table 70: Write Leveling Matrix
Note 1 applies to the entire table

MR1[7]	MR1[12]	MR1[3, 6, 9]	DRAM ODT Ball	DRAM RTT_NOM		DRAM State	Case	Notes
				DQS	DQ			
Disabled	See normal operations					Write leveling not enabled	0	
Enabled (1)	Disabled (1)	n/a	Low	Off	Off	DQS not receiving: not terminated Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	1	2
		20Ω, 30Ω, 40Ω, 60Ω, or 120Ω	High	On		DQS not receiving: terminated by RTT Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	2	
	Enabled (0)	n/a	Low	Off		DQS receiving: not terminated Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	3	3
		40Ω, 60Ω, or 120Ω	High	On		DQS receiving: terminated by RTT Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	4	

- Notes:
- Expected usage if used during write leveling: Case 1 may be used when DRAM are on a dual-rank module and on the rank not being leveled or on any rank of a module not being leveled on a multislotted system. Case 2 may be used when DRAM are on any rank of a module not being leveled on a multislotted system. Case 3 is generally not used. Case 4 is generally used when DRAM are on the rank that is being leveled.
 - Since the DRAM DQS is not being driven (MR1[12] = 1), DQS ignores the input strobe, and all RTT_NOM values are allowed. This simulates a normal standby state to DQS.
 - Since the DRAM DQS is being driven (MR1[12] = 0), DQS captures the input strobe, and only some RTT_NOM values are allowed. This simulates a normal write state to DQS.

Write Leveling Procedure

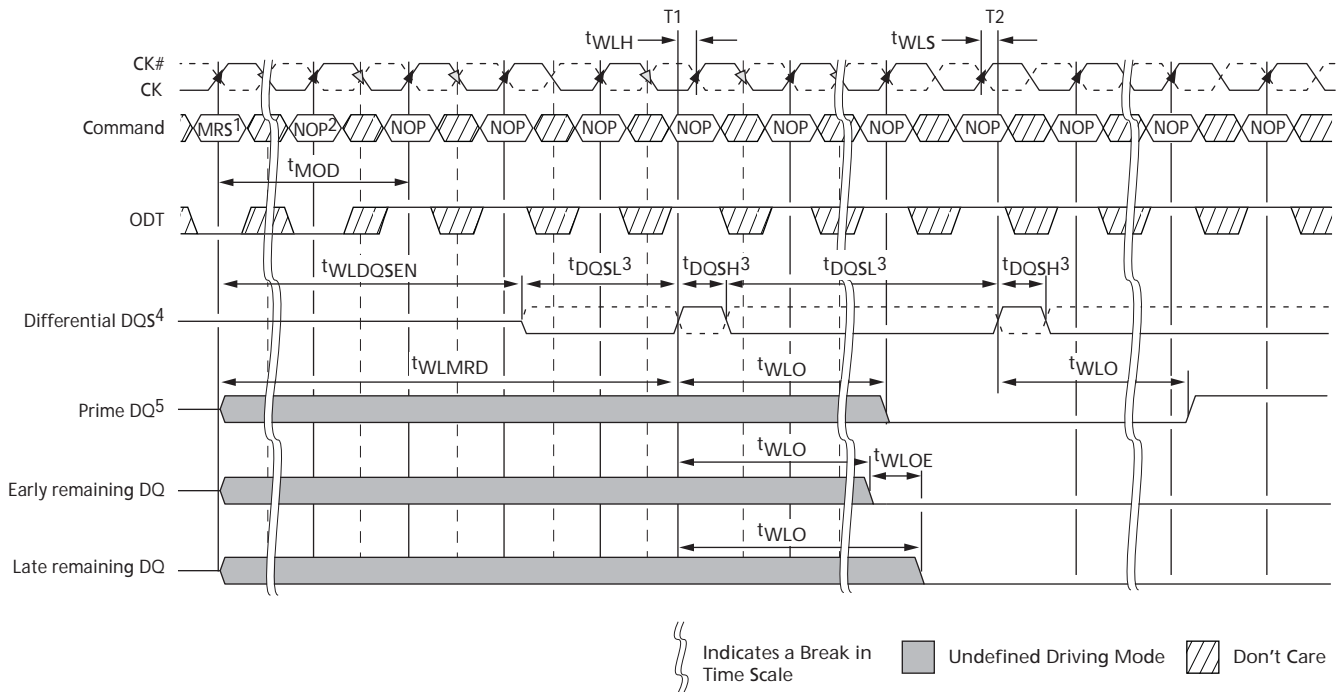
A memory controller initiates the DRAM write leveling mode by setting MR1[7] to a “1,” assuming the other programmable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the write leveling mode going from a High-Z state to an undefined driving state, so the DQ bus should not be driven. During write leveling mode, only the NOP or DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to a “1” in the other ranks. The memory controller may assert ODT after a t^{MOD} delay as the DRAM will be ready to process the ODT transition. ODT should be turned on prior to DQS being driven LOW by at least ODTL on delay ($WL - 2 t^{\text{CK}}$), provided it does not violate the aforementioned t^{MOD} delay requirement.

The memory controller may drive DQS LOW and DQS# HIGH after t^{WLDQSEN} has been satisfied. The controller may begin to toggle DQS after t^{WLMRD} (one DQS toggle is DQS transitioning from a LOW state to a HIGH state with DQS# transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a minimum, ODTL on and t^{AON} must be satisfied at least one clock prior to DQS toggling.

After t^{WLMRD} and a DQS LOW preamble (t^{WPRE}) have been satisfied, the memory controller may provide either a single DQS toggle or multiple DQS toggles to sample CK for a given DQS-to-CK skew. Each DQS toggle must not violate t^{DQSL} (MIN) and t^{DQSH} (MIN) specifications. t^{DQSL} (MAX) and t^{DQSH} (MAX) specifications are not applicable during write leveling mode. The DQS must be able to distinguish the CK's rising edge within t^{WLS} and t^{WLH} . The prime DQ will output the CK's status asynchronously from the associated DQS rising edge CK capture within t^{WLO} . The remaining DQ that always drive LOW when DQS is toggling must be LOW within t^{WLOE} after the first t^{WLO} is satisfied (the prime DQ going LOW). As previously noted, DQS is an input and not an output during this process. Figure 46 on page 106 depicts the basic timing parameters for the overall write leveling procedure.

The memory controller will likely sample each applicable prime DQ state and determine whether to increment or decrement its DQS delay setting. After the memory controller performs enough DQS toggles to detect the CK's “0-to-1” transition, the memory controller should lock the DQS delay setting for that DRAM. After locking the DQS setting, leveling for the rank will have been achieved, and the write leveling mode for the rank should be disabled or reprogrammed (if write leveling of another rank follows).

Figure 46: Write Leveling Sequence



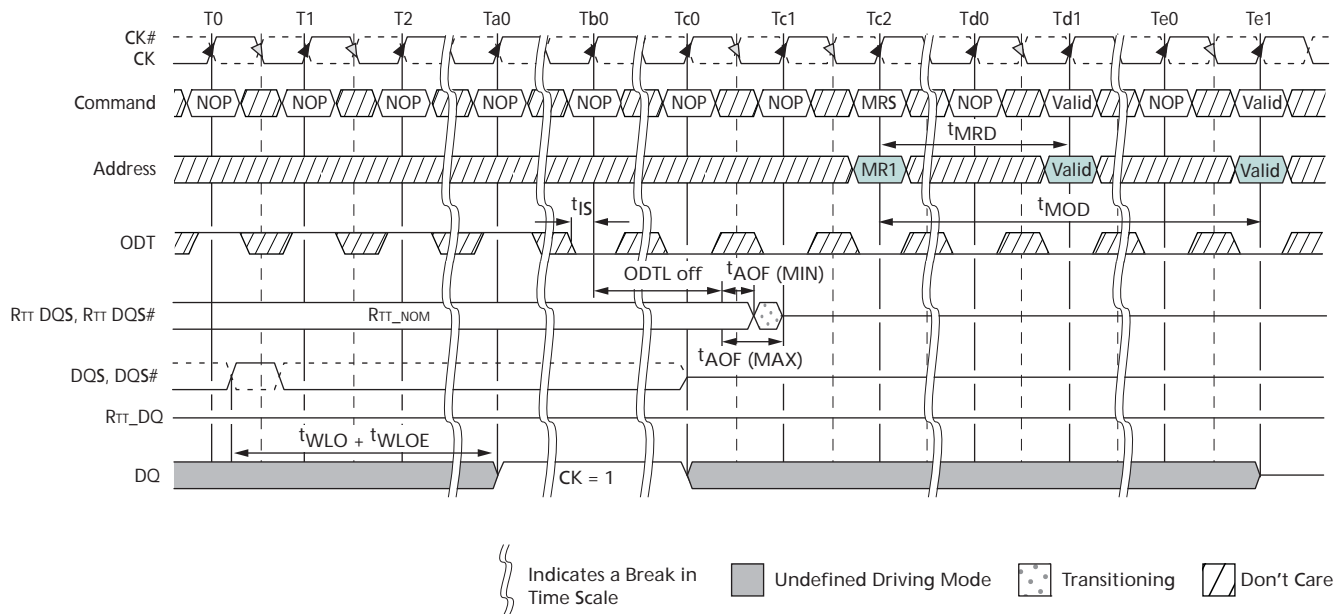
- Notes:
1. MRS: Load MR1 to enter write leveling mode.
 2. NOP: NOP or DES.
 3. DQS, DQS# needs to fulfill minimum pulse width requirements t_{DQSH} (MIN) and t_{DQSL} (MIN) as defined for regular writes. The maximum pulse width is system-dependent.
 4. Differential DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. The solid line represents DQS; the dotted line represents DQS#.
 5. DRAM drives leveling feedback on a prime DQ (DQ0 for x4 and x8). The remaining DQ are driven LOW and remain in this state throughout the leveling procedure.

Write Leveling Mode Exit Procedure

After the DRAM are leveled, they must exit from write leveling mode before the normal mode can be used. Figure 47 on page 107 depicts a general procedure in exiting write leveling mode. After the last rising DQS (capturing a “1” at T0), the memory controller should stop driving the DQS signals after t_{WLO} (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at $\sim T_{b0}$). The DQ balls become undefined when DQS no longer remains LOW, and they remain undefined until t_{MOD} after the MRS command (at T_{e1}).

The ODT input should be deasserted LOW such that ODTL off (MIN) expires after the DQS is no longer driving LOW. When ODT LOW satisfies t_{IS} , ODT must be kept LOW (at $\sim T_{b0}$) until the DRAM is ready for either another rank to be leveled or until the normal mode can be used. After DQS termination is switched off, write level mode should be disabled via the MRS command (at T_{c2}). After t_{MOD} is satisfied (at T_{e1}), any valid command may be registered by the DRAM. Some MRS commands may be issued after t_{MRD} (at T_{d1}).

Figure 47: Exit Write Leveling



Notes: 1. The DQ result, "= 1," between Ta0 and Tc0, is a result of the DQS, DQS# signals capturing CK HIGH just after the T0 state.

Operations

Initialization

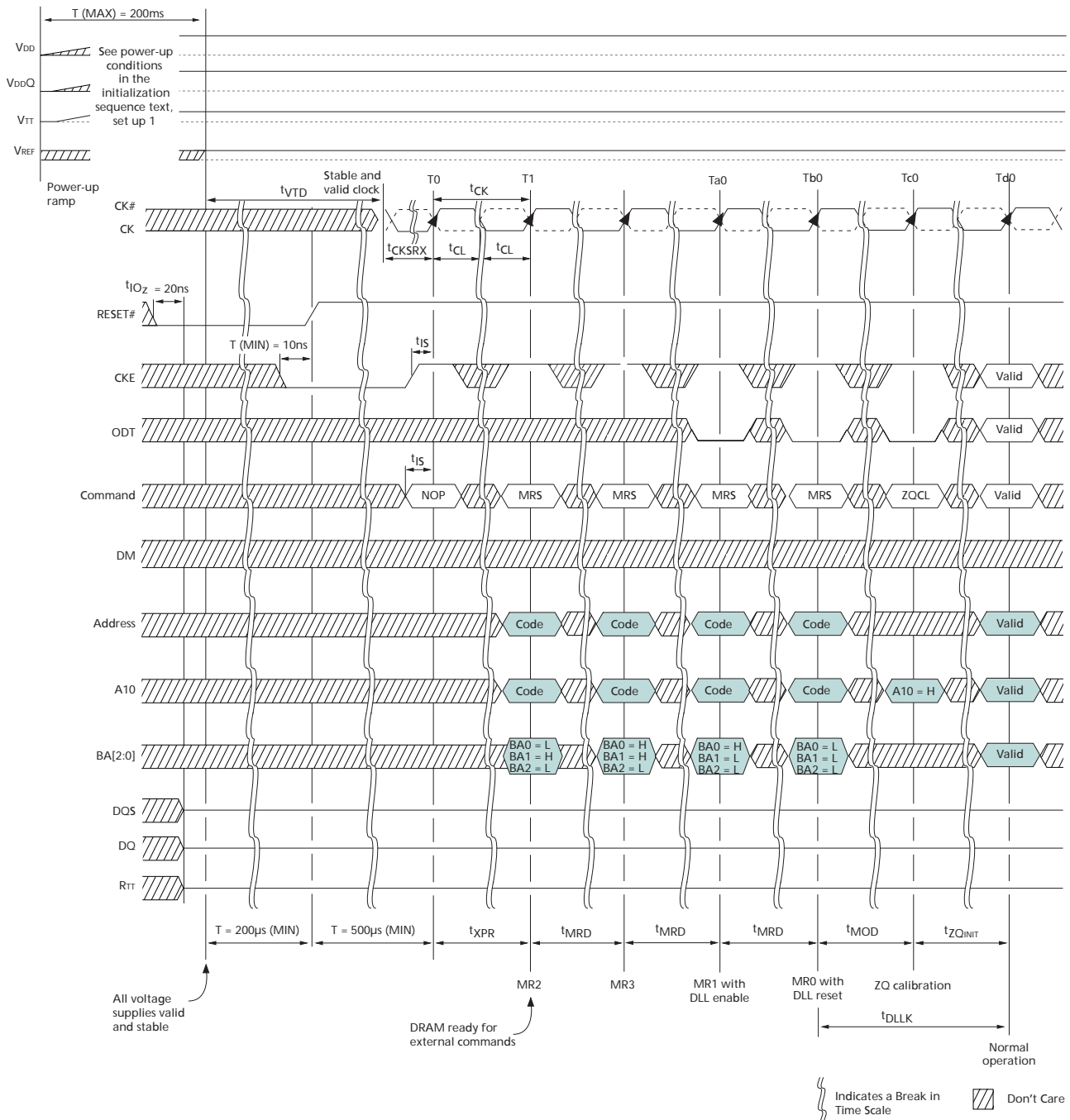
The following sequence is required for power up and initialization, as shown in Figure 48 on page 109:

1. Apply power. RESET# is recommended to be below $0.2 \times VDDQ$ during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (RTT is also High-Z). All other inputs, including ODT, may be undefined.

During power up, either of the following conditions may exist and must be met:

- Condition A:
 - VDD and VDDQ are driven from a single-power converter output and are ramped with a maximum delta voltage between them of $\Delta V \leq 300\text{mV}$. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side, and must be greater than or equal to VSSQ and VSS on the other side.
 - Both VDD and VDDQ power supplies ramp to VDD (MIN) and VDDQ (MIN) within $t_{VDDPR} = 200\text{ms}$.
 - VREFDQ tracks $VDD \times 0.5$, VREFCA tracks $VDD \times 0.5$.
 - VTT is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, t_{VTD} should be greater than or equal to zero to avoid device latchup.
 - Condition B:
 - VDD may be applied before or at the same time as VDDQ.
 - VDDQ may be applied before or at the same time as VTT, VREFDQ, and VREFCA.
 - No slope reversals are allowed in the power supply ramp for this condition.
2. Until stable power, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200 μs to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.
 3. CKE must be LOW 10ns prior to RESET# transitioning HIGH.
 4. After RESET# transitions HIGH, wait 500 μs (minus one clock) with CKE LOW.
 5. After this CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least t_{IS} prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.
 6. After CKE is registered HIGH and after t_{XPR} has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
 7. Issue an MRS command to MR3 with the applicable settings.
 8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.
 9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. t_{DLLK} (512) cycles of clock input are required to lock the DLL.
 10. Issue a ZQCL command to calibrate RTT and RON values for the process voltage temperature (PVT). Prior to normal operation, t_{ZQINIT} must be satisfied.
 11. When t_{DLLK} and t_{ZQINIT} have been satisfied, the DDR3 SDRAM will be ready for normal operation.

Figure 48: Initialization Sequence



Mode Registers

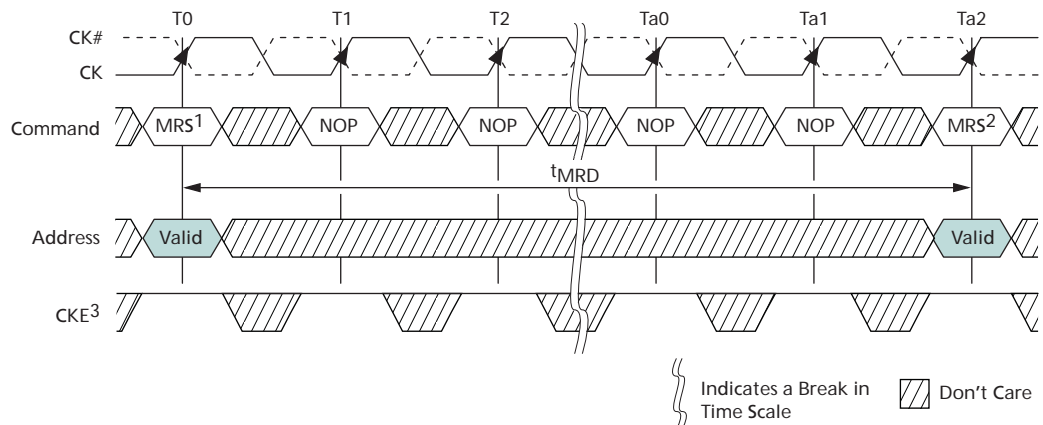
Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3 SDRAM. A mode register is programmed via the MODE REGISTER SET (MRS) command during initialization, and it retains the stored information (except for MR0[8] which is self-clearing) until it is either reprogrammed, RESET# goes LOW, or until the device loses power.

Contents of a mode register can be altered by reexecuting the MRS command. If the user chooses to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state (t_{RP} is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: t_{MRD} and t_{MOD} .

The controller must wait t_{MRD} before initiating any subsequent MRS commands (see Figure 49).

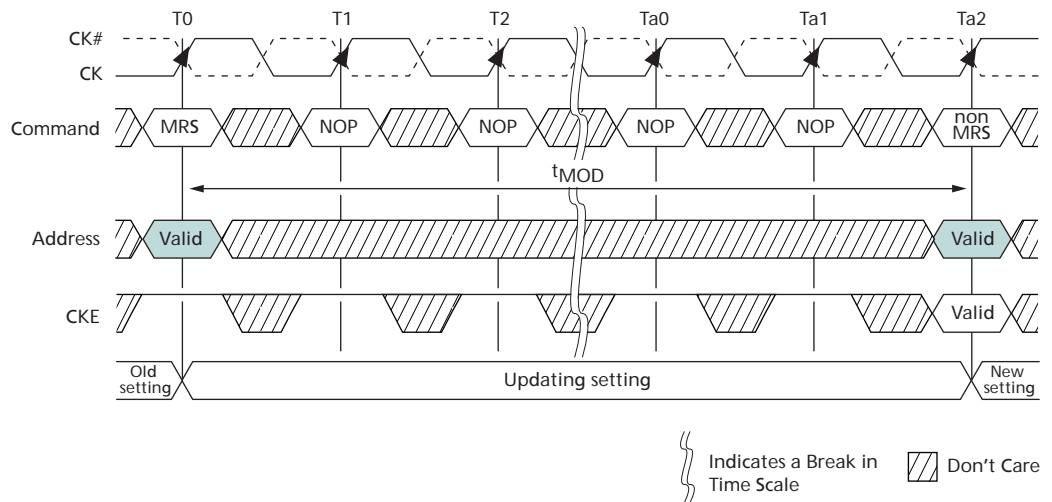
Figure 49: MRS-to-MRS Command Timing (t_{MRD})



- Notes:
1. Prior to issuing the MRS command, all banks must be idle and precharged, t_{RP} (MIN) must be satisfied, and no data bursts can be in progress.
 2. t_{MRD} specifies the MRS-to-MRS command minimum cycle time.
 3. CKE must be registered HIGH from the MRS command until $t_{MRSPDEN}$ (MIN) (see "Power-Down Mode" on page 153).
 4. For a CAS latency change, t_{XPDLL} timing must be met before any nonMRS command.

The controller must also wait t_{MOD} before initiating any nonMRS commands (excluding NOP and DES), as shown in Figure 50 on page 111. The DRAM requires t_{MOD} in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until t_{MOD} has been satisfied, the updated features are to be assumed unavailable.

Figure 50: MRS-to-nonMRS Command Timing (t_{MOD})



- Notes:
1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, t_{RP} must be satisfied, and no data bursts can be in progress).
 2. Prior to $Ta2$ when t_{MOD} (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
 3. If RTT was previously enabled, ODT must be registered LOW at $T0$ so that ODTL is satisfied prior to $Ta1$. ODT must also be registered LOW at each rising CK edge from $T0$ until t_{MOD} (MIN) is satisfied at $Ta2$.
 4. CKE must be registered HIGH from the MRS command until $t_{MRSPDEN}$ (MIN), at which time power-down may occur (see "Power-Down Mode" on page 153).

Mode Register 0 (MR0)

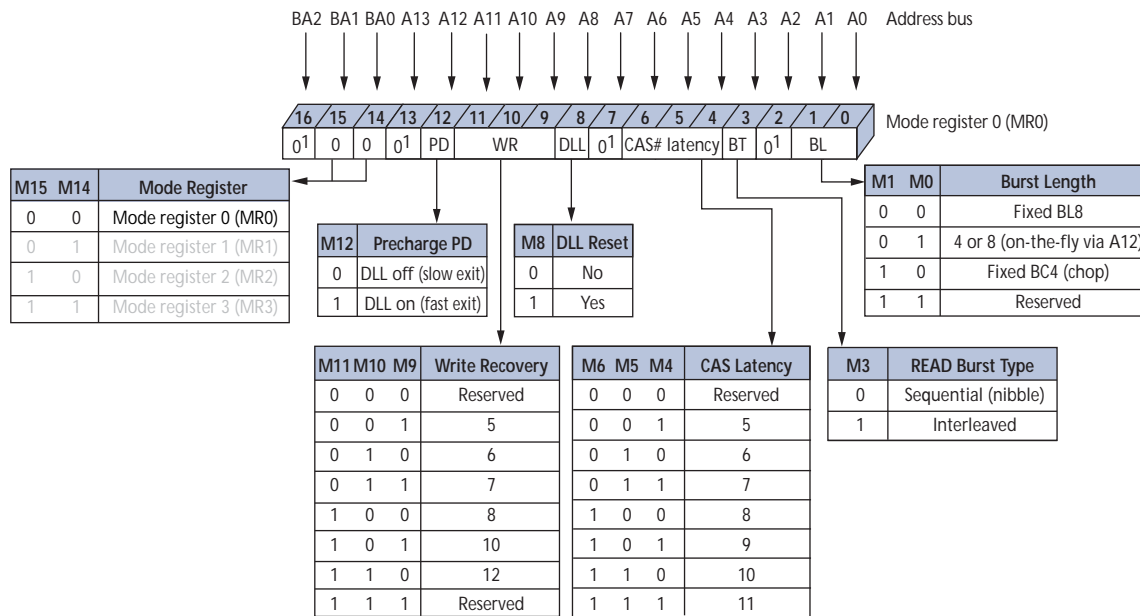
The base register, MR0, is used to define various DDR3 SDRAM modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and precharge power-down mode, as shown in Figure 51 on page 112.

Burst Length

Burst length is defined by MR0[1:0] (see Figure 51 on page 112). Read and write accesses to the DDR3 SDRAM are burst-oriented, with the burst length being programmable to "4" (chop mode), "8" (fixed), or selectable using A12 during a READ/WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to "01" during a READ/WRITE command, if A12 = 0, then BC4 (chop) mode is selected. If A12 = 1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE, are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by $A[i:2]$ when the burst length is set to "4" and by $A[i:3]$ when the burst length is set to "8" (where A_i is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Figure 51: Mode Register 0 (MR0) Definitions



Notes: 1. MR0[16, 13, 7, 2] are reserved for future use and must be programmed to "0."

Burst Type

Accesses within a given burst may be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3], as shown in Figure 51. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 71 on page 113. DDR3 only supports 4-bit burst chop and 8-bit burst access modes. Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

Table 71: Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
4 chop	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4
8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

- Notes:
1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
 2. Z = Data and strobe output drivers are in tri-state.
 3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
 4. X = "Don't Care."

DLL RESET

DLL RESET is defined by MR0[8] (see Figure 51 on page 112). Programming MR0[8] to "1" activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of "0" after the DLL RESET function has been initiated.

Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 512 (^tDLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in invalid output timing specifications, such as ^tDQSCK timings.

Write Recovery

WRITE recovery time is defined by MR0[11:9] (see Figure 51 on page 112). Write recovery values of 5, 6, 7, 8, 10, or 12 may be used by programming MR0[11:9]. The user is required to program the correct value of write recovery and is calculated by dividing ^tWR (ns) by ^tCK (ns) and rounding up a noninteger value to the next integer: WR (cycles) = roundup (^tWR [ns]/^tCK [ns]).

Precharge Power-Down (Precharge PD)

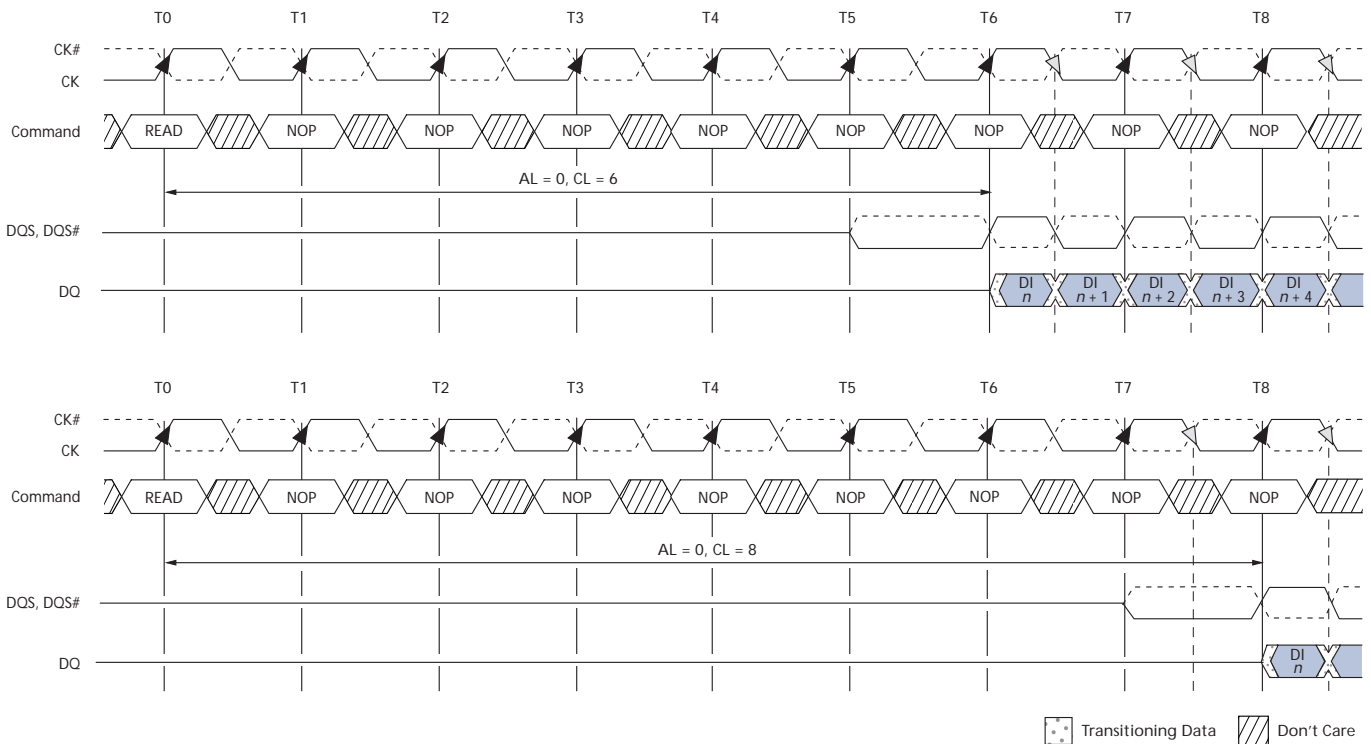
The precharge PD bit applies only when precharge power-down mode is being used. When MR0[12] is set to “0,” the DLL is off during precharge power-down providing a lower standby current mode; however, t_{XPDLL} must be satisfied when exiting. When MR0[12] is set to “1,” the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, t_{XP} must be satisfied when exiting (see “Power-Down Mode” on page 153).

CAS Latency (CL)

The CL is defined by MR0[6:4], as shown in Figure 51 on page 112. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The CL can be set to 5, 6, 7, 8, 9, or 10. DDR3 SDRAM do not support half-clock latencies.

Examples of CL = 6 and CL = 8 are shown in Figure 52. If an internal READ command is registered at clock edge n , and the CAS latency is m clocks, the data will be available nominally coincident with clock edge $n + m$. Table 52 on page 66 through Table 54 on page 68 indicate the CLs supported at various operating frequencies.

Figure 52: READ Latency



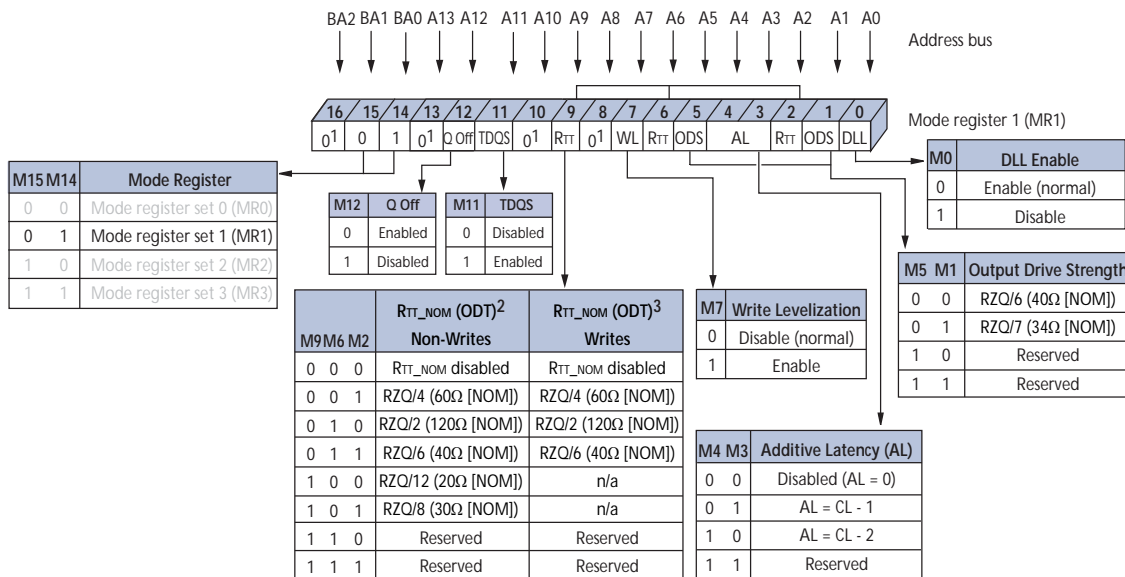
- Notes:
1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.
 2. Shown with nominal t_{DQSK} and nominal t_{DSDQ} .

Mode Register 1 (MR1)

The mode register 1 (MR1) controls additional functions and features not available in the other mode registers: Q OFF (OUTPUT DISABLE), TDQS (for the x8 configuration only), DLL ENABLE/DLL DISABLE, RTT_NOM value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits shown in Figure 53. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, until RESET# goes LOW, or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is performed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters ⁴MRD and ⁴MOD before initiating a subsequent operation.

Figure 53: Mode Register 1 (MR1) Definition



- Notes:
1. MR1[16, 13, 10, 8] are reserved for future use and must be programmed to "0."
 2. During write leveling, if MR1[7] and MR1[12] are "1" then all RTT_NOM values are available for use.
 3. During write leveling, if MR1[7] is a "1," but MR1[12] is a "0," then only RTT_NOM write values are available for use.

DLL Enable/DLL Disable

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command, as shown in Figure 53. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation and is automatically reenabled and reset upon exit of SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled even upon exit of SELF REFRESH operation until it is reenabled and reset.

The DRAM is not tested to check—nor does Micron warrant compliance with—normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

1. ODT is not allowed to be used.
2. The output data is no longer edge-aligned to the clock.
3. CL and CWL can only be six clocks.

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled (see “DLL Disable Mode” on page 98). Disabling the DLL also implies the need to change the clock frequency (see “Input Clock Frequency Change” on page 101).

Output Drive Strength

The DDR3 SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3 SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and VSSQ. The value of the resistor must be $240\Omega \pm 1\%$.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by MR1[12], as shown in Figure 53 on page 115. When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3 SDRAM outputs (DQ and DQS, DQS#) are tri-stated. The output disable feature is intended to be used during IDD characterization of the READ current and during t^{DQSS} margining (write leveling) only.

TDQS Enable

Termination data strobe (TDQS) is a feature of the x8 DDR3 SDRAM configuration, which provides termination resistance (R_{TT}), that may be useful in some system configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register (MR1[11]), the R_{TT} that is applied to DQS and DQS# is also applied to TDQS and TDQS#. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance R_{TT} only. The OUTPUT DATA STROBE function of RDQS is not provided by TDQS; thus, R_{ON} does not apply to TDQS and TDQS#. The TDQS and DM functions share the same ball. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided, and the TDQS# ball is not used. The TDQS function is available in the x8 DDR3 SDRAM configuration only and must be disabled via the mode register for the x4 and x16 configurations.

On-Die Termination

ODT resistance RTT_NOM is defined by MR1[9, 6, 2] (see Figure 53 on page 115). The RTT termination value applies to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls. DDR3 supports multiple RTT termination values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω .

Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. RTT_NOM termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT enabled (RTT_WR) temporarily replaces RTT_NOM with RTT_WR .

The actual effective termination, RTT_EFF , may be different from the RTT targeted due to nonlinearity of the termination. For RTT_EFF values and calculations (see “On-Die Termination (ODT)” on page 161).

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when RTT is turned on (ODTL on) and off (ODTL off), assuming ODT has been enabled via MR1[9, 6, 2].

Timings for ODT are detailed in “On-Die Termination (ODT)” on page 161.

WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7], as shown in Figure 53 on page 115. Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks.

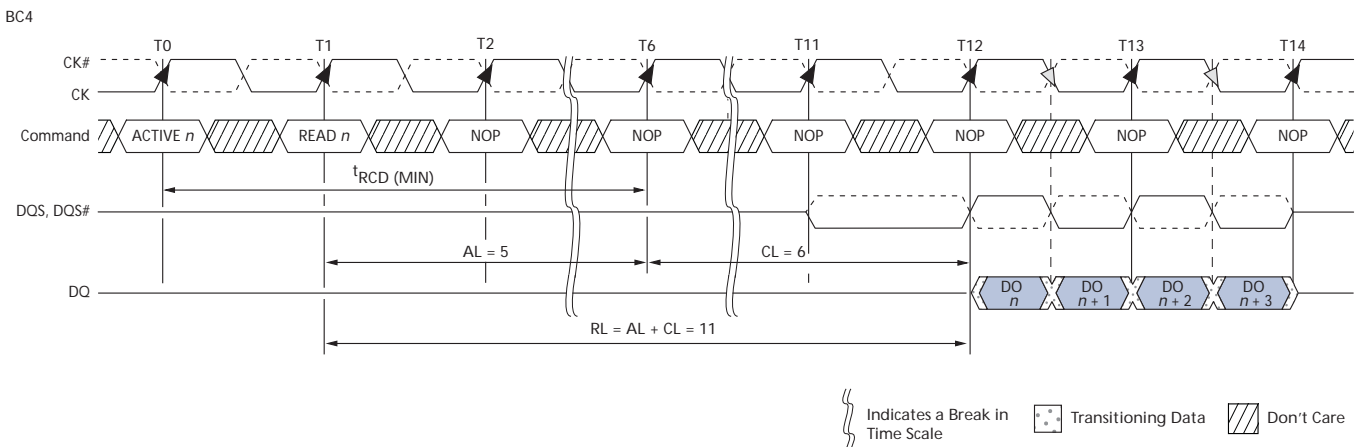
The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining t_{DQSS} , t_{DSS} , and t_{DSH} specifications without supporting write leveling in systems which use fly-by topology-based modules. Write leveling timing and detailed operation information is provided in “Write Leveling” on page 103.

POSTED CAS ADDITIVE Latency (AL)

AL is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1[4, 3] define the value of AL as shown in Figure 54 on page 118. MR1[4, 3] enable the user to program the DDR3 SDRAM with an $AL = 0$, $CL - 1$, or $CL - 2$.

With this feature, the DDR3 SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to t_{RCD} (MIN). The only restriction is $ACTIVATE$ to READ or WRITE + $AL \geq t_{RCD}$ (MIN) must be satisfied. Assuming t_{RCD} (MIN) = CL , a typical application using this feature sets $AL = CL - 1 \cdot t_{CK} = t_{RCD}$ (MIN) - $1 \cdot t_{CK}$. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3 SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), $RL = AL + CL$. WRITE latency (WL) is the sum of CAS WRITE latency and AL, $WL = AL + CWL$ (see “Mode Register 2 (MR2)” on page 118). Examples of READ and WRITE latencies are shown in Figure 54 on page 118 and Figure 56 on page 119.

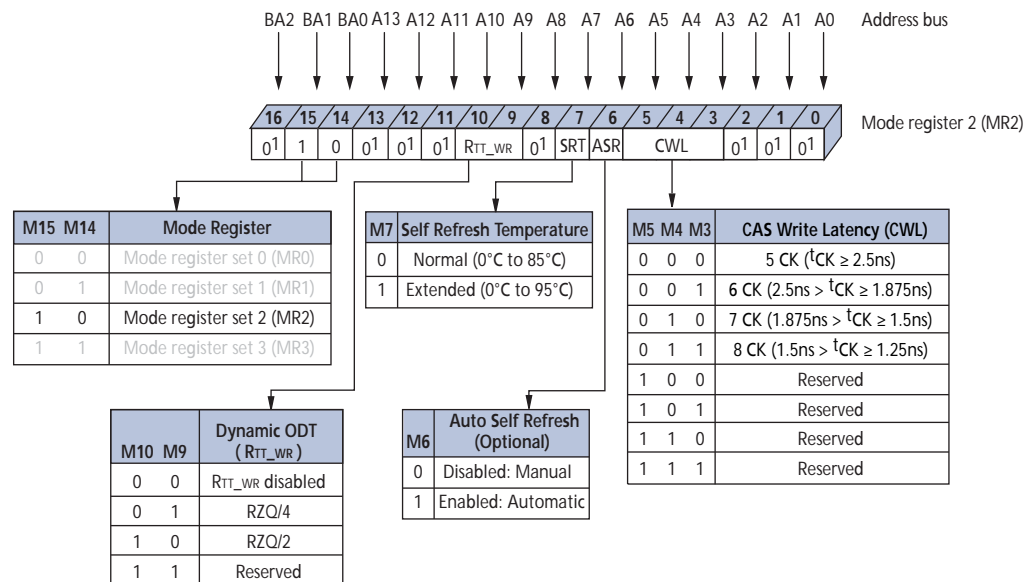
Figure 54: READ Latency (AL = 5, CL = 6)



Mode Register 2 (MR2)

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT (RTT_WR). These functions are controlled via the bits shown in Figure 55. The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time t_{MRD} and t_{MOD} before initiating a subsequent operation.

Figure 55: Mode Register 2 (MR2) Definition

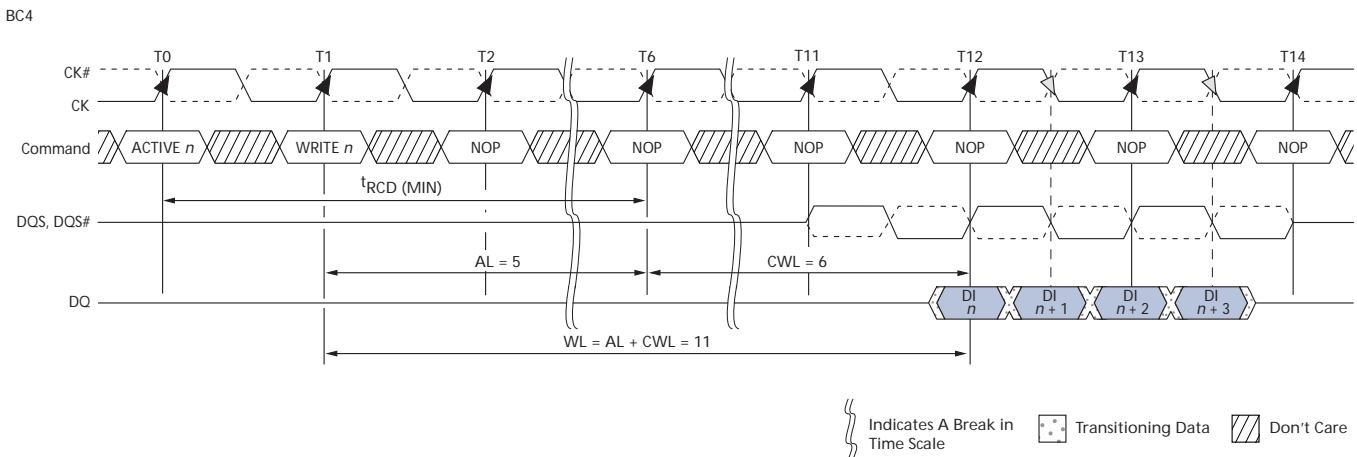


Notes: 1. MR2[16, 13:11, 8, and 2:0] are reserved for future use and must all be programmed to "0."

CAS Write Latency (CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 55 on page 118). The overall WRITE latency (WL) is equal to CWL + AL (Figure 53 on page 115), as shown in Figure 56.

Figure 56: CAS Write Latency



AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function.

When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1X refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds a T_C of 85°C while in self refresh unless the user enables the SRT feature listed below when the T_C is between 85°C and 95°C.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1X to 2X when the case temperature exceeds 85°C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.

The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if ASR is enabled, the standard self refresh current specifications do not apply (see "Extended Temperature Usage" on page 152).

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1X refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a T_C of 85°C while in self refresh mode unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1X to 2X, regardless of the case temperature. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode. The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if SRT is enabled, the standard self refresh current specifications do not apply (see "Extended Temperature Usage" on page 152).

SRT vs. ASR

If the normal case temperature limit of 85°C is not exceeded, then neither SRT nor ASR is required, and both can be disabled throughout operation. However, if the extended temperature option of 95°C is needed, the user is required to provide a 2X refresh rate during (manual) refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2X rate.

SRT forces the DRAM to switch the internal self refresh rate from 1X to 2X. Self refresh is performed at the 2X refresh rate regardless of the case temperature.

ASR automatically switches the DRAM's internal self refresh rate from 1X to 2X. However, while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1X to 2X over the supported temperature range. One other disadvantage with ASR is the DRAM cannot always switch from a 1X to a 2X refresh rate at an exact case temperature of 85°C. Although the DRAM will support data integrity when it switches from a 1X to a 2X refresh rate, it may switch at a lower temperature than 85°C.

Since only one mode is necessary, SRT and ASR cannot be enabled at the same time.

DYNAMIC ODT

The dynamic ODT (R_{TT_WR}) feature is defined by MR2[10, 9]. Dynamic ODT is enabled when a value is selected. This new DDR3 SDRAM feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination “on-the-fly.”

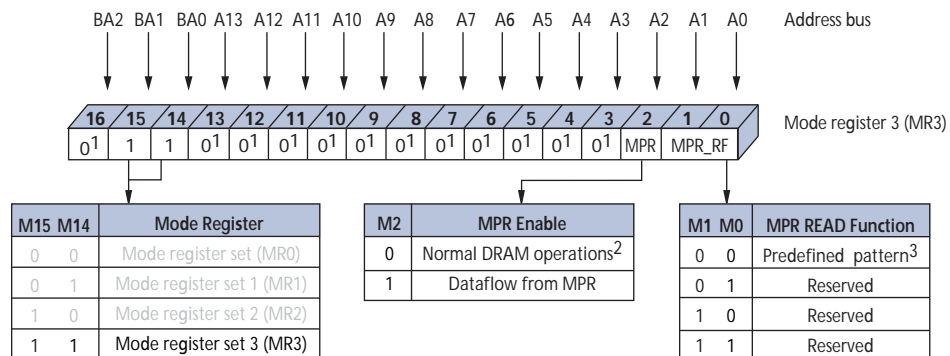
With dynamic ODT (R_{TT_WR}) enabled, the DRAM switches from normal ODT (R_{TT_NOM}) to dynamic ODT (R_{TT_WR}) when beginning a WRITE burst and subsequently switches back to ODT (R_{TT_NOM}) at the completion of the WRITE burst. If R_{TT_NOM} is disabled, the R_{TT_NOM} value will be High-Z. Special timing parameters must be adhered to when dynamic ODT (R_{TT_WR}) is enabled: ODT_{LCNW} , ODT_{LCNW4} , ODT_{LCNW8} , $ODTH4$, $ODTH8$, and t_{ADC} .

Dynamic ODT is only applicable during WRITE cycles. If ODT (R_{TT_NOM}) is disabled, dynamic ODT (R_{TT_WR}) is still permitted. R_{TT_NOM} and R_{TT_WR} can be used independent of one other. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT (R_{TT_NOM}). For details on dynamic ODT operation, refer to “On-Die Termination (ODT)” on page 161.

Mode Register 3 (MR3)

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in Figure 57. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time ^tMRD and ^tMOD before initiating a subsequent operation.

Figure 57: Mode Register 3 (MR3) Definition



- Notes:
1. MR3[16 and 13:4] are reserved for future use and must all be programmed to "0."
 2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
 3. Intended to be used for READ synchronization.

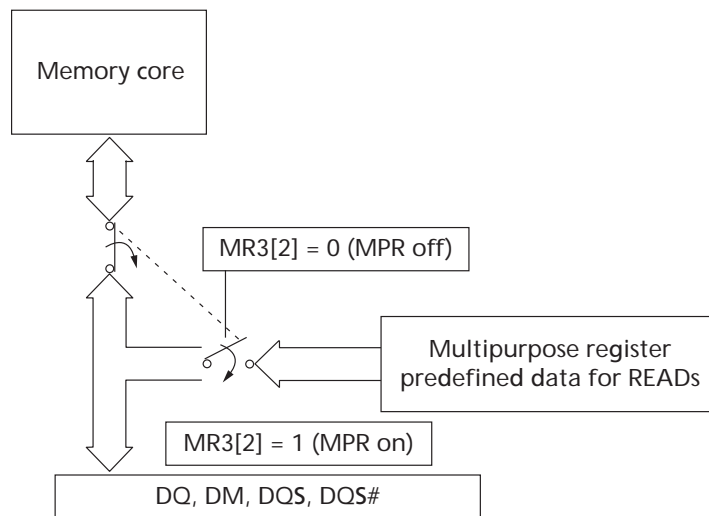
MULTIPURPOSE REGISTER (MPR)

The MULTIPURPOSE REGISTER function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 58 on page 122.

If MR3[2] is a "0," then the MPR access is disabled, and the DRAM operates in normal mode. However, if MR3[2] is a "1," then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] is equal to "00," then a predefined read pattern for system calibration is selected.

To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1 (see Table 72 on page 122). Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and ^tRP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or a RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled (see Table 73 on page 123). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0). Power-down mode, self refresh, and any other nonREAD/RDAP command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Figure 58: Multipurpose Register (MPR) Block Diagram



- Notes:
1. A predefined data pattern can be read out of the MPR with an external READ command.
 2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

Table 72: MPR Functional Description of MR3 Bits

MR3[2]	MR3[1:0]	Function
MPR	MPR READ Function	
0	"Don't Care"	Normal operation, no MPR transaction All subsequent READs come from the DRAM memory array All subsequent WRITES go to the DRAM memory array
1	A[1:0] (see Table 73 on page 123)	Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2

MPR Functional Description

The MPR JEDEC definition allows for either a prime DQ (DQ0 on a x4 and a x8; on a x16, DQ0 = lower byte and DQ8 = upper byte) to output the MPR data with the remaining DQs driven LOW or for all DQs to output the MPR data. The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows:

- A[1:0] must be set to "00" as the burst order is fixed per nibble
- A2 selects the burst order:
 - BL8, A2 is set to "0," and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7
- For burst chop 4 cases, the burst order is switched on the nibble base and:
 - A2 = 0; burst order = 0, 1, 2, 3
 - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB
- A[9:3] are a "Don't Care"
- A10 is a "Don't Care"

- A11 is a “Don’t Care”
- A12: Selects burst chop mode on-the-fly, if enabled within MR0
- A13 is a “Don’t Care”
- BA[2:0] are a “Don’t Care”

MPR Register Address Definitions and Bursting Order

The MPR currently supports a single data format. This data format is a predefined read pattern for system calibration. The predefined pattern is always a repeating 0–1 bit pattern.

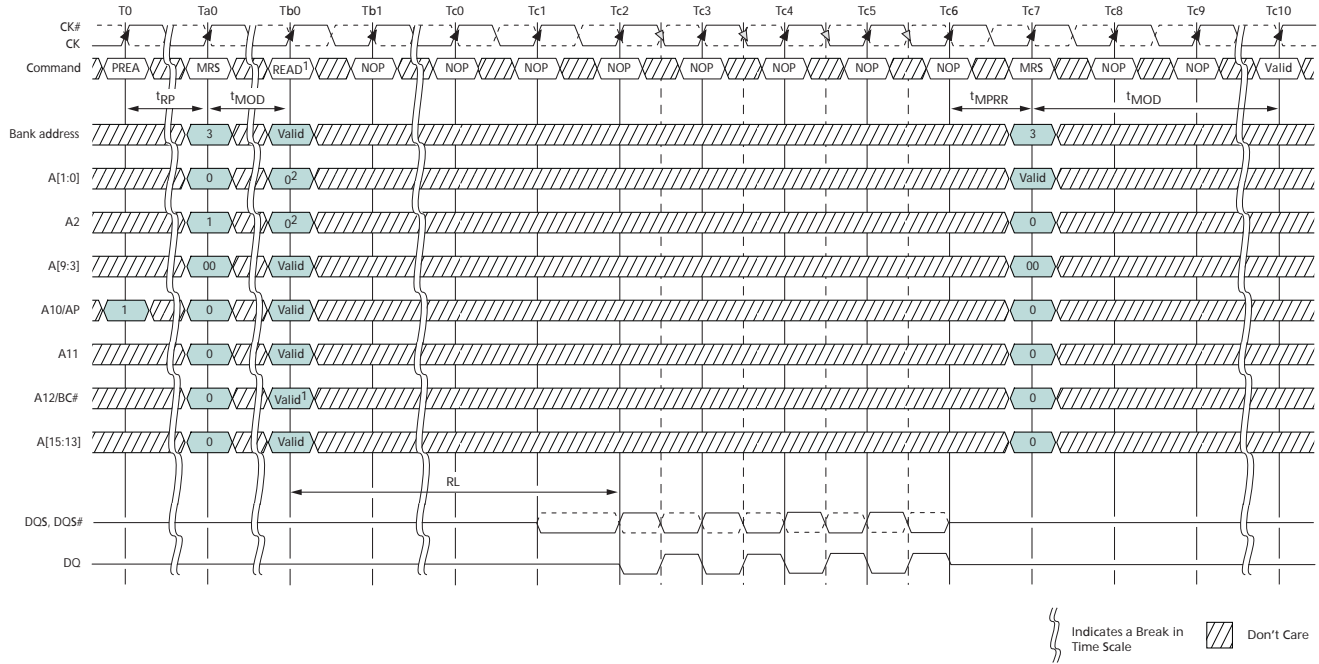
Examples of the different types of predefined READ pattern bursts are shown in Figure 59 on page 124, Figure 60 on page 125, Figure 61 on page 126, and Figure 62 on page 127.

Table 73: MPR Readouts and Burst Order Bit Mapping

MR3[2]	MR3[1:0]	Function	Burst Length	Read A[2:0]	Burst Order and Data Pattern
1	00	READ predefined pattern for system calibration	BL8	000	Burst order: 0, 1, 2, 3, 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1, 0, 1, 0, 1
			BC4	000	Burst order: 0, 1, 2, 3 Predefined pattern: 0, 1, 0, 1
			BC4	100	Burst order: 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1
1	01	RFU	n/a	n/a	n/a
			n/a	n/a	n/a
			n/a	n/a	n/a
1	10	RFU	n/a	n/a	n/a
			n/a	n/a	n/a
			n/a	n/a	n/a
1	11	RFU	n/a	n/a	n/a
			n/a	n/a	n/a
			n/a	n/a	n/a

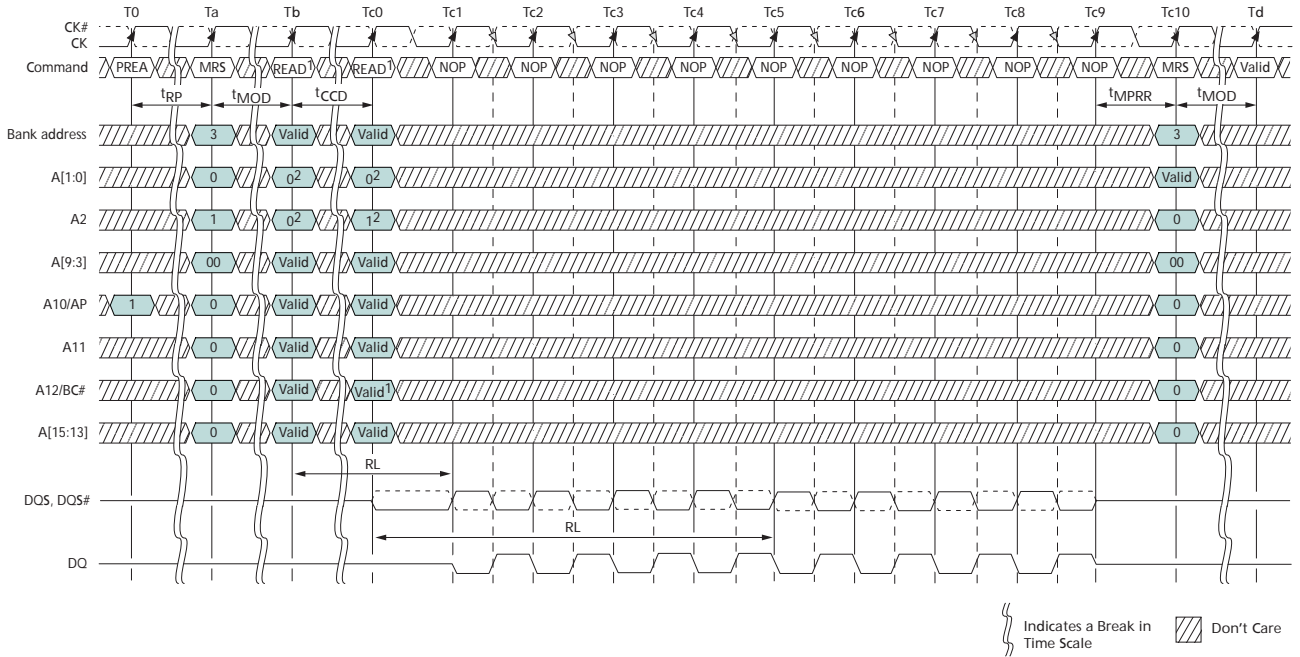
Notes: 1. Burst order bit 0 is assigned to LSB, and burst order bit 7 is assigned to MSB of the selected MPR agent.

Figure 59: MPR System Read Calibration with BL8: Fixed Burst Order Single Readout



- Notes:
1. READ with BL8 either by MRS or OTF.
 2. Memory controller must drive 0 on A[2:0].

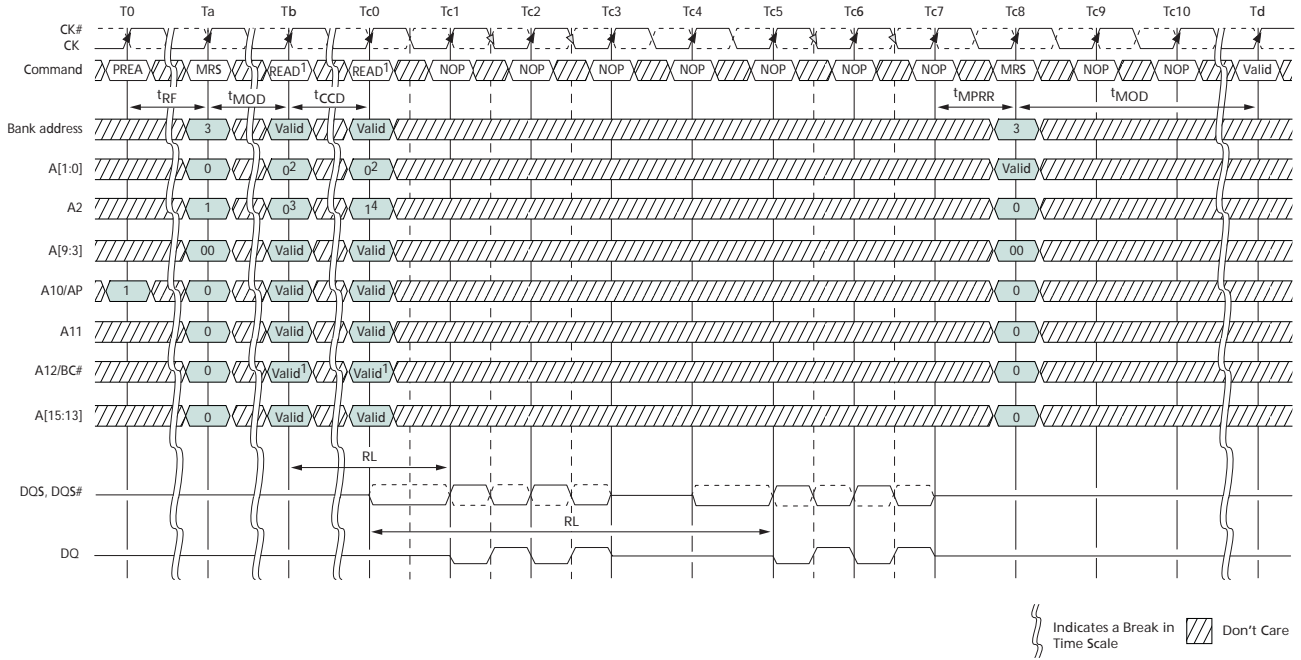
Figure 60: MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout



- Notes:
1. READ with BL8 either by MRS or OTF.
 2. Memory controller must drive 0 on A[2:0].

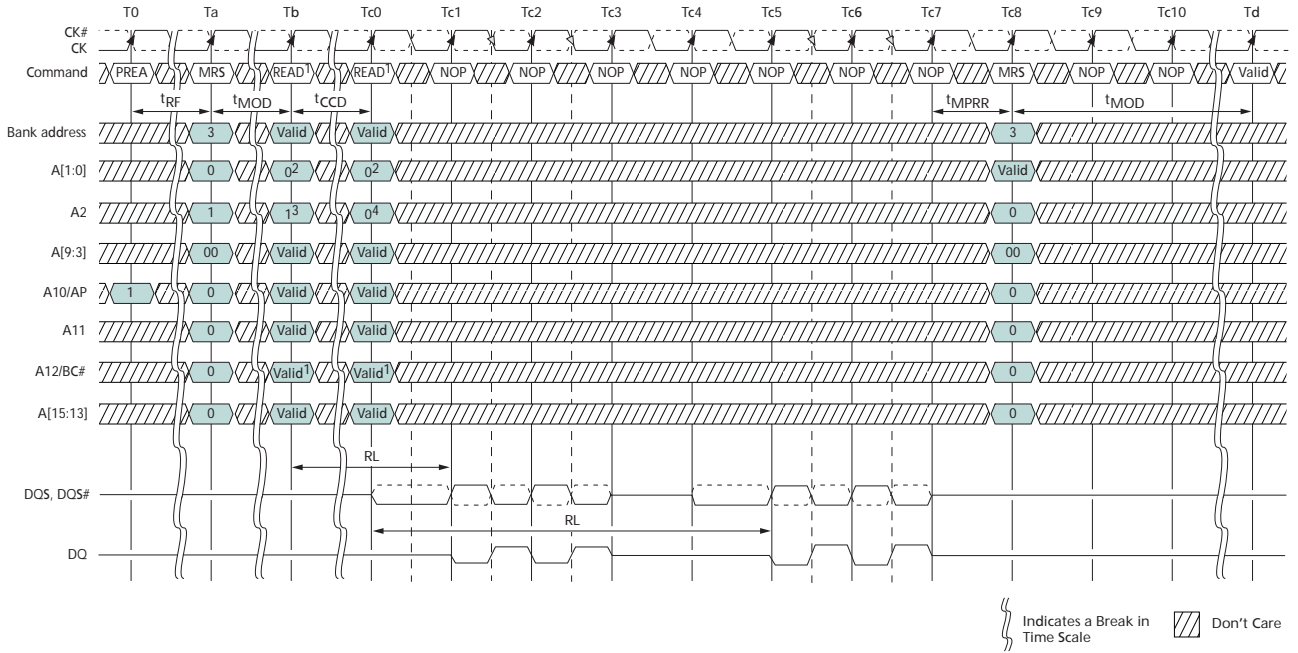


Figure 61: MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble



- Notes:
1. READ with BC4 either by MRS or OTF.
 2. Memory controller must drive 0 on A[1:0].
 3. A2 = 0 selects lower 4 nibble bits 0 . . . 3.
 4. A2 = 1 selects upper 4 nibble bits 4 . . . 7.

Figure 62: MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble



- Notes:
1. READ with BC4 either by MRS or OTF.
 2. Memory controller must drive 0 on A[1:0].
 3. A2 = 1 selects upper 4 nibble bits 4 . . . 7.
 4. A2 = 0 selects lower 4 nibble bits 0 . . . 3.



MPR Read Predefined Pattern

The predetermined read calibration pattern is a fixed pattern of 0, 1, 0, 1, 0, 1, 0, 1. The following is an example of using the read out predetermined read calibration pattern. The example is to perform multiple reads from the multipurpose register in order to do system level read timing calibration based on the predetermined and standardized pattern.

The following protocol outlines the steps used to perform the read calibration:

- Precharge all banks
- After t_{RP} is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all subsequent reads and loads the predefined pattern into the MPR. As soon as t_{MRD} and t_{MOD} are satisfied, the MPR is available
- Data WRITE operations are not allowed until the MPR returns to the normal DRAM state
- Issue a read with burst order information (all other address pins are “Don’t Care”):
 - A[1:0] = 00 (data burst order is fixed starting at nibble)
 - A2 = 0 (for BL8, burst order is fixed as 0, 1, 2, 3, 4, 5, 6, 7)
 - A12 = 1 (use BL8)
- After $RL = AL + CL$, the DRAM bursts out the predefined read calibration pattern (0, 1, 0, 1, 0, 1, 0, 1)
- The memory controller repeats the calibration reads until read data capture at memory controller is optimized
- After the last MPR READ burst and after t_{MPRR} has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] = “Don’t Care” to the normal DRAM state. All subsequent read and write accesses will be regular reads and writes from/to the DRAM array
- When t_{MRD} and t_{MOD} are satisfied from the last MRS, the regular DRAM commands (such as activate a memory bank for regular read or write access) are permitted

MODE REGISTER SET (MRS)

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state (t_{RP} is satisfied and no data bursts are in progress). The controller must wait the specified time t_{MRD} before initiating a subsequent operation such as an ACTIVATE command (see Figure 49 on page 110). There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by t_{MOD} . Both t_{MRD} and t_{MOD} parameters are shown in Figure 49 on page 110 and Figure 50 on page 111. Violating either of these requirements will result in unspecified operation.

ZQ CALIBRATION

The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (RON) and ODT values (RTT) over process, voltage, and temperature, provided a dedicated 240Ω (±1 percent) external resistor is connected from the DRAM’s ZQ ball to VSSQ.

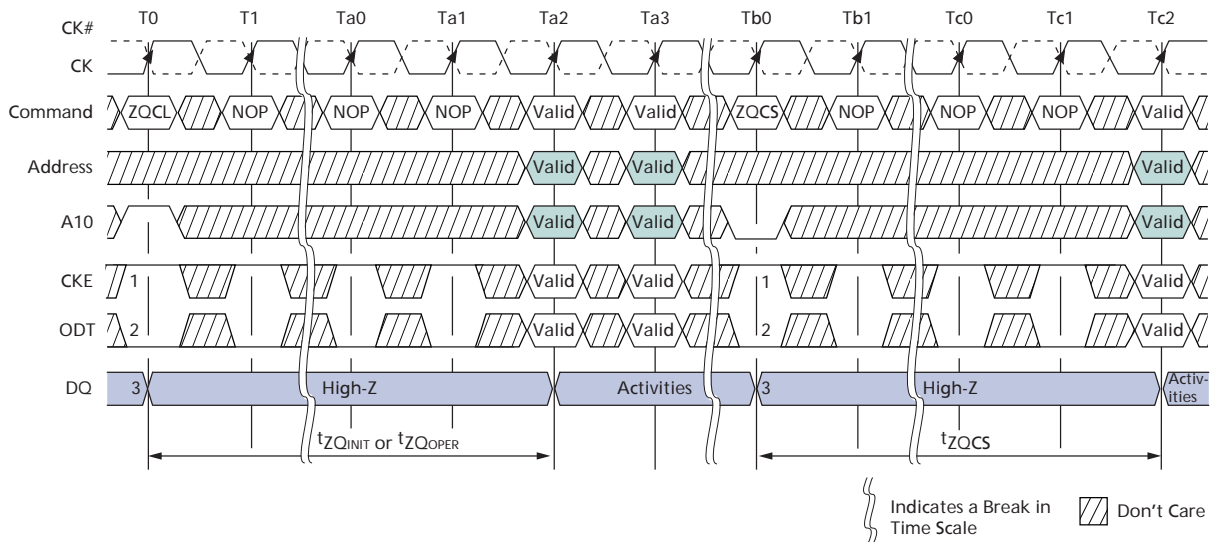
DDR3 SDRAM need a longer time to calibrate RON and ODT at power-up initialization and self refresh exit and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands: ZQ CALIBRATION LONG (ZQCL) and ZQ CALIBRATION SHORT (ZQCS). An example of ZQ calibration timing is shown in Figure 63.

All banks must be precharged and t^{RP} must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than another ZQCL or ZQCS command may be issued to another DRAM) can be performed on the DRAM channel by the controller for the duration of t^{ZQINIT} or t^{ZQOPER} . The quiet time on the DRAM channel helps accurately calibrate RON and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

In dual-rank systems that share the ZQ resistor between devices, the controller must not allow overlap of t^{ZQINIT} , t^{ZQOPER} , or t^{ZQCS} between ranks.

Figure 63: ZQ Calibration Timing (ZQCL and ZQCS)



- Notes:
1. CKE must be continuously registered HIGH during the calibration procedure.
 2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
 3. All devices connected to the DQ bus should be High-Z during calibration.

ACTIVATE

Before any READ or WRITE commands can be issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row, subject to the t^{RCD} specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to t^{RCD} (MIN). In this operation, the DRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to t^{RCD} (MIN) with the requirement that $(\text{ACTIVATE-to-READ/WRITE}) + \text{AL} \geq t^{\text{RCD}}$ (MIN) (see "POSTED CAS ADDITIVE Latency (AL)" on page 117). t^{RCD} (MIN) should be divided by the clock period and rounded up to

the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to t_{CCD} (MIN).

A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by t_{RC} .

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by t_{RRD} . No more than four bank ACTIVATE commands may be issued in a given t_{FAW} (MIN) period, and the t_{RRD} (MIN) restriction still applies. The t_{FAW} (MIN) parameter applies, regardless of the number of banks already opened or closed.

Figure 64: Example: Meeting t_{RRD} (MIN) and t_{RCD} (MIN)

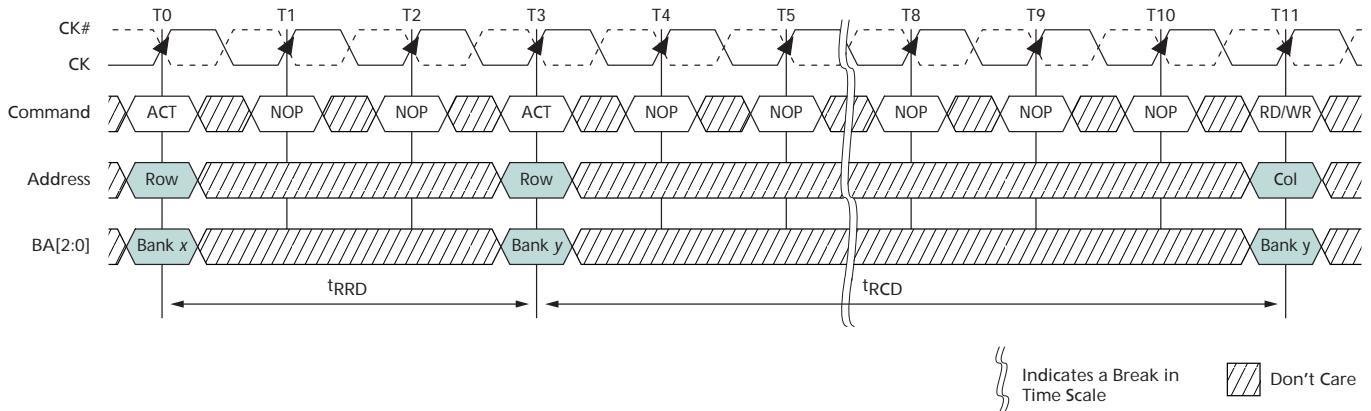
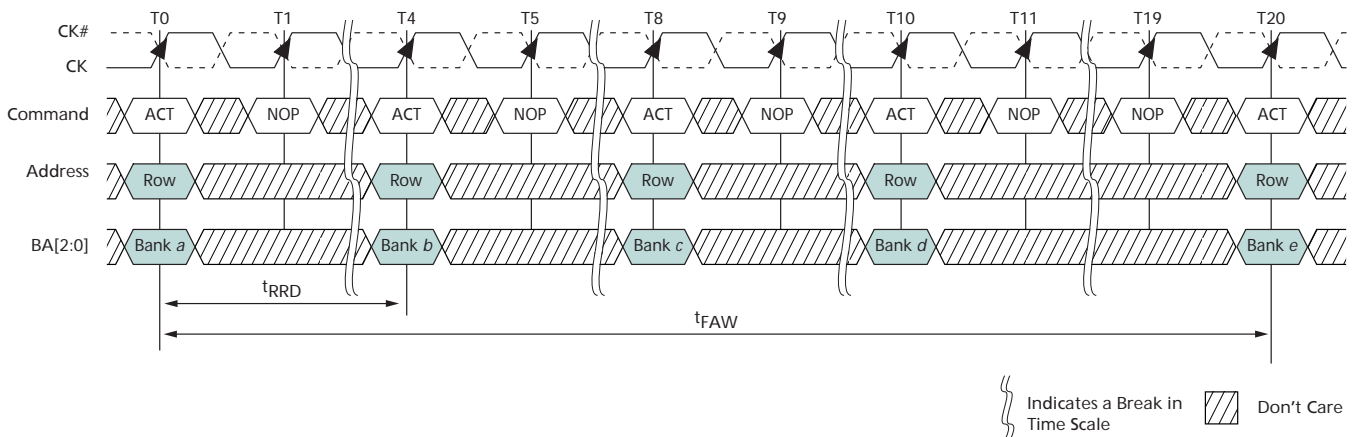


Figure 65: Example: t_{FAW}

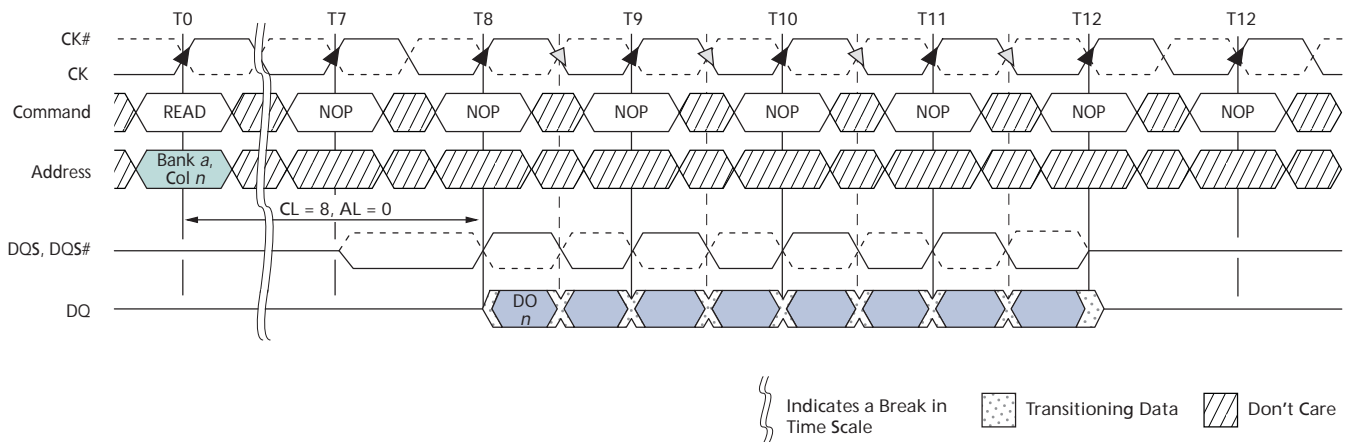


READ

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of POSTED CAS ADDITIVE latency (AL) and CAS latency (CL) ($RL = AL + CL$). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#). Figure 66 shows an example of RL based on a CL setting of 8 and an AL setting of 0.

Figure 66: READ Latency



- Notes:
1. DO n = data-out from column n .
 2. Subsequent elements of data-out appear in the programmed order following DO n .

DQS, DQS# is driven by the DRAM along with the output data. The initial low state on DQS and HIGH state on DQS# is known as the READ preamble (tRPRE). The low state on DQS and the HIGH state on DQS#, coincident with the last data-out element, is known as the READ postamble (tRPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of tDQSQ (valid data-out skew), tQH (data-out window hold), and the valid data window are depicted in Figure 77 on page 139. A detailed explanation of tDQSCK (DQS transition skew to CK) is also depicted in Figure 77 on page 139.

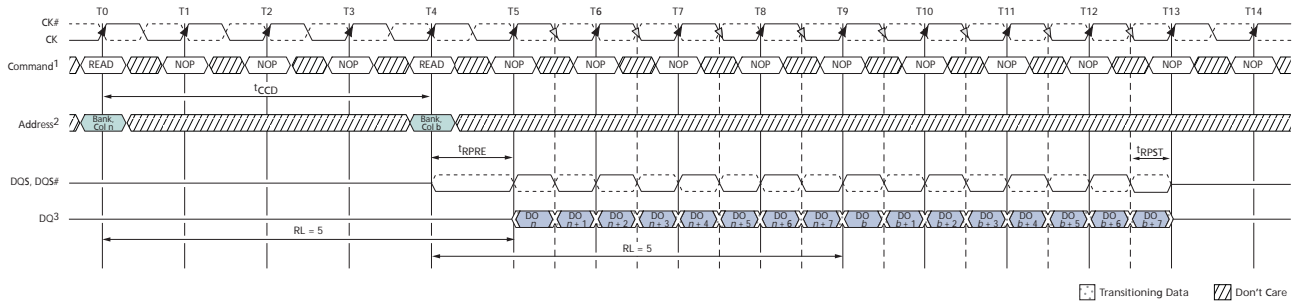
Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued tCCD cycles after the first READ command. This is shown for BL8 in Figure 67 on page 133. If BC4 is enabled, tCCD must still be met which will cause a gap in the data output, as shown in Figure 68 on page 133. Nonconsecutive read data is reflected in Figure 69 on page 134. DDR3 SDRAM do not allow interrupting or truncating any READ burst.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst for BL8 is shown in Figure 70 on page 134 (BC4 is shown in Figure 71 on page 135). To ensure the read data is completed before the write data is on the bus, the minimum READ-to-WRITE timing is $RL + {}^tCCD - WL + 2{}^tCK$.

A READ burst may be followed by a PRECHARGE command to the same bank provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called tRTP (READ-to-PRECHARGE). tRTP starts AL cycles later than the READ command. Examples for BL8 are shown in Figure 72 on page 135 and BC4 in Figure 73 on page 136. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

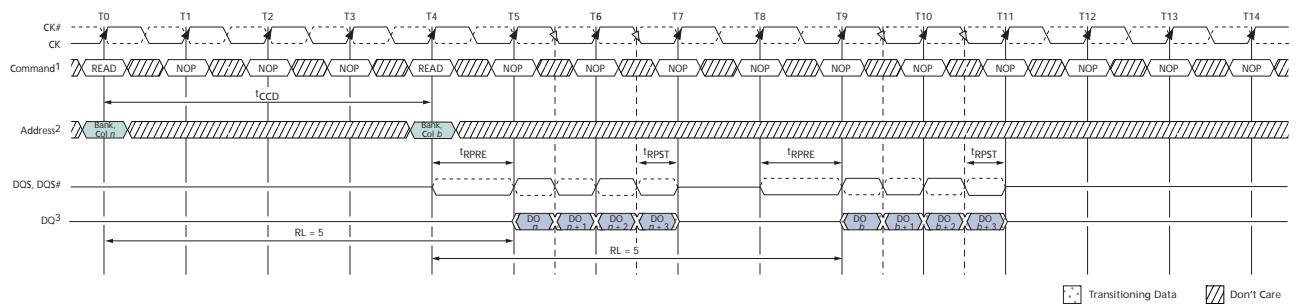
If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DRAM starts an auto precharge operation on the rising edge which is AL + tRTP cycles after the READ command. DRAM support a tRAS lockout feature (see Figure 75 on page 136). If tRAS (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until tRAS (MIN) is satisfied. If tRTP (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until tRTP (MIN) is satisfied. In case the internal precharge is pushed out by tRTP , tRP starts at the point at which the internal precharge happens (not at the next rising clock edge after this event). The time from READ with auto precharge to the next ACTIVATE command to the same bank is $AL + ({}^tRTP + {}^tRP)^*$, where "*" means rounded up to the next integer. In any event, internal precharge does not start earlier than four clocks after the last 8n-bit prefetch.

Figure 67: Consecutive READ Bursts (BL8)



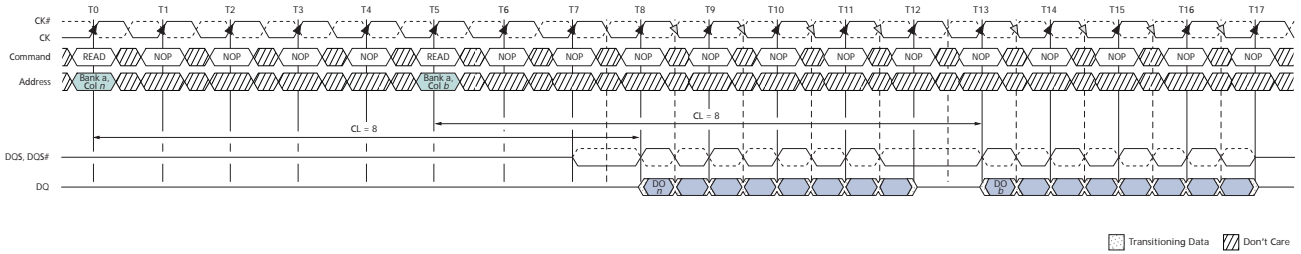
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BL8 setting is activated by either $MR0[1:0] = 00$ or $MR0[1:0] = 01$ and $A12 = 1$ during READ command at T0 and T4.
 3. DO_n (or b) = data-out from column n (or column b).
 4. BL8, $RL = 5$ ($CL = 5$, $AL = 0$).

Figure 68: Consecutive READ Bursts (BC4)



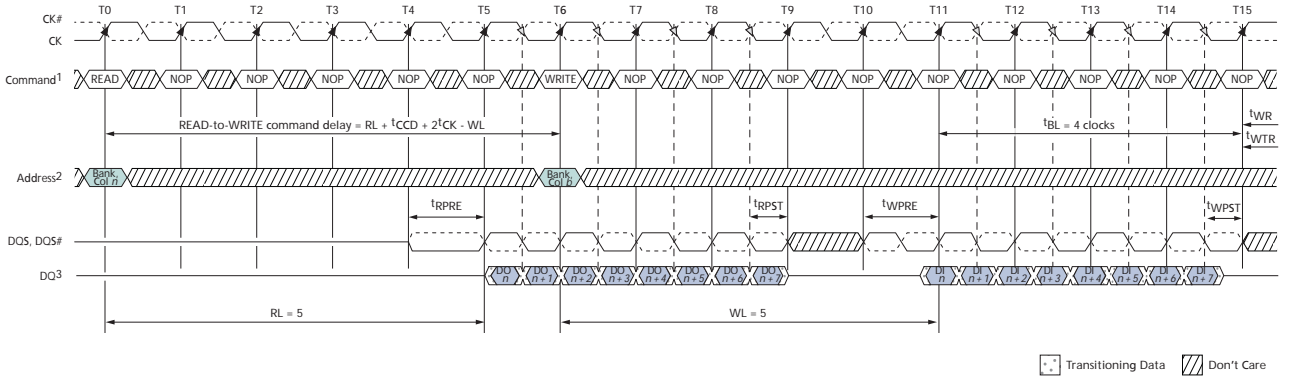
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BC4 setting is activated by either $MR0[1:0] = 10$ or $MR0[1:0] = 01$ and $A12 = 0$ during READ command at T0 and T4.
 3. DO_n (or b) = data-out from column n (or column b).
 4. BC4, $RL = 5$ ($CL = 5$, $AL = 0$).

Figure 69: Nonconsecutive READ Bursts



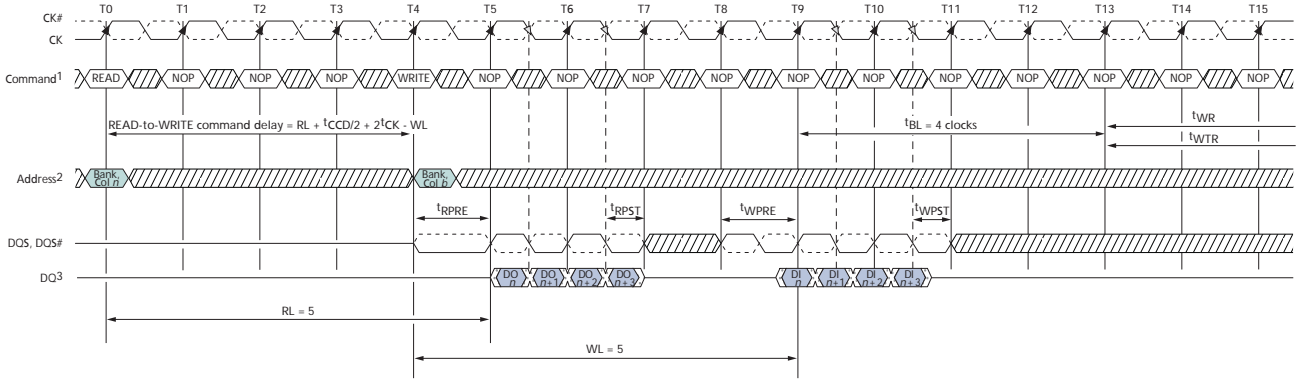
- Notes:
1. AL = 0, RL = 8.
 2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
 3. Seven subsequent elements of data-out appear in the programmed order following DO *n*.
 4. Seven subsequent elements of data-out appear in the programmed order following DO *b*.

Figure 70: READ (BL8) to WRITE (BL8)



- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BL8 setting is activated by either MRO[1:0] = 00 or MRO[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.
 3. DO *n* = data-out from column, DI *b* = data-in for column *b*.
 4. BL8, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

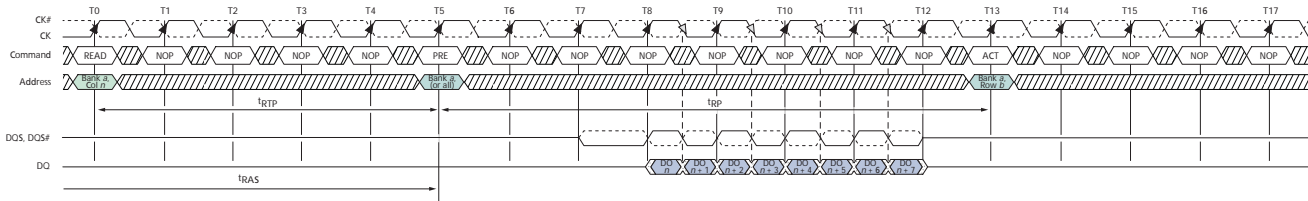
Figure 71: READ (BC4) to WRITE (BC4) OTF



□ Transitional Data ▨ Don't Care

- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.
 3. DO n = data-out from column n ; DI n = data-in from column b .
 4. BC4, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 72: READ to PRECHARGE (BL8)



□ Transitional Data ▨ Don't Care

Figure 73: READ to PRECHARGE (BC4)

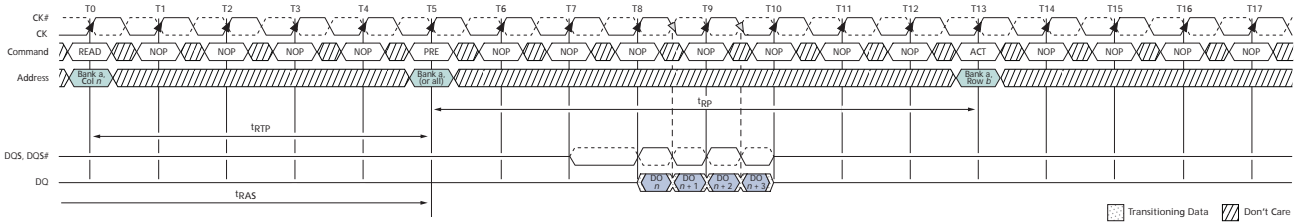


Figure 74: READ to PRECHARGE (AL = 5, CL = 6)

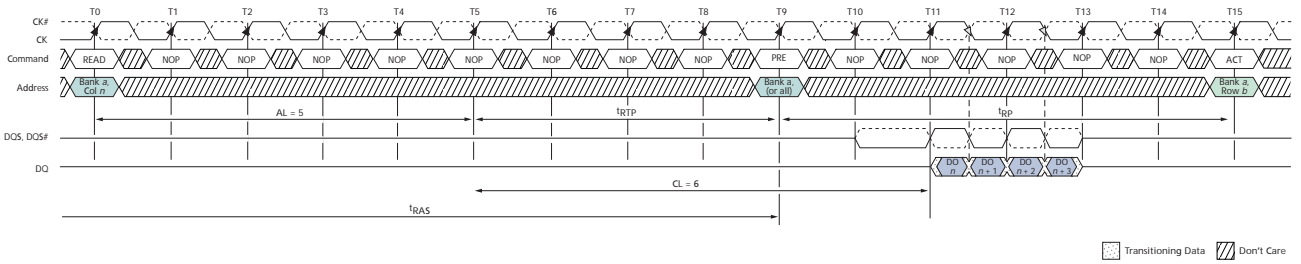
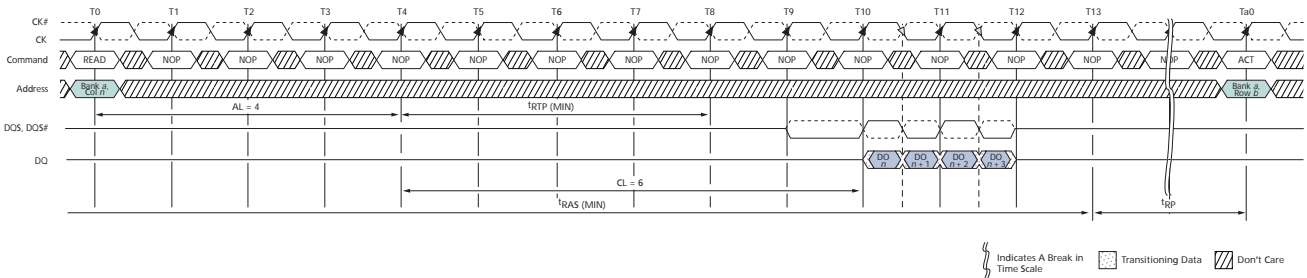


Figure 75: READ with Auto Precharge (AL = 4, CL = 6)



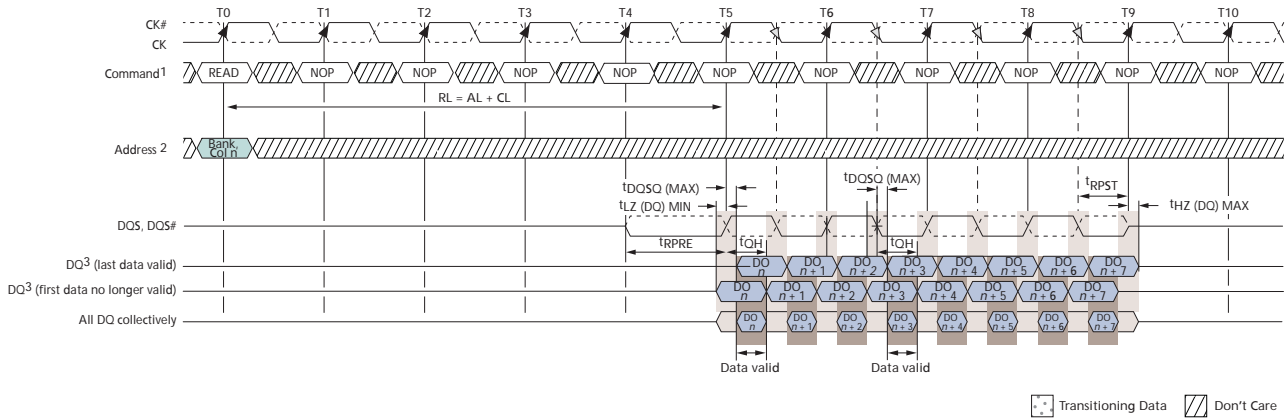
A DQS to DQ output timing is shown in Figure 76 on page 138. The DQ transitions between valid data outputs must be within t_{DQSQ} of the crossing point of DQS, DQS#. DQS must also maintain a minimum HIGH and LOW time of t_{QSH} and t_{QSL} . Prior to the READ preamble, the DQ balls will either be floating or terminated depending on the status of the ODT signal.

Figure 77 on page 139 shows the strobe-to-clock timing during a READ. The crossing point DQS, DQS# must transition within $\pm t_{DQSCK}$ of the clock crossing point. The data out has no timing relationship to clock, only to DQS, as shown in Figure 77 on page 139.

Figure 77 on page 139 also shows the READ preamble and postamble. Normally, both DQS and DQS# are High-Z to save power (VDDQ). Prior to data output from the DRAM, DQS is driven LOW and DQS# is HIGH for t_{RPRE} . This is known as the READ preamble.

The READ postamble, t_{RPST} , is one half clock from the last DQS, DQS# transition. During the READ postamble, DQS is driven LOW and DQS# is HIGH. When complete, the DQ will either be disabled or will continue terminating depending on the state of the ODT signal. Figure 82 on page 142 demonstrates how to measure t_{RPST} .

Figure 76: Data Output Timing - t^1DQSQ and Data Valid Window



- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BL8 setting is activated by either MR0[1, 0] = 0, 0 or MR0[0, 1] = 0, 1 and A12 = 1 during READ command at T0.
 3. DO n = data-out from column n .
 4. BL8, RL = 5 (AL = 0, CL = 5).
 5. Output timings are referenced to V_{DDQ}/2 and DLL on and locked.
 6. t^1DQSQ defines the skew between DQS, DQS# to data and does not define DQS, DQS# to clock.
 7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving t_{HZ} (DQS) and t_{HZ} (DQ) or begins driving t_{LZ} (DQS), t_{LZ} (DQ). Figure 78 shows a method to calculate the point when the device is no longer driving t_{HZ} (DQS) and t_{HZ} (DQ) or begins driving t_{LZ} (DQS), t_{LZ} (DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters t_{LZ} (DQS), t_{LZ} (DQ), t_{HZ} (DQS), and t_{HZ} (DQ) are defined as single-ended.

Figure 77: Data Strobe Timing - READS

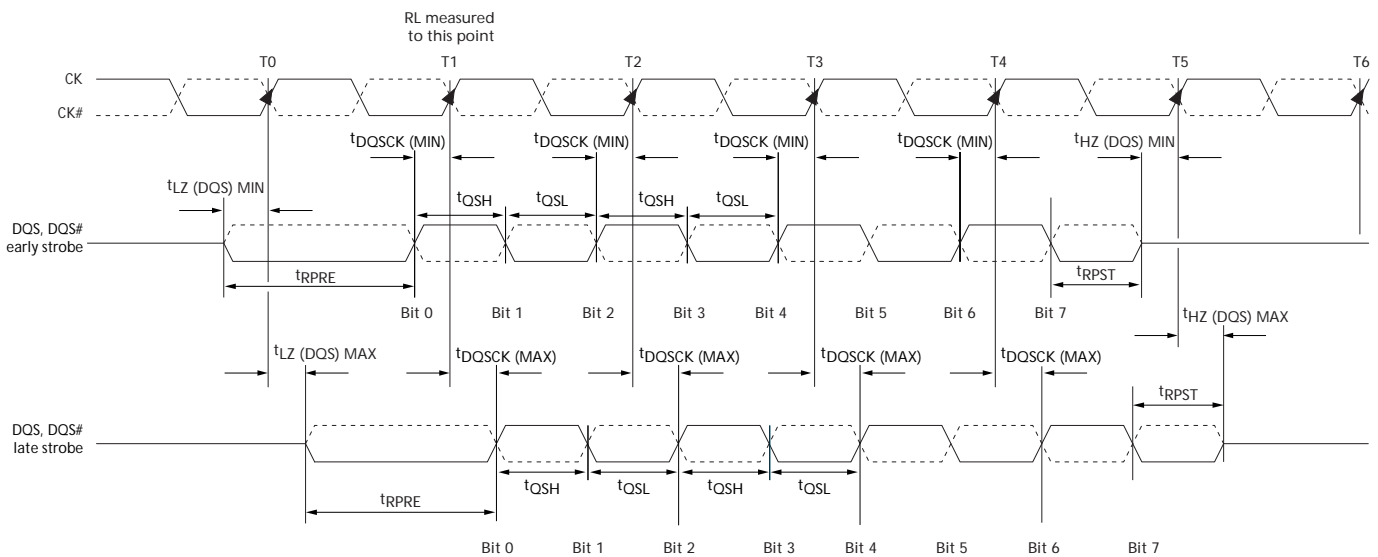
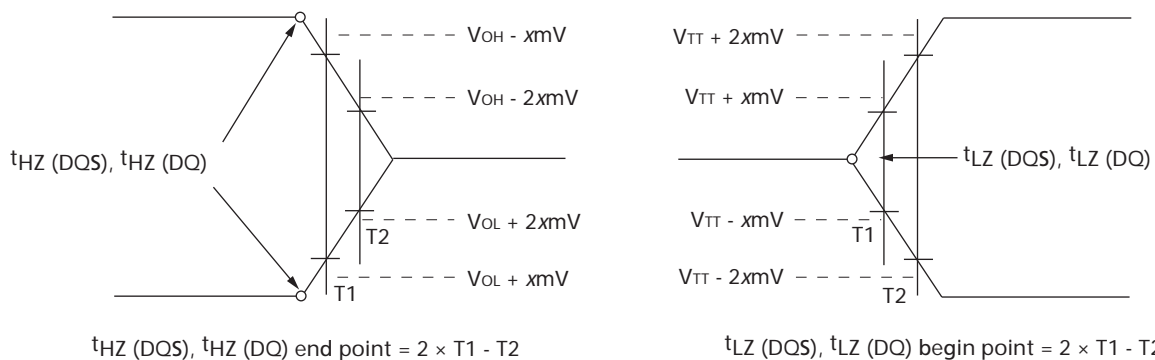


Figure 78: Method for Calculating t_{LZ} and t_{HZ}



$$t_{HZ} (DQS), t_{HZ} (DQ) \text{ end point} = 2 \times T1 - T2$$

$$t_{LZ} (DQS), t_{LZ} (DQ) \text{ begin point} = 2 \times T1 - T2$$

- Notes:
1. Within a burst, the rising strobe edge is not necessarily fixed at $t_{DQSK} (MIN)$ or $t_{DQSK} (MAX)$. Instead, the rising strobe edge can vary between $t_{DQSK} (MIN)$ and $t_{DQSK} (MAX)$.
 2. The DQS high pulse width is defined by t_{QSH} , and the DQS low pulse width is defined by t_{QSL} . Likewise, $t_{LZ} (DQS) MIN$ and $t_{HZ} (DQS) MIN$ are not tied to $t_{DQSK} (MIN)$ (early strobe case) and $t_{LZ} (DQS) MAX$ and $t_{HZ} (DQS) MAX$ are not tied to $t_{DQSK} (MAX)$ (late strobe case); however, they tend to track one another.
 3. The minimum pulse width of the READ preamble is defined by $t_{RPRE} (MIN)$. The minimum pulse width of the READ postamble is defined by $t_{RPST} (MIN)$.

Figure 79: t_{RPRE} Timing

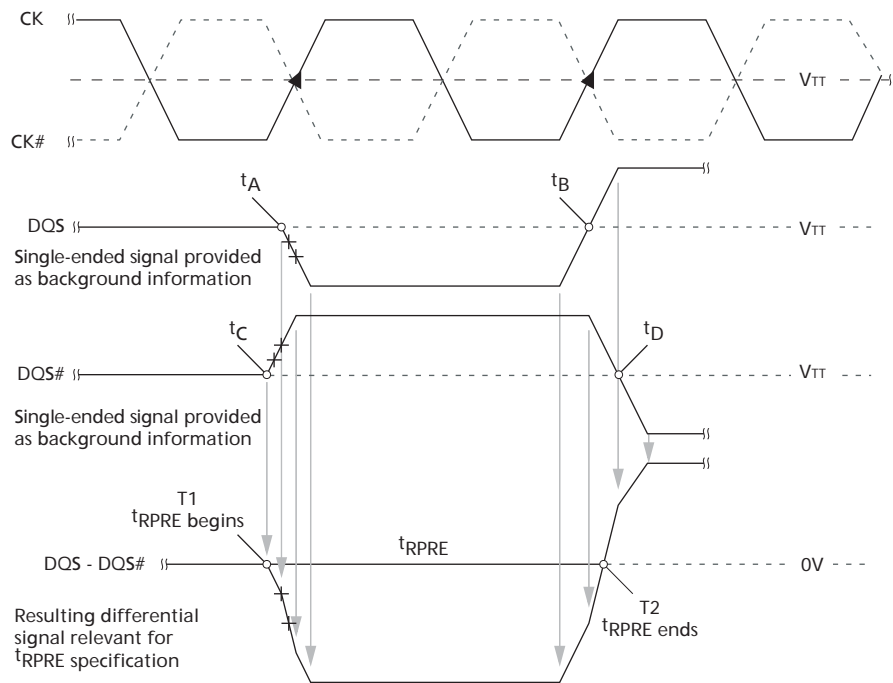
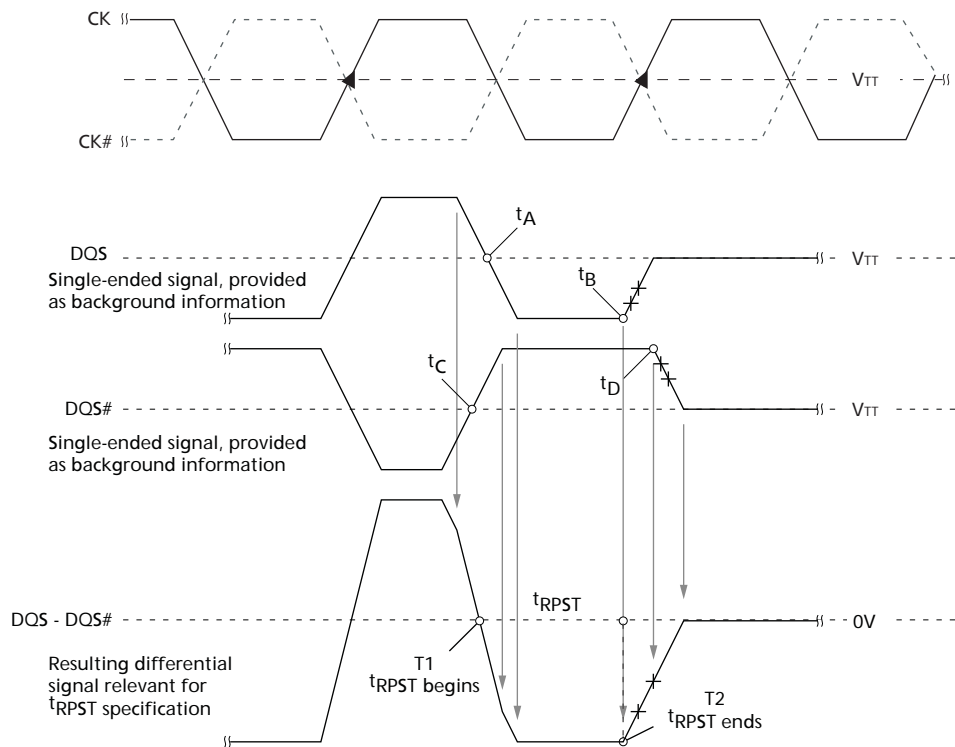


Figure 80: t_{RPST} Timing



WRITE

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted. For the generic WRITE commands used in Figure 83 on page 143 through Figure 91 on page 148, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered on a rising edge of DQS following the WRITE latency (WL) clocks later and subsequent data elements will be registered on successive edges of DQS. WRITE latency (WL) is defined as the sum of POSTED CAS ADDITIVE latency (AL) and CAS WRITE latency (CWL): $WL = AL + CWL$. The values of AL and CWL are programmed in the MR0 and MR2 registers, respectively. Prior to the first valid DQS edge, a full cycle is needed (including a dummy crossover of DQS, DQS#) and specified as the WRITE preamble shown in Figure 83 on page 143. The half cycle on DQS following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQS is WL clocks $\pm t_{DQSS}$. Figure 84 on page 144 through Figure 91 on page 148 show the nominal case where $t_{DQSS} = 0ns$; however, Figure 83 on page 143 includes $t_{DQSS} (MIN)$ and $t_{DQSS} (MAX)$ cases.

Data may be masked from completing a WRITE using data mask. The mask occurs on the DM ball aligned to the write data. If DM is LOW, the write completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z, and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be t_{CCD} clocks following the previous WRITE command. The first data element from the new burst is applied after the last element of a completed burst. Figures 84 and 85 on page 144 show concatenated bursts. An example of nonconsecutive WRITES is shown in Figure 86 on page 145.

Data for any WRITE burst may be followed by a subsequent READ command after t_{WTR} has been met (see Figures 87 and 88 on page 146 and Figure 89 on page 147).

Data for any WRITE burst may be followed by a subsequent PRECHARGE command providing t_{WR} has been met, as shown in Figure 90 on page 148 and Figure 91 on page 148.

Both t_{WTR} and t_{WR} starting time may vary depending on the mode register settings (fixed BC4, BL8 vs. OTF).

Figure 81: t_{WPRE} Timing

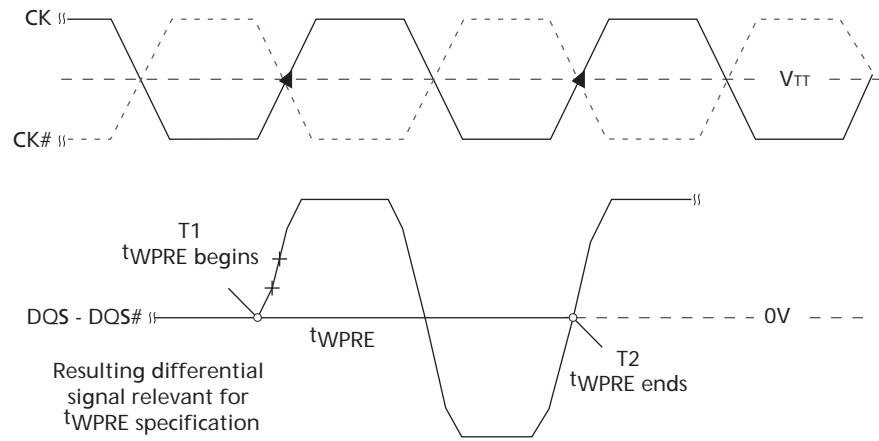


Figure 82: t_{WPST} Timing

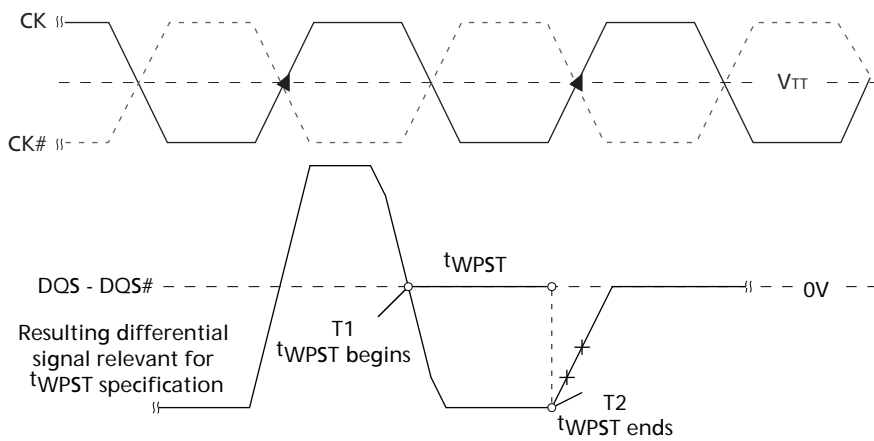
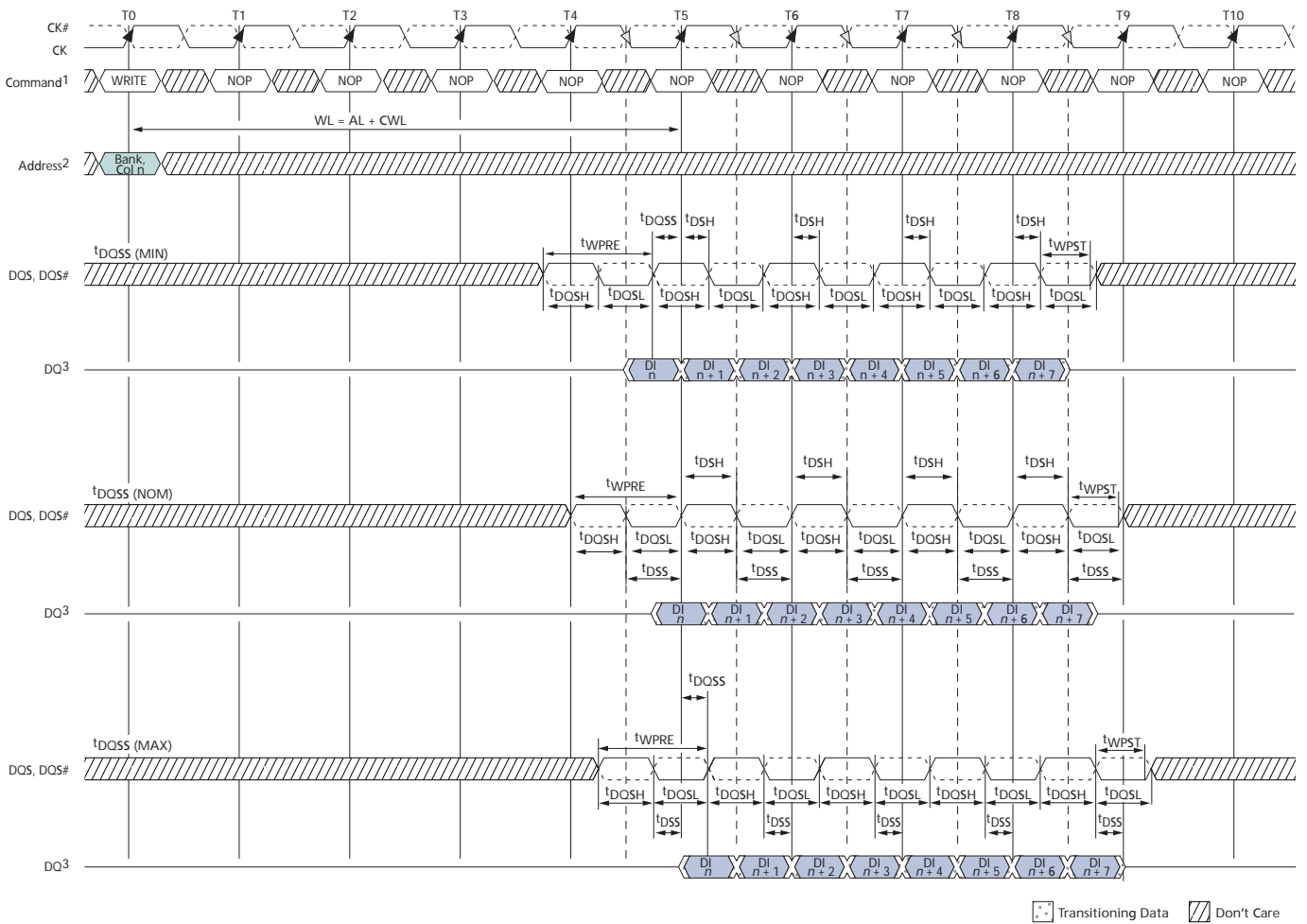
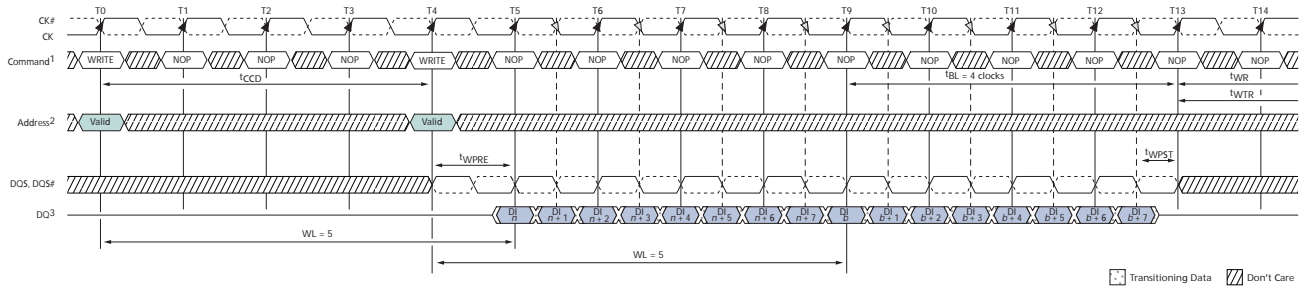


Figure 83: Write Burst



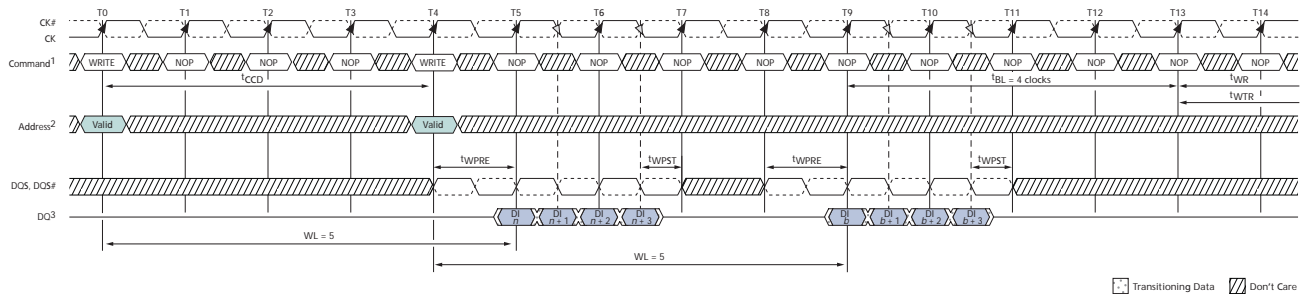
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE command at T0.
 3. DI n = data-in for column n .
 4. BL8, WL = 5 (AL = 0, CWL = 5).
 5. t_{DQSS} must be met at each rising clock edge.
 6. t_{WPST} is usually depicted as ending at the crossing of DQS, DQS#; however, t_{WPST} actually ends when DQS no longer drives LOW and DQS# no longer drives HIGH.

Figure 84: Consecutive WRITE (BL8) to WRITE (BL8)



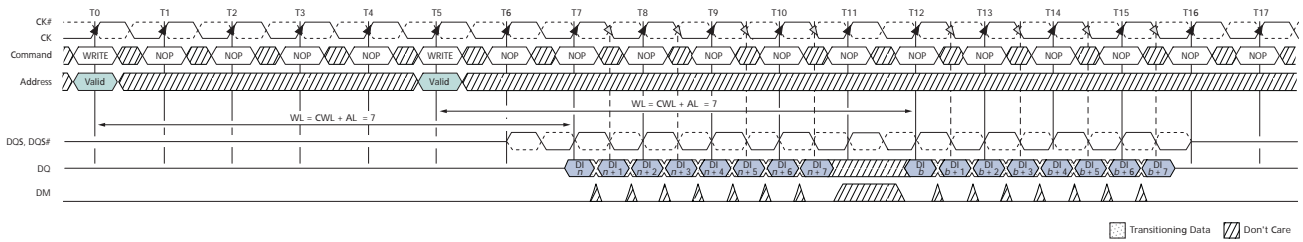
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE commands at T0 and T4.
 3. DI n (or b) = data-in for column n (or column b).
 4. BL8, WL = 5 (AL = 0, CWL = 5).

Figure 85: Consecutive WRITE (BC4) to WRITE (BC4) via MRS or OTF



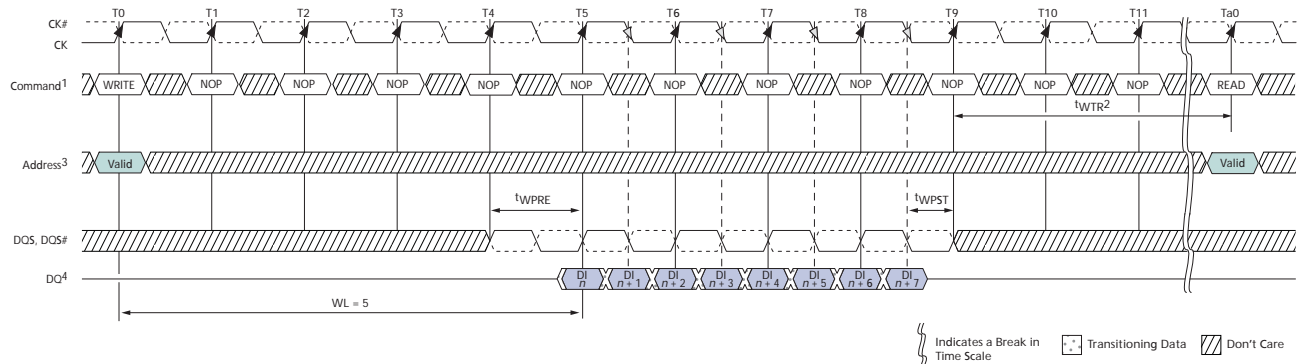
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. BC4, WL = 5 (AL = 0, CWL = 5).
 3. DI n (or b) = data-in for column n (or column b).
 4. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and T4.

Figure 86: Nonconsecutive WRITE to WRITE



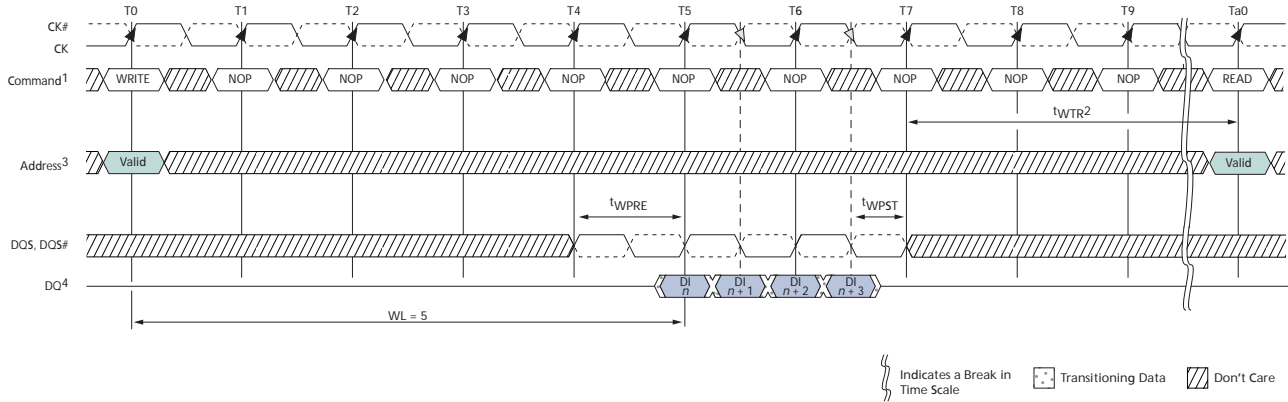
- Notes:
1. DI n (or b) = data-in for column n (or column b).
 2. Seven subsequent elements of data-in are applied in the programmed order following DO n .
 3. Each WRITE command may be to any bank.
 4. Shown for WL = 7 (CWL = 7, AL = 0).

Figure 87: WRITE (BL8) to READ (BL8)



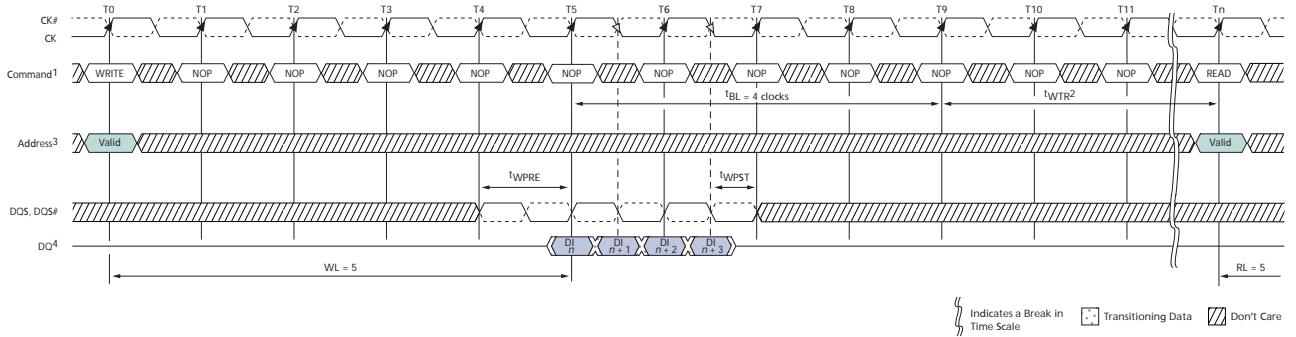
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. t_{WTR}^2 controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T9.
 3. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and MR0[12] = 1 during the WRITE command at T0. The READ command at Ta0 can be either BC4 or BL8, depending on MR0[1:0] and the A12 status at Ta0.
 4. DI n = data-in for column n .
 5. RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 88: WRITE to READ (BC4 Mode Register Setting)



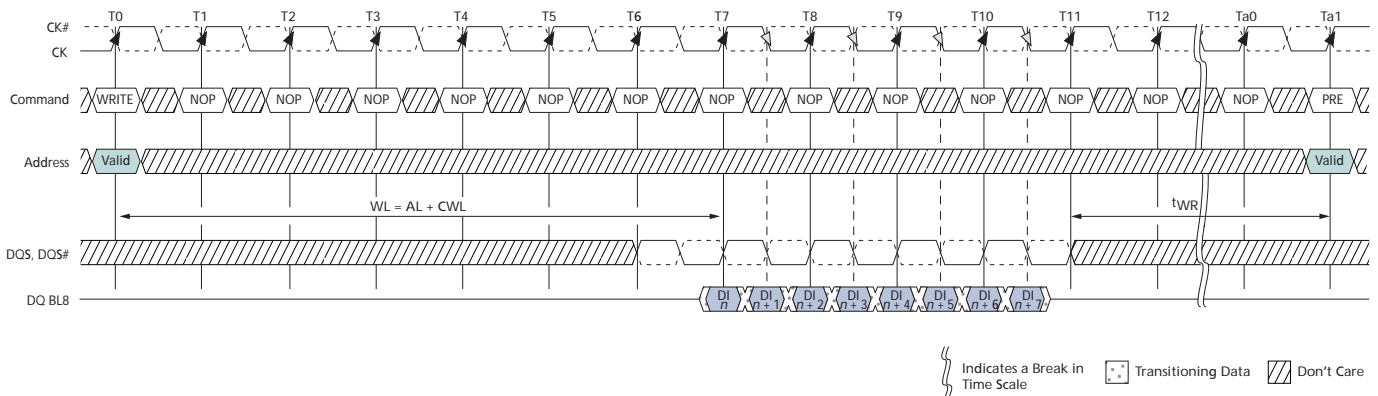
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. t_{WTR2} controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T7.
 3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0 and the READ command at Ta0.
 4. DI n = data-in for column n .
 5. BC4 (fixed), WL = 5 (AL = 0, CWL = 5), RL = 5 (AL = 0, CL = 5).

Figure 89: WRITE (BC4 OTF) to READ (BC4 OTF)



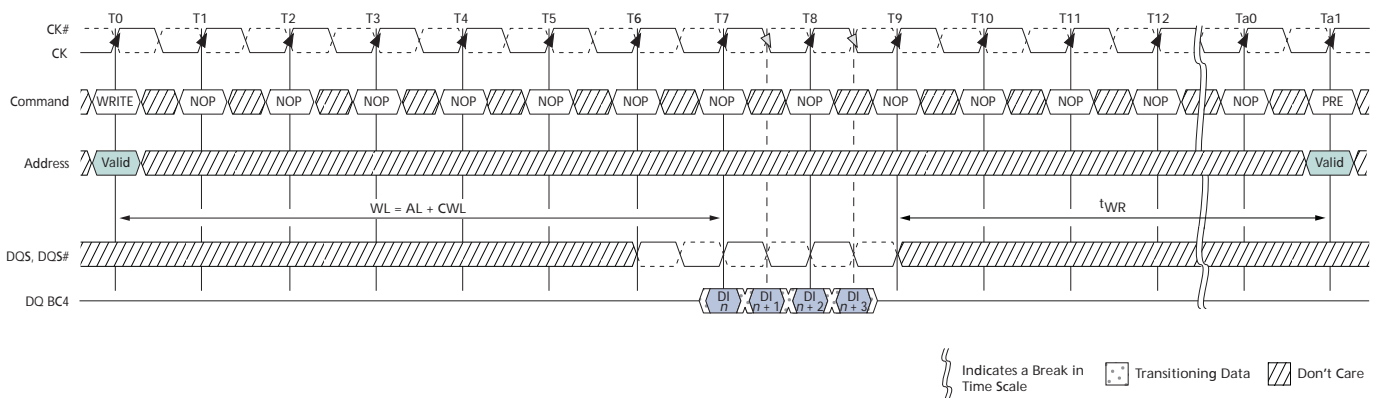
- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. t_{WTR} controls the WRITE-to-READ delay to the same device and starts after t_{BL} .
 3. The BC4 OTF setting is activated by $MR0[1:0] = 01$ and $A12 = 0$ during the WRITE command at T_0 and the READ command at T_n .
 4. DI_n = data-in for column n .
 5. BC4, $RL = 5$ ($AL = 0$, $CL = 5$), $WL = 5$ ($AL = 0$, $CWL = 5$).

Figure 90: WRITE (BL8) to PRECHARGE



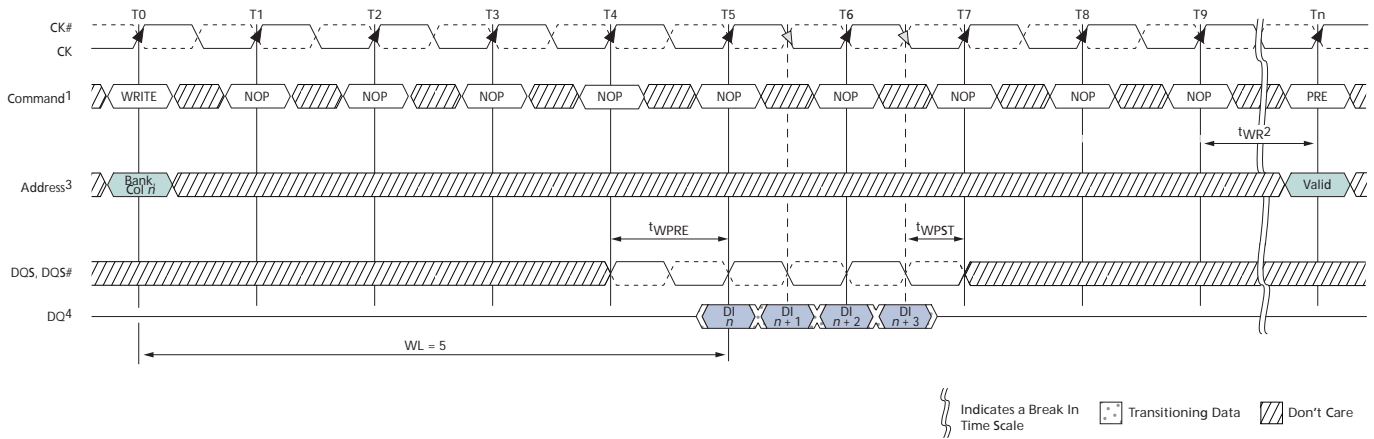
- Notes:
1. DI n = data-in from column n .
 2. Seven subsequent elements of data-in are applied in the programmed order following DO n .
 3. Shown for WL = 7 (AL = 0, CWL = 7).

Figure 91: WRITE (BC4 Mode Register Setting) to PRECHARGE



- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The write recovery time (t_{WR}) is referenced from the first rising clock edge after the last write data is shown at T7. t_{WR} specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
 3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0.
 4. DI n = data-in for column n .
 5. BC4 (fixed), WL = 5, RL = 5.

Figure 92: WRITE (BC4 OTF) to PRECHARGE



- Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 2. The write recovery time (t_{WR}) is referenced from the rising clock edge at T_9 . t_{WR} specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
 3. The BC4 setting is activated by $MRO[1:0] = 01$ and $A12 = 0$ during the WRITE command at T_0 .
 4. DI_n = data-in for column n .
 5. BC4 (OTF), $WL = 5$, $RL = 5$.

DQ Input Timing

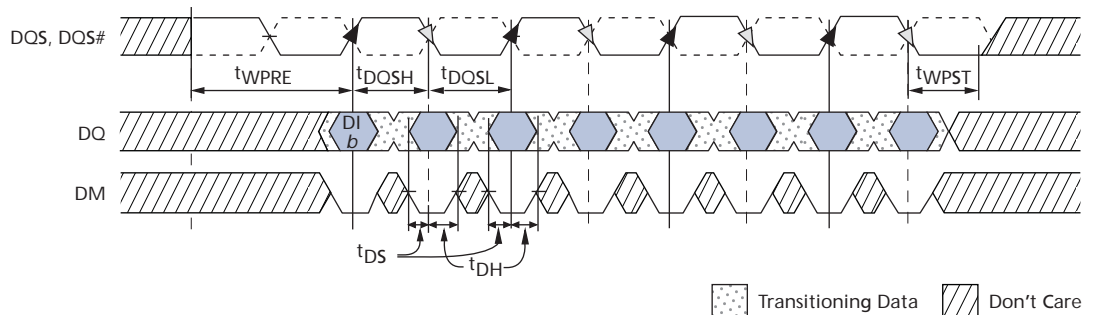
Figure 83 on page 143 shows the strobe to clock timing during a WRITE. DQS, DQS# must transition within $0.25t_{CK}$ of the clock transitions as limited by t_{DQSS} . All data and data mask setup and hold timings are measured relative to the DQS, DQS# crossing, not the clock crossing.

The WRITE preamble and postamble are also shown. One clock prior to data input to the DRAM, DQS must be HIGH and DQS# must be LOW. Then for a half clock, DQS is driven LOW (DQS# is driven HIGH) during the WRITE preamble, t_{WPST} . Likewise, DQS must be kept LOW by the controller after the last data is written to the DRAM during the WRITE postamble, t_{WPST} .

Data setup and hold times are shown in Figure 93 on page 149. All setup and hold times are measured from the crossing points of DQS and DQS#. These setup and hold values pertain to data input and data mask input.

Additionally, the half period of the data input strobe is specified by t_{DQSH} and t_{DQSL} .

Figure 93: Data Input Timing



PRECHARGE

Input A10 determines whether one bank or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA[2:0] select the bank.

When all banks are to be precharged, inputs BA[2:0] are treated as “Don’t Care.” After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued.

SELF REFRESH

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled and reset upon exiting self refresh. All power supply inputs (including VREFCA and VREFDQ) must be maintained at valid levels upon entry/exit and during self refresh mode operation. VREFDQ may float or not drive VDDQ/2 while in the self refresh mode under certain conditions:

- $VSS < V_{refDQ} < VDD$ is maintained
- VREFDQ is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after VREFDQ is valid
- All other self refresh mode exit timing requirements are met

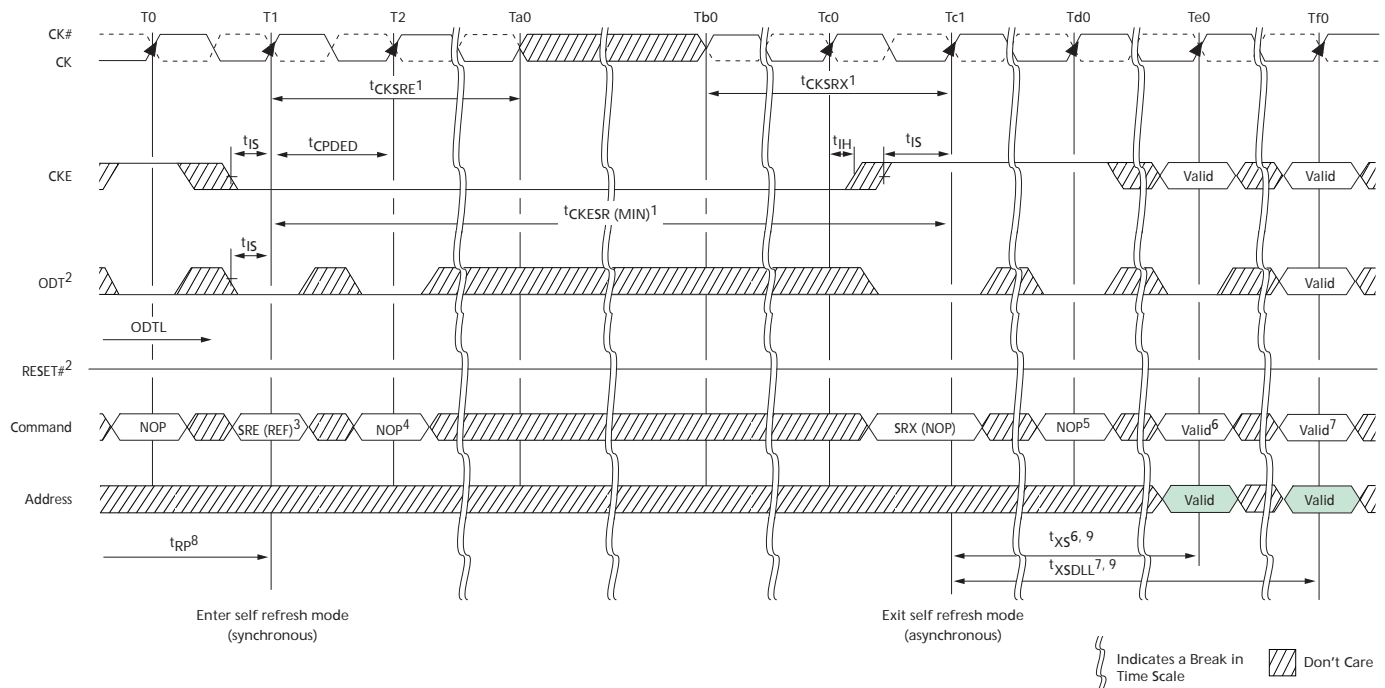
The DRAM must be idle with all banks in the precharge state (t_{RP} is satisfied and no bursts are in progress) before a self refresh entry command can be issued. ODT must also be turned off before self refresh entry by registering the ODT ball LOW prior to the self refresh entry command (see “On-Die Termination (ODT)” on page 161 for timing requirements). If RTT_NOM and RTT_WR are disabled in the mode registers, ODT can be a “Don’t Care.” After the self refresh entry command is registered, CKE must be held LOW to keep the DRAM in self refresh mode.

After the DRAM has entered self refresh mode, all external control signals, except CKE and RESET#, become “Don’t Care.” The DRAM initiates a minimum of one REFRESH command internally within the t_{CKE} period when it enters self refresh mode.

The requirements for entering and exiting self refresh mode depend on the state of the clock during self refresh mode. First and foremost, the clock must be stable (meeting t_{CK} specifications) when self refresh mode is entered. If the clock remains stable and the frequency is not altered while in self refresh mode, then the DRAM is allowed to exit self refresh mode after t_{CKESR} is satisfied (CKE is allowed to transition HIGH t_{CKESR} later than when CKE was registered LOW). Since the clock remains stable in self refresh mode (no frequency change), t_{CKSRE} and t_{CKSRX} are not required. However, if the clock is altered during self refresh mode (turned-off or frequency change), then t_{CKSRE} and t_{CKSRX} must be satisfied. When entering self refresh mode, t_{CKSRE} must be satisfied prior to altering the clock's frequency. Prior to exiting self refresh mode, t_{CKSRX} must be satisfied prior to registering CKE HIGH.

When CKE is HIGH during self refresh exit, NOP or DES must be issued for t_{XS} time. t_{XS} is required for the completion of any internal refresh that is already in progress and must be satisfied before a valid command not requiring a locked DLL can be issued to the device. t_{XS} is also the earliest time self refresh reentry may occur (see Figure 94 on page 151). Before a command requiring a locked DLL can be applied, a ZQCL command must be issued, t_{ZQOPER} timing must be met, and t_{XSDLL} must be satisfied. ODT must be off during t_{XSDLL} .

Figure 94: Self Refresh Entry/Exit Timing



- Notes:
1. The clock must be valid and stable meeting t_{CK} specifications at least t_{CKSRE} after entering self refresh mode, and at least t_{CKSRX} prior to exiting self refresh mode, if the clock is stopped or altered between states Ta0 and Tb0. If the clock remains valid and unchanged from entry and during self refresh mode, then t_{CKSRE} and t_{CKSRX} do not apply; however, t_{CKESR} must be satisfied prior to exiting at SRX.
 2. ODT must be disabled and RTT off prior to entering self refresh at state T1. If both RTT_NOM and RTT_WR are disabled in the mode registers, ODT can be a "Don't Care."
 3. Self refresh entry (SRE) is synchronous via a REFRESH command with CKE LOW.
 4. A NOP or DES command is required at T2 after the SRE command is issued prior to the inputs becoming "Don't Care."
 5. NOP or DES commands are required prior to exiting self refresh mode until state Te0.
 6. t_{XS} is required before any commands not requiring a locked DLL.
 7. t_{XSDLL} is required before any commands requiring a locked DLL.
 8. The device must be in the all banks idle state prior to entering self refresh mode. For example, all banks must be precharged, t_{RP} must be met, and no data bursts can be in progress.
 9. Self refresh exit is asynchronous; however, t_{XS} and t_{XSDLL} timings start at the first rising clock edge where CKE HIGH satisfies t_{ISXR} at Tc1. t_{CKSRX} timing is also measured so that t_{ISXR} is satisfied at Tc1.

Extended Temperature Usage

Micron's DDR3 SDRAM support the optional extended temperature range of 0°C to 95°C, T_C . Thus, the SRT and ASR options must be used at a minimum.

The extended temperature range DRAM must be refreshed externally at 2X (double refresh) anytime the case temperature is above 85°C (and does not exceed 95°C). The external refreshing requirement is accomplished by reducing the refresh period from 64ms to 32ms. However, self refresh mode requires either ASR or SRT to support the extended temperature. Thus either ASR or SRT must be enabled when T_C is above 85°C or self refresh cannot be used until the case temperature is at or below 85°C. Table 74 summarizes the two extended temperature options and Table 75 summarizes how the two extended temperature options relate to one another.

Table 74: Self Refresh Temperature and Auto Self Refresh Description

Field	MR2 Bits	Description
Self Refresh Temperature (SRT)		
SRT	7	If ASR is disabled (MR2[6] = 0), SRT must be programmed to indicate T_{OPER} during self refresh: *MR2[7] = 0: Normal operating temperature range (0°C to 85°C) *MR2[7] = 1: Extended operating temperature range (0°C to 95°C) If ASR is enabled (MR2[7] = 1), SRT must be set to 0, even if the extended temperature range is supported *MR2[7] = 0: SRT is disabled
Auto Self Refresh (ASR)		
ASR	6	When ASR is enabled, the DRAM automatically provides SELF REFRESH power management functions, (refresh rate for all supported operating temperature values) * MR2[6] = 1: ASR is enabled (M7 must = 0) When ASR is not enabled, the SRT bit must be programmed to indicate T_{OPER} during SELF REFRESH operation * MR2[6] = 0: ASR is disabled, must use manual self refresh temperature (SRT)

Table 75: Self Refresh Mode Summary

MR2[6] (ASR)	MR2[7] (SRT)	SELF REFRESH Operation	Permitted Operating Temperature Range for Self Refresh Mode
0	0	Self refresh mode is supported in the normal temperature range	Normal (0°C to 85°C)
0	1	Self refresh mode is supported in normal and extended temperature ranges; When SRT is enabled, it increases self refresh power consumption	Normal and extended (0°C to 95°C)
1	0	Self refresh mode is supported in normal and extended temperature ranges; Self refresh power consumption may be temperature-dependent	Normal and extended (0°C to 95°C)
1	1	Illegal	

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while either an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down IDD specifications are not applicable until such operations have been completed. Depending on the previous DRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied (as noted in Table 76). Timing diagrams detailing the different power-down mode entry and exits are shown in Figure 95 on page 154 through Figure 104 on page 159.

Table 76: Command to Power-Down Entry Parameters

DRAM Status	Last Command Prior to CKE LOW ¹	Parameter (Min)	Parameter Value	Figure
Idle or active	ACTIVATE	^t ACTPDEN	1 ^t CK	Figure 102 on page 158
Idle or active	PRECHARGE	^t PRPDEN	1 ^t CK	Figure 103 on page 158
Active	READ or READAP	^t RDPDEN	RL + 4 ^t CK + 1 ^t CK	Figure 98 on page 156
Active	WRITE: BL8OTF, BL8MRS, BC4OTF	^t WRPDEN	WL + 4 ^t CK + ^t WR/ ^t CK	Figure 99 on page 156
Active	WRITE: BC4MRS	^t WRAPDEN	WL + 2 ^t CK + ^t WR/ ^t CK	Figure 99 on page 156
Active	WRITEAP: BL8OTF, BL8MRS, BC4OTF		WL + 4 ^t CK + WR + 1 ^t CK	Figure 100 on page 157
Active	WRITEAP: BC4MRS		WL + 2 ^t CK + WR + 1 ^t CK	Figure 100 on page 157
Idle	REFRESH	^t REFPDEN	1 ^t CK	Figure 101 on page 157
Power-down	REFRESH	^t XPDLL	Greater of 10 ^t CK or 24ns	Figure 105 on page 159
Idle	MODE REGISTER SET	^t MRS PDEN	^t MOD	Figure 104 on page 159

Notes: 1. If slow-exit mode precharge power-down is enabled and entered, ODT becomes asynchronous ^tANPD prior to CKE going LOW and remains asynchronous until ^tANPD + ^tXPDLL after CKE goes HIGH.

Entering power-down disables the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. NOP or DES commands are required until ^tCPDED has been satisfied, at which time all specified input/output buffers will be disabled. The DLL should be in a locked state when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after all in-progress commands are complete, the DRAM will be in active power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-down mode must be programmed to exit with either a slow exit mode or a fast exit mode. When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL remains on when entering active power-down as well. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered. Refer to "Asynchronous ODT Mode" on page 173 for detailed ODT usage requirements in slow exit mode precharge power-down. A summary of the two power-down modes is listed in Table 77 on page 154.

While in either power-down state, CKE is held LOW, RESET# is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are a “Don’t Care.” If RESET# goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until t_{PD} (MIN) has been satisfied. The maximum time allowed for power-down duration is t_{PD} (MAX) ($9 \times t_{REFI}$).

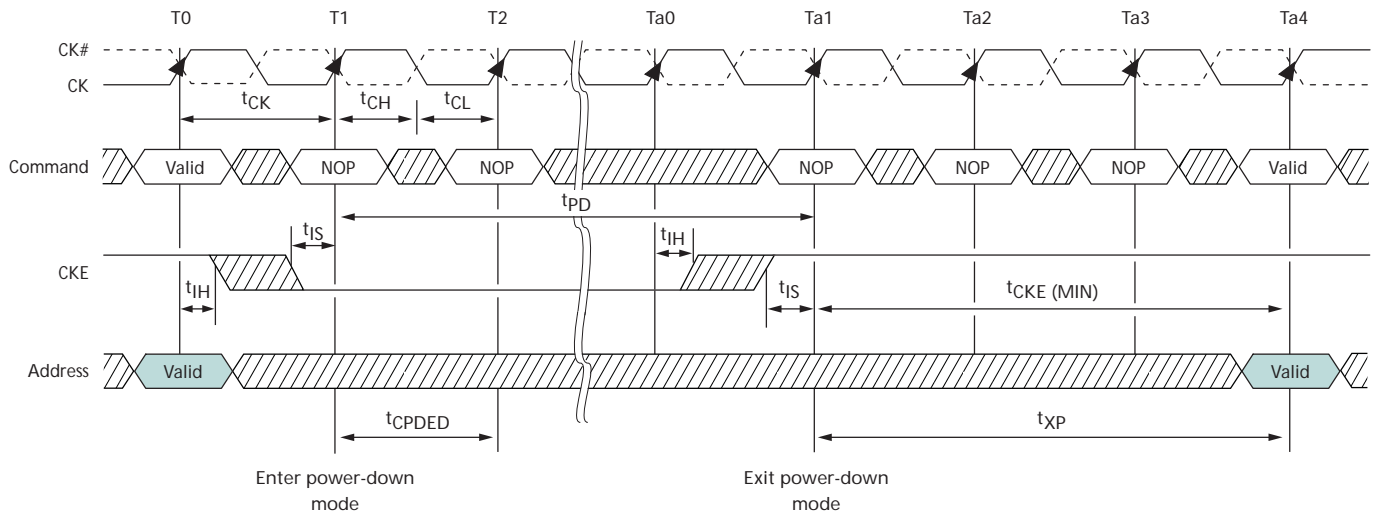
The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until t_{CKE} has been satisfied. A valid, executable command may be applied after power-down exit latency, t_{XP} t_{XPDLL} have been satisfied. A summary of the power-down modes is listed in Table 77.

For certain CKE-intensive operations, for example, repeating a power-down exit to refresh to power-down entry sequence, the number of clock cycles between power-down exit and power-down entry may not be sufficient enough to keep the DLL properly updated. In addition to meeting t_{PD} when the REFRESH command is used in between power-down exit and power-down entry, two other conditions must be met. First, t_{XP} must be satisfied before issuing the REFRESH command. Second, t_{XPDLL} must be satisfied before the next power-down may be entered. An example is shown in Figure 105 on page 159.

Table 77: Power-Down Modes

DRAM State	MR1[12]	DLL State	Power-Down Exit	Relevant Parameters
Active (any bank open)	“Don’t Care”	On	Fast	t_{XP} to any other valid command
Precharged (all banks precharged)	1	On	Fast	t_{XP} to any other valid command
	0	Off	Slow	t_{XPDLL} to commands that require the DLL to be locked (READ, RDAP, or ODT on) t_{XP} to any other valid command

Figure 95: Active Power-Down Entry and Exit



⎵ Indicates a Break in Time Scale
 Don't Care

Figure 96: Precharge Power-Down (Fast-Exit Mode) Entry and Exit

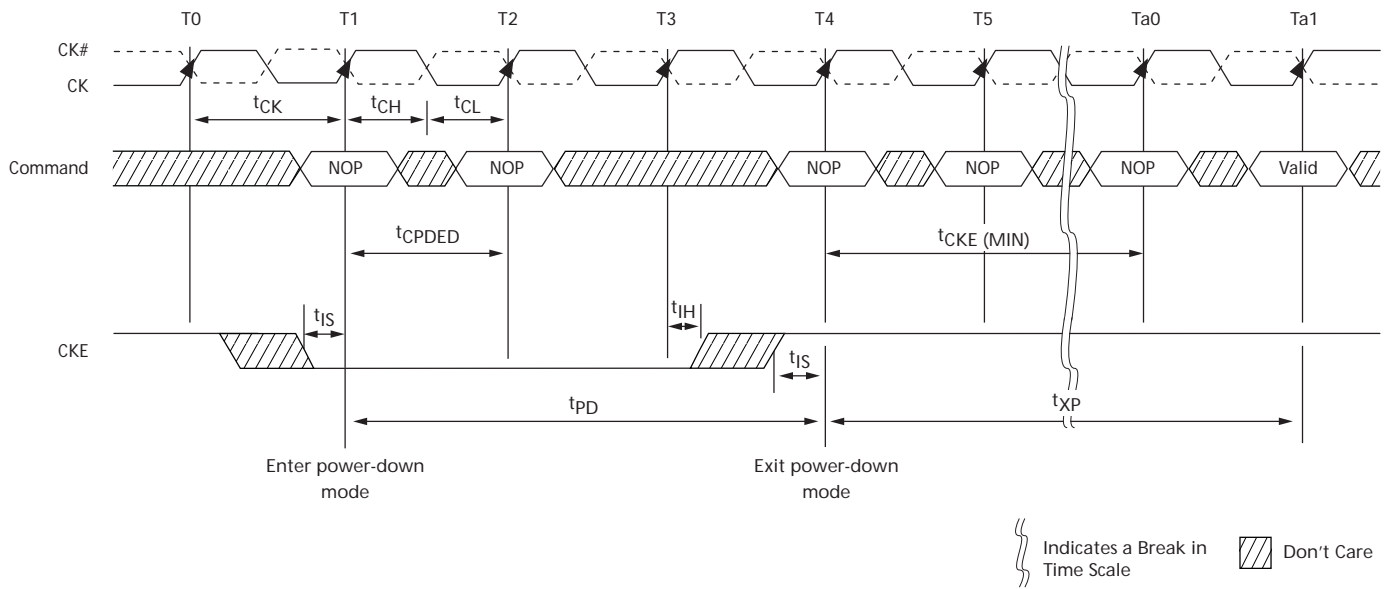
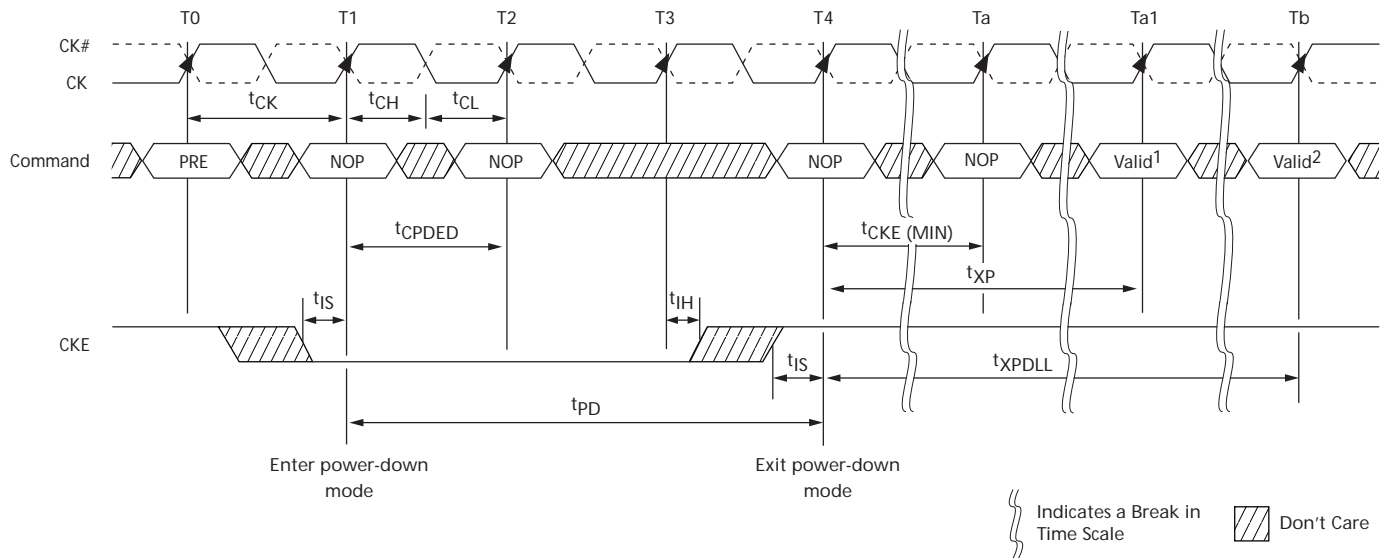


Figure 97: Precharge Power-Down (Slow-Exit Mode) Entry and Exit



- Notes:
1. Any valid command not requiring a locked DLL.
 2. Any valid command requiring a locked DLL.

Figure 98: Power-Down Entry After READ or READ with Auto Precharge (RDAP)

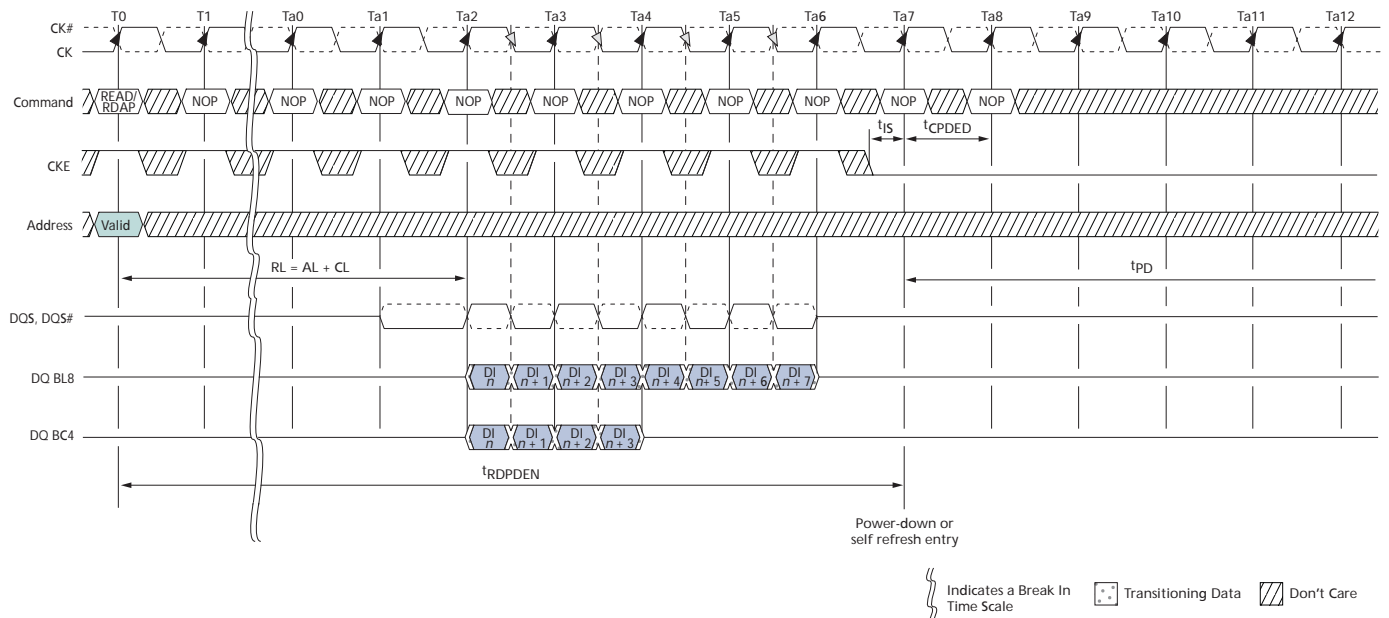
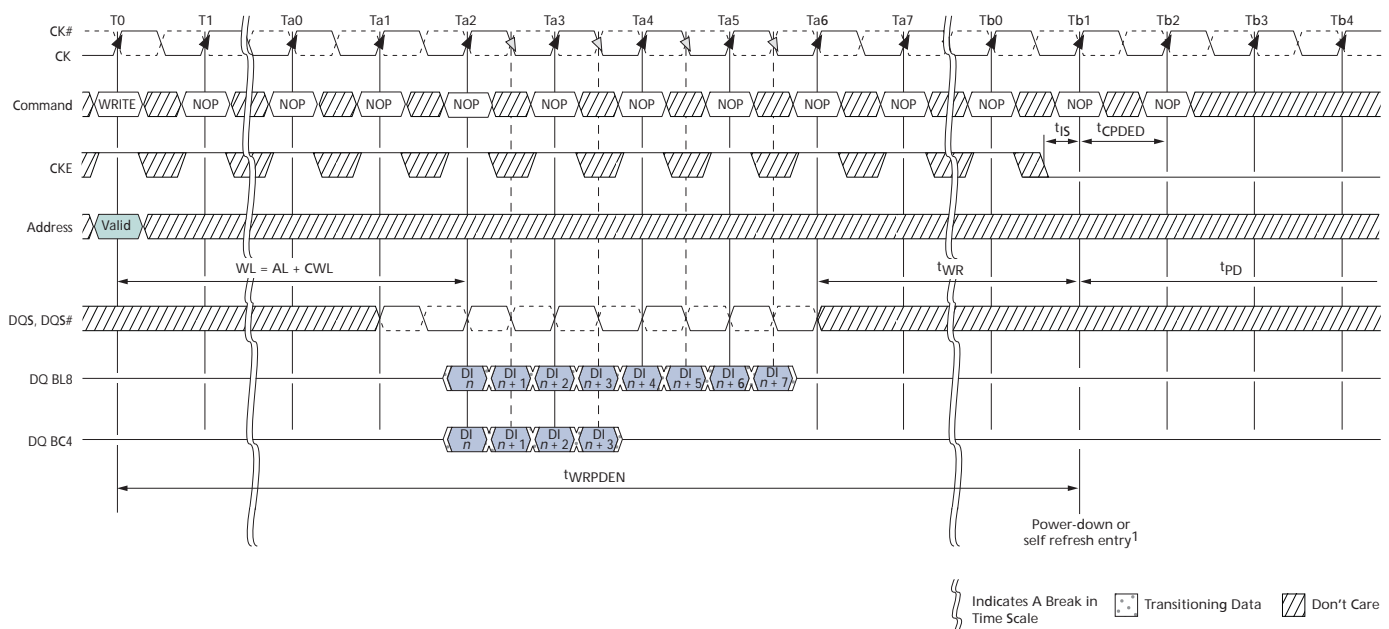
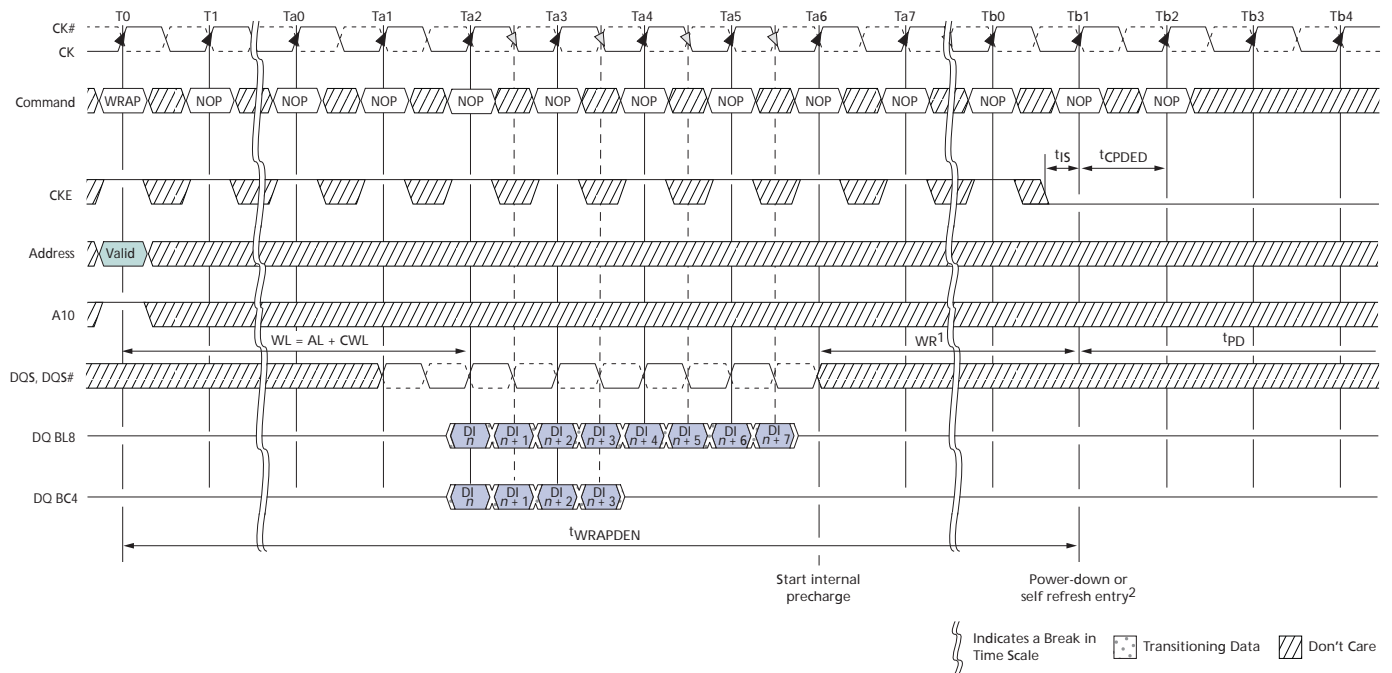


Figure 99: Power-Down Entry After WRITE



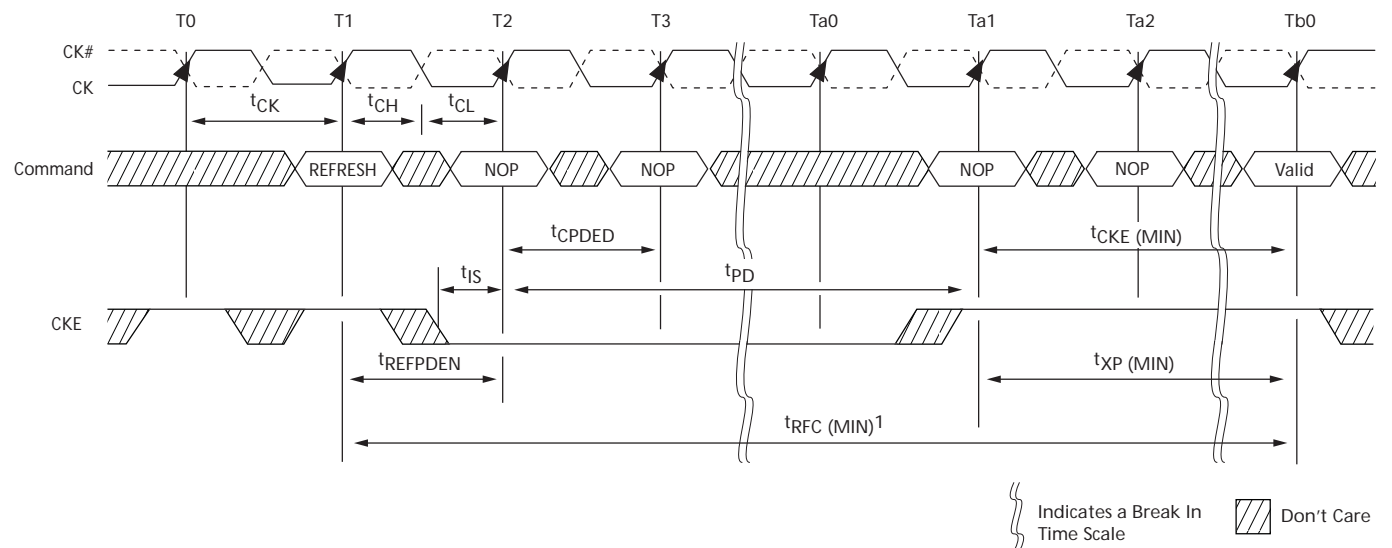
Notes: 1. CKE can go LOW 2^tCK earlier if BC4MRS.

Figure 100: Power-Down Entry After WRITE with Auto Precharge (WRAP)



- Notes: 1. t_{WR} is programmed through MR0[11:9] and represents $t_{WR}(\text{MIN})n_s/t_{CK}$ rounded up to the next integer t_{CK} .
 2. CKE can go LOW 2^t_{CK} earlier if BC4MRS.

Figure 101: REFRESH to Power-Down Entry



- Notes: 1. After CKE goes HIGH during t_{RFC} , CKE must remain HIGH until t_{RFC} is satisfied.

Figure 102: ACTIVATE to Power-Down Entry

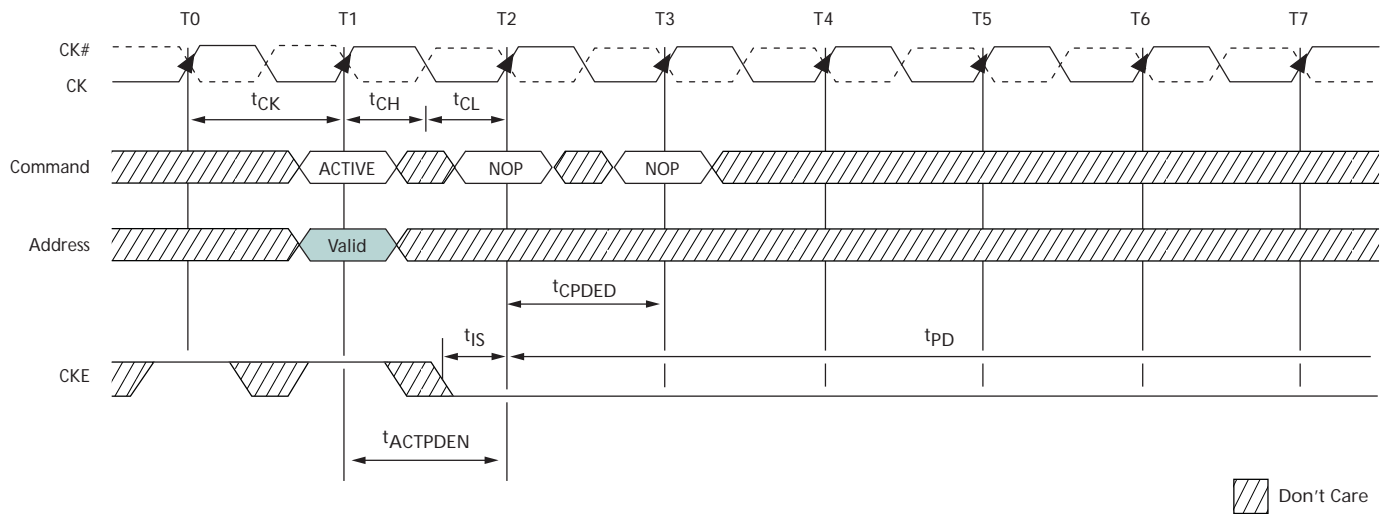


Figure 103: PRECHARGE to Power-Down Entry

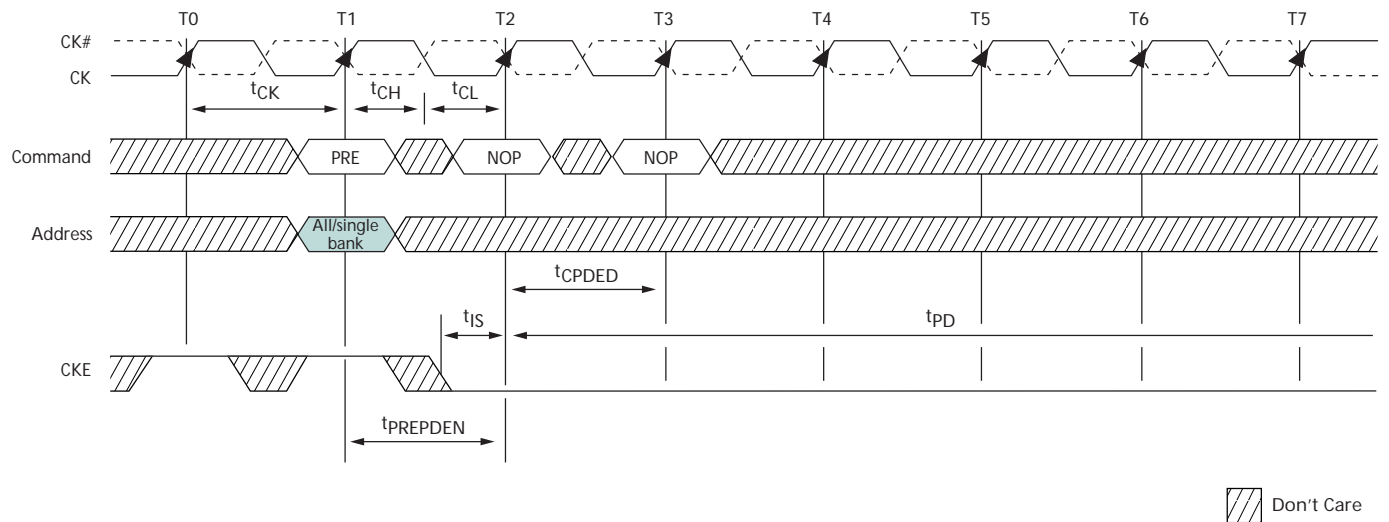


Figure 104: MRS Command to Power-Down Entry

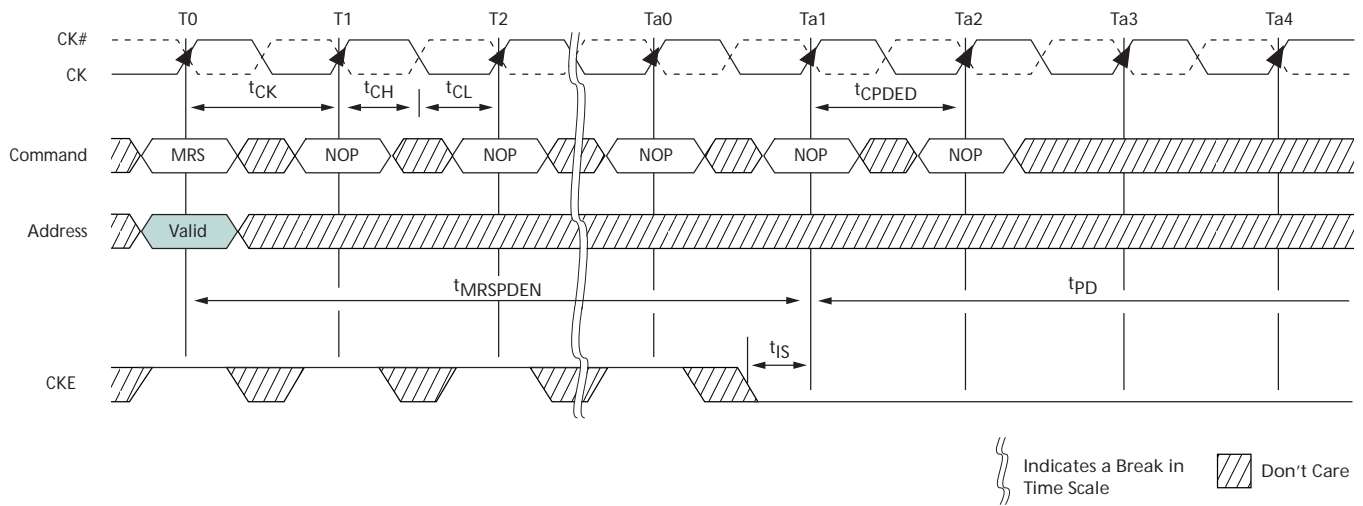
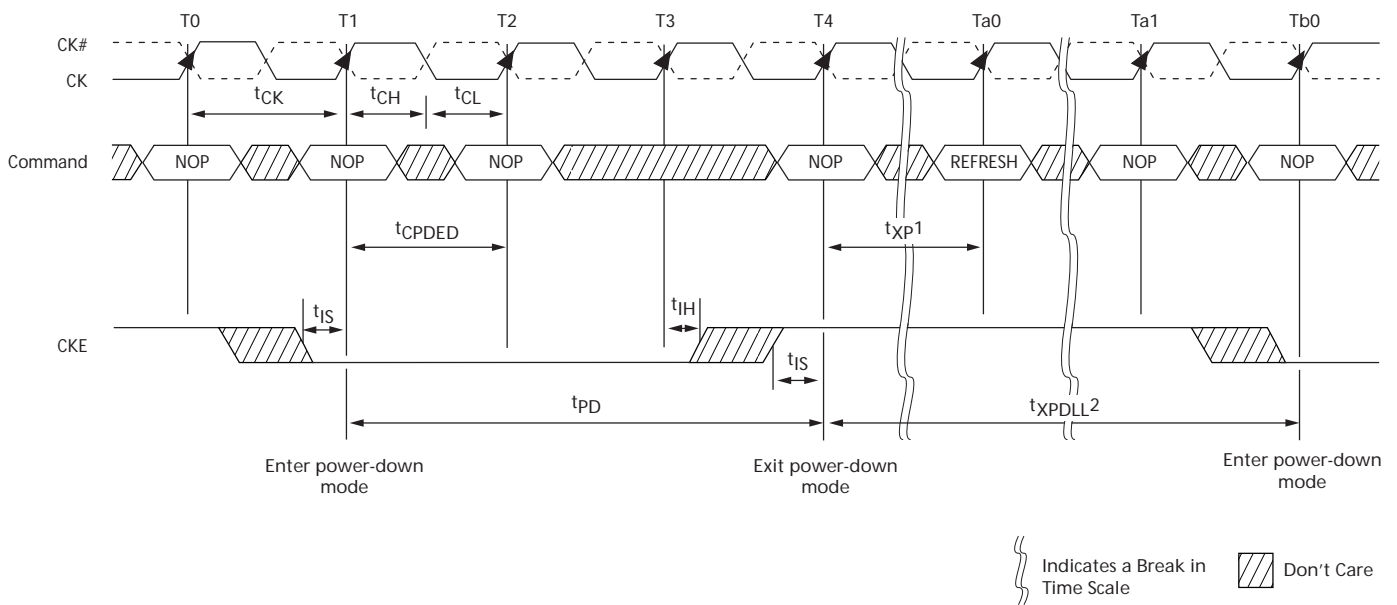


Figure 105: Power-Down Exit to Refresh to Power-Down Entry

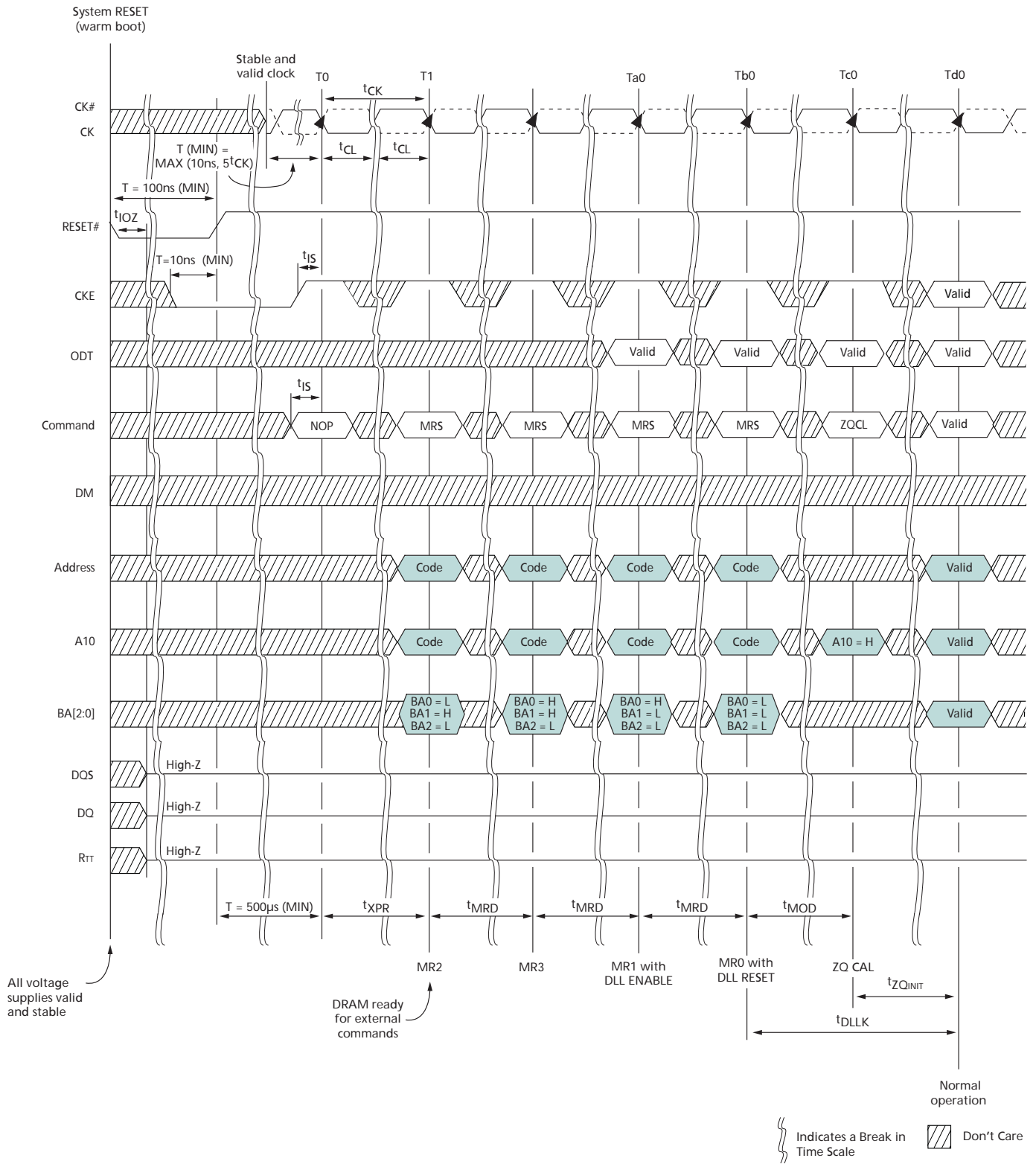


- Notes:
1. t_{XP} must be satisfied before issuing the command.
 2. t_{XPDLL} must be satisfied (referenced to the registration of power-down exit) before the next power-down can be entered.

RESET

The RESET signal (RESET#) is an asynchronous signal that triggers any time it drops LOW, and there are no restrictions about when it can go LOW. After RESET# goes LOW, it must remain LOW for 100ns. During this time, the outputs are disabled, ODT (RTT) turns off (High-Z), and the DRAM resets itself. CKE should be brought LOW prior to RESET# being driven HIGH. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power up were executed (see Figure 106 on page 160). All refresh counters on the DRAM are reset, and data stored in the DRAM is assumed unknown after RESET# has gone LOW.

Figure 106: RESET Sequence

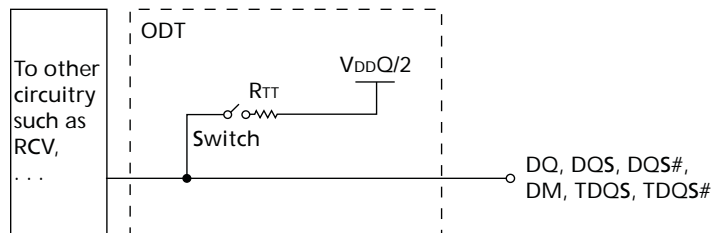


On-Die Termination (ODT)

ODT is a feature that enables the DRAM to enable/disable and turn on/off termination resistance for each DQ, DQS, DQS#, and DM for the x4 and x8 configurations (and TDQS, TDQS# for the x8 configuration, when enabled). ODT is applied to each DQ, UDQS, UDQS#, LDQS, LDQS#, UDM, and LDM signal for the x16 configuration.

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DRAM controller to independently turn on/off the DRAM's internal termination resistance for any grouping of DRAM devices. The ODT feature is not supported during DLL disable mode. A simple functional representation of the DRAM ODT feature is shown in Figure 107. The switch is enabled by the internal ODT control logic, which uses the external ODT ball and other control information.

Figure 107: On-Die Termination



Functional Representation of ODT

The value of R_{TT} (ODT termination value) is determined by the settings of several mode register bits (see Table 81 on page 164). The ODT ball is ignored while in self refresh mode (must be turned off prior to self refresh entry) or if mode registers MR1 and MR2 are programmed to disable ODT. ODT is comprised of nominal ODT and dynamic ODT modes and either of these can function in synchronous or asynchronous mode (when the DLL is off during precharge power-down or when the DLL is synchronizing). Nominal ODT is the base termination and is used in any allowable ODT state. Dynamic ODT is applied only during writes and provides OTF switching from no R_{TT} or R_{TT_NOM} to R_{TT_WR} .

The actual effective termination, R_{TT_EFF} , may be different from the R_{TT} targeted due to nonlinearity of the termination. For R_{TT_EFF} values and calculations, see “ODT Characteristics” on page 52.

Nominal ODT

ODT (NOM) is the base termination resistance for each applicable ball, it is enabled or disabled via MR1[9, 6, 2] (see Figure 53 on page 115), and it is turned on or off via the ODT ball (see Table 78 on page 162).

Table 78: Truth Table – ODT (Nominal)

Note 1 applies to the entire table

MR1[9, 6, 2]	ODT Pin	DRAM Termination State	DRAM State	Notes
000	0	RTT_NOM disabled, ODT off	Any valid	2
000	1	RTT_NOM disabled, ODT on	Any valid except self refresh, read	3
000–101	0	RTT_NOM enabled, ODT off	Any valid	2
000–101	1	RTT_NOM enabled, ODT on	Any valid except self refresh, read	3
110 and 111	X	RTT_NOM reserved, ODT on or off	Illegal	

- Notes:
1. Assumes dynamic ODT is disabled (see “Dynamic ODT” on page 163 when enabled).
 2. ODT is enabled and active during most writes for proper termination, but it is not illegal to have it off during writes.
 3. ODT must be disabled during reads. The RTT_NOM value is restricted during writes. Dynamic ODT is applicable if enabled.

Nominal ODT resistance RTT_{NOM} is defined by MR1[9, 6, 2], as shown in Figure 53 on page 115. The RTT_{NOM} termination value applies to the output pins previously mentioned. DDR3 SDRAM supports multiple RTT_{NOM} values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω . RTT_{NOM} termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access or when it is not in self refresh mode.

Write accesses use RTT_{NOM} if dynamic ODT (RTT_{WR}) is disabled. If RTT_{NOM} is used during writes, only $RZQ/2$, $RZQ/4$, and $RZQ/6$ are allowed (see Table 81 on page 164). ODT timings are summarized in Table 79, as well as listed in Table 56 on page 70.

Examples of nominal ODT timing are shown in conjunction with the synchronous mode of operation in “Synchronous ODT Mode” on page 168.

Table 79: ODT Parameter

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Units
ODTL on	ODT synchronous turn on delay	ODT registered HIGH	$RTT_{ON} \pm t_{AON}$	$CWL + AL - 2$	t_{CK}
ODTL off	ODT synchronous turn off delay	ODT registered HIGH	$RTT_{OFF} \pm t_{AOF}$	$CWL + AL - 2$	t_{CK}
t_{AONPD}	ODT asynchronous turn on delay	ODT registered HIGH	RTT_{ON}	1–9	ns
t_{AOFPD}	ODT asynchronous turn off delay	ODT registered HIGH	RTT_{OFF}	1–9	ns
ODTH4	ODT minimum HIGH time after ODT assertion or write (BC4)	ODT registered HIGH or write registration with ODT HIGH	ODT registered LOW	$4t_{CK}$	t_{CK}
ODTH8	ODT minimum HIGH time after write (BL8)	Write registration with ODT HIGH	ODT registered LOW	$6t_{CK}$	t_{CK}
t_{AON}	ODT turn-on relative to ODTL on completion	Completion of ODTL on	RTT_{ON}	See Table 56 on page 70	ps
t_{AOF}	ODT turn-off relative to ODTL off completion	Completion of ODTL off	RTT_{OFF}	$0.5t_{CK} \pm 0.2t_{CK}$	t_{CK}

Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command, essentially changing the ODT termination on the fly. With dynamic ODT (RTT_WR) enabled, the DRAM switches from nominal ODT (RTT_NOM) to dynamic ODT (RTT_WR) when beginning a WRITE burst and subsequently switches back to nominal ODT (RTT_NOM) at the completion of the WRITE burst. This requirement is supported by the dynamic ODT feature, as described below:

Functional Description

The dynamic ODT mode is enabled if either MR2[9] or MR2[10] is set to “1.” Dynamic ODT is not supported during DLL disable mode so RTT_WR must be disabled. The dynamic ODT function is described, as follows:

- Two RTT values are available—RTT_NOM and RTT_WR:
 - The value for RTT_NOM is preselected via MR1[9, 6, 2]
 - The value for RTT_WR is preselected via MR2[10, 9]
- During DRAM operation without READ or WRITE commands, the termination is controlled as follows:
 - Nominal termination strength RTT_NOM is used
 - Termination on/off timing is controlled via the ODT ball and latencies ODTL on and ODTL off
- When a WRITE command (WR, WRAP, WRS4, WRS8, WRAPS4, WRAPS8) is registered, and if dynamic ODT is enabled, the ODT termination is controlled as follows:
 - A latency of OD TLCNW after the WRITE command: termination strength RTT_NOM switches to RTT_WR
 - A latency of OD TLCWN8 (for BL8, fixed or OTF) or OD TLCWN4 (for BC4, fixed or OTF) after the WRITE command: termination strength RTT_WR switches back to RTT_NOM
 - On/off termination timing is controlled via the ODT ball and determined by OD TL on, OD TL off, OD TH4, and OD TH8
 - During the ^tADC transition window, the value of RTT is undefined

ODT is constrained during writes and when dynamic ODT is enabled (see Table 80). ODT timings listed in Table 79 on page 162 also apply to dynamic ODT mode.

Table 80: Dynamic ODT Specific Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Units
OD TLCNW	Change from RTT_NOM to RTT_WR	Write registration	RTT switched from RTT_NOM to RTT_WR	WL - 2	^t CK
OD TLCWN4	Change from RTT_WR to RTT_NOM (BC4)	Write registration	RTT switched from RTT_WR to RTT_NOM	4 ^t CK + OD TL off	^t CK
OD TLCWN8	Change from RTT_WR to RTT_NOM (BL8)	Write registration	RTT switched from RTT_WR to RTT_NOM	6 ^t CK + OD TL off	^t CK
^t ADC	RTT change skew	OD TLCNW completed	RTT transition complete	0.5 ^t CK ± 0.2 ^t CK	tCK

Table 81: Mode Registers for RTT_NOM

MR1 (RTT_NOM)			RTT_NOM (RZQ)	RTT_NOM (Ohms)	RTT_NOM Mode Restriction
M9	M6	M2			
0	0	0	Off	Off	n/a
0	0	1	RZQ/4	60	Self refresh
0	1	0	RZQ/2	120	
0	1	1	RZQ/6	40	
1	0	0	RZQ/12	20	Self refresh, write
1	0	1	RZQ/8	30	
1	1	0	Reserved	Reserved	n/a
1	1	1	Reserved	Reserved	n/a

Notes: 1. RZQ = 240Ω. If RTT_NOM is used during WRITES, only RZQ/2, RZQ/4, RZQ/6 are allowed.

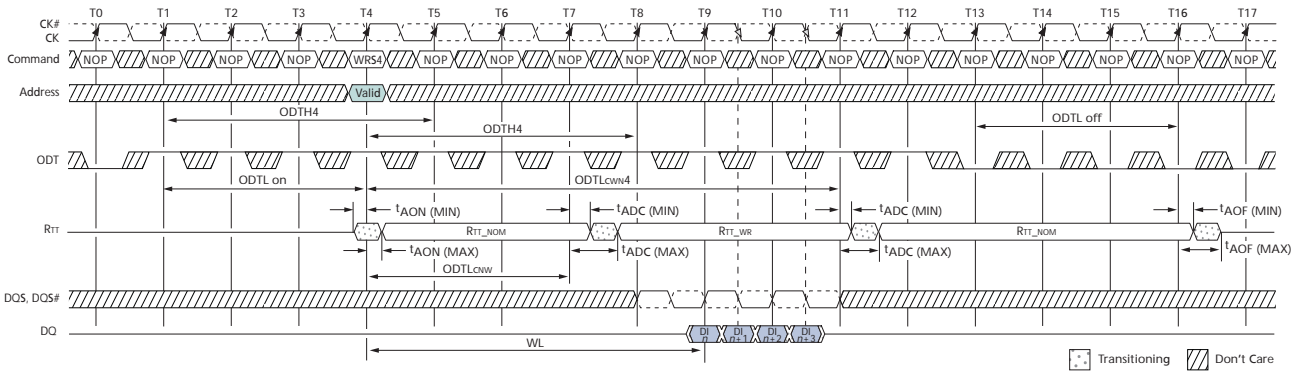
Table 82: Mode Registers for RTT_WR

MR2 (RTT_WR)		RTT_WR (RZQ)	RTT_WR (Ohms)
M10	M9		
0	0	Dynamic ODT off: WRITE does not affect RTT_NOM	
0	1	RZQ/4	60
1	0	RZQ/2	120
1	1	Reserved	Reserved
n/a	n/a	n/a	n/a
n/a	n/a	n/a	n/a
n/a	n/a	n/a	n/a
n/a	n/a	n/a	n/a

Table 83: Timing Diagrams for Dynamic ODT

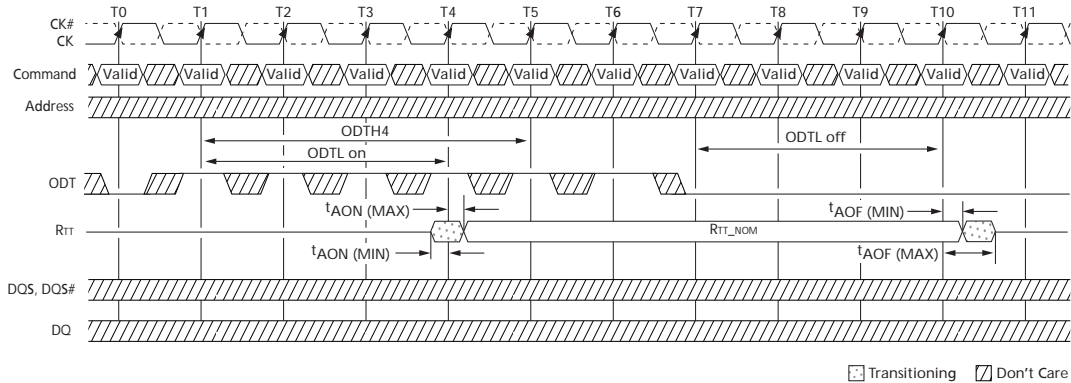
Figure and Page	Title
Figure 108 on page 165	Dynamic ODT: ODT Asserted Before and After the WRITE, BC4
Figure 109 on page 165	Dynamic ODT: Without WRITE Command
Figure 110 on page 166	Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8
Figure 111 on page 167	Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4
Figure 112 on page 167	Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4

Figure 108: Dynamic ODT: ODT Asserted Before and After the WRITE, BC4



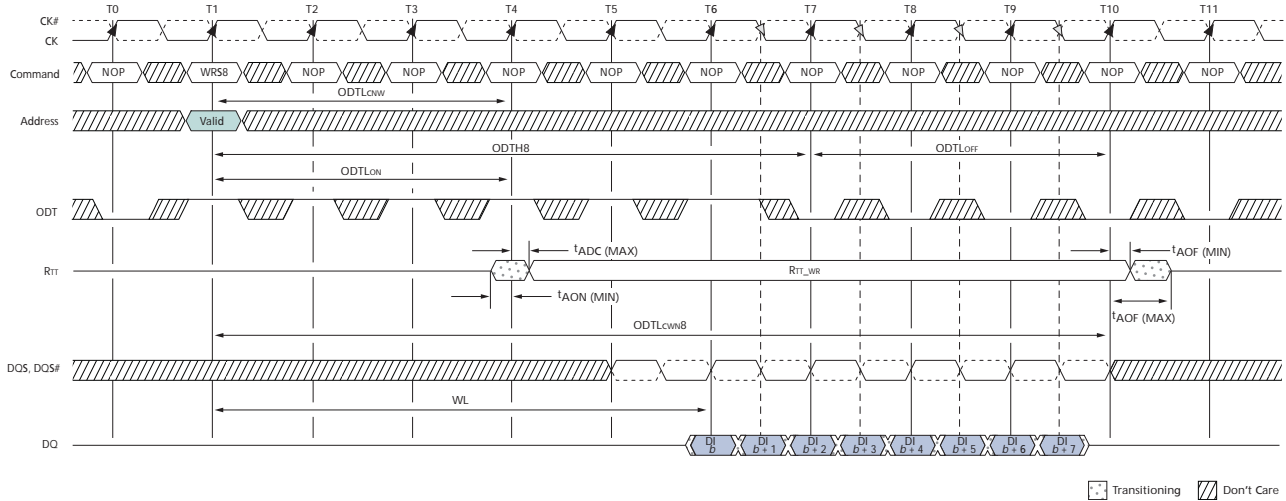
- Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM and RTT_WR are enabled.
 2. ODT_{H4} applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODT_{H4} is satisfied if ODT goes LOW at T8 (four clocks after the WRITE command).

Figure 109: Dynamic ODT: Without WRITE Command



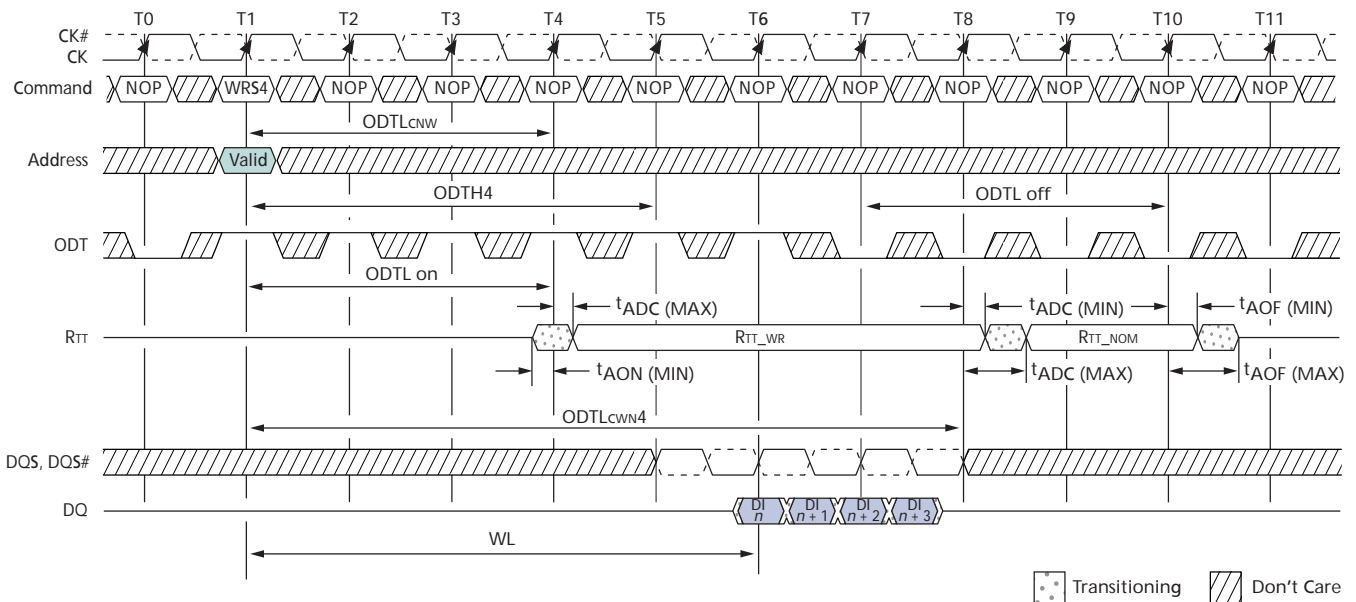
- Notes:
1. AL = 0, CWL = 5. RTT_NOM is enabled and RTT_WR is either enabled or disabled.
 2. ODT_{H4} is defined from ODT registered HIGH to ODT registered LOW; in this example, ODT_{H4} is satisfied. ODT registered LOW at T5 is also legal.

Figure 110: Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8



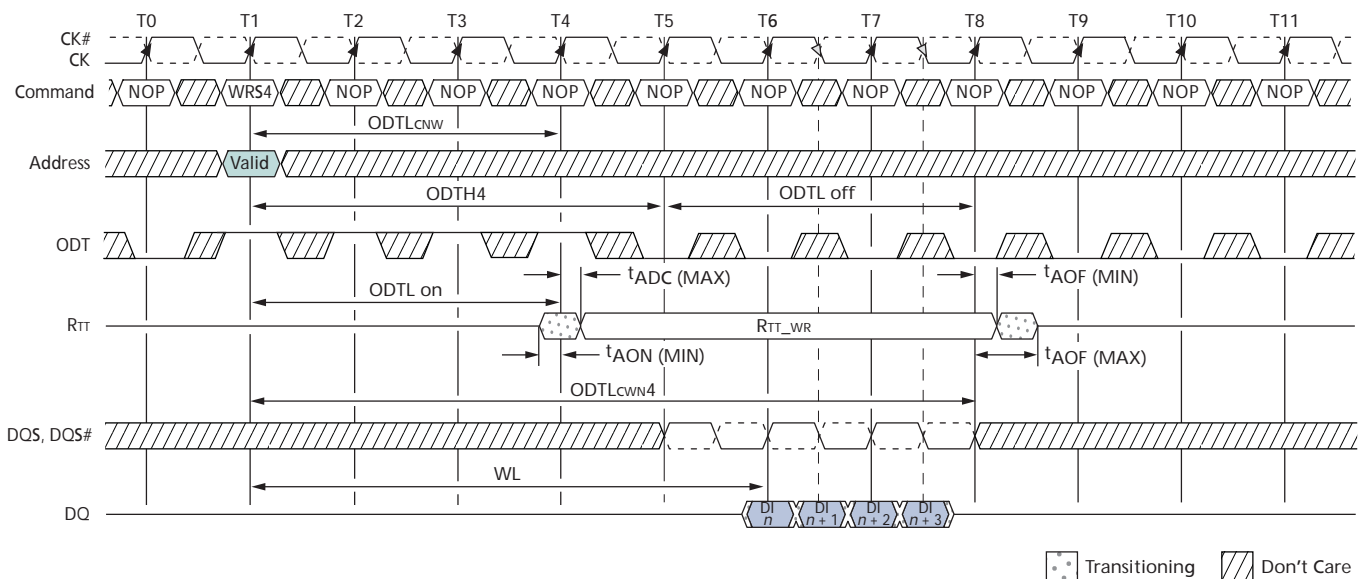
- Notes:
1. Via MRS or OTF; AL = 0, CWL = 5. If R_{TT_NOM} can be either enabled or disabled, ODT can be HIGH. R_{TT_WR} is enabled.
 2. In this example, ODTH8 = 6 is satisfied exactly.

Figure 111: Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4



- Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM and RTT_WR are enabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW, so in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Figure 112: Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4



- Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM can be either enabled or disabled. If disabled, ODT can remain HIGH. RTT_WR is enabled.
2. In this example ODTH4 = 4 is satisfied exactly.

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked and when either `RTT_NOM` or `RTT_WR` is enabled. Based on the power-down definition, these modes are:

- Any bank active with `CKE HIGH`
- Refresh mode with `CKE HIGH`
- Idle mode with `CKE HIGH`
- Active power-down mode (regardless of `MR0[12]`)
- Precharge power-down mode if DLL is enabled during precharge power-down by `MR0[12]`

ODT Latency and Posted ODT

In synchronous ODT mode, `RTT` turns on `ODTL` on clock cycles after `ODT` is sampled HIGH by a rising clock edge and turns off `ODTL` off clock cycles after `ODT` is registered LOW by a rising clock edge. The actual on/off times varies by t_{AON} and t_{AOF} around each clock edge (see Table 84 on page 169). The ODT latency is tied to the WRITE latency (`WL`) by `ODTL on = WL - 2` and `ODTL off = WL - 2`.

Since write latency is made up of CAS WRITE latency (`CWL`) and ADDITIVE latency (`AL`), the `AL` programmed into the mode register (`MR1[4, 3]`) also applies to the ODT signal. The DRAM's internal ODT signal is delayed a number of clock cycles defined by the `AL` relative to the external ODT signal. Thus `ODTL on = CWL + AL - 2` and `ODTL off = CWL + AL - 2`.

Timing Parameters

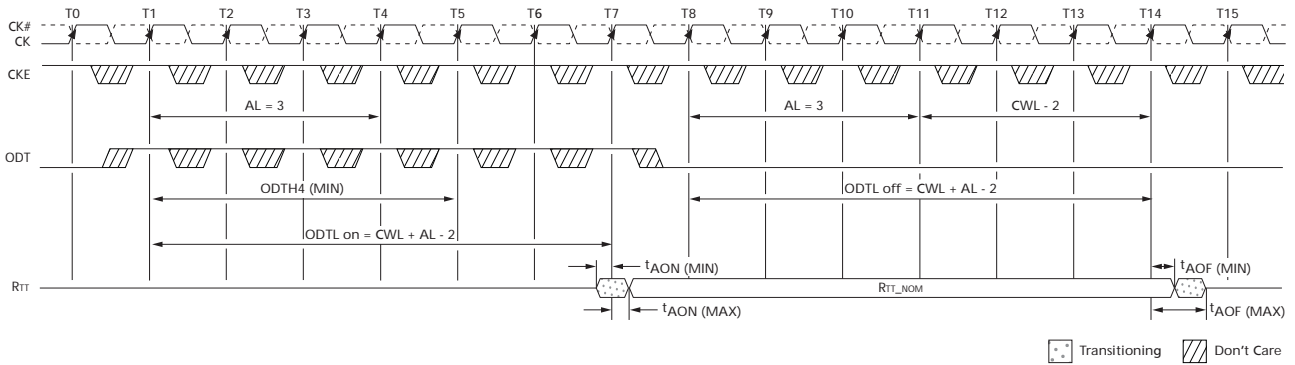
Synchronous ODT mode uses the following timing parameters: `ODTL on`, `ODTL off`, `ODTH4`, `ODTH8`, t_{AON} , and t_{AOF} (see Table 84 and Figure 113 on page 169). The minimum `RTT` turn-on time ($t_{AON} [MIN]$) is the point at which the device leaves High-Z and ODT resistance begins to turn on. Maximum `RTT` turn-on time ($t_{AON} [MAX]$) is the point at which ODT resistance is fully on. Both are measured relative to `ODTL on`. The minimum `RTT` turn-off time ($t_{AOF} [MIN]$) is the point at which the device starts to turn off ODT resistance. Maximum `RTT` turn off time ($t_{AOF} [MAX]$) is the point at which ODT has reached High-Z. Both are measured from `ODTL off`.

When `ODT` is asserted, it must remain HIGH until `ODTH4` is satisfied. If a `WRITE` command is registered by the DRAM with `ODT HIGH`, then `ODT` must remain HIGH until `ODTH4` (`BC4`) or `ODTH8` (`BL8`) after the `WRITE` command (see Figure 114 on page 170). `ODTH4` and `ODTH8` are measured from `ODT` registered HIGH to `ODT` registered LOW or from the registration of a `WRITE` command until `ODT` is registered LOW.

Table 84: Synchronous ODT Parameters

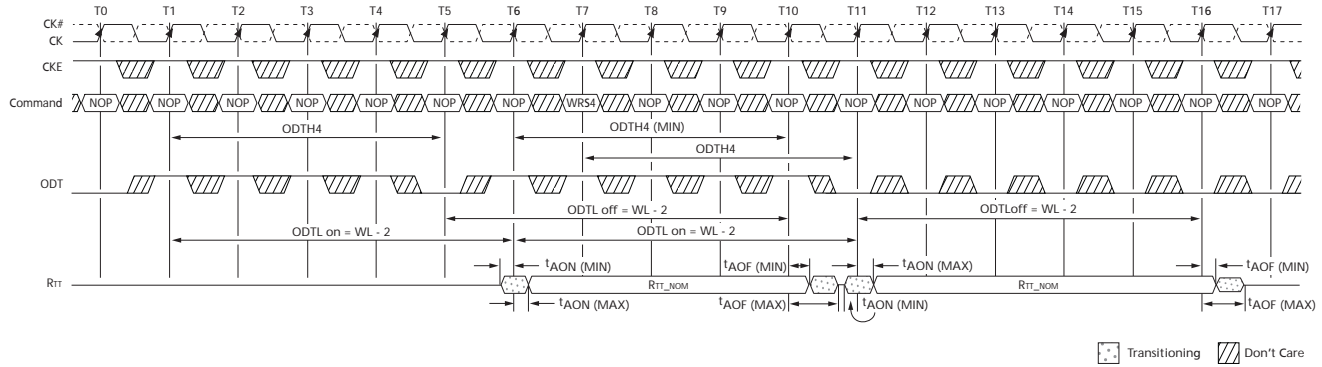
Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Units
ODTL on	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT_ON} \pm t_{AON}$	$CWL + AL - 2$	t_{CK}
ODTL off	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT_OFF} \pm t_{AOF}$	$CWL + AL - 2$	t_{CK}
ODTH4	ODT minimum HIGH time after ODT assertion or WRITE (BC4)	ODT registered HIGH, or write registration with ODT HIGH	ODT registered LOW	$4t_{CK}$	t_{CK}
ODTH8	ODT minimum HIGH time after WRITE (BL8)	Write registration with ODT HIGH	ODT registered LOW	$6t_{CK}$	t_{CK}
t_{AON}	ODT turn-on relative to ODTL on completion	Completion of ODTL on	R_{TT_ON}	See Table 56 on page 70	ps
t_{AOF}	ODT turn-off relative to ODTL off completion	Completion of ODTL off	R_{TT_OFF}	$0.5t_{CK} \pm 0.2t_{CK}$	t_{CK}

Figure 113: Synchronous ODT



Notes: 1. AL = 3; CWL = 5; ODTL on = WL = 6.0; ODTL off = WL - 2 = 6. RTT_NOM is enabled.

Figure 114: Synchronous ODT (BC4)



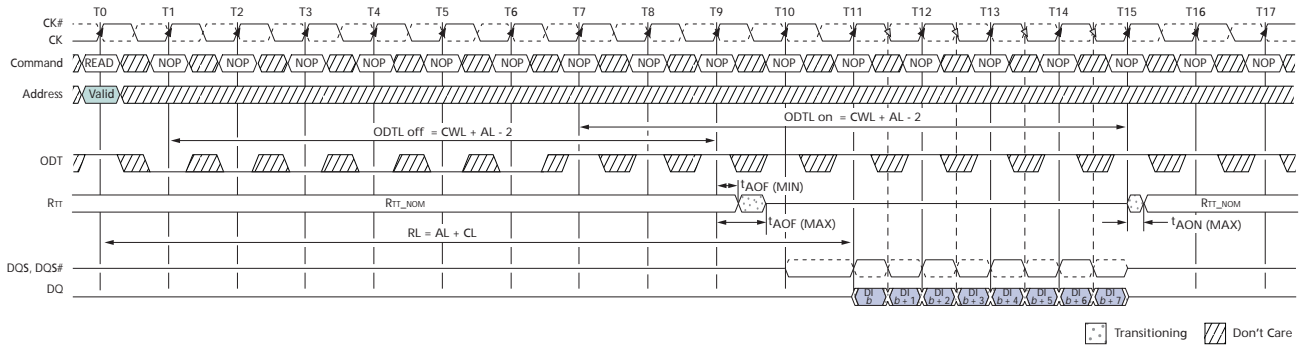
- Notes:
1. WL = 7. Rtt_NOM is enabled. Rtt_WR is disabled.
 2. ODT must be held HIGH for at least ODTH4 after assertion (T1).
 3. ODT must be kept HIGH ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (T7).
 4. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of the WRITE command with ODT HIGH to ODT registered LOW.
 5. Although ODTH4 is satisfied from ODT registered HIGH at T6, ODT must not go LOW before T11 as ODTH4 must also be satisfied from the registration of the WRITE command at T7.

ODT Off During READs

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least one-half clock cycle before the READ preamble by driving the ODT ball LOW (if either RTT_NOM or RTT_WR is enabled). RTT may not be enabled until the end of the postamble as shown in the example in Figure 115 on page 172.

Note: ODT may be disabled earlier and enabled later than shown in Figure 115 on page 172.

Figure 115: ODT During READs



- Notes: 1. ODT must be disabled externally during READs by driving ODT LOW. For example, $CL = 6$; $AL = CL - 1 = 5$; $RL = AL + CL = 11$; $CWL = 5$; $ODTL_{on} = CWL + AL - 2 = 8$; $ODTL_{off} = CWL + AL - 2 = 8$. Rtt_{NOM} is enabled. Rtt_{WR} is a "Don't Care."

Asynchronous ODT Mode

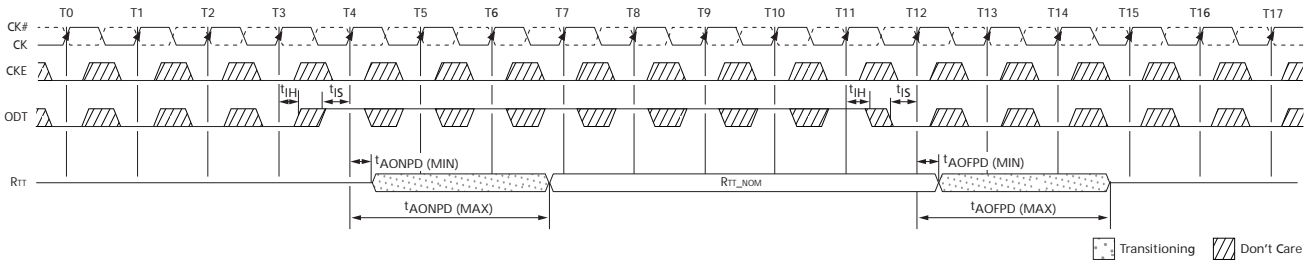
Asynchronous ODT mode is available when the DRAM runs in DLL on mode and when either `RTT_NOM` or `RTT_WR` is enabled; however, the DLL is temporarily turned off in precharged power-down standby (via `MR0[12]`). Additionally, ODT operates asynchronously when the DLL is synchronizing after being reset. See “Power-Down Mode” on page 153 for definition and guidance over power-down details.

In asynchronous ODT timing mode, the internal ODT command is not delayed by AL relative to the external ODT command. In asynchronous ODT mode, ODT controls `RTT` by analog time. The timing parameters t_{AONPD} and t_{AOFPD} (see Table 85 on page 174) replace `ODTL on`/ t_{AON} and `ODTL off`/ t_{AOE} , respectively, when ODT operates asynchronously (see Figure 116 on page 174).

The minimum `RTT` turn-on time (t_{AONPD} [MIN]) is the point at which the device termination circuit leaves High-Z and ODT resistance begins to turn on. Maximum `RTT` turn-on time (t_{AONPD} [MAX]) is the point at which ODT resistance is fully on. t_{AONPD} (MIN) and t_{AONPD} (MAX) are measured from ODT being sampled HIGH.

The minimum `RTT` turn-off time (t_{AOFPD} [MIN]) is the point at which the device termination circuit starts to turn off ODT resistance. Maximum `RTT` turn-off time (t_{AOFPD} [MAX]) is the point at which ODT has reached High-Z. t_{AOFPD} (MIN) and t_{AOFPD} (MAX) are measured from ODT being sampled LOW.

Figure 116: Asynchronous ODT Timing with Fast ODT Transition



Notes: 1. AL is ignored.

Table 85: Asynchronous ODT Timing Parameters for All Speed Bins

Symbol	Description	Min	Max	Units
t_{AONPD}	Asynchronous RTT turn-on delay (power-down with DLL off)	2	8.5	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (power-down with DLL off)	2	8.5	ns

Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry)

There is a transition period around power-down entry (PDE) where the DRAM's ODT may exhibit either synchronous or asynchronous behavior. This transition period occurs if the DLL is selected to be off when in precharge power-down mode by the setting $MR0[12] = 0$. Power-down entry begins t_{ANPD} prior to CKE first being registered LOW, and it ends when CKE is first registered LOW. t_{ANPD} is equal to the greater of $ODTL_{off} + 1t_{CK}$ or $ODTL_{on} + 1t_{CK}$. If a REFRESH command has been issued, and it is in progress when CKE goes LOW, power-down entry will end t_{RFC} after the REFRESH command rather than when CKE is first registered LOW. Power-down entry will then become the greater of t_{ANPD} and $t_{RFC} - \text{REFRESH command to CKE registered LOW}$.

ODT assertion during power-down entry results in an R_{TT} change as early as the lesser of $t_{AONPD}(\text{MIN})$ and $ODTL_{on} \times t_{CK} + t_{AON}(\text{MIN})$ or as late as the greater of $t_{AONPD}(\text{MAX})$ and $ODTL_{on} \times t_{CK} + t_{AON}(\text{MAX})$. ODT de-assertion during power-down entry may result in an R_{TT} change as early as the lesser of $t_{AOFPD}(\text{MIN})$ and $ODTL_{off} \times t_{CK} + t_{AOF}(\text{MIN})$ or as late as the greater of $t_{AOFPD}(\text{MAX})$ and $ODTL_{off} \times t_{CK} + t_{AOF}(\text{MAX})$. Table 86 on page 176 summarizes these parameters.

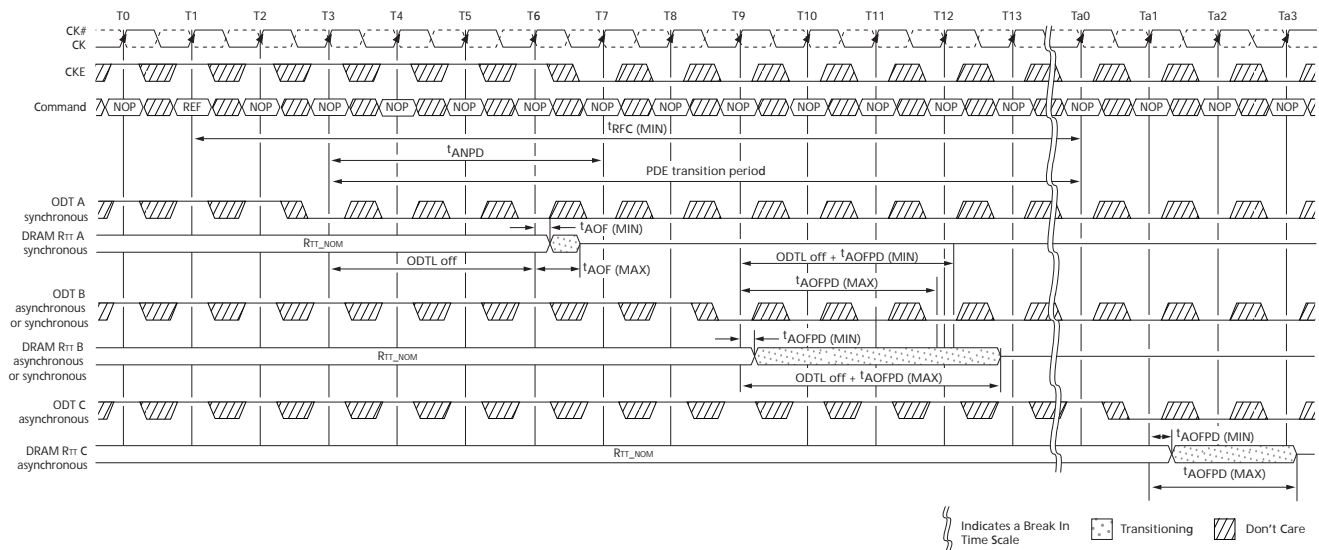
If the AL has a large value, the uncertainty of the state of R_{TT} becomes quite large. This is because $ODTL_{on}$ and $ODTL_{off}$ are derived from the WL and WL is equal to $CWL + AL$. Figure 117 on page 176 shows three different cases:

- ODT_A: Synchronous behavior before t_{ANPD}
- ODT_B: ODT state changes during the transition period with $t_{AONPD}(\text{MIN})$ less than $ODTL_{on} \times t_{CK} + t_{AON}(\text{MIN})$ and $t_{AONPD}(\text{MAX})$ greater than $ODTL_{on} \times t_{CK} + t_{AON}(\text{MAX})$
- ODT_C: ODT state changes after the transition period with asynchronous behavior

Table 86: ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period

Description	Min	Max
Power-down entry transition period (power-down entry)	Greater of: t_{ANPD} or t_{RFC} - refresh to CKE LOW	
Power-down exit transition period (power-down exit)	$t_{ANPD} + t_{XPDLL}$	
ODT to R _{TT} turn-on delay (ODTL on = WL - 2)	Lesser of: t_{AONPD} (MIN) (1ns) or ODTL on $\times t_{CK} + t_{AON}$ (MIN)	Greater of: t_{AONPD} (MAX) (9ns) or ODTL on $\times t_{CK} + t_{AON}$ (MAX)
ODT to R _{TT} turn-off delay (ODTL off = WL - 2)	Lesser of: t_{AOFPD} (MIN) (1ns) or ODTL off $\times t_{CK} + t_{AOF}$ (MIN)	Greater of: t_{AOFPD} (MAX) (9ns) or ODTL off $\times t_{CK} + t_{AOF}$ (MAX)
t_{ANPD}	WL - 1 (greater of ODTL off + 1 or ODTL on + 1)	

Figure 117: Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry



Notes: 1. AL = 0; CWL = 5; ODTL off = WL - 2 = 3.



2Gb: x4, x8, x16 DDR3 SDRAM
 On-Die Termination (ODT)

Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit)

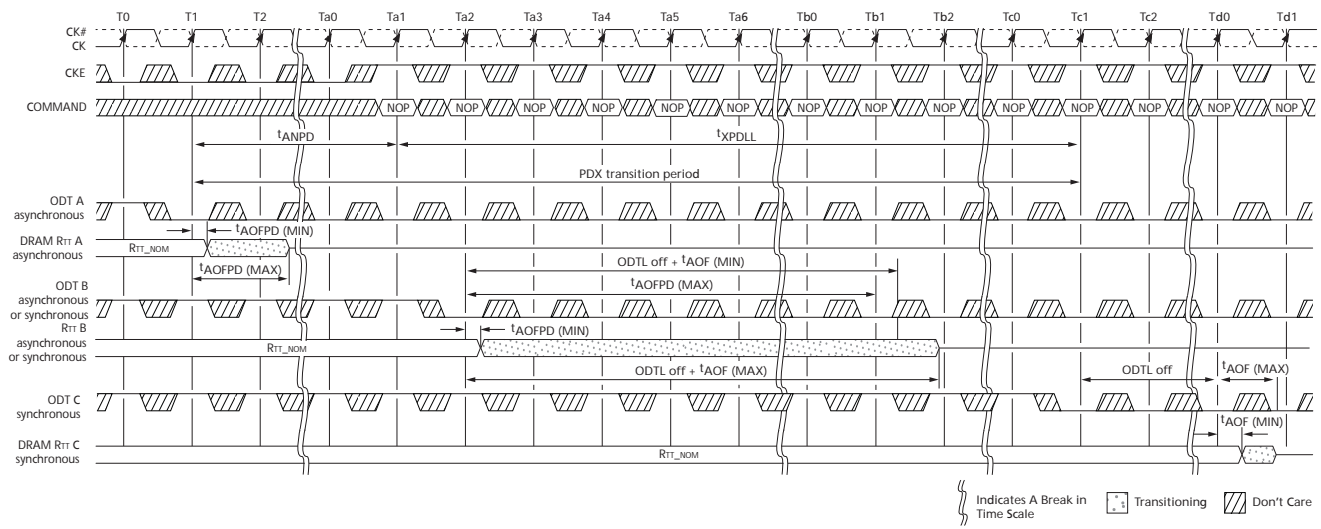
The DRAM's ODT may exhibit either asynchronous or synchronous behavior during power-down exit (PDX). This transition period occurs if the DLL is selected to be off when in precharge power-down mode by setting MR0[12] to "0." Power-down exit begins t_{ANPD} prior to CKE first being registered HIGH, and it ends t_{XPDLL} after CKE is first registered HIGH. t_{ANPD} is equal to the greater of $ODTL_{off} + 1t_{CK}$ or $ODTL_{on} + 1t_{CK}$. The transition period is t_{ANPD} plus t_{XPDLL} .

ODT assertion during power-down exit results in an RTT change as early as the lesser of $t_{AONPD} (MIN)$ and $ODTL_{on} \times t_{CK} + t_{AON} (MIN)$ or as late as the greater of $t_{AONPD} (MAX)$ and $ODTL_{on} \times t_{CK} + t_{AON} (MAX)$. ODT de-assertion during power-down exit may result in an RTT change as early as the lesser of $t_{AOFPD} (MIN)$ and $ODTL_{off} \times t_{CK} + t_{AOF} (MIN)$ or as late as the greater of $t_{AOFPD} (MAX)$ and $ODTL_{off} \times t_{CK} + t_{AOF} (MAX)$. Table 86 on page 176 summarizes these parameters.

If the AL has a large value, the uncertainty of the RTT state becomes quite large. This is because $ODTL_{on}$ and $ODTL_{off}$ are derived from the WL, and WL is equal to $CWL + AL$. Figure 118 on page 178 shows three different cases:

- ODT C: asynchronous behavior before t_{ANPD}
- ODT B: ODT state changes during the transition period, with $t_{AOFPD} (MIN)$ less than $ODTL_{off} \times t_{CK} + t_{AOF} (MIN)$ and $ODTL_{off} \times t_{CK} + t_{AOF} (MAX)$ greater than $t_{AOFPD} (MAX)$
- ODT A: ODT state changes after the transition period with synchronous response

Figure 118: Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit



Notes: 1. $CL = 6$; $AL = CL - 1$; $CWL = 5$; $ODTL\ off = WL - 2 = 8$.

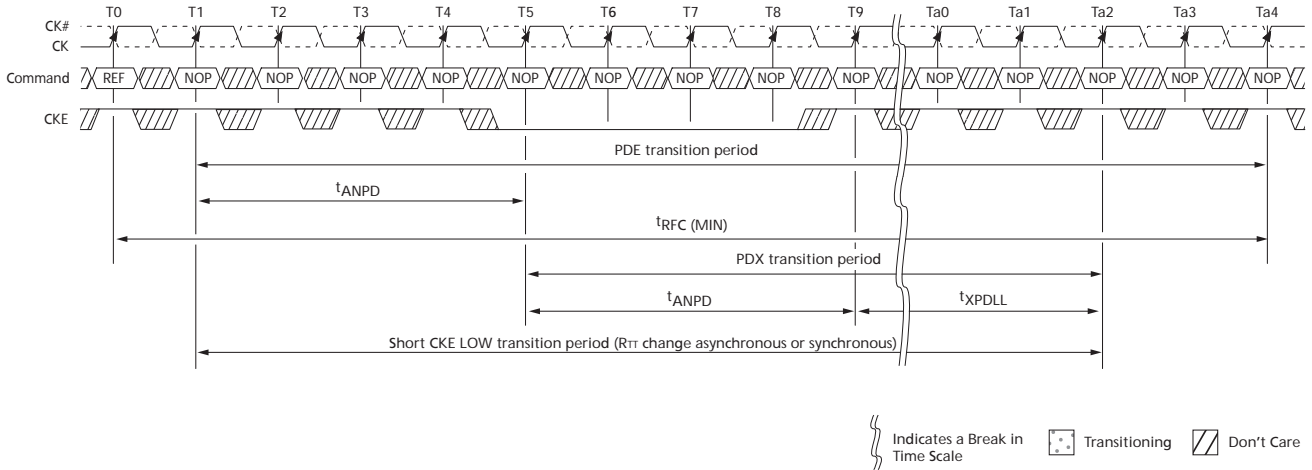


Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse)

If the time in the precharge power down or idle states is very short (short CKE LOW pulse), the power-down entry and power-down exit transition periods will overlap. When overlap occurs, the response of the DRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of the power-down entry transition period to the end of the power-down exit transition period even if the entry period ends later than the exit period (see Figure 119 on page 180).

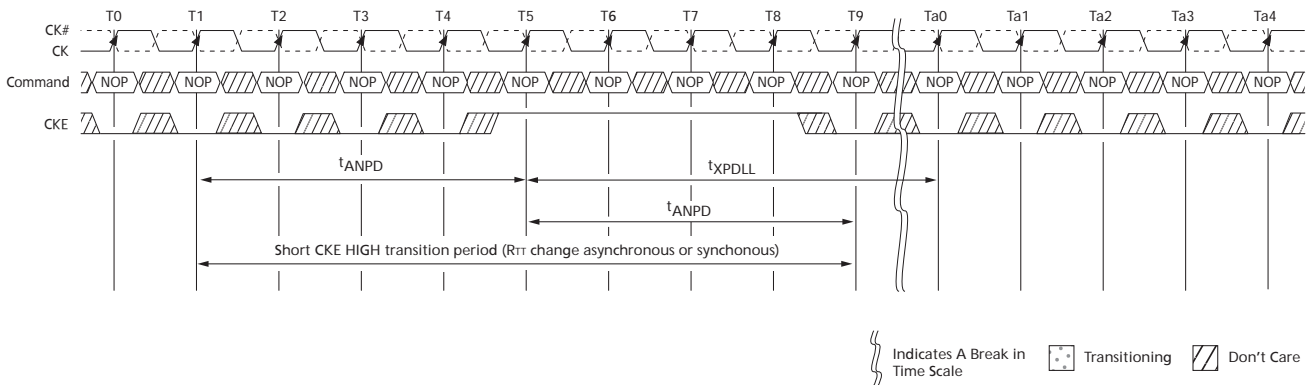
If the time in the idle state is very short (short CKE HIGH pulse), the power-down exit and power-down entry transition periods overlap. When this overlap occurs, the response of the DRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of power-down exit transition period to the end of the power-down entry transition period (see Figure 119 on page 180).

Figure 119: Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping



Notes: 1. AL = 0, WL = 5, $t_{ANPD} = 4$.

Figure 120: Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping



Notes: 1. AL = 0, WL = 5, $t_{ANPD} = 4$.



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