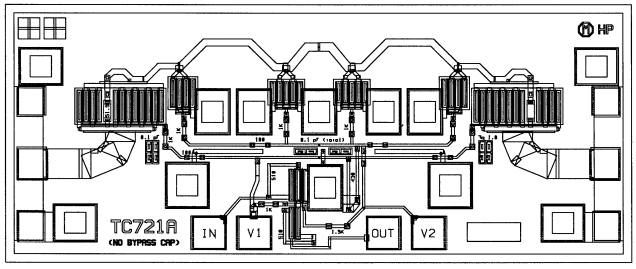
HMMC-1002
DC–50 GHz Variable Attenuator

Data Sheet

Description
The HMMC-1002 is a monolithic, voltage variable, GaAs IC attenuator that operates from DC to 50 GHz. It is fabricated using MWTC's MMICB process which features an MBE epitaxial layer, backside ground vias, and FET gate lengths of approximately 0.4 mm. The variable resistive elements of the HMMC-1002 are two 750 mm wide series FETs and four 200 mm wide shunt FETs. The distributed topology of the HMMC-1002 minimizes the parasitic effects of its series and shunt FETs, allowing the HMMC-1002 to exhibit a wide dynamic range across its full bandwidth. An on-chip DC reference circuit may be used to maintain optimum VSWR for any attenuation setting or to improve the attenuation versus voltage linearity of the attenuator circuit.

Features
- **Specified Frequency Range:**
  DC–26.5 GHz
- **Return Loss:**
  10 dB
- **Minimum Attenuation:**
  2.0 dB
- **Maximum Attenuation:**
  30.0 dB



Chip Size:	1470 x 610 µm (57.9 x 24.0 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
RF Pad Dimensions:	60 x 70 µm (2.4 x 2.8 mils), or larger
DC Pad Dimensions:	75 x 75 µm (3.0 x 3.0 mils), or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DC-RF}	DC Voltage to RF Ports	V	-0.6	+1.6
V_1	V_1 Control Voltage	V	-5.0	+0.5
V_2	V_2 Control Voltage	V	-5.0	+0.5
V_{DC}	DC In/DC Out	V	-0.6	+1.0
P_{IN}	RF Input Power	dBm		17
T_{mina}	Min. Ambient Operating Temp.	°C	-55	
T_{maxa}	Max. Ambient Operating Temp.	°C		+125
T_{stg}	Storage Temperature	°C	-65	+165
T_{max}	Max. Assembly Temp. (for 60 sec. max.)	°C		+300

Notes:
1. Operation in excess of any one of these conditions may result in damage to this device.

HMMC-1002 DC Specifications/Physical Properties, $T_A = 25°C$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{V1}	V_1 Control Current, (V_1 = -4V)	mA	5.3	9.3	12
I_{V2}	V_2 Control Current, (V_2 = -4V)	mA	5.3	9.3	12
V_P	Pinch-Off Voltage, (V_2, W/V_1 = 0 V) (Four 200 µm wide shunt FETs, V_{DD} = 1 V @ RF_{in}, I_{DD} = 5 mA)	V	-0.6	-1.3	-2.5

Electrical Specifications[1], $T_A = 25°C$, $Z_0 = 50\ \Omega$

Parameters and Test Conditions	Units	Freq. (GHz)	Min.	Typ.	Max.
Minimum Attenuation, $\lvert S_{21} \rvert$ V_1 = 0 V, V_2 = -4 V	dB	1.5 8.0 20.00 26.5 50.0		1.0 1.4 1.7 2.0 3.9	2.4 2.4 2.4 2.4
Input/Output Return Loss @ Min. Attenuation Setting, (V_1 = 0 V, V_2 = -4 V)	dB	<26.5 <50.0	10	16 8	
Maximum Attenuation, $\lvert S_{21} \rvert$ (V_1 = -4 V, V_2 = 0 V)	dB	1.5 8.0 20.0 26.5 50.0	27 27 27 27	30 38 38 40 35	
Input/Output Return Loss @ Max. Attenuation Setting, V_1 = -4 V, V_2 = 0 V	dB	<26.5 <50.0	8	10 10	
DC Power Dissipation, V_1 = -5 V, V_2 = -5 V (does not include input signals)	mW				152

Note:
1. Attenuation is a positive number; whereas, S_{21} as measured on a Network Analyzer would be a negative number.

Application

The HMMC-1002 is designed to be used as a gain control block in an ALC assembly. Because of its wide dynamic range and return loss performance, the HMMC-1002 may also be used as a broadband pulse modulator or single-pole single-throw, non-reflective switch.

Operation

The attenuation value of the HMMC-1002 is adjusted by apply-ing negative voltage to V_2. At any attenuation setting, optimum VSWR is obtained by applying negative voltage to V_1. Applying negative voltage (V_2) to the gates of the shunt FETs sets the source-to-drain resistance and establishes the attenuation level. Applying negative voltage (V_1) to the gates of the series FETs optimizes the input and output match for different attenuation settings. In some applications, a single setting of V_1 may provide sufficient input and output match over the desired attenuation range (V_1). For any HMMC-1002 the values of V_1 may be adjusted so that the device attenuation versus voltage is monotonic for both V_1 and V_2; however, this will slightly degrade the input and output return loss.

The attenuation and input/output match of the HMMC-1002 may also be controlled using only a single input voltage by utilizing the on-chip DC reference circuit and the driver circuit shown in Figure 4. This circuit optimizes VSWR for any attenuation setting. Because of process variations, the values of V_{REF}, R_{REF}, and R_L are different for each wafer if optimum performance is required. Typical values for these elements are given. The ratio of the resistors R_1 and R_2 determines the sensitivity of the attenuation versus voltage performance of the attenuator.

Assembly Techniques

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical fac-Figure tors in successful GaAs MMIC performance and reliability. Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Additional References:

AN#31, "2–26.5 Variable Gain Amplifier Using HMMC-5021/22/26 and HMMC-1002 GaAs MMIC Components," AN#37, "HMMC-1002 Attenuator: Attenuation Control, "AN#44, "DC–50 GHz Variable Attenuator: S-Parameters," AN#45, "HMMC-1002 DC–50 GHz Variable Attenuator: Switching Speed Limitations, and PN#10, "HMMC-1002 50 GHz Attenuator 0–50 GHz Performance."

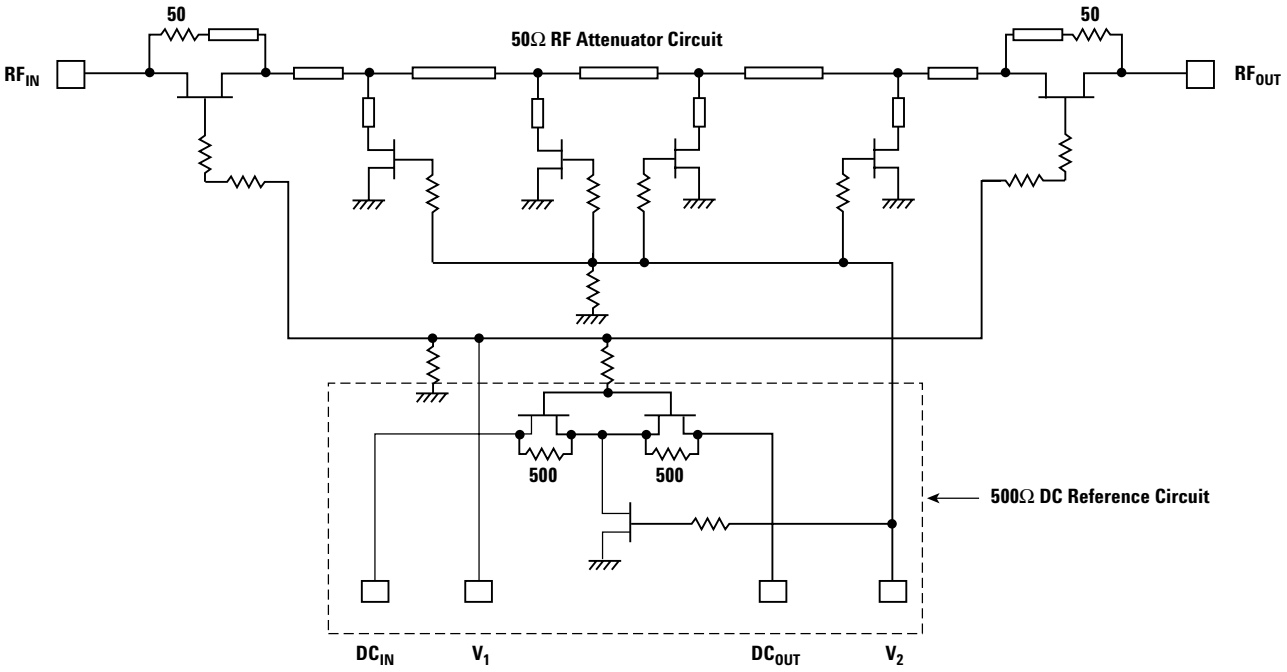
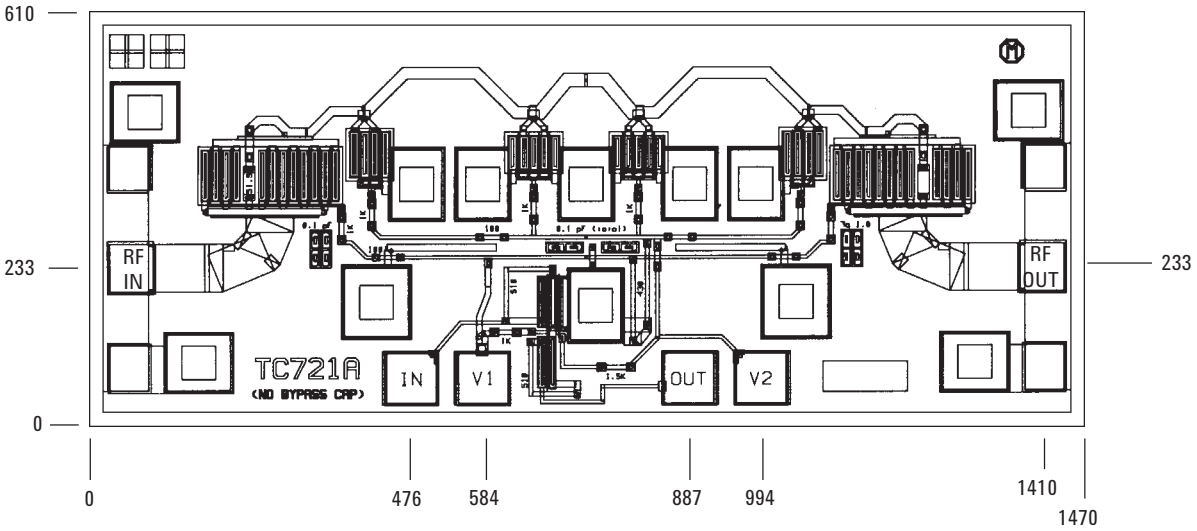


Figure 1. HMMC-1002 Schematic.



Notes:

1. All dimensions in microns and shown to center of bond pad.
2. DC_{in}, V1, DC_{out}, and V_2 bonding pads are 75 x 75 microns.
3. RF input and output bonding pads are 60 x 70 microns.
4. Chip thickness: 127 ± 15 µm.

Figure 2. HMMC-1002 Bonding Pad Locations.

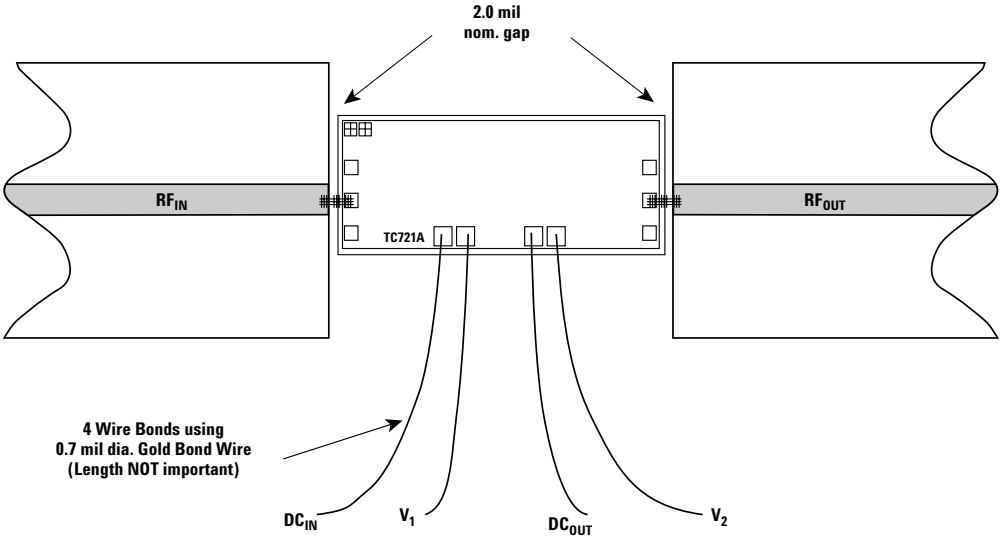


Figure 3. HMMC-1002 Assembly Diagram.

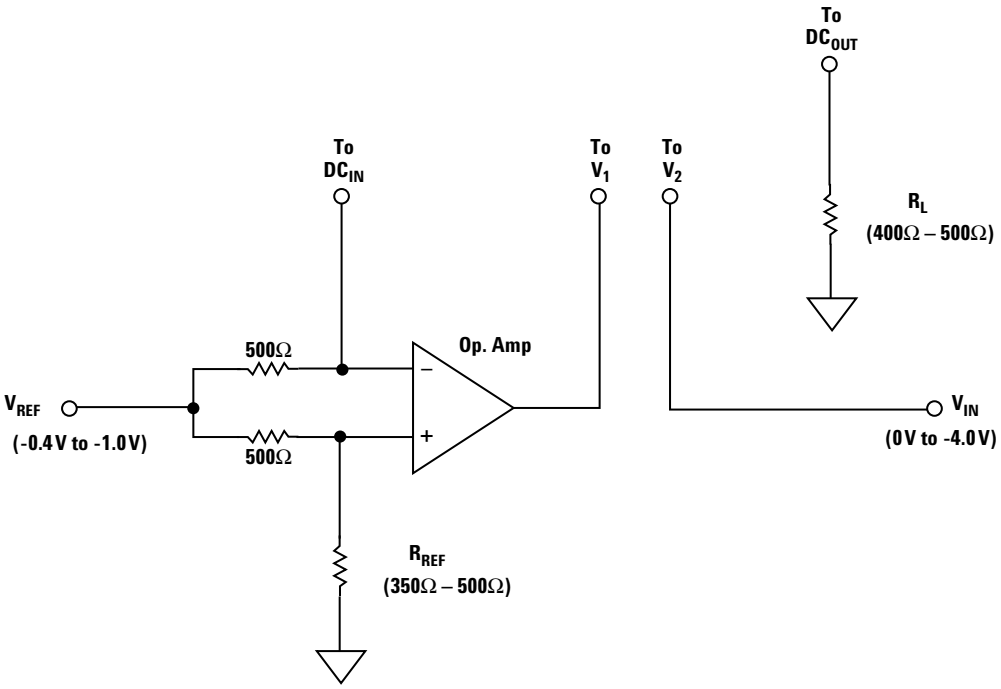


Figure 4. Attenuator Driver.

HMMC-1002 Typical Performance

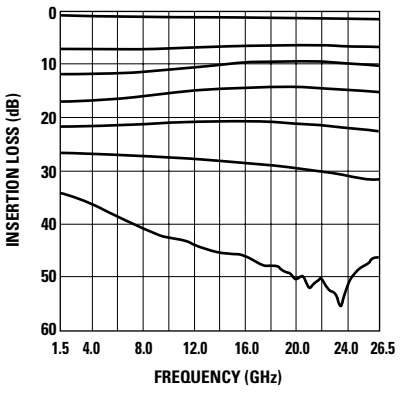


Figure 5. Attenuation vs. Frequency[1].

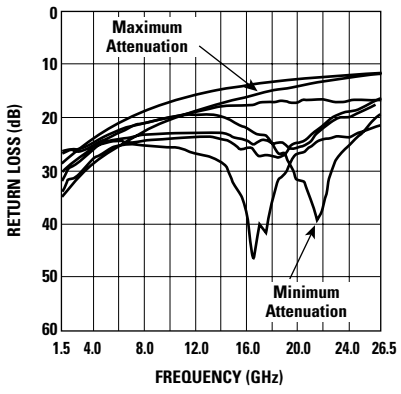


Figure 6. Output Return Loss vs. Frequency[1].

Note:

1. Data obtained from on-wafer measurements. T_{chuck} = 25°C.

HMMC-1002 Typical Power Performance

All Attenuation Settings were done at 1 GHz.

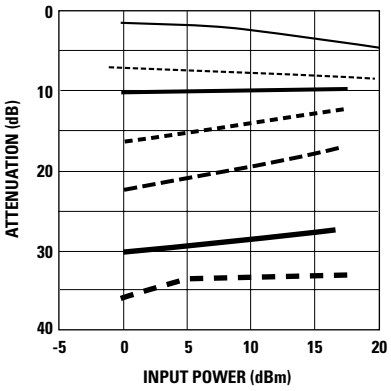


Figure 7. Attenuation vs. Input Power @ 50.0 MHz.[1].

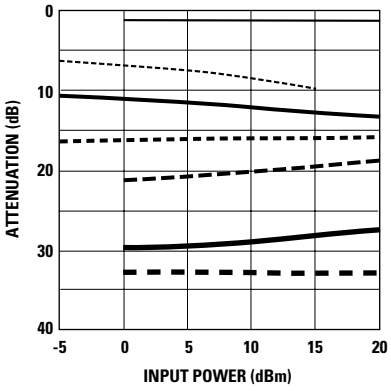


Figure 8. Attenuation vs. Input Power @ 2.0 GHz.[1].

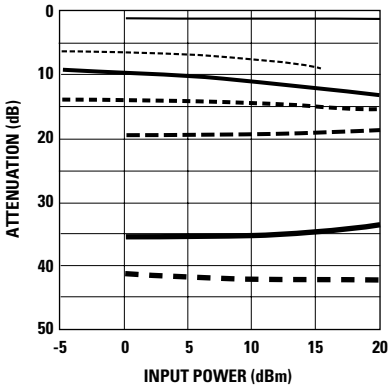


Figure 9. Attenuation vs. Input Power @ 10.0 GHz.[1].

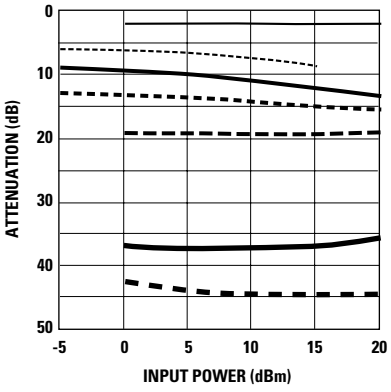


Figure 10. Attenuation vs. Input Power @ 14.0 GHz.[1].

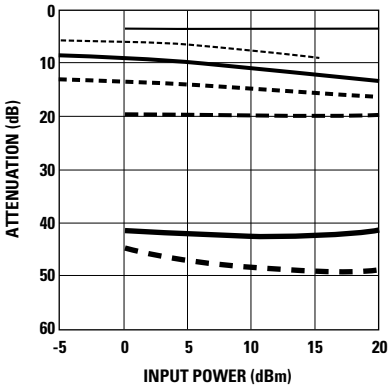


Figure 11. Attenuation vs. Input Power @ 18.0 GHz.[1].

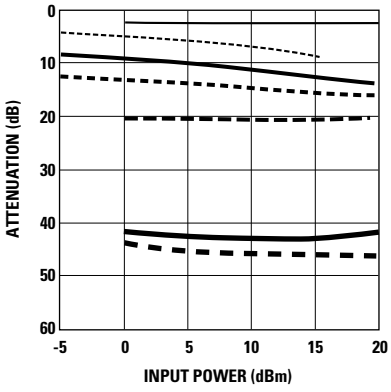


Figure 12. Attenuation vs. Input Power @ 22.0 GHz.[1].

Note:

1. Data taken with the device mounted in connectorized package.

Key for Attenuation Settings:

- Min.
- Min. + 5 dB
- Min. + 10 dB
- Min. + 15 dB
- Min. + 20 dB
- Min. + 30 dB
- Max.

HMMC-1002 Typical Harmonic Performance

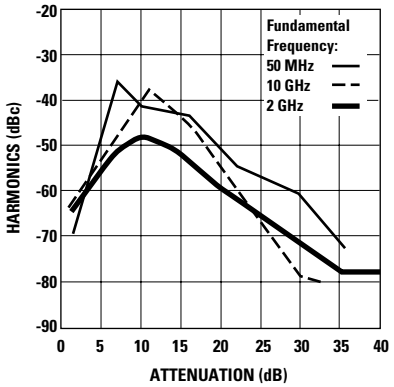


Figure 13. Second Harmonic Suppression vs. Attenuation. Input Power = 0 dBm[1].

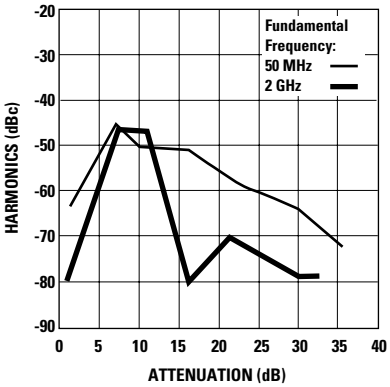


Figure 14. Third Harmonic Suppression vs. Attenuation. Input Power = 0 dBm[1].

Note:

1. Data taken with the device mounted in connectorized package.

HMMC-1002 Typical Temperature Performance

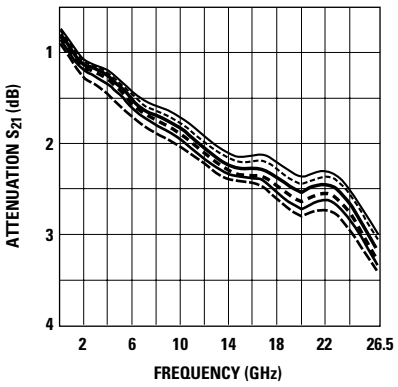


Figure 15. Attenuation vs. Temperature @ Minimum Attenuation.[1].

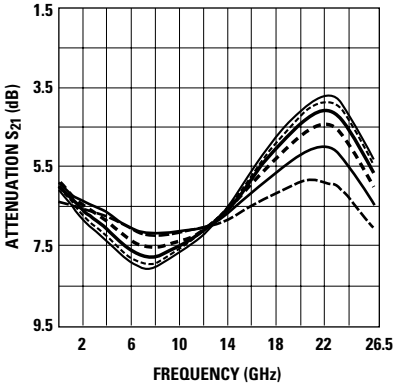


Figure 16. Attenuation vs. Temperature @ 5 dB Attenuation.[1].

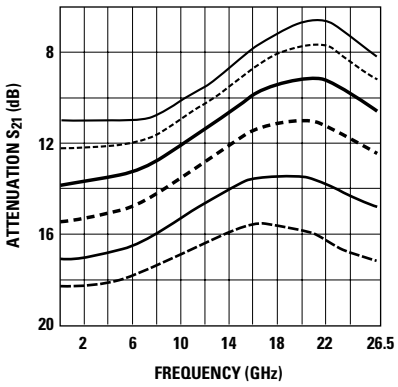


Figure 17. Attenuation vs. Temperature @ 10 dB Attenuation.[1].

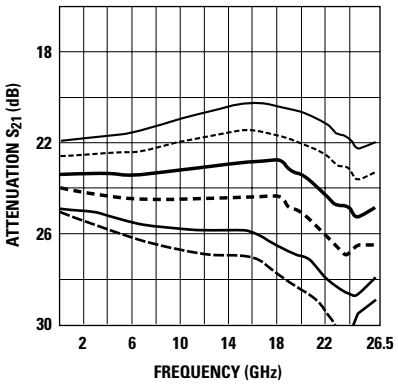


Figure 18. Attenuation vs. Temperature @ 20 dB Attenuation.[1].

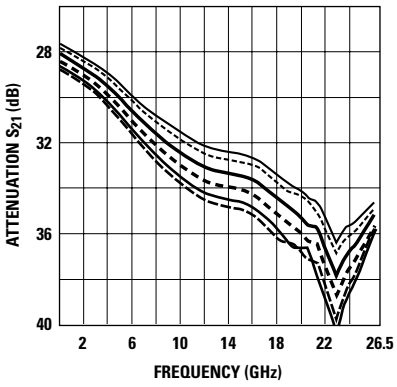


Figure 19. Attenuation vs. Temperature @ 30 dB Attenuation.[1].

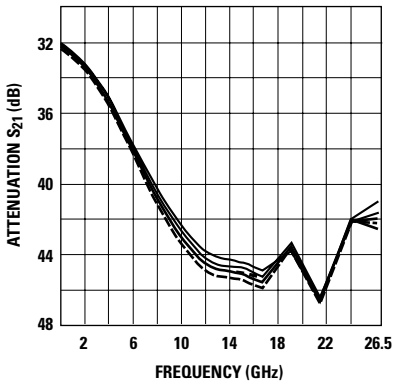


Figure 20. Attenuation vs. Temperature @ Max. Attenuation.[1].

Note:
1. Data taken with the device mounted in connectorized package.

Key for Temperature Settings:
- -55°C
- -25°C
- 0° C
- +25°C
- +55°C
- +85°C

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Avago Technologies' sales representative.

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

Obsoletes 5965-5452E
5988-1892EN April 3, 2006