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REALVIEW® VERSATILE FAMILY

DATA SHEET

The ARM® RealView® family of feature rich development boards provides an excellent environment for prototyping system-on-chip designs. Through a range of plug-in options, hardware and software applications can be developed and debugged.

The high performance Versatile family enhances the end-user experience for benchmarking and application development. It simplifies hardware and software development, which shortens time to market.

Logic Tiles are the basic building blocks for FPGA prototyping with ARM boards. Because of their flexible interconnect, Logic Tiles can be used to prototype complete systems on chip, but they are normally used to expand with custom AMBA peripherals the ARM subsystems provided on RealView Platform Baseboards and the RealView Emulation Baseboard.

This datasheet describes the Logic Tile for XC5VLX330 Xilinx Virtex-5 FPGA. Logic Tiles are based on a single FPGA to provide the highest flexibility in terms of the number of FPGAs in the system. The signals from the FPGA are routed to the upper and lower stacking headers, so that the design in the FPGA can communicate with the design on the baseboard or on extra Logic Tiles on top of it.

Logic Tile for XC5VLX330 FPGA

The Logic Tile for the Xilinx XC5VLX330 FPGA is implemented in a 65-nanometer process with wider Look-Up-Tables inputs (6-input LUTs), which reduce critical path delays, facilitating timing closure for ASIC prototyping. It has the same I/O interconnect as the Logic Tiles for the Xilinx Virtex-4 FPGA with a maximum clock frequency and capacity increase, making system partitioning easier. The Logic Tile for the Xilinx Virtex-5 FPGA also features an on-board 32MB ZBT SRAM.

Logic Tiles feature configurable switches, which allow flexible interconnect between boards without the need of cables. The clock architecture of Logic Tiles allows you to stack up to five of them together with minimal clock skew.

Most of the signals on the Logic Tile stacking connectors work at 3.3V, but one complete set of connectors have a configurable I/O voltage.

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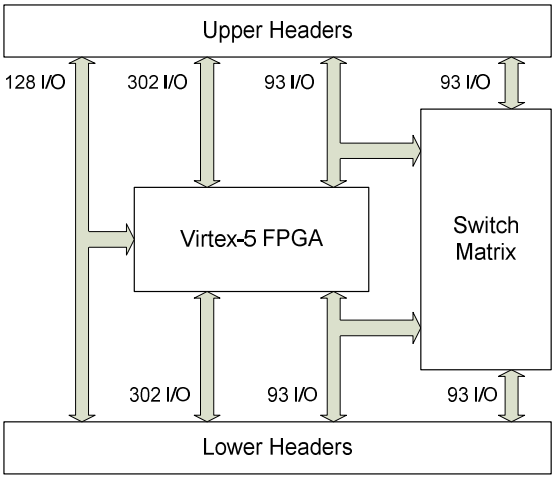
Specification

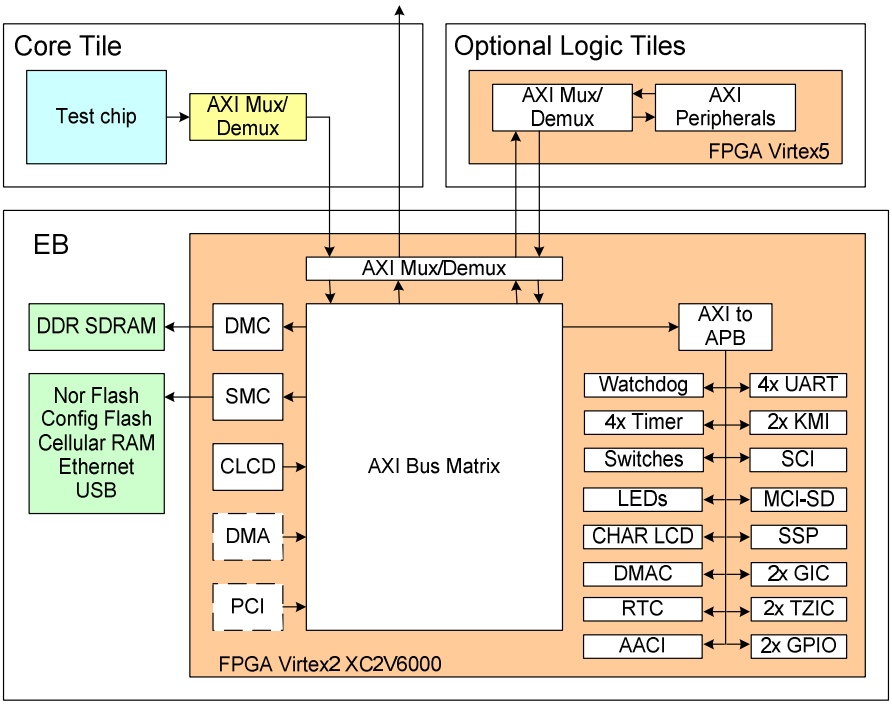
Logic Tile Features

- Virtex-5 XC5VLX330 FPGA
- 2 JTAG scan-chains for debug and FPGA programming
- Configuration Flash to store 2 FPGA images
- 8 User switches
- 8 User LEDs
- 3 programmable clock generators
- Push button
- Battery for FPGA encryption key
- On-board 32MB ZBT SRAM



Comparison with Virtex-4 Logic Tiles

Feature	LT-XC4VLX160 LT-XC4VLX200	LT-XC5VLX330
FPGA slices	68K / 89K	331K
Header I/O pins	918	918
External clock signals	21	21
ZBT SRAM	-	32MB
FPGA block RAM	0.65MB / 0.7MB	1.3MB
User LEDs and switches	8	8
Header I/O fold switches	Upper and lower	Upper and lower



Deliverables

- Documentation
- Example RTL and FPGA bit-files for a Logic Tile on top of a RealView Platform Baseboard or Emulation Baseboard
- Utility to reprogram the FPGA configuration Flash with RealView ICE or the USB debugger integrated on RealView baseboards

I/O signals on stacking connectors

The stacking connectors and I/O connections are a superset of the Virtex-II and Virtex-4 Logic Tiles.

Header	Top	Bottom
HDRX	144	144
HDRY	144	144
HDRZ	107	107
HDRZ through	128	

On-board switches can be configured to connect signals from the FPGA to these pins or to route signals straight through the board

Example system: Core Tile for ARM11 MPCore, Emulation Baseboard and Logic Tiles

Ordering Information

Part number	Description	Distributor
LT330-BD-0239A	Logic Tile for XC5VLX330	