

## N-Channel Enhancement-Mode Vertical DMOS FETs

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{iss}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### General Description

The Supertex VN2210 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

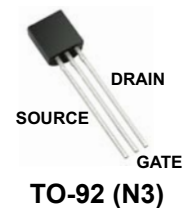
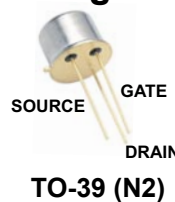
### Ordering Information

Device	Package Options		$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$I_{D(ON)}$ (min) (A)
	TO-39	TO-92			
VN2210	VN2210N2†	VN2210N3-G	100	0.35	8.0

-G indicates package is RoHS compliant ('Green')  
 † package is RoHS compliant ('Green')



### Pin Configurations



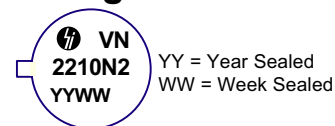
### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$+300^{\circ}C$

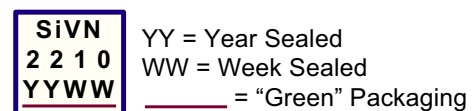
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Product Marking



Package may or may not include the following marks: Si or **TO-39 (N2)**



Package may or may not include the following marks: Si or **TO-92 (N3)**

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (A)	$I_D$ (pulsed) (A)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}$ <sup>†</sup> (A)	$I_{DRM}$ (A)
TO-39	1.7	10	6.0	21	125	1.7	10
TO-92	1.2	8.0	1.0	125	170	1.2	8.0

### Notes:

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

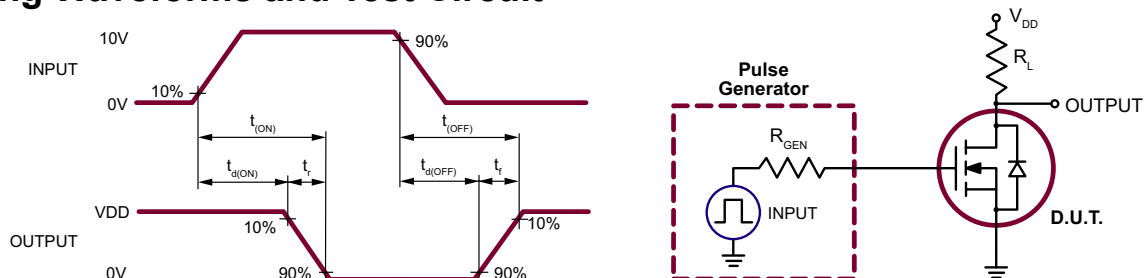
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	100	-	-	V	$V_{GS} = 0V, I_D = 10\text{mA}$
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.4	V	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-4.3	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$I_{GSS}$	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero gate voltage drain current	-	-	50	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
		-	-	10	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	3.0	4.5	-	A	$V_{GS} = 5.0V, V_{DS} = 25V$
		8.0	17	-		$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	0.4	0.5	$\Omega$	$V_{GS} = 5.0V, I_D = 1.0A$
		-	0.27	0.35		$V_{GS} = 10V, I_D = 4.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.85	1.2	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 4.0A$
$G_{FS}$	Forward transconductance	1200	-	-	mmho	$V_{DS} = 25V, I_D = 2.0A$
$C_{ISS}$	Input capacitance	-	300	500	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0\text{MHz}$
$C_{OSS}$	Common source output capacitance	-	125	200		
$C_{RSS}$	Reverse transfer capacitance	-	50	65		
$t_{d(ON)}$	Turn-on time	-	10	15	ns	$V_{DD} = 25V,$ $I_D = 2.0A,$ $R_{GEN} = 10\Omega$
$t_r$	Rise time	-	10	15		
$t_{d(OFF)}$	Turn-off time	-	50	65		
$t_f$	Fall time	-	30	50		
$V_{SD}$	Diode forward voltage drop	-	1.0	1.6	V	$V_{GS} = 0V, I_{SD} = 4.0A$
$t_{rr}$	Reverse recovery time	-	500	-	ns	$V_{GS} = 0V, I_{SD} = 1.0A$

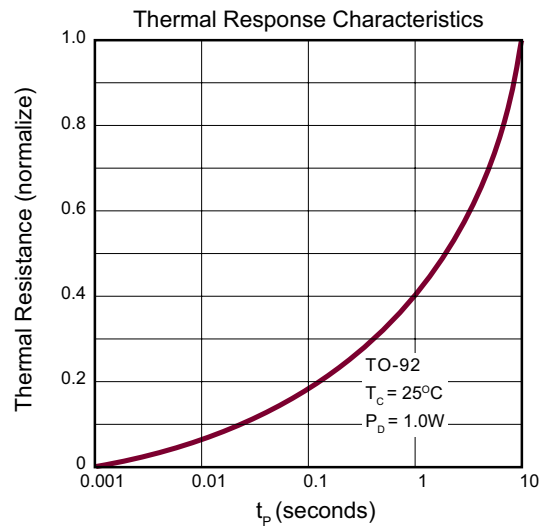
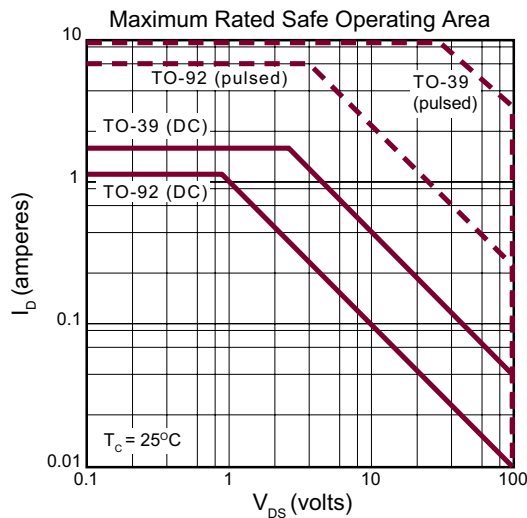
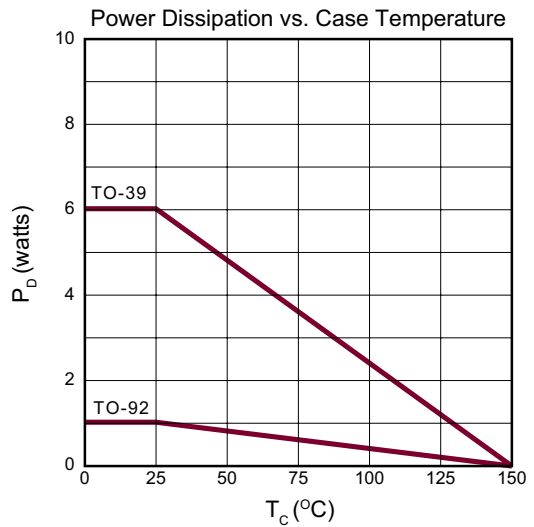
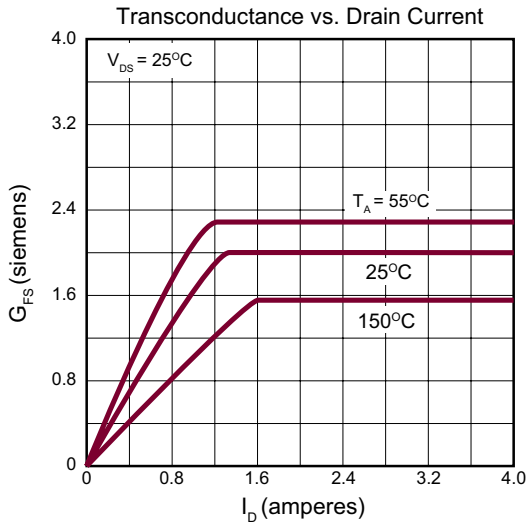
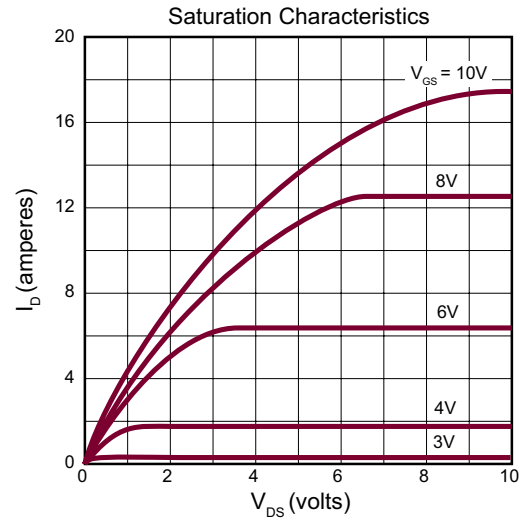
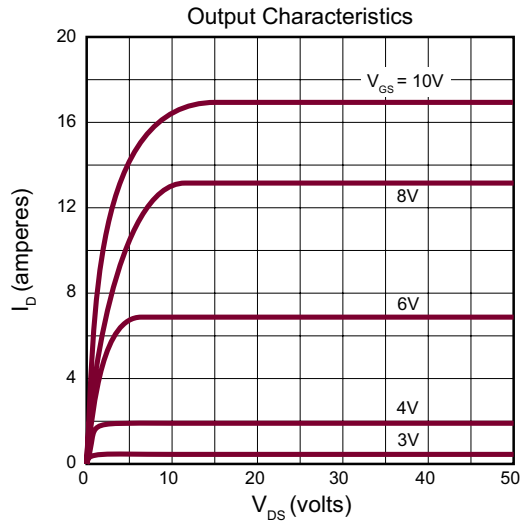
### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

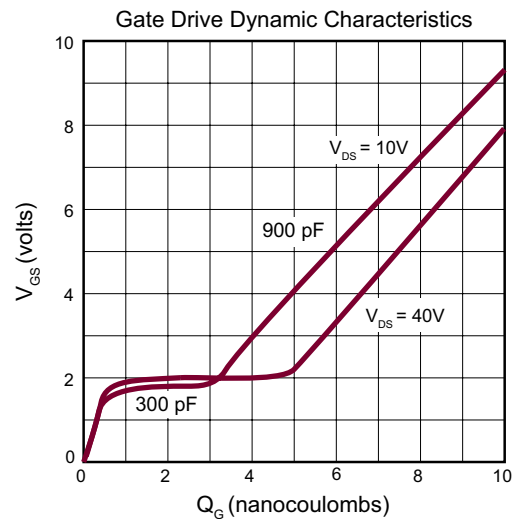
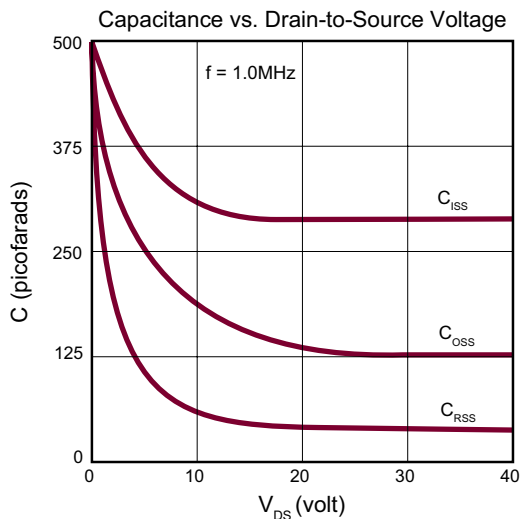
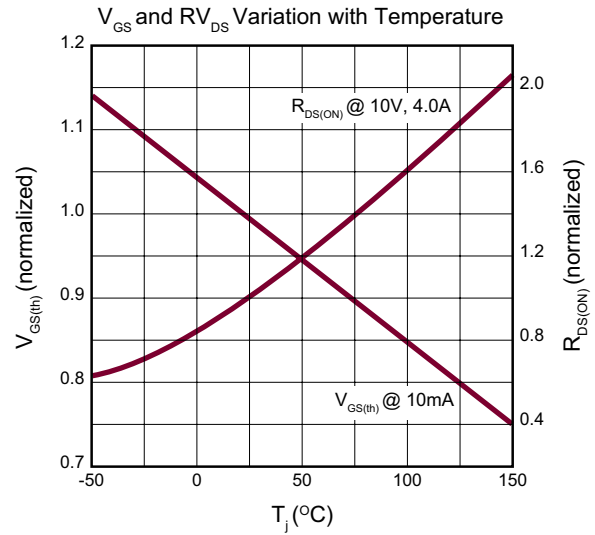
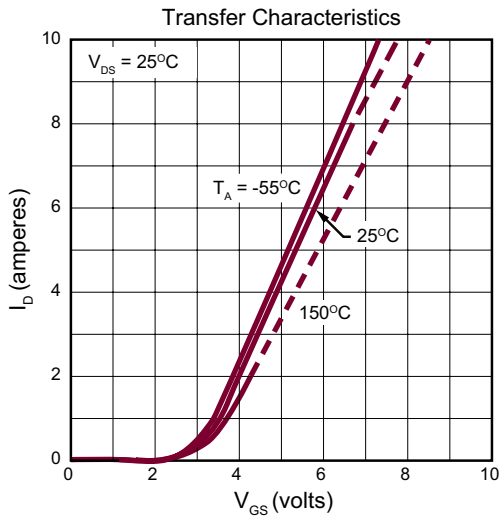
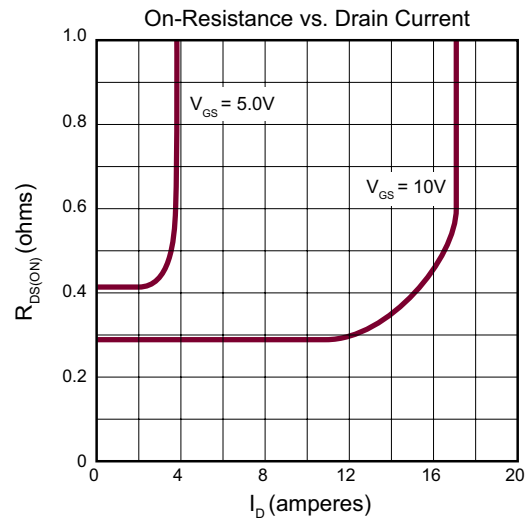
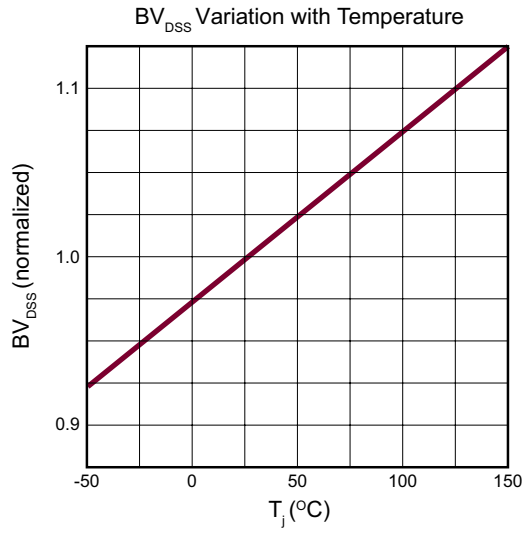
## Switching Waveforms and Test Circuit



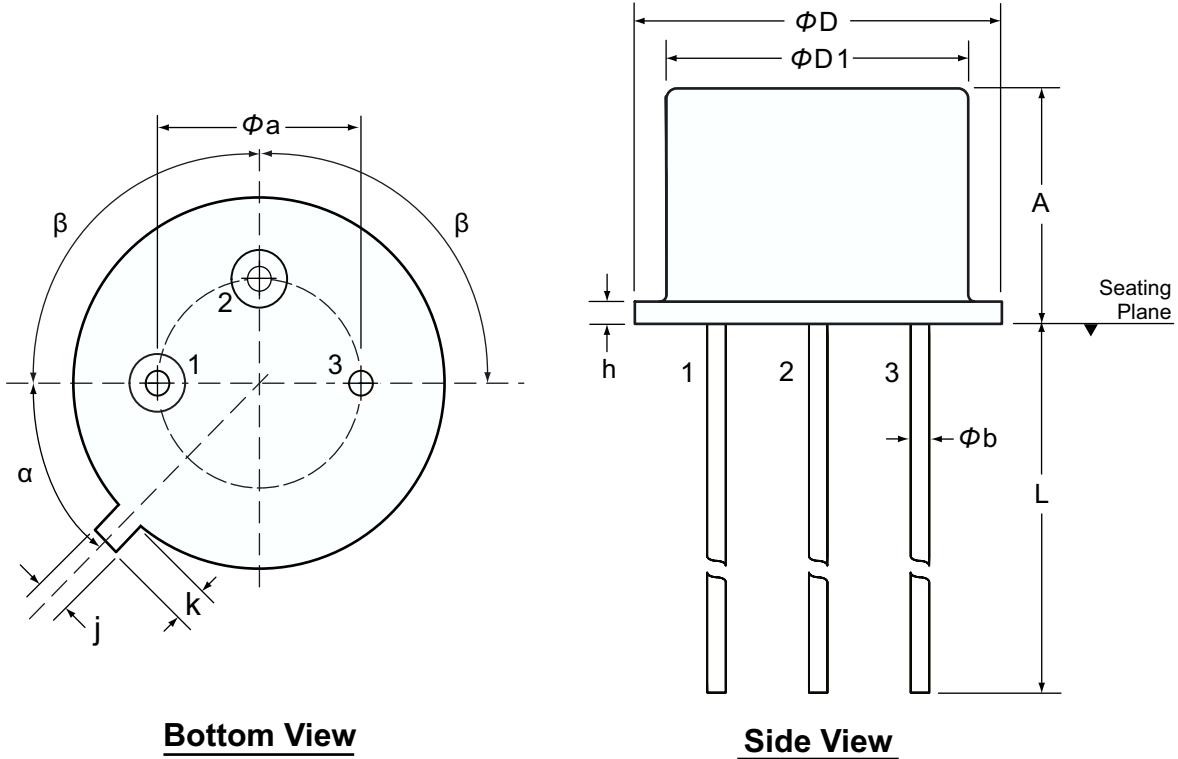
## Typical Performance Curves



Typical Performance Curves (cont.)



### 3-Lead TO-39 Package Outline (N2)



**Bottom View**

**Side View**

Symbol	$\alpha$	$\beta$	A	$\phi_a$	$\phi_b$	$\phi_D$	$\phi_{D1}$	h	j	k	L	
Dimension (inches)	MIN	45° NOM	90° NOM	.240	.190	.016	.350	.315	.009	.028	.029	.500
	NOM			-	-	-	-	-	-	-	-	-
	MAX			.260	.210	.021	.370	.335	.125	.034	.040	.560*

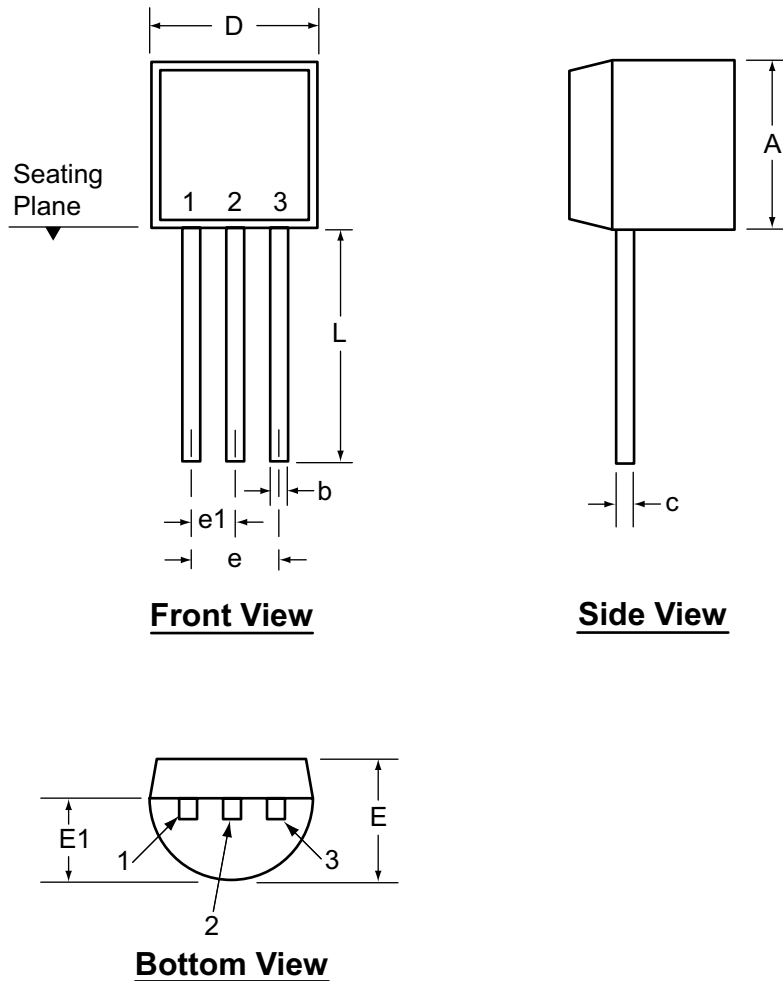
JEDEC Registration TO-39.

\* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO39N2, Version B052009.

### 3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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