

## N-Channel JFETs

**2N5484    SST5484**  
**2N5485    SST5485**  
**2N5486    SST5486**

<b>PRODUCT SUMMARY</b>				
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_{DSS}$ Min (mA)
2N/SST5484	-0.3 to -3	-25	3	1
2N/SST5485	-0.5 to -4	-25	3.5	4
2N/SST5486	-2 to -6	-25	4	8

### FEATURES

- Excellent High-Frequency Gain: Gps 13 dB (typ) @ 400 MHz – 5485/6
- Very Low Noise: 2.5 dB (typ) @ 400 MHz – 5485/6
- Very Low Distortion
- High AC/DC Switch Off-Isolation

### BENEFITS

- Wideband High Gain
- Very High System Sensitivity
- High Quality of Amplification
- High-Speed Switching Capability
- High Low-Level Signal Amplification

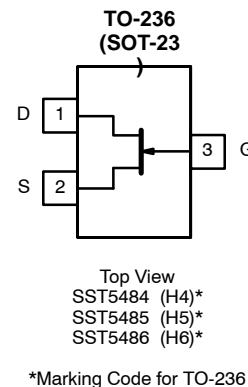
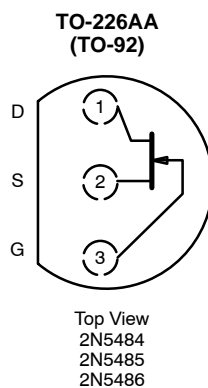
### APPLICATIONS

- High-Frequency Amplifier/Mixer
- Oscillator
- Sample-and-Hold
- Very Low Capacitance Switches

### DESCRIPTION

The 2N/SST5484 series consists of n-channel JFETs designed to provide high-performance amplification, especially at high frequencies up to and beyond 400 MHz.

The 2N series, TO-226AA (TO-92), and SST series, TO-236 (SOT-23), packages provide low-cost options and are available with tape-and-reel to support automated assembly (see Packaging Information).



For applications information see AN102 and AN105.



### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage ..... -25 V  
 Gate Current ..... 10 mA  
 Lead Temperature ..... 300°C  
 Storage Temperature ..... -65 to 150°C

Operating Junction Temperature ..... -55 to 150°C  
 Power Dissipation<sup>a</sup> ..... 350 mW

Notes

a. Derate 2.8 mW/°C above 25°C

SPECIFICATIONS FOR 2N SERIES (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ <sup>a</sup>	Limits						Unit
				2N5484		2N5485		2N5486		
				Min	Max	Min	Max	Min	Max	
<b>Static</b>										
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 nA		-0.3	-3	-0.5	-4	-2	-6	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V		1	5	4	10	8	20	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	-0.002		-1		-1		-1	nA
		T <sub>A</sub> = 100°C	-0.2		-200		-200		-200	
Gate Operating Current <sup>c</sup>	I <sub>G</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 1 mA	-20							μA
Gate-Source Forward Voltage <sup>c</sup>	V <sub>GS(F)</sub>	I <sub>G</sub> = 10 mA, V <sub>DS</sub> = 0 V	0.8							V
<b>Dynamic</b>										
Common-Source Forward Transconductance <sup>NO TAG</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V f = 1 kHz		3	6	3.5	7	4	8	mS
Common-Source Output Conductance <sup>NO TAG</sup>	g <sub>os</sub>				50		60		75	μS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V f = 1 MHz	2.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>		0.7		1		1		1	
Common-Source Output Capacitance	C <sub>oss</sub>		1		2		2		2	
Equivalent Input Noise Voltage <sup>c</sup>	e <sub>n</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V f = 100 Hz	10							nV/ √Hz
<b>High-Frequency</b>										
Common-Source Transconductance <sup>d</sup>	Y <sub>fs(RE)</sub>	V <sub>DS</sub> = 15 V V <sub>GS</sub> = 0 V	f = 100 MHz	5.5	2.5					mS
			f = 400 MHz	5.5		3		3.5		
Common-Source Output Conductance <sup>d</sup>	Y <sub>os(RE)</sub>		f = 100 MHz	45		75				μS
			f = 400 MHz	65		100		100		
Common-Source Input Conductance <sup>d</sup>	Y <sub>is(RE)</sub>		f = 100 MHz	0.05		0.1				mS
			f = 400 MHz	0.8				1	1	
Common-Source Power Gain <sup>d</sup>	G <sub>ps</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA f = 100 MHz	20	16	25					dB
		V <sub>DS</sub> = 15 V I <sub>D</sub> = 4 mA	f = 100 MHz	21		18	30	18	30	
			f = 400 MHz	13		10	20	10	20	
Noise Figure <sup>d</sup>	NF	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V R <sub>G</sub> = 1 MΩ, f = 1 kHz	0.3		2.5		2.5		2.5	dB
		V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA R <sub>G</sub> = 1 kΩ, f = 100 MHz	2		3					
			V <sub>DS</sub> = 15 V I <sub>D</sub> = 4 mA R <sub>G</sub> = 1 kΩ	f = 100 MHz	1		2		2	
				f = 400 MHz	2.5		4		4	



**SPECIFICATIONS FOR SST SERIES (T<sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Conditions	Typ <sup>b</sup>	Limits						Unit
				SST5484		SST5485		SST5486		
				Min	Max	Min	Max	Min	Max	
<b>Static</b>										
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 nA		-0.3	-3	-0.5	-4	-2	-6	
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V		1	5	4	10	8	20	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	-0.002		-1		-1		-1	nA
		T <sub>A</sub> = 100 °C	-0.2		-200		-200		-200	nA
Gate Operating Current <sup>c</sup>	I <sub>G</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 1 mA	-20							pA
Gate-Source Forward Voltage <sup>c</sup>	V <sub>GS(F)</sub>	I <sub>G</sub> = 10 mA, V <sub>DS</sub> = 0 V	0.8							V
<b>Dynamic</b>										
Common-Source Forward Transconductance <sup>NO TAG</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V f = 1 kHz		3	6	3.5	7	4	8	mS
Common-Source Output Conductance <sup>NO TAG</sup>	g <sub>os</sub>				50		60		75	μS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V f = 1 MHz	2.2							pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>		0.7							
Common-Source Output Capacitance	C <sub>oss</sub>		1							
Equivalent Input Noise Voltage <sup>c</sup>	e <sub>n</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V f = 100 Hz	10							nV/ √Hz
<b>High-Frequency</b>										
Common-Source Transconductance	Y <sub>fs</sub>	V <sub>DS</sub> = 15 V V <sub>GS</sub> = 0 V	f = 100 MHz	5.5						mS
			f = 400 MHz	5.5						
Common-Source Output Conductance	Y <sub>os</sub>		f = 100 MHz	45						μS
			f = 400 MHz	65						
Common-Source Input Conductance	Y <sub>is</sub>		f = 100 MHz	0.05						mS
			f = 400 MHz	0.8						
Common-Source Power Gain	G <sub>ps</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA f = 100 MHz	20							dB
		V <sub>DS</sub> = 15 V I <sub>D</sub> = 4 mA	f = 100 MHz	21						
			f = 400 MHz	13						
Noise Figure	NF	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V R <sub>G</sub> = 1 MΩ, f = 1 kHz	0.3							dB
		V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 mA R <sub>G</sub> = 1 kΩ, f = 100 MHz	2							
		V <sub>DS</sub> = 15 V I <sub>D</sub> = 4 mA R <sub>G</sub> = 1 kΩ	f = 100 MHz	1						
			f = 400 MHz	2.5						

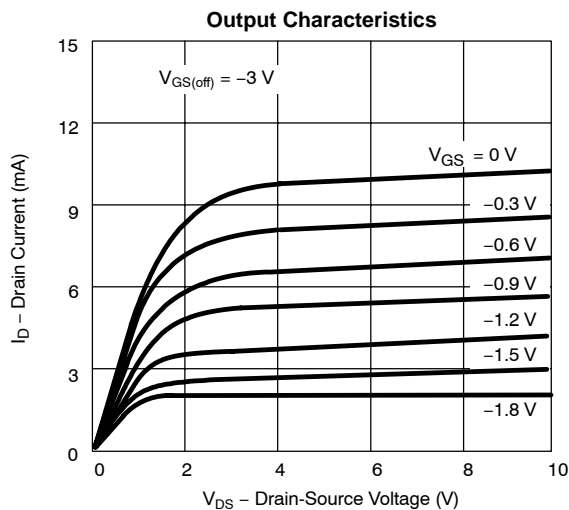
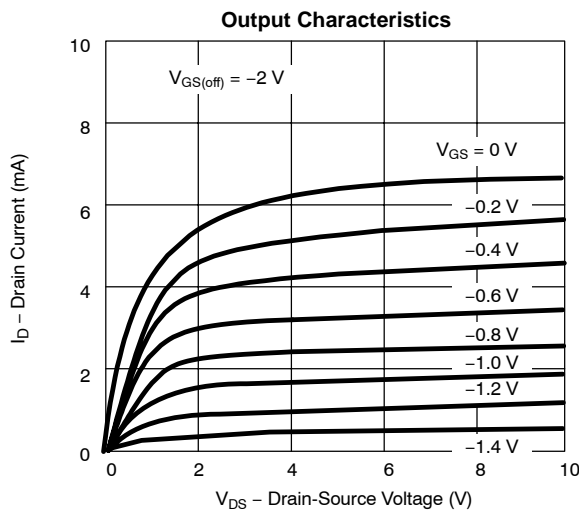
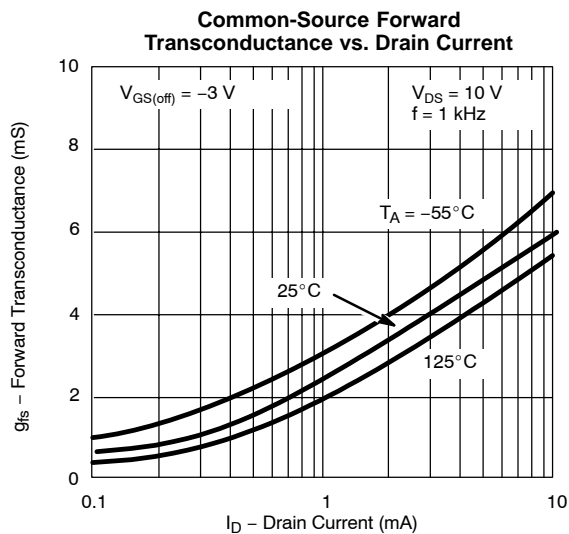
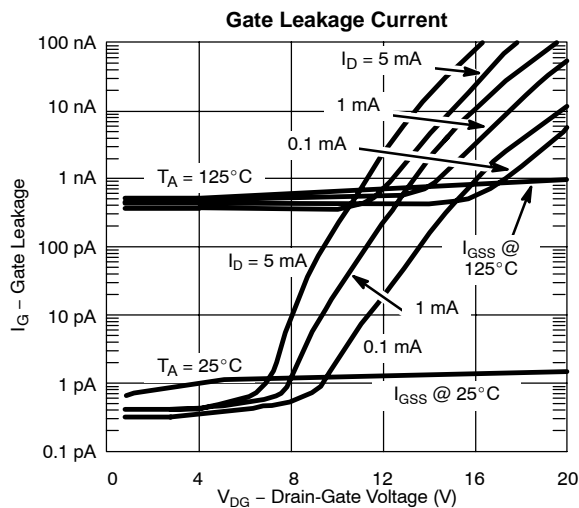
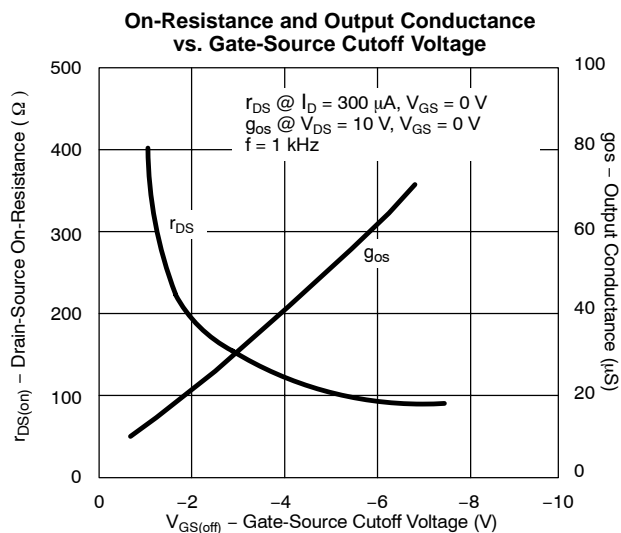
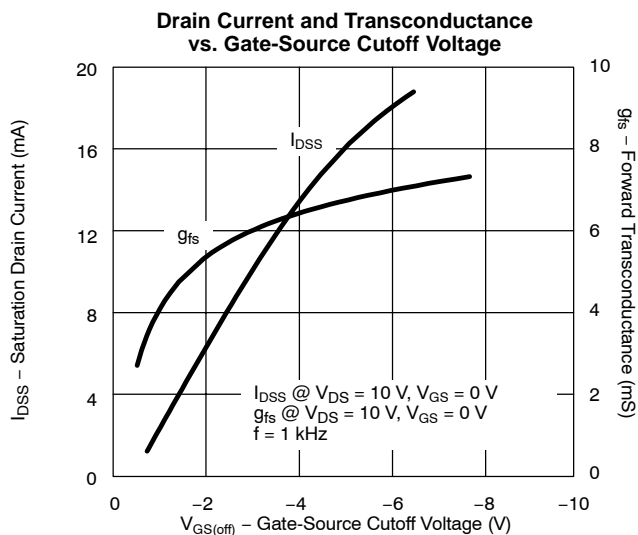
Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
- c. This parameter not registered with JEDEC.
- d. Not a production test.

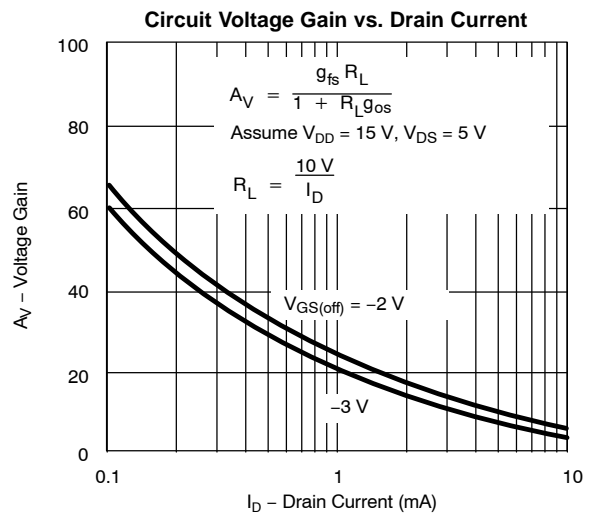
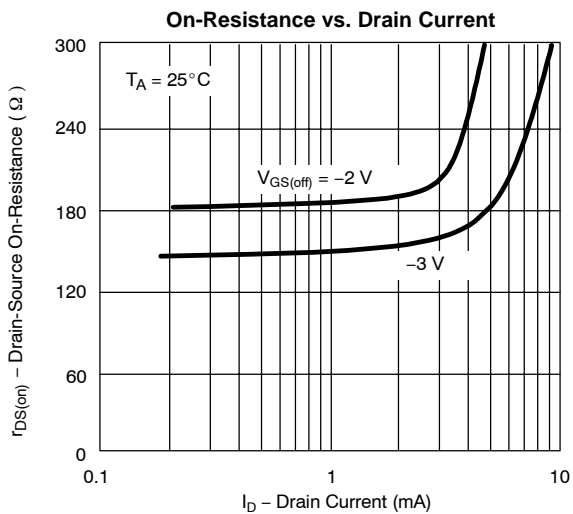
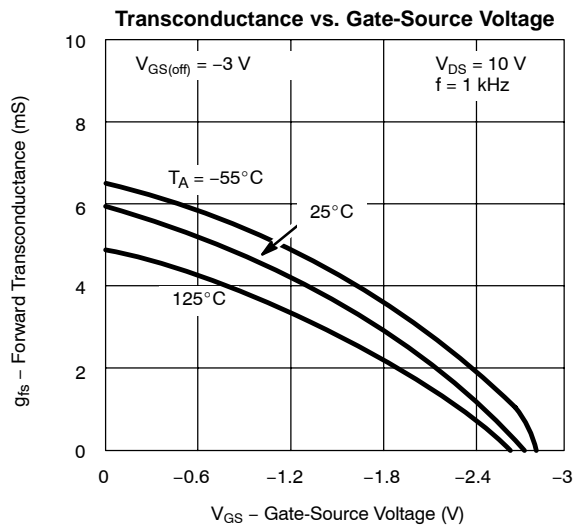
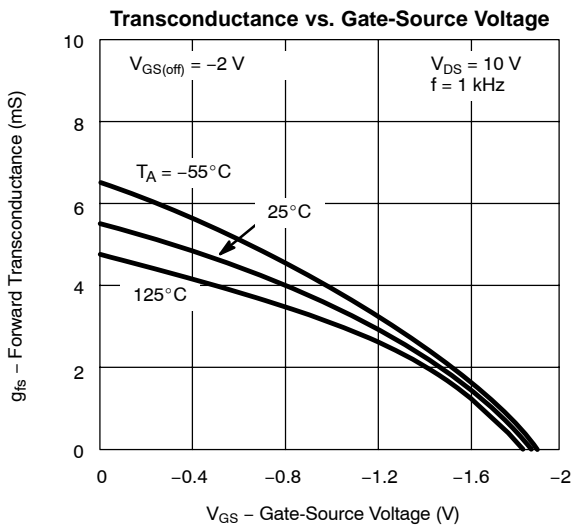
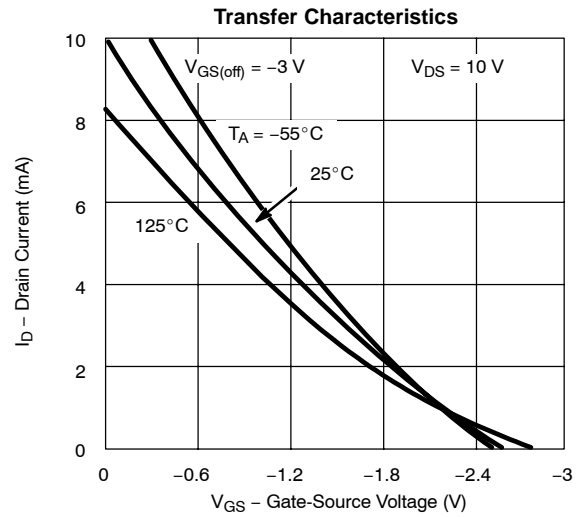
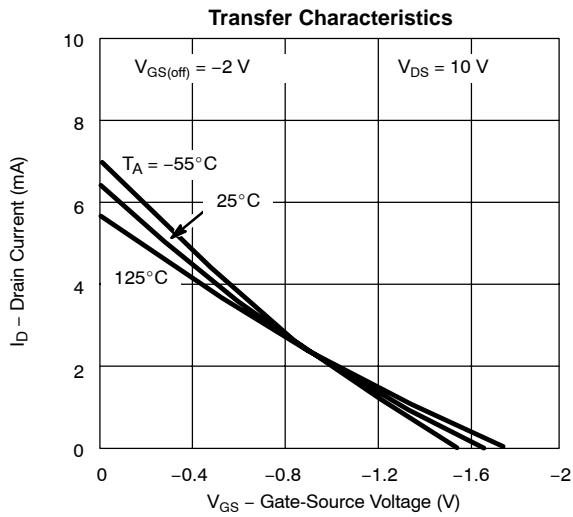
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Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

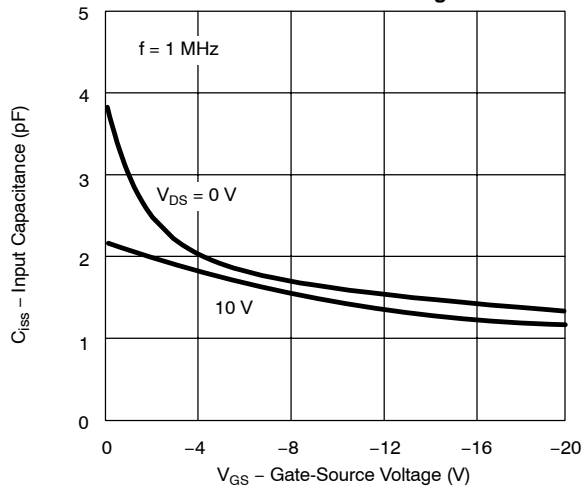


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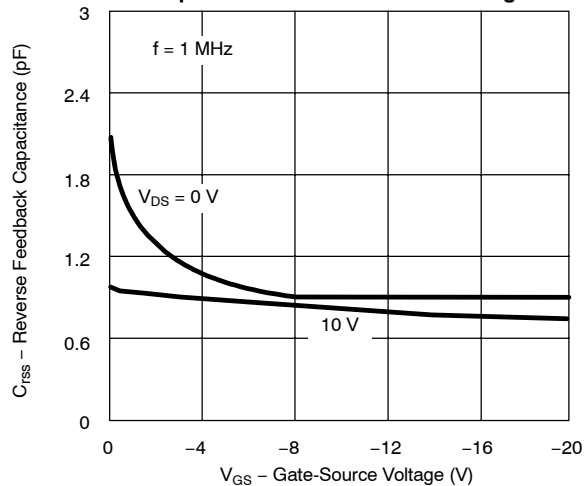


**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

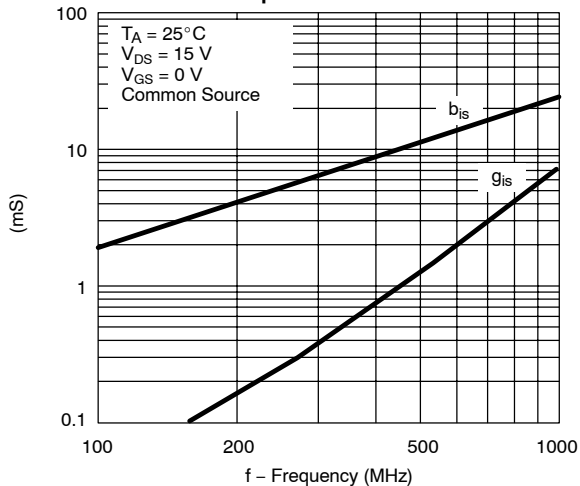
**Common-Source Input Capacitance vs. Gate-Source Voltage**



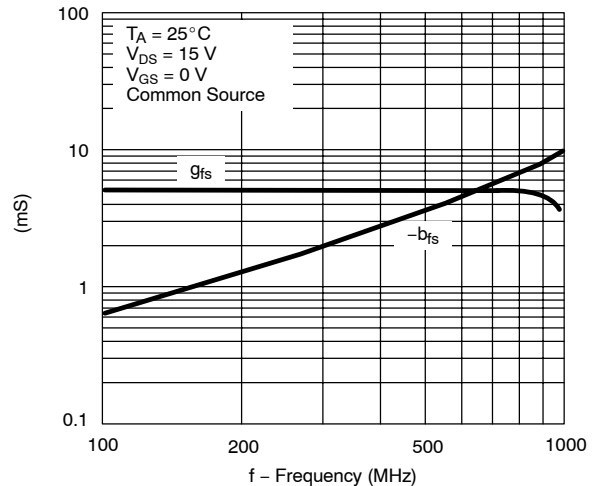
**Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage**



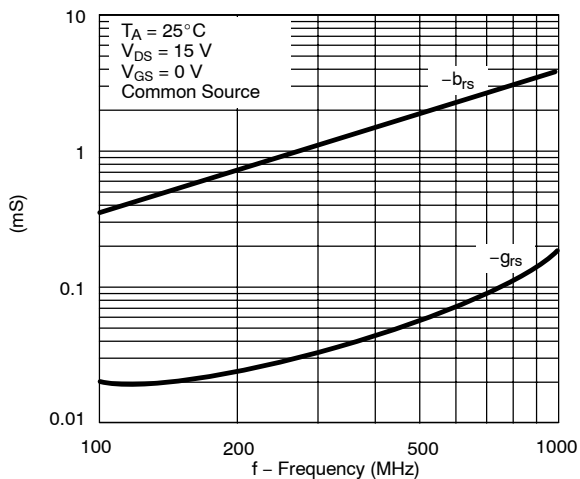
**Input Admittance**



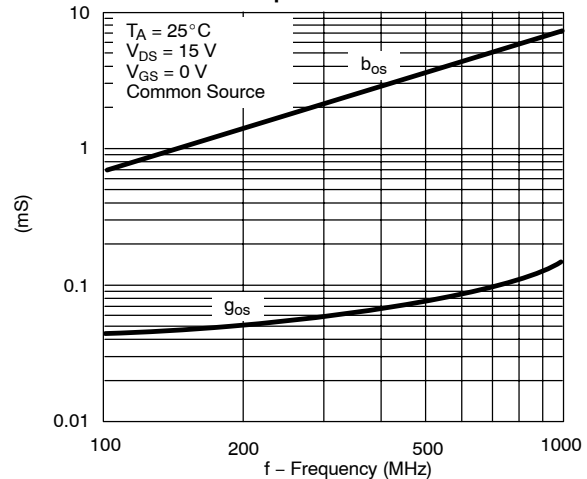
**Forward Admittance**



**Reverse Admittance**

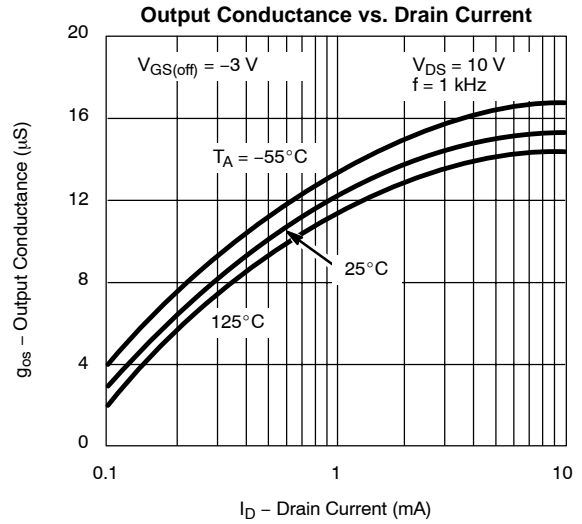
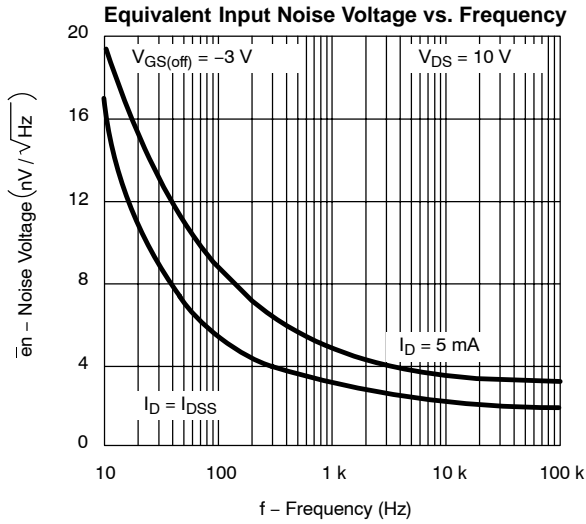


**Output Admittance**





**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70246>.



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