

N-Channel JFETs

J111 SST111
J112 SST112
J113 SST113

PRODUCT SUMMARY				
Part Number	V _{GS(off)} (V)	r _{DS(on)} Max (Ω)	I _{D(off)} Typ (pA)	t _{ON} Typ (ns)
J/SST111	-3 to -10	30	5	4
J/SST112	-1 to -5	50	5	4
J/SST113	≤ -3	100	5	4

FEATURES

- Low On-Resistance: 111 < 30 Ω
- Fast Switching—t_{ON}: 4 ns
- Low Leakage: 5 pA
- Low Capacitance: 3 pF
- Low Insertion Loss

BENEFITS

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error,” Excellent Accuracy
- Good Frequency Response, Low Glitches
- Eliminates Additional Buffering

APPLICATIONS

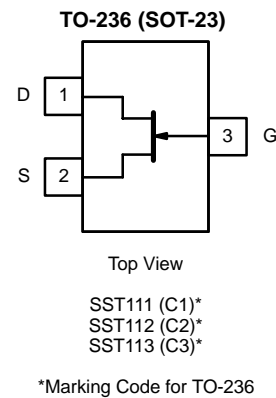
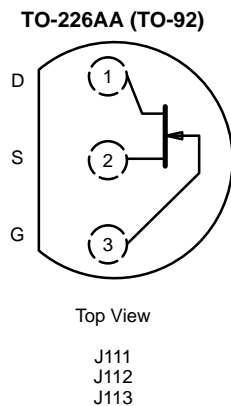
- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters

DESCRIPTION

The J/SST111 series consists of all-purpose analog switches designed to support a wide range of applications. The J/SST113 are useful in a high-gain amplifier mode.

For similar products in TO-206AA(TO-18) packaging, see the 2N/PN/SST4391 series, 2N4856A/4857A/4858A, and 2N5564/5565/5566 (duals) data sheets.

The J series, TO-226AA (TO-92) plastic package, provides low cost, while the SST series, TO236 (SOT-23) package, provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information).



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-35 V
Gate Current	50 mA
Lead Temperature (1/16" from case for 10 seconds)	300 °C
Storage Temperature	-55 to 150 °C
Operating Junction Temperature	-55 to 150 °C

Power Dissipation ^a	
(TO-236)	350 mW
(TO-226AA)	360 mW

Notes
a. Derate 2.8 mW/°C above 25 °C

For applications information see AN105.



SPECIFICATIONS (T _A = 25 °C UNLESS OTHERWISE NOTED)										
Parameter	Symbol	Test Conditions	Typ ^a	Limits						Unit
				J/SST111		J/SST112		J/SST113		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 5 V, I _D = 1 μA		-3	-10	-1	-5		-3	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 15 V, V _{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I _{GSS}	V _{GS} = -15 V, V _{DS} = 0 V	-0.005		-1		-1		-1	nA
		T _A = 125 °C	-3							
Gate Operating Current	I _G	V _{DG} = 15 V, I _D = 10 mA	-5							pA
Drain Cutoff Current	I _{D(off)}	V _{DS} = 5 V, V _{GS} = -10 V	0.005		1		1		1	nA
		T _A = 125 °C	3							
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, V _{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V	0.7							V
Dynamic										
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 20 V, I _D = 1 mA f = 1 kHz	6							mS
Common-Source Output Conductance	g _{os}		25							μS
Drain-Source On-Resistance	r _{ds(on)}	V _{GS} = 0 V, I _D = 0 mA f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C _{iss}	V _{DS} = 0 V, V _{GS} = -10 V f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		3		5		5		5	
Equivalent Input Noise Voltage	e _n	V _{DG} = 10 V, I _D = 1 mA f = 1 kHz	3							nV/ √Hz
Switching										
Turn-On Time	t _{d(on)}	V _{DD} = 10 V, V _{GS(H)} = 0 V See Switching Circuit	2							ns
	t _r		2							
Turn-Off Time	t _{d(off)}		6							
	t _f		15							

Notes

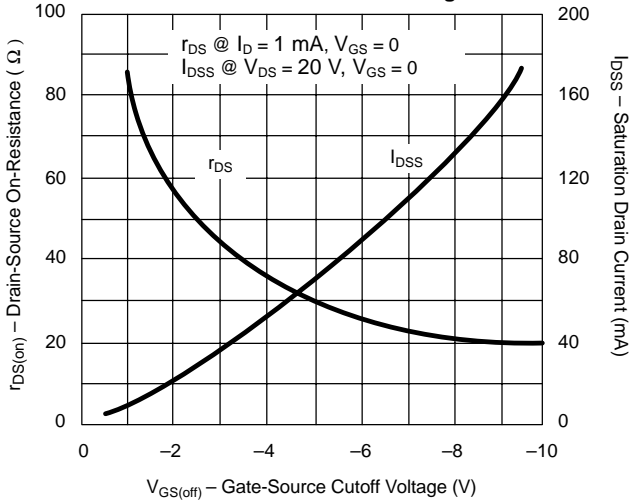
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

NCB

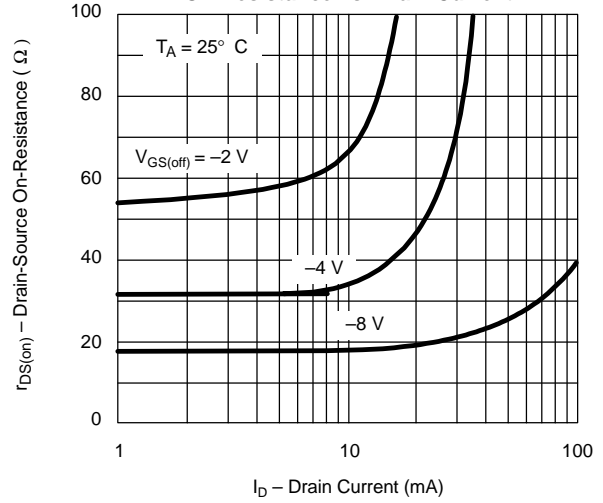


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

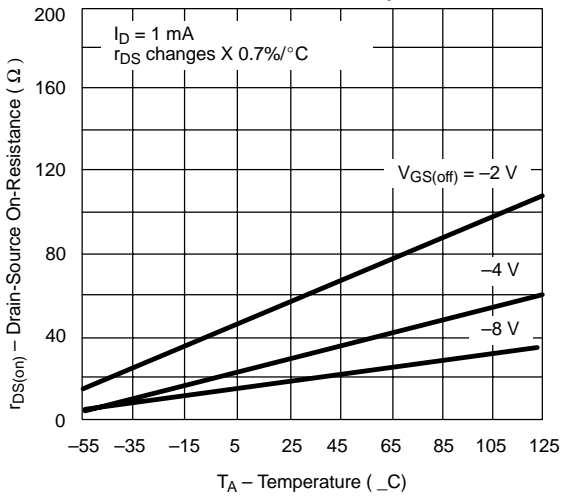
On-Resistance and Drain Current vs. Gate-Source Cutoff Voltage



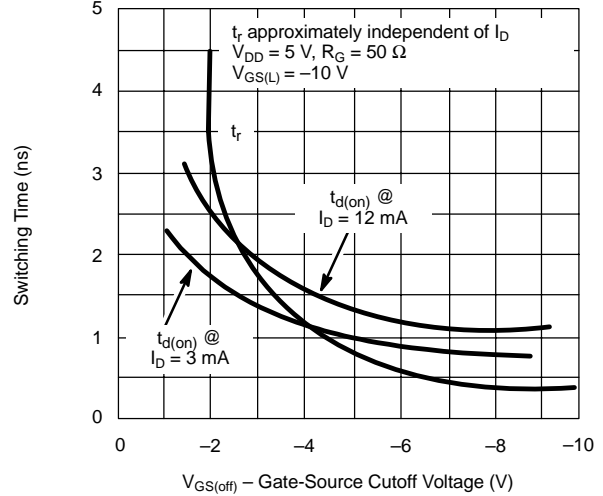
On-Resistance vs. Drain Current



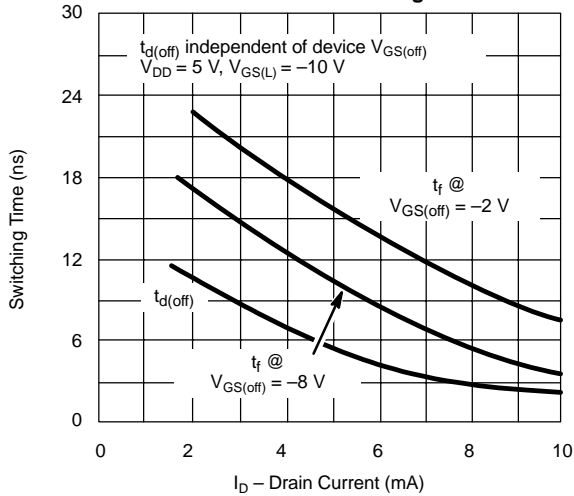
On-Resistance vs. Temperature



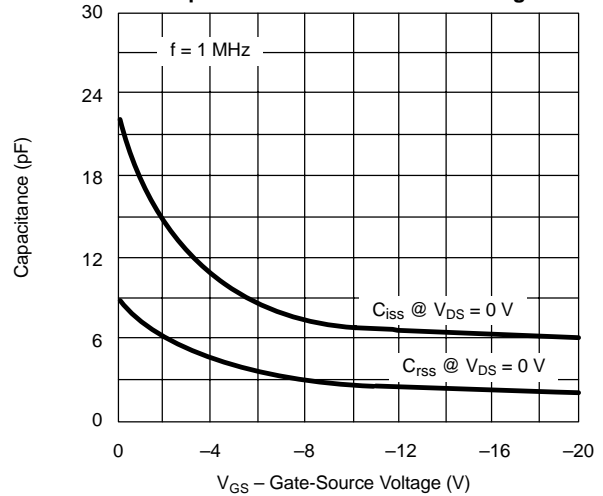
Turn-On Switching



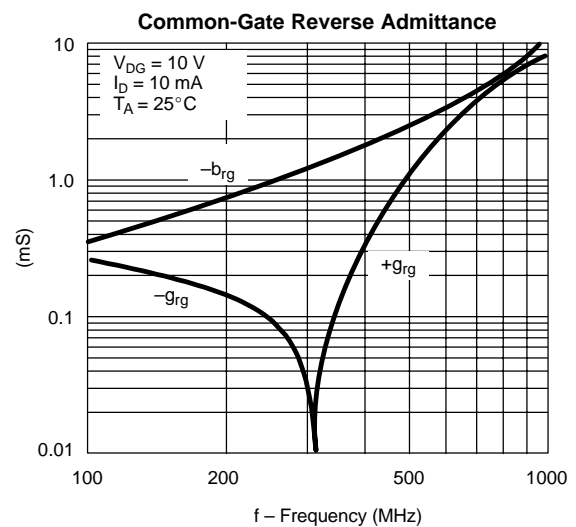
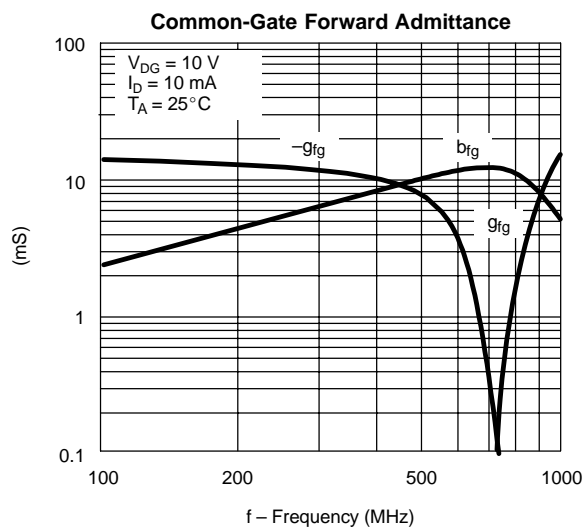
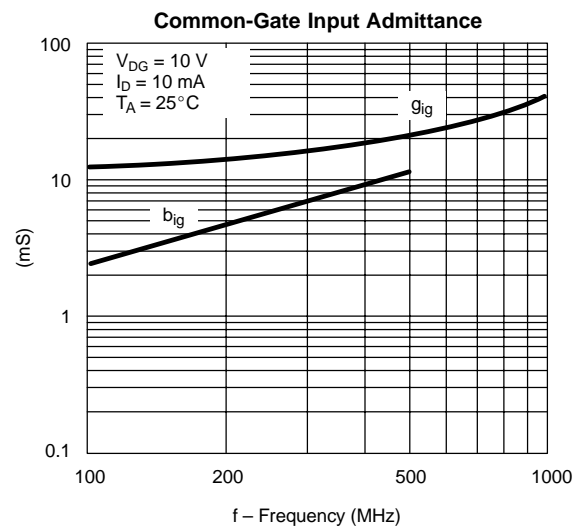
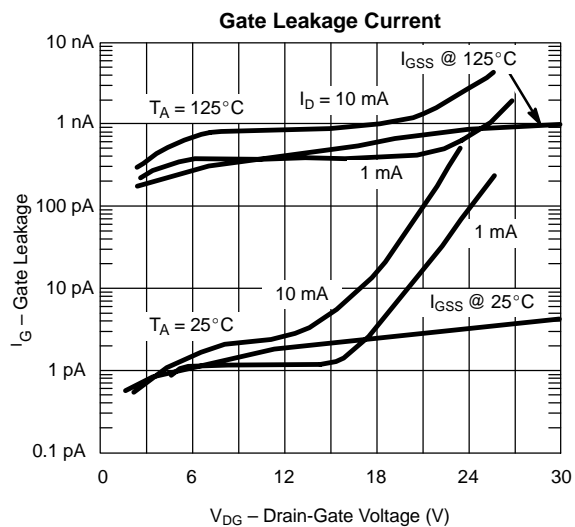
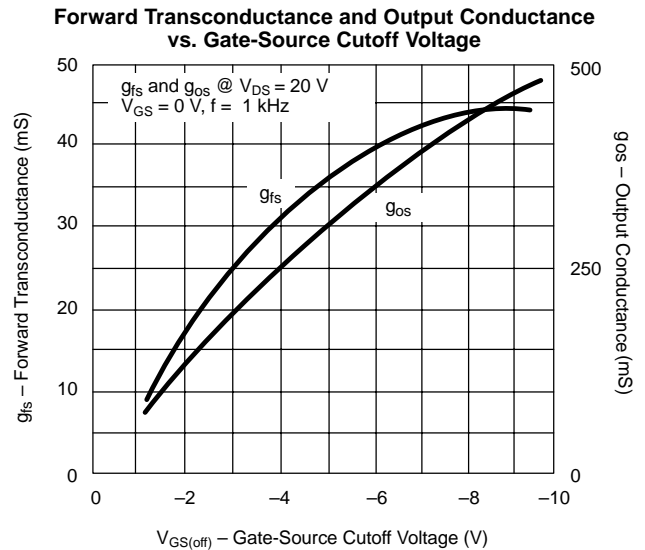
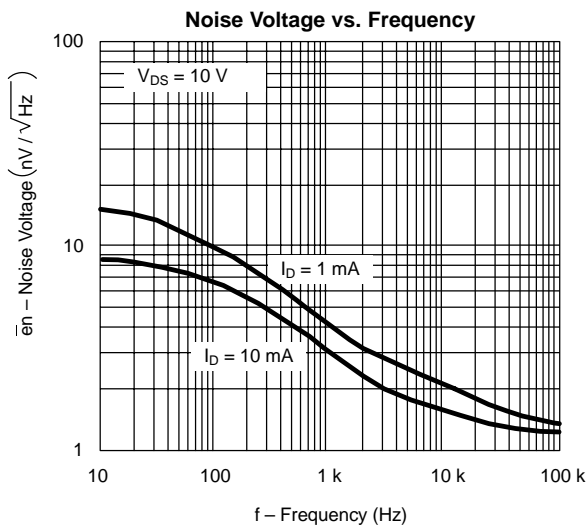
Turn-Off Switching



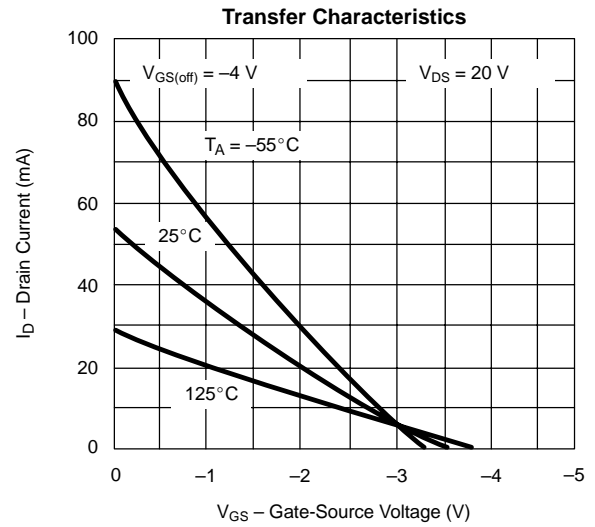
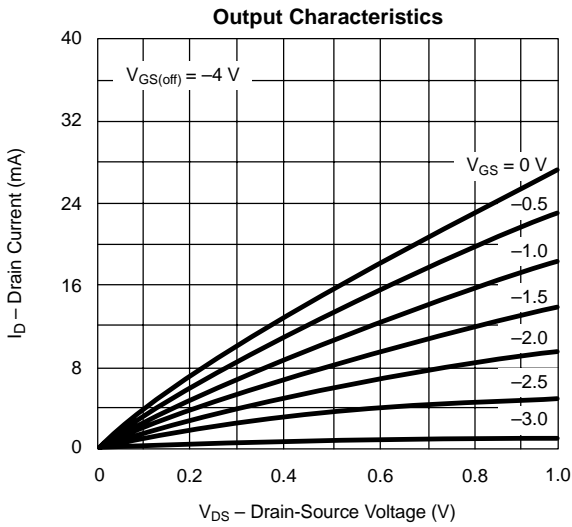
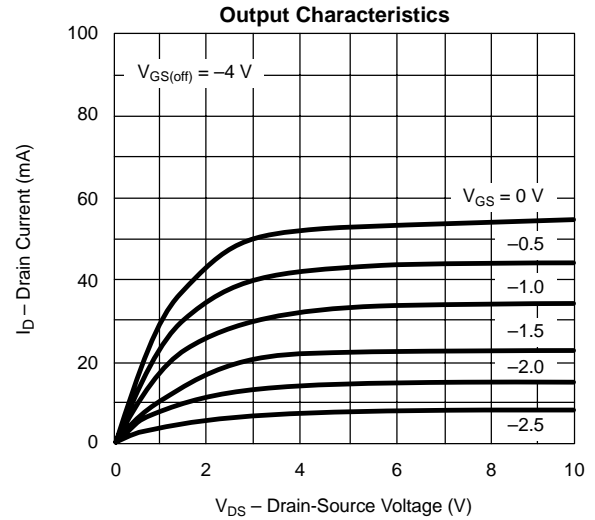
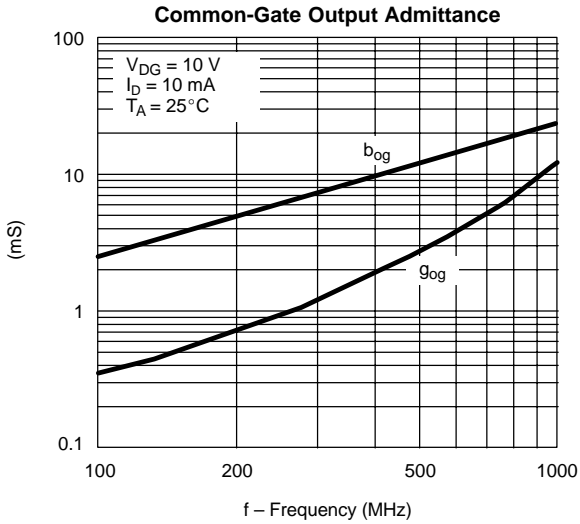
Capacitance vs. Gate-Source Voltage



TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



SWITCHING TIME TEST CIRCUIT			
	J/SST111	J/SST112	J/SST113
$V_{GS(L)}$	-12 V	-7 V	-5 V
R_L^*	800 Ω	1600 Ω	3200 Ω
$I_{D(on)}$	12 mA	6 mA	3 mA

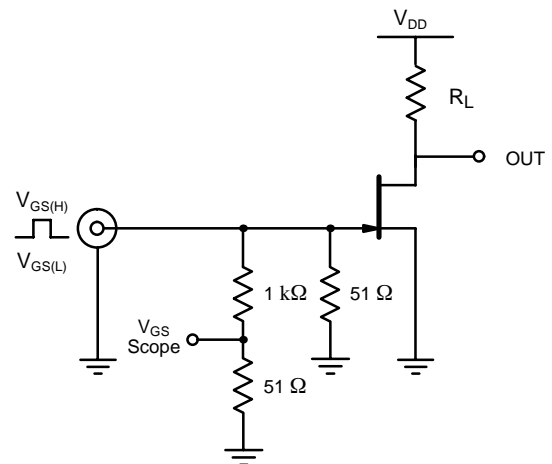
*Non-inductive

INPUT PULSE

Rise Time < 1 ns
 Fall Time < 1 ns
 Pulse Width 100 ns
 PRF 1 MHz

SAMPLING SCOPE

Rise Time 0.4 ns
 Input Resistance 10 M Ω
 Input Capacitance 1.5 pF





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