

## Matched N-Channel JFET Pairs

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
U440	-1 to -6	-25	4.5	-1	10
U441	-1 to -6	-25	4.5	-1	20

### FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 85 dB.

### BENEFITS

- Minimum Parasitics Ensuring Maximum High-Frequency Performance
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

### APPLICATIONS

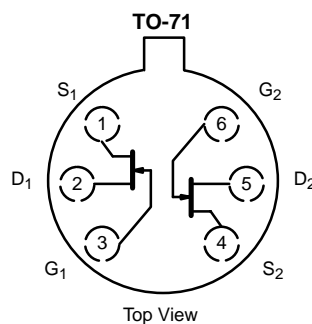
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

### DESCRIPTION

The U440/441 are matched pairs of JFETs mounted in a single TO-71 package. This two-chip design reduces parasitics and gives better performance at very high frequencies while ensuring extremely tight matching. These devices are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

The hermetically-sealed TO-71 package is available with full military screening per MIL-S-19500 (see Military Information).

For similar products in SO-8 packaging see the SST440/SST441 data sheet. For low-noise options, see the SST/U401 series data sheet. For low-leakage alternatives, see the U421/423 data sheet.



### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-25 V
Gate-Gate Voltage	±50 V
Gate Current	50 mA
Lead Temperature ( $1/16$ " from case for 10 sec.)	300°C
Storage Temperature	-65 to 200°C

Operating Junction Temperature	-55 to 150°C
Power Dissipation :	Per Side <sup>a</sup> 250 mW
	Total <sup>b</sup> 500 mW

#### Notes

- Derate 2 mW/°C above 25°C
- Derate 4 mW/°C above 25°C



SPECIFICATIONS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Typ <sup>a</sup>	Limits				Unit
				U440		U441		
				Min	Max	Min	Max	
<b>Static</b>								
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA	-3.5	-1	-6	-1	-6	V
Saturation Drain Current <sup>b</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0 V						pA
			T <sub>A</sub> = 125 °C	-2				
Gate Operating Current	I <sub>G</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA						pA
			T <sub>A</sub> = 125 °C	-0.3				
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = 1 mA, V <sub>DS</sub> = 0 V	0.7					V
<b>Dynamic</b>								
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g <sub>os</sub>		70		200		200	μS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 1 MHz	3					pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>		1					
Equivalent Input Noise Voltage	$\bar{e}_n$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 10 kHz	4					nV/ √Hz
<b>Matching</b>								
Differential Gate-Source Voltage	V <sub>GS1</sub> - V <sub>GS2</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA	6		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA T <sub>A</sub> = -55 to 125 °C	20					μV/°C
Saturation Drain Current Ratio <sup>c</sup>	$\frac{I_{DSS1}}{I_{DSS2}}$	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V	0.97					
Transconductance Ratio <sup>c</sup>	$\frac{g_{fs1}}{g_{fs2}}$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 mA f = 1 kHz	0.97					
Common Mode Rejection Ratio	CMRR	V <sub>DG</sub> = 5 to 10 V, I <sub>D</sub> = 5 mA	85					dB

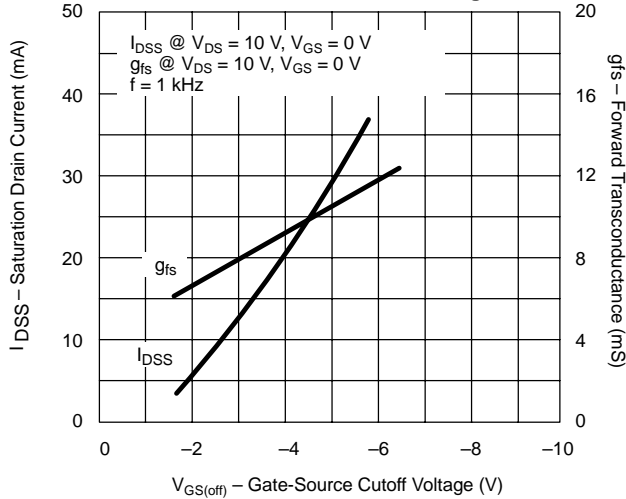
## Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.  
c. Assumes smaller value in the numerator.

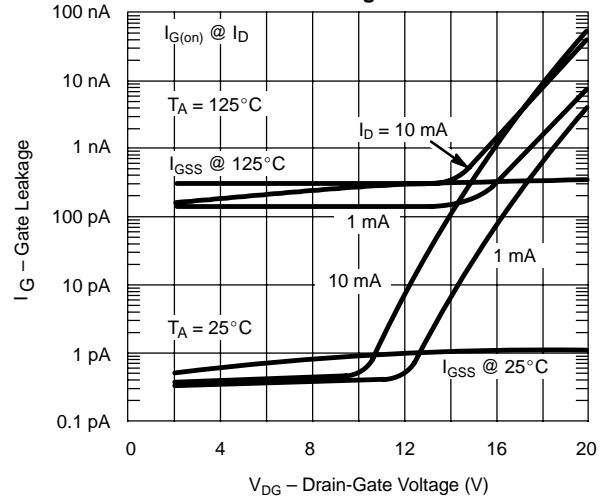
NZFD

**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

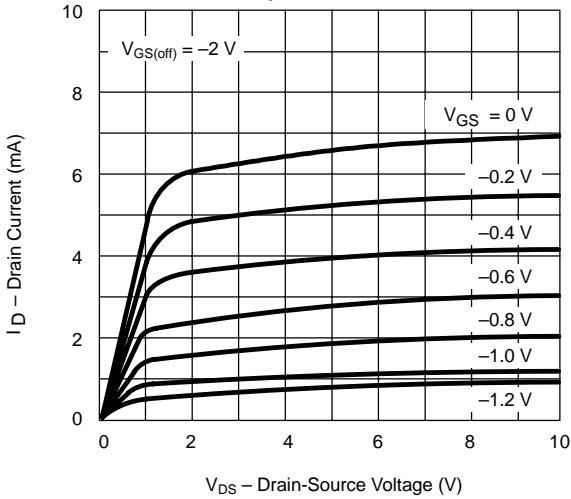
**Drain Current and Transconductance vs. Gate-Source Cutoff Voltage**



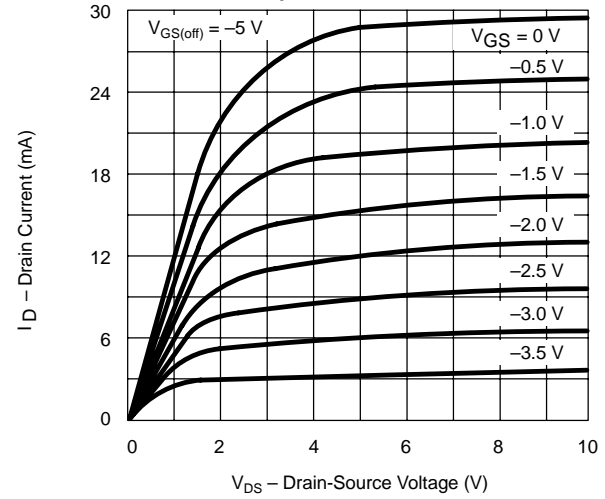
**Gate Leakage Current**



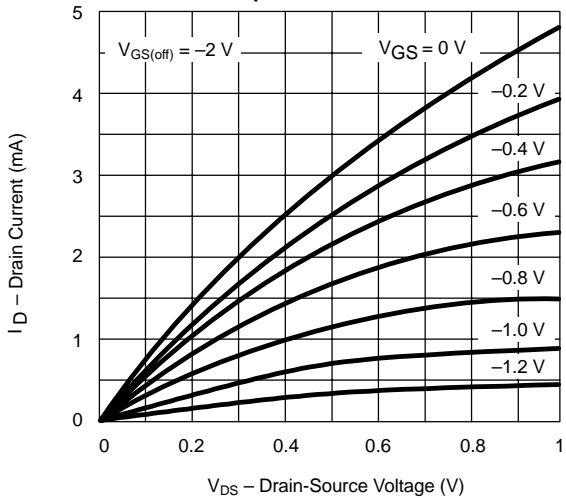
**Output Characteristics**



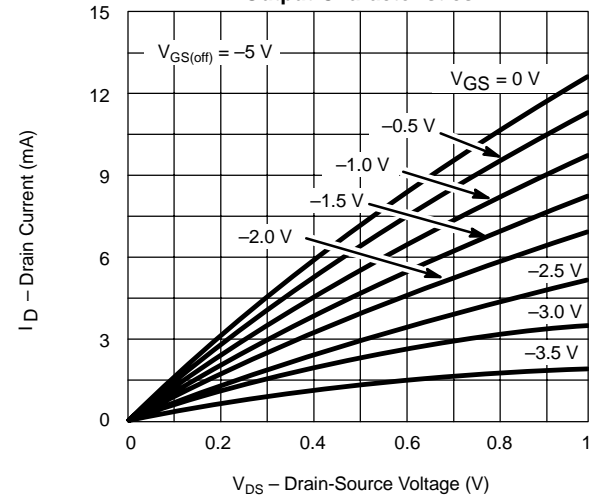
**Output Characteristics**



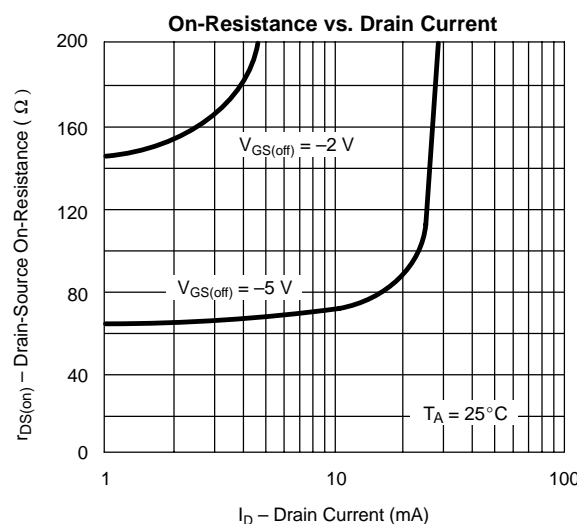
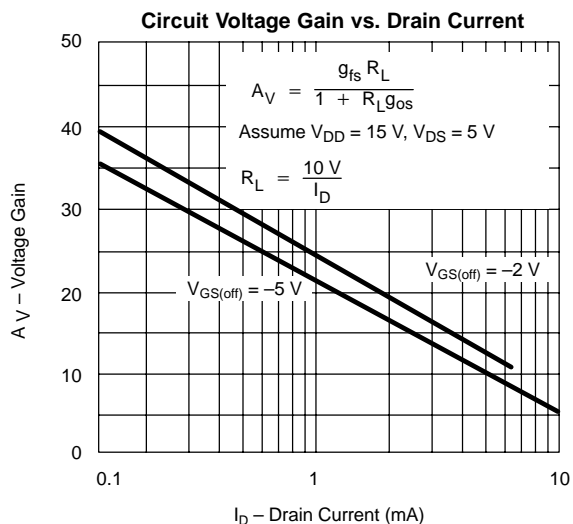
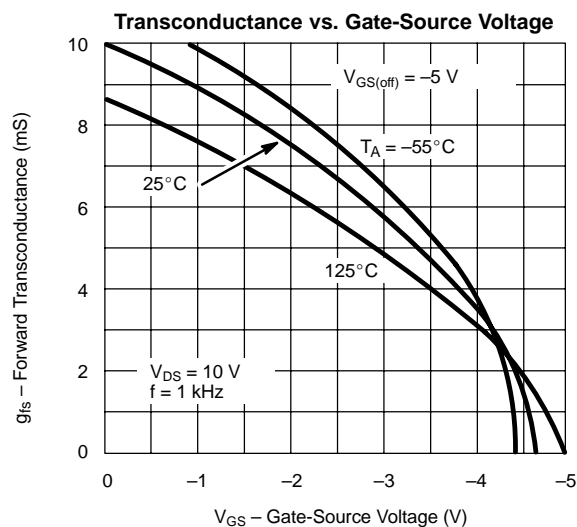
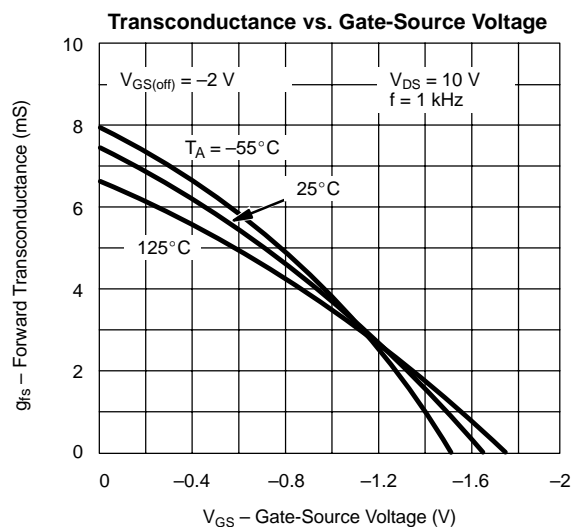
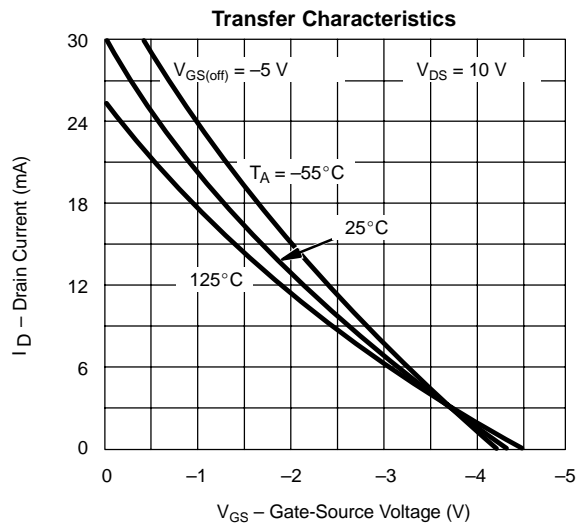
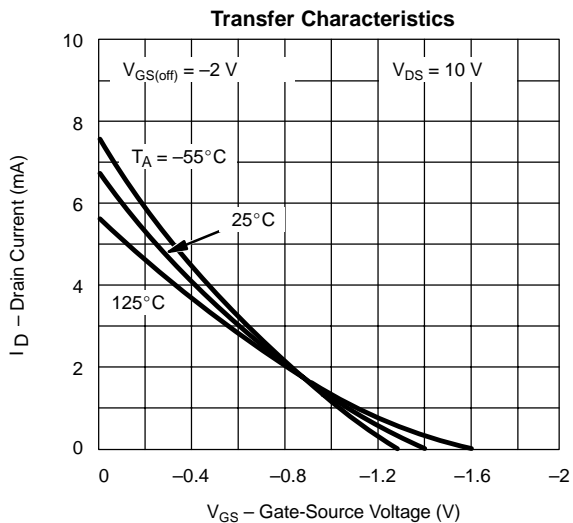
**Output Characteristics**



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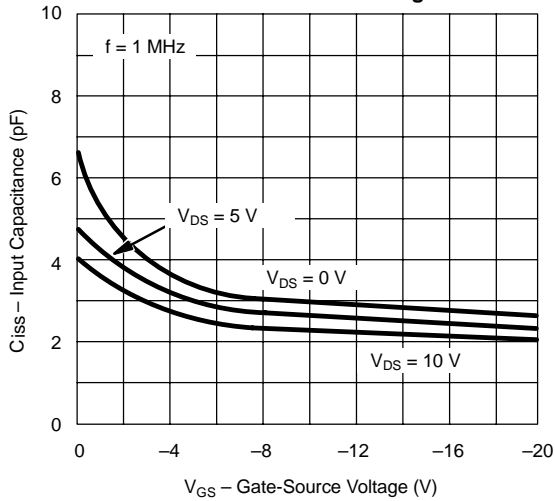


**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)**

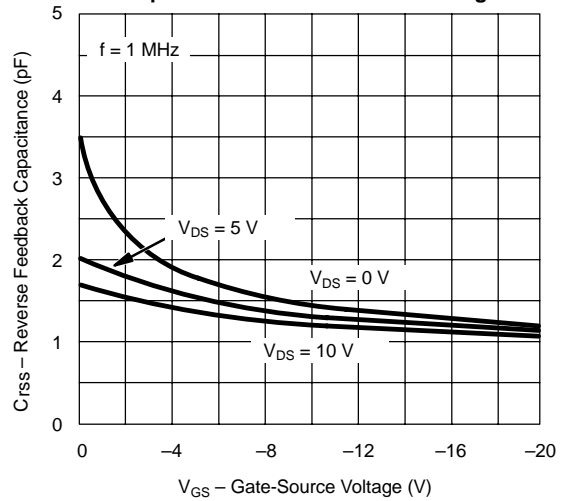


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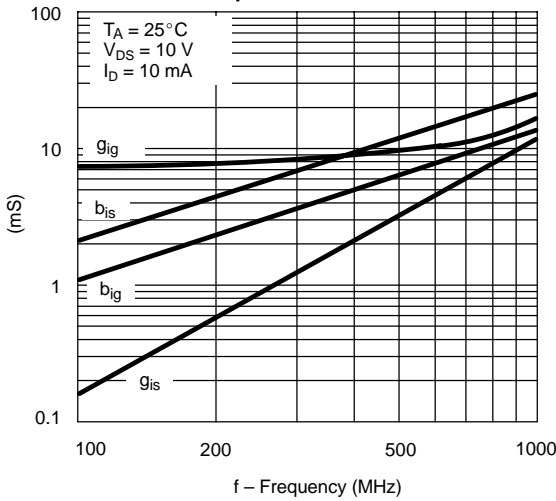
**Common-Source Input Capacitance vs. Gate-Source Voltage**



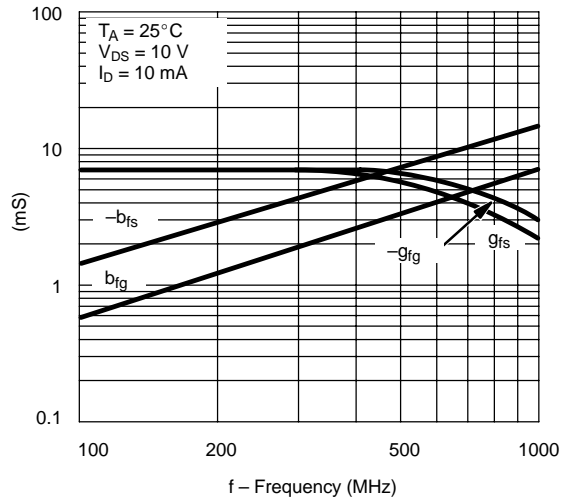
**Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage**



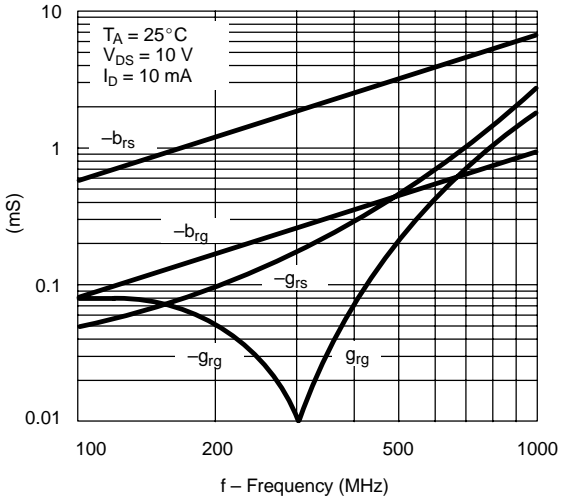
**Input Admittance**



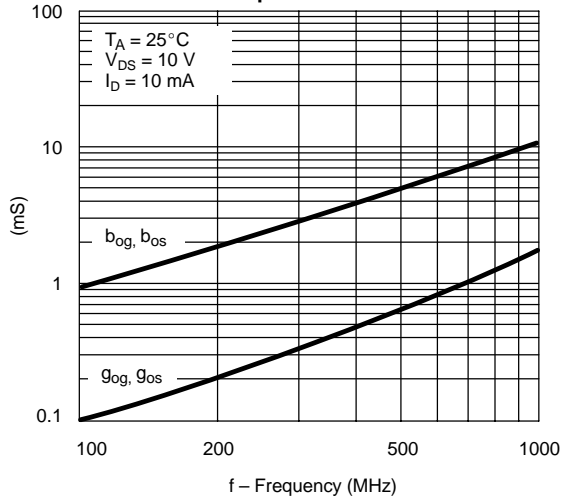
**Forward Admittance**



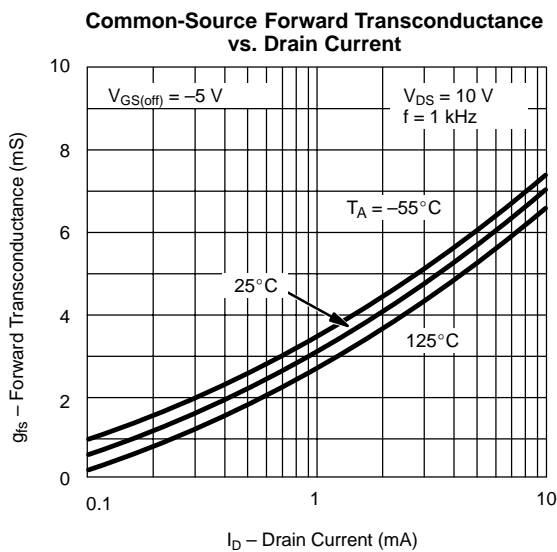
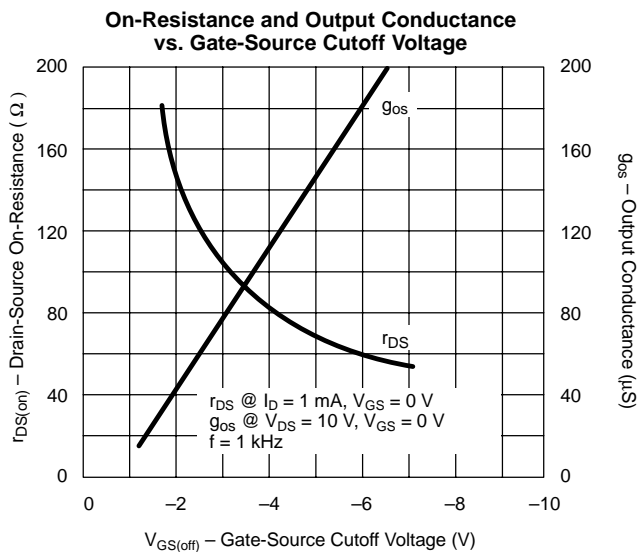
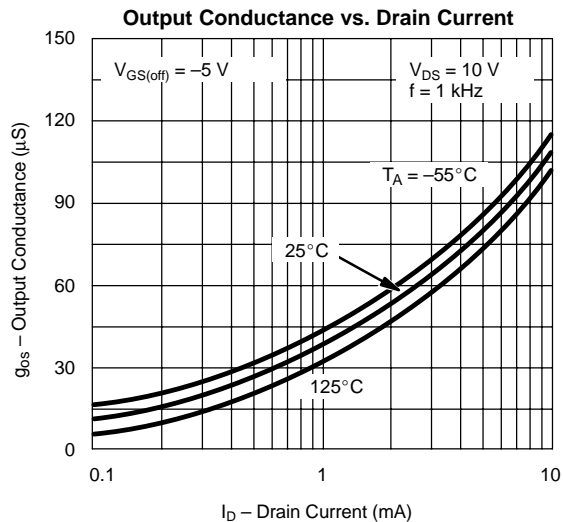
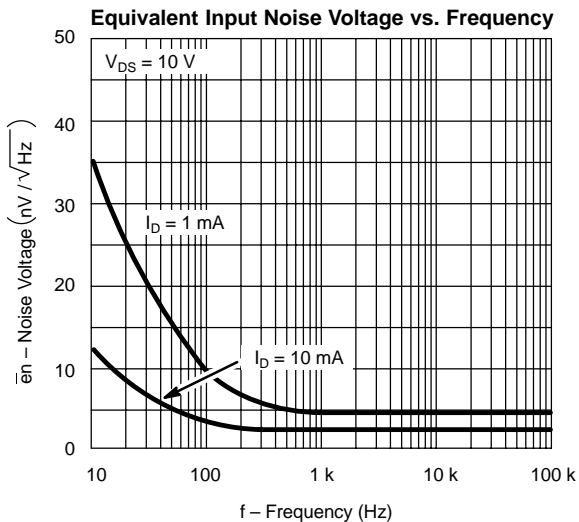
**Reverse Admittance**



**Output Admittance**



**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**





## Disclaimer

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