

# SOT89 P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ISSUE 1 - NOVEMBER 1998

**ZVP4424Z**

## FEATURES

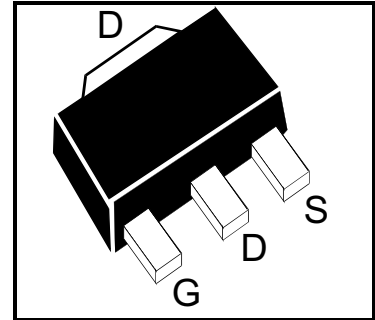
- \* 240 Volt  $V_{DS}$
- \*  $R_{DS(on)} = 8.8\Omega$  typical at  $V_{GS} = -3.5V$
- \* Low threshold and Fast switching

## APPLICATIONS

- \* Electronic hook switches
- \* Telecoms and Battery powered equipment

COMPLEMENTARY TYPE - ZVN4424Z

PARTMARKING DETAIL - 24P



## ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	-240	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	-200	mA
Pulsed Drain Current	$I_{DM}$	-1.0	A
Gate Source Voltage	$V_{GS}$	$\pm 40$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{tot}$	1†	W
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

† recommended  $P_{tot}$  calculated using FR4 measuring 15x15x0.6mm  
Refer to the handling instructions for soldering surface mount components.

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## ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

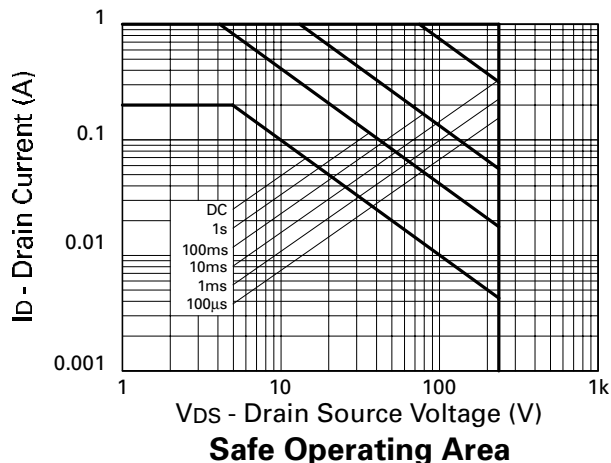
PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	-240			V	$I_D = -1\text{mA}$ , $V_{GS} = 0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-0.7	-1.4	-2.0	V	$I_D = -1\text{mA}$ , $V_{DS} = V_{GS}$
Gate-Body Leakage	$I_{GSS}$			100	nA	$V_{GS} = \pm 40\text{V}$ , $V_{DS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$			-10 -100	$\mu\text{A}$ $\mu\text{A}$	$V_{DS} = -240\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = -190\text{V}$ , $V_{GS} = 0\text{V}$ , $T = 125^{\circ}\text{C}$
On-State Drain Current	$I_{D(on)}$	-0.75	-1.0		A	$V_{DS} = -10\text{V}$ , $V_{GS} = -10\text{V}$
Static Drain-Source On-State Resistance	$R_{DS(on)}$		7.1 8.8	9 11	$\Omega$ $\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -200\text{mA}$ $V_{GS} = -3.5\text{V}$ , $I_D = -100\text{mA}$
Forward Transconductance (1) (2)	$g_{fs}$	125			mS	$V_{DS} = -10\text{V}$ , $I_D = -0.2\text{A}$
Input Capacitance (2)	$C_{iss}$		100	200	pF	$V_{DS} = -25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$
Common Source Output Capacitance (2)	$C_{oss}$		18	25	pF	
Reverse Transfer Capacitance (2)	$C_{rss}$		5	15	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	15	ns	$V_{DD} \approx -50\text{V}$ , $I_D = -0.25\text{A}$ , $V_{GEN} = -10\text{V}$
Rise Time (2)(3)	$t_r$		8	15	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		26	40	ns	
Fall Time (2)(3)	$t_f$		20	30	ns	

(1) Measured under pulsed conditions. Width=300 $\mu\text{s}$ . Duty cycle  $\leq 2\%$

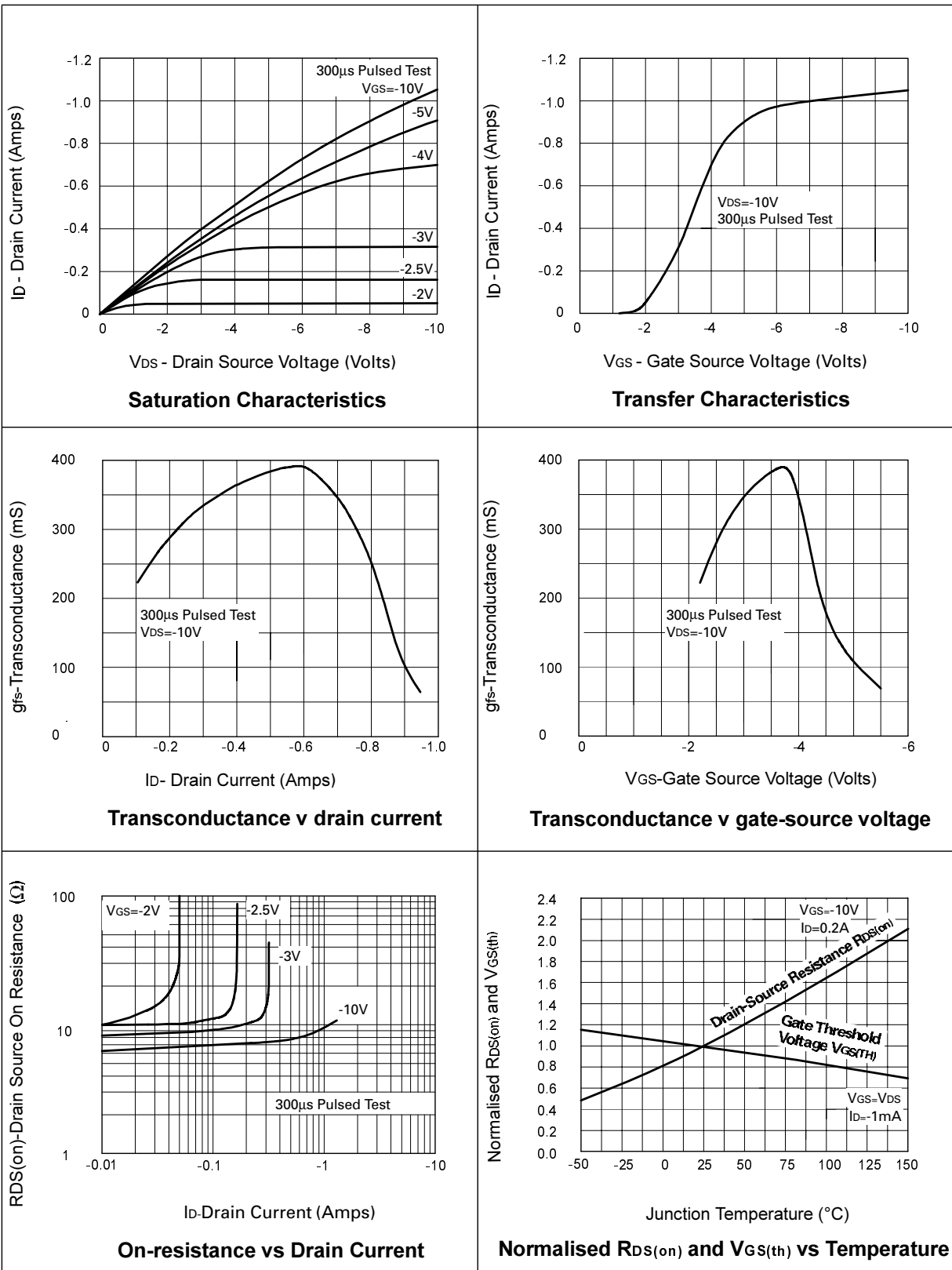
(2) Sample test.

(3) Switching times measured with 50 $\Omega$  source impedance and <5ns rise time on a pulse generator  
Spice parameter data is available upon request for this device

## TYPICAL CHARACTERISTICS



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