FAIRCHILD
SEMICONDUCTOR®

November 2007

FDJ129P

P-Channel -2.5 Vgs Specified PowerTrench® MOSFET

General Description

This P-Channel -2.5V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load switch

Features

- –4.2 A, –20 V. $R_{DS(ON)}$ = 70 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 120 mΩ @ V_{GS} = –2.5 V

- Low gate charge

- High performance trench technology for extremely low $R_{DS(ON)}$

- Compact industry standard SC75-6 surface mount package

- RoHS Compliant

SC75-6 FLMP

Bottom Drain
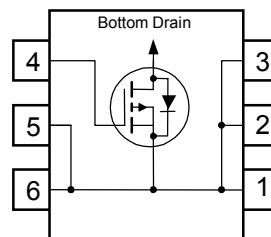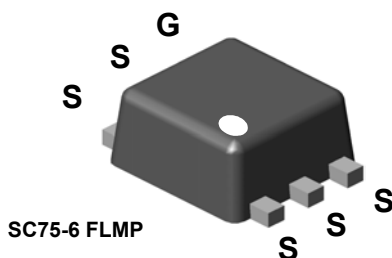
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Drain Current – Continuous	(Note 1a)	–4.2	A
	– Pulsed		–16	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.6	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	77	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.A	FDJ129P	7''	8mm	3000 units

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Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA,Referenced to 25°C		–18		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –12 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.6	–1.1	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA,Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –4.2 A V_{GS} = –2.5 V, I_D = –3.3 A V_{GS} = –4.5 V, I_D = –4.2,T_J=125°C		54 91 72	70 120 100	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–8			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –4.2 A		11		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz		585	780	pF
C_{oss}	Output Capacitance			124	170	pF
C_{rss}	Reverse Transfer Capacitance			61	95	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn–On Rise Time			9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			17	30	ns
t_f	Turn–Off Fall Time			10	20	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –4.2 A, V_{GS} = –4.5 V		4	6	nC
Q_{gs}	Gate–Source Charge			1.1		nC
Q_{gd}	Gate–Drain Charge			1.2		nC
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain–Source Diode Forwar Voltage	V_{GS} = 0 V, I_S = –1.5 A (Note 2)		–0.7	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = –4.2 A, d_{iF}/d_t = 100 A/μs		16		nS
Q_{rr}	Diode Reverse Recovery Charge			13		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a)   77°C/W when mounted on a 1in^2 pad of 2 oz copper.
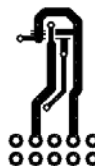
b)   110°C/W when mounted on a minimum pad of 2 oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

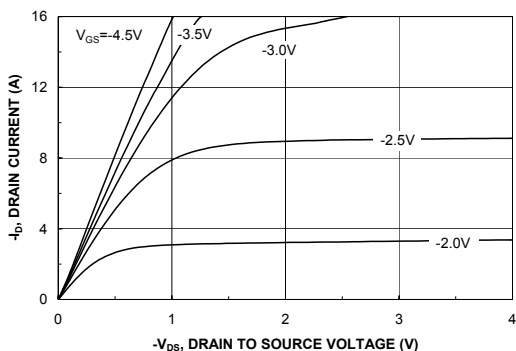FDJ129P Rev G (W)

Typical Characteristics

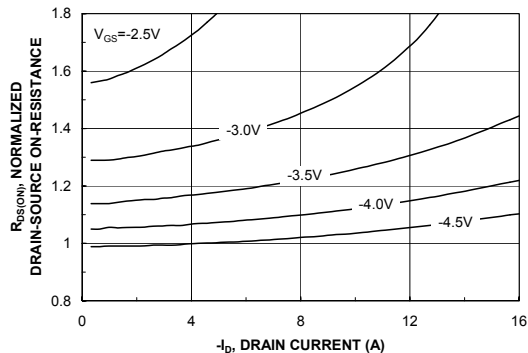**Figure 1. On-Region Characteristics.**

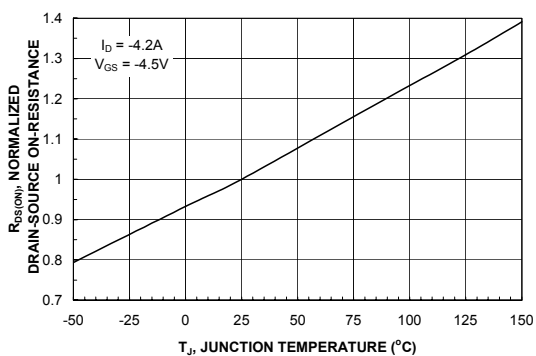**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

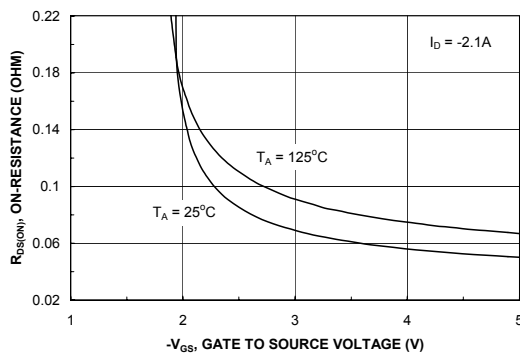**Figure 3. On-Resistance Variation withTemperature.**

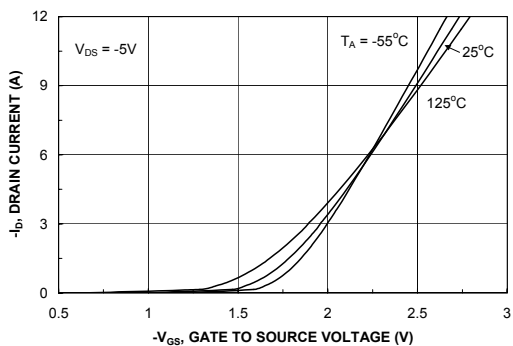**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**
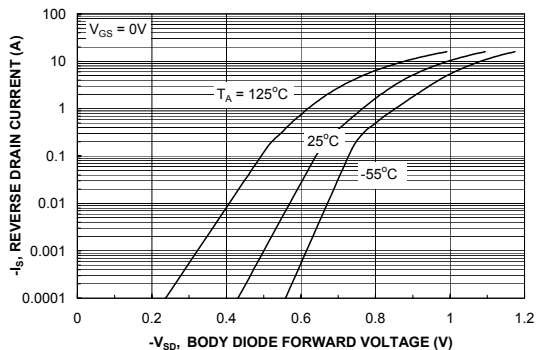

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
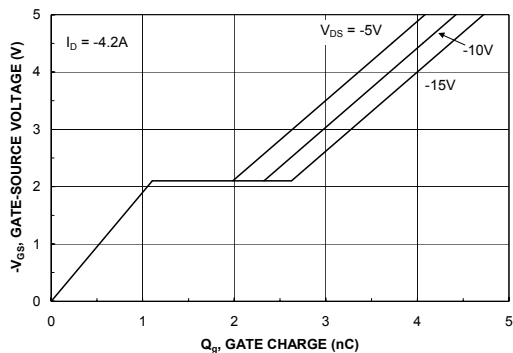
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Typical Characteristics

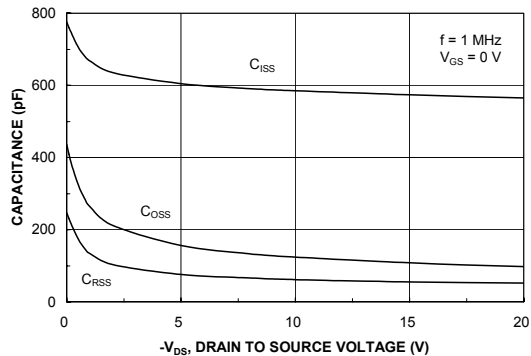**Figure 7. Gate Charge Characteristics.**

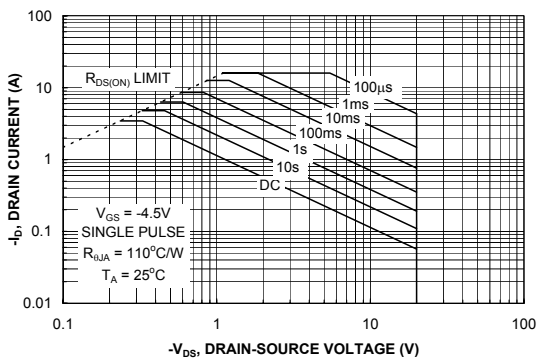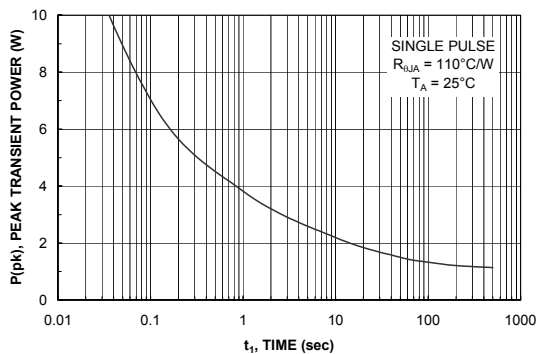**Figure 8. Capacitance Characteristics.**

Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

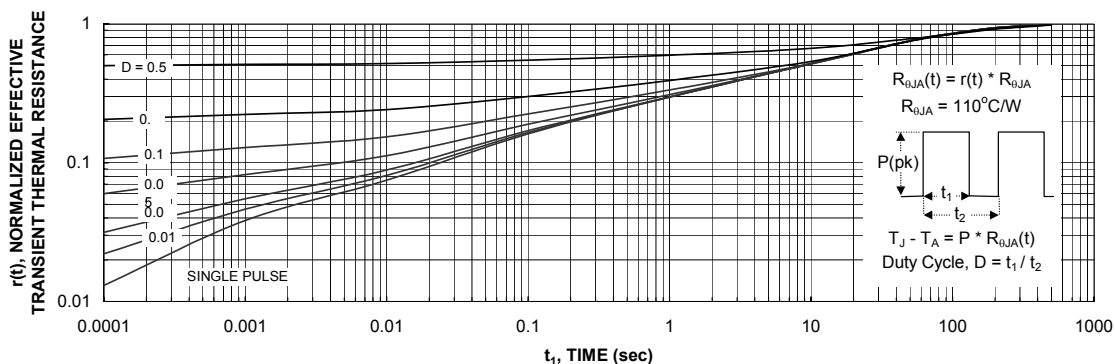**Figure 11. Transient Thermal Response Curve.**
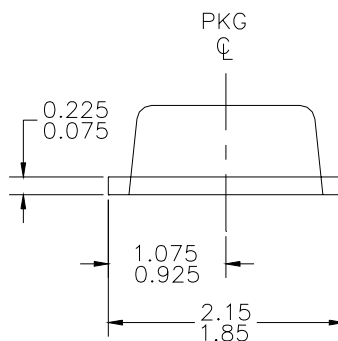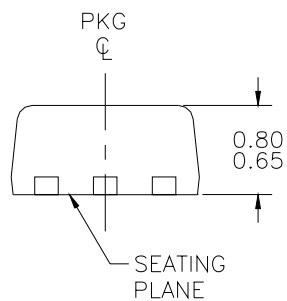
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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Dimensional Outline and Pad Layout

1.70
1.50

A

PKG
℄

6   4   B

PKG ℄

1   3

(0.20)

0.275
0.125

0.50

⊕ 0.075 Ⓜ A B

1.00

1.75
1.55

PKG
℄

0.30 MIN

DRAIN
TERMINAL

6   4

0.90   PKG
℄

0.50 MIN

1   3

0.50

1.00

2.35 MIN

1.35

LAND PATTERN RECOMMENDATION

PKG
℄

0.80
0.65

SEATING
PLANE

PKG
℄

0.225
0.075

1.075
0.925

2.15
1.85

DRAIN   PKG
℄

1   3

(0.24)

(0.18)

PKG ℄

(0.75)

(1.20)

6   4

BOTTOM VIEW
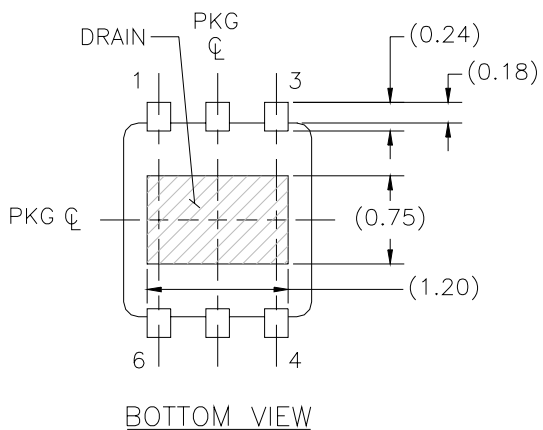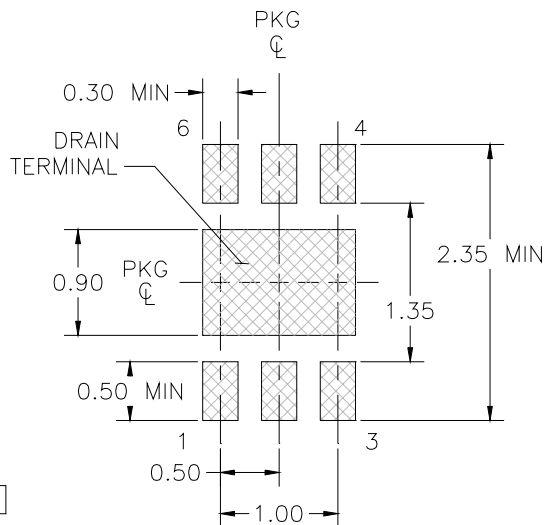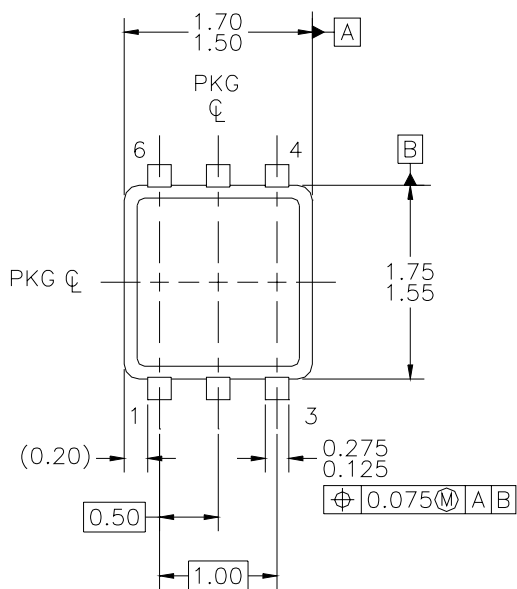
NOTES: UNLESS OTHERWISE SPECIFIED

A)   NO PACKAGE STANDARD REFERENCE
     AS OF JULY 13, 2000.
B)   ALL DIMENSIONS ARE IN MILLIMETERS.
C)   DIMENSIONS DO NOT INCLUDE BURRS
     OR MOLD FLASH.

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