FAIRCHILD

SEMICONDUCTOR ™

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FDG315N

N-Channel Logic Level PowerTrench® MOSFET

General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications

- DC/DC converter
- Load switch
- Power Management

Features

- 2 A, 30 V. $R_{DS(ON)}$ = 0.12 Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 0.16 Ω @ V_{GS} = 4.5 V.

- Low gate charge (2.1nC typical).

- High performance trench technology for extremely low $R_{DS(ON)}$.

- Compact industry standard SC70-6 surface mount package.

SC70-6
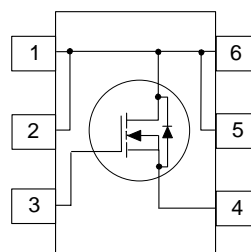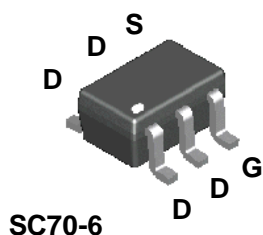
Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	2	A
	- Pulsed		6	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.75	W
		(Note 1b)	0.48	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	260	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.15	FDG315N	7''	8mm	3000 units

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Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		26		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V			1	µA
I_{GSS}	Gate-Body Leakage Forward	$V_{GS} = 16$ V, $V_{DS} = 0$ V			100	nA
I_{GSS}	Gate-Body Leakage Reverse	$V_{GS} = -16$ V, $V_{DS} = 0$ V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		-4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 2$ A $V_{GS} = 10$ V, $I_D = 2$ A, $T_J = 125°C$ $V_{GS} = 4.5$ V, $I_D = 1.7$ A		0.100 0.140 0.130	0.12 0.20 0.16	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5$ V, $V_{DS} = 5$ V	3			A
G_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 2$ A		5		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, f = 1.0 MHz		220		pF
C_{oss}	Output Capacitance			50		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10$ V, $R_{GEN} = 6$ Ω		3	6	ns
t_r	Turn-On Rise Time			11	22	ns
$t_{d(off)}$	Turn-Off Delay Time			7	14	ns
t_f	Turn-Off Fall Time			3	6	ns
Q_g	Total Gate Charge	$V_{DS} = 15$ V, $I_D = 2$ A, $V_{GS} = 5$ V		2.1	4	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			0.7		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 0.42$ A (Note 2)		0.7	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 170°C/W when mounted on a 1 in² pad of 2oz copper.

b) 260°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

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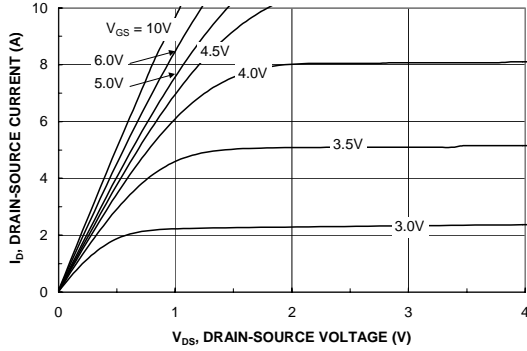
Typical Characteristics
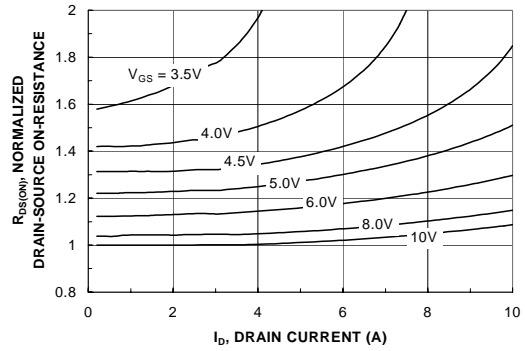

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation
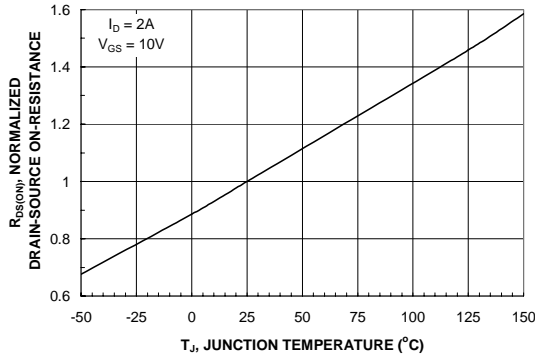with Drain Current and Gate Voltage.

Figure 3. On-Resistance Variation
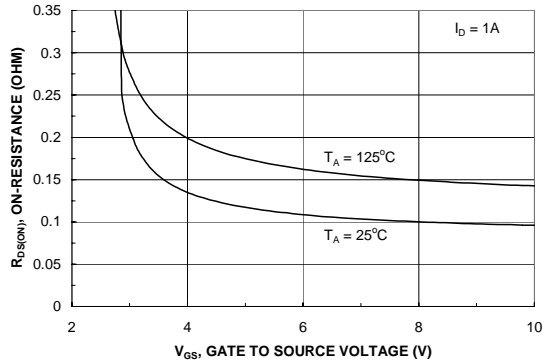with Temperature.

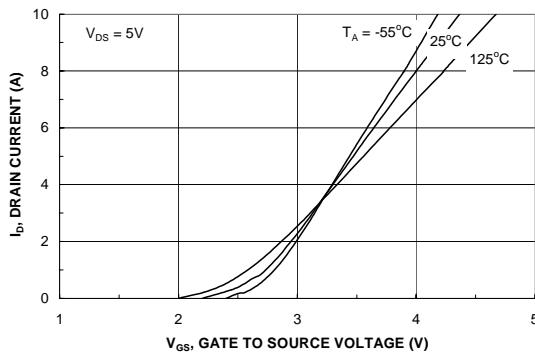Figure 4. On-Resistance Variation
with Gate-to-Source Voltage.

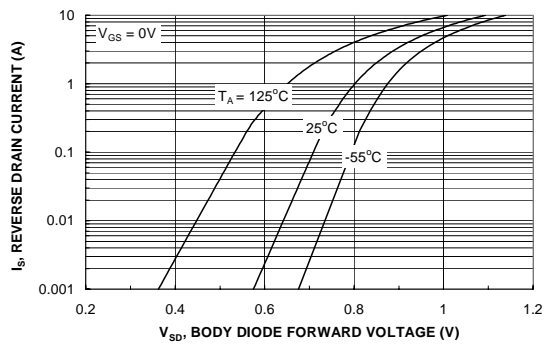Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage
Variation with Source Current
and Temperature.

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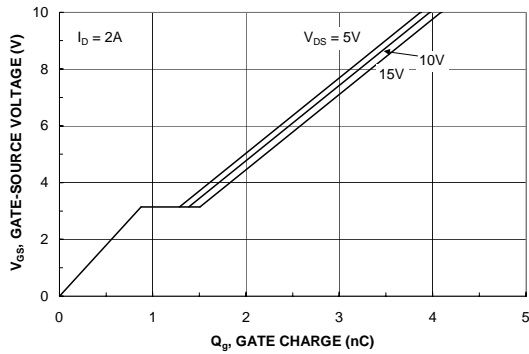## Typical Characteristics (continued)

Figure 7. Gate-Charge Characteristics.
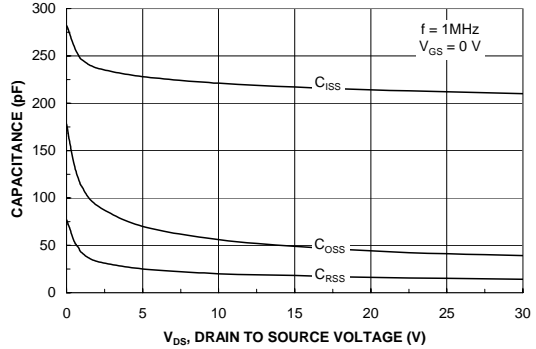

Figure 8. Capacitance Characteristics.
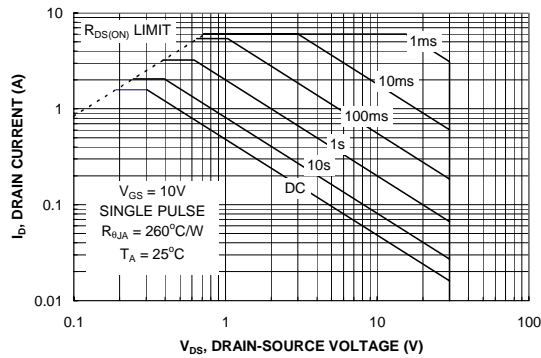

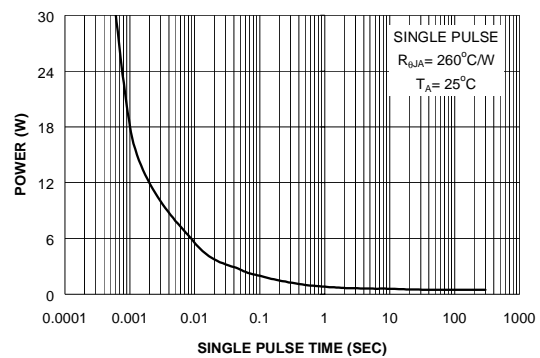**Figure 9. Maximum Safe Operating Area.**

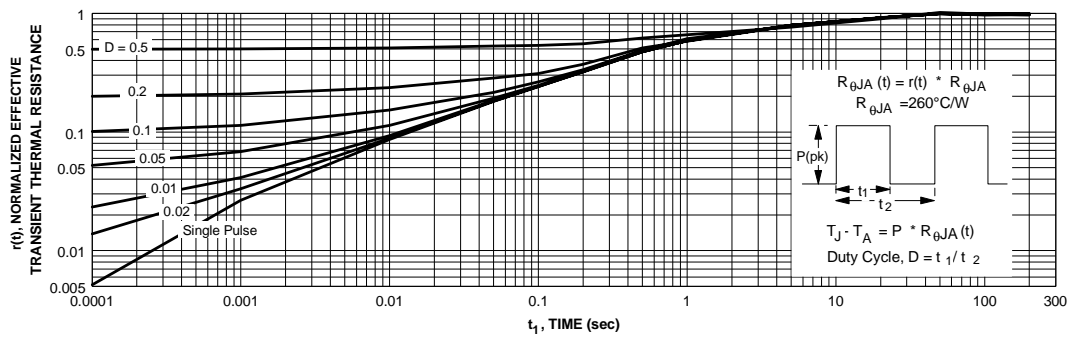**Figure 10. Single Pulse Maximum Power Dissipation.**

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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EnSigna™	OPTOLOGIC™	SuperSOT™-8	
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