

PolarP™ Power MOSFET

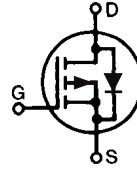
IXTR32P60P

$$V_{DSS} = -600V$$

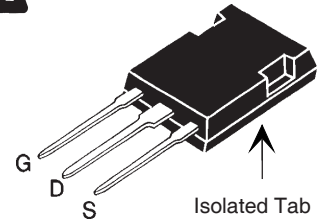
$$I_{D25} = -18A$$

$$R_{DS(on)} \leq 385m\Omega$$

P-Channel Enhancement Mode
Avalanche Rated



ISOPLUS247 (IXTR)
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	- 600	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	- 600	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$	- 18	A
I_{DM}	$T_C = 25^\circ C$, pulse width limited by T_{JM}	- 90	A
I_{AR}	$T_C = 25^\circ C$	- 32	A
E_{AS}	$T_C = 25^\circ C$	3.5	J
dV/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	10	V/ns
P_D	$T_C = 25^\circ C$	310	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	1.6mm (0.062 in.) from case for 10s	300	$^\circ C$
T_{SOLD}	Plastic body for 10s	260	$^\circ C$
V_{ISOL}	50/60 Hz, RMS	$t = 1min$ 2500	V~
	$I_{ISOL} \leq 1mA$	$t = 1s$ 3000	V~
M_d	Mounting force	20..120/4.5..27	N/lb.
Weight		5	g

Features

- Silicon chip on Direct-Copper Bond (DCB) substrate
 - UL recognized package
 - Isolated mounting surface
 - 2500V electrical isolation
- Avalanche rated
- The rugged PolarP™ process
- Low Q_G
- Low Drain-to-Tab capacitance
- Low package inductance
 - easy to drive and to protect

Applications

- High side switching
- Push-pull amplifiers
- DC Choppers
- Automatic test equipment
- Load-Switch Application
- Fuel Injection Systems

Symbol	Test Conditions ($T_J = 25^\circ C$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	- 500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	- 2.5		- 4.5 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0V$			- 50 μA - 250 μA
$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = -16A$, Note 1			385 m Ω

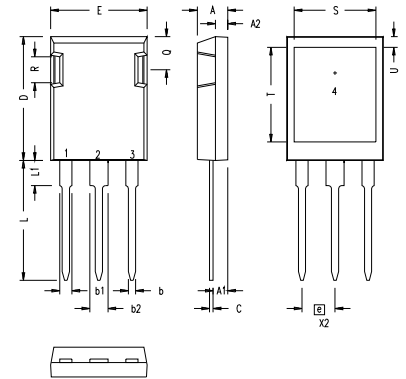
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = -10\text{V}$, $I_D = -16\text{A}$, Note 1	21	32	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1\text{MHz}$		11.1	nF
C_{oss}			925	pF
C_{rss}			77	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = -16\text{A}$ $R_G = 1\Omega$ (External)		37	ns
t_r			27	ns
$t_{d(off)}$			95	ns
t_f			33	ns
$Q_{g(on)}$	$V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = -16\text{A}$		196	nC
Q_{gs}			54	nC
Q_{gd}			58	nC
R_{thJC}			0.40	$^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			- 32 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			- 128 A
V_{SD}	$I_F = -16\text{A}$, $V_{GS} = 0\text{V}$, Note 1			- 2.8 V
t_{rr}	$I_F = -16\text{A}$, $-di/dt = -150\text{A}/\mu\text{s}$		480	nS
Q_{RM}			11.4	μC
I_{RM}	$V_R = -100\text{V}$, $V_{GS} = 0\text{V}$		- 47.6	A

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

ISOPLUS247 (IXTR) Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

- 1 - GATE
- 2 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)
- 4 - NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ 25°C

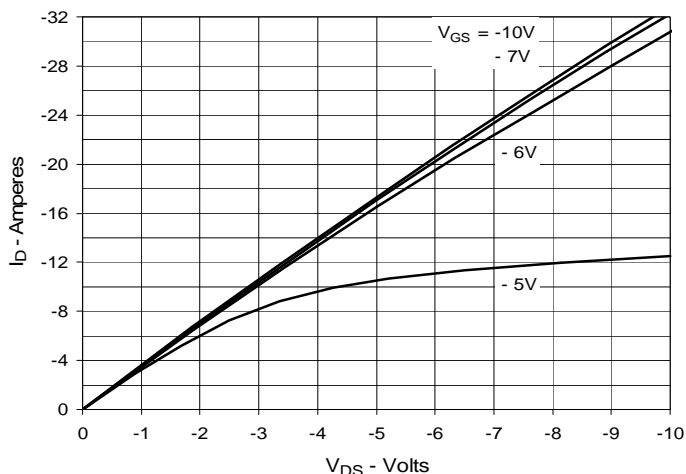


Fig. 2. Extended Output Characteristics @ 25°C

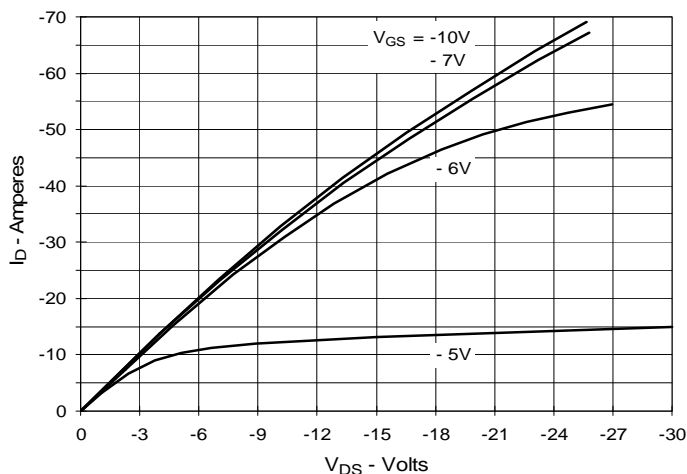


Fig. 3. Output Characteristics @ 125°C

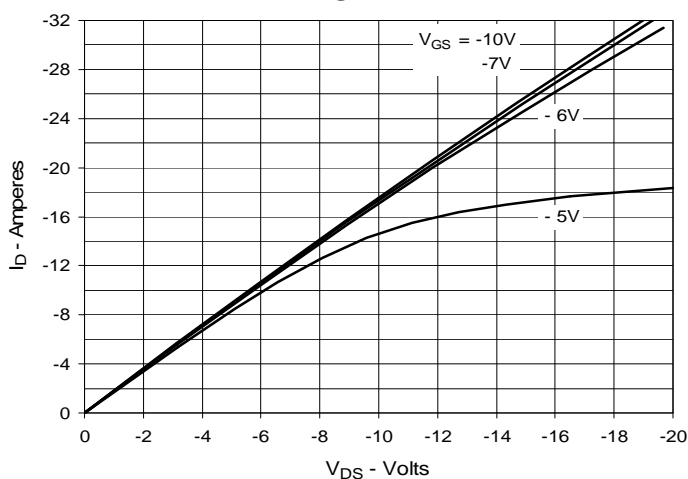


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = -16A$ vs. Junction Temperature

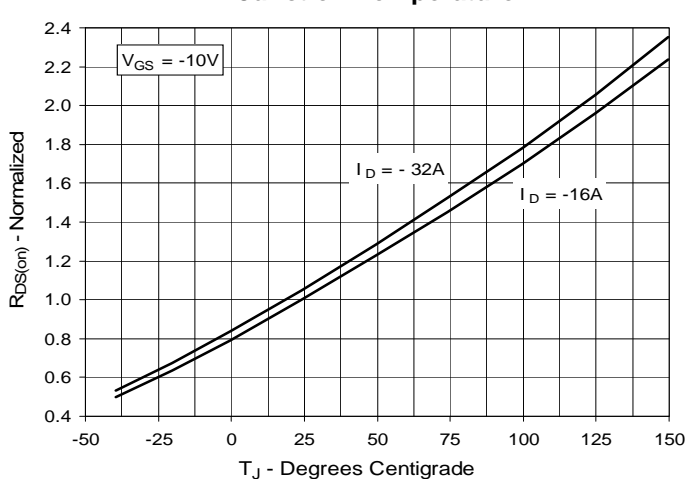


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = -16A$ vs. Drain Current

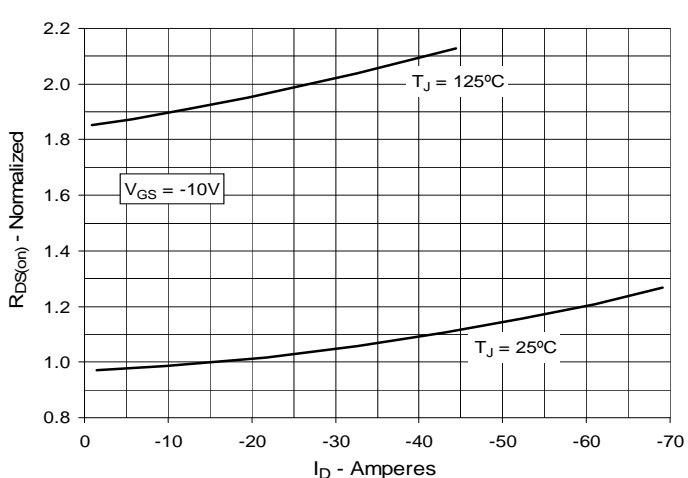


Fig. 6. Maximum Drain Current vs. Case Temperature

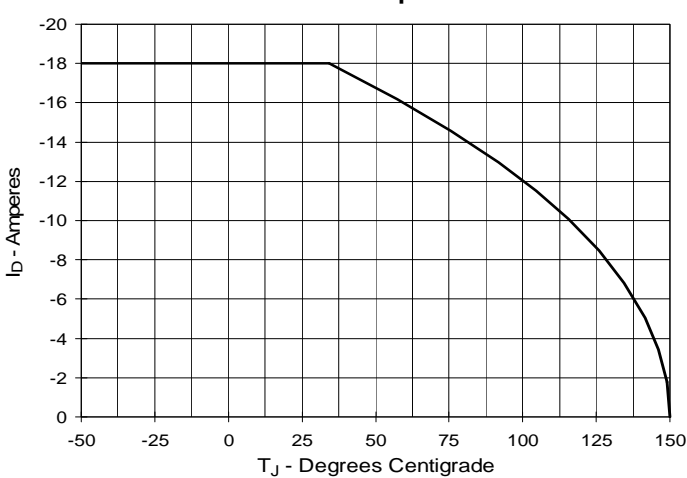


Fig. 7. Input Admittance

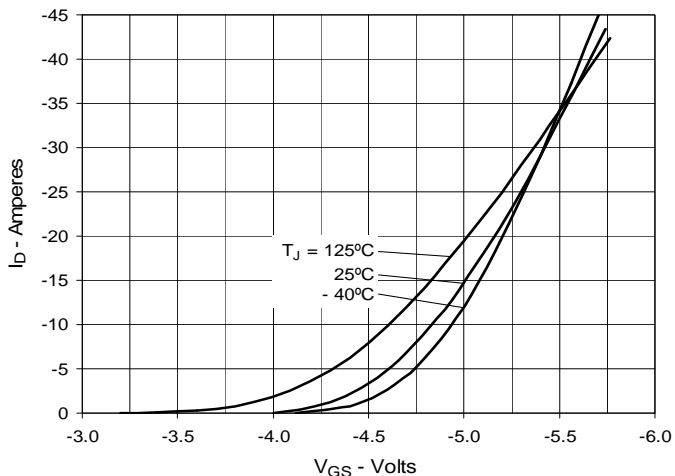


Fig. 8. Transconductance

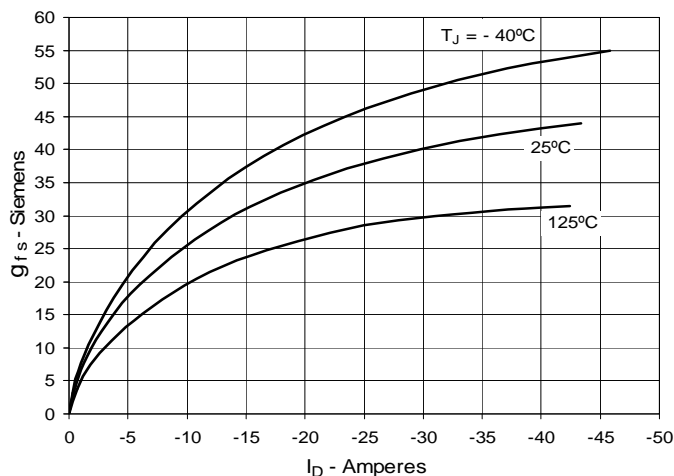


Fig. 9. Forward Voltage Drop of Intrinsic Diode

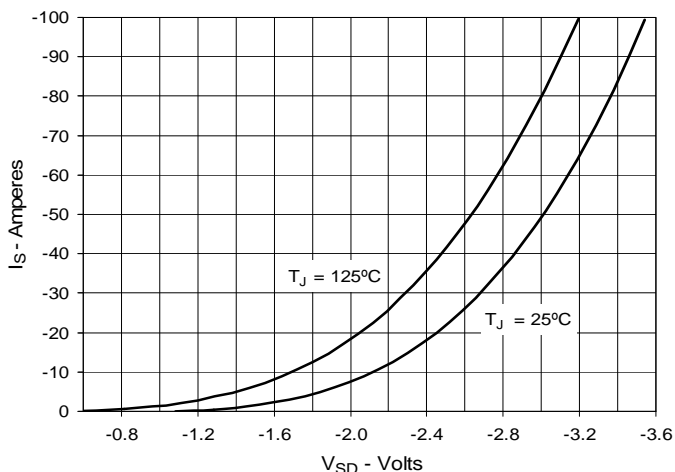


Fig. 10. Gate Charge

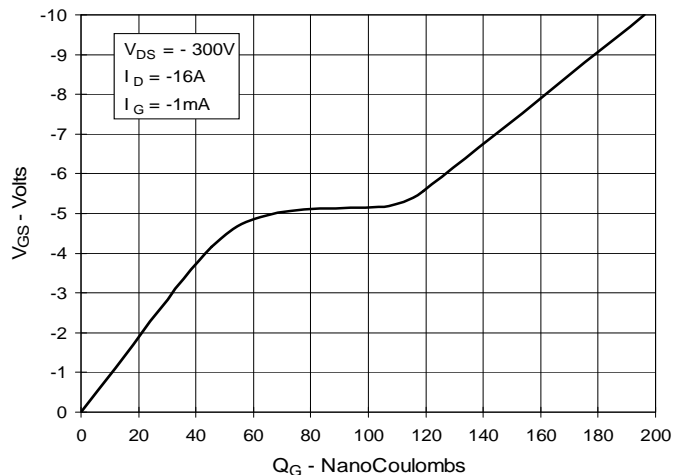


Fig. 11. Capacitance

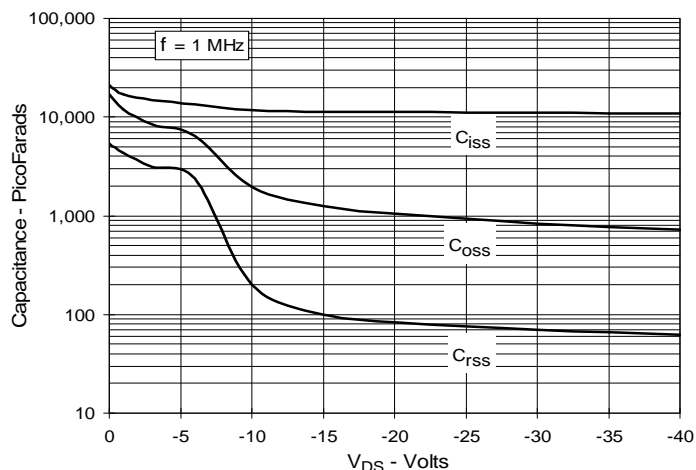
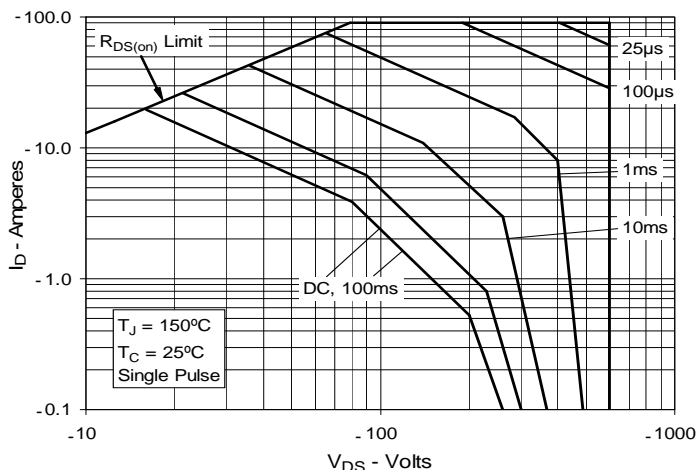


Fig. 12. Forward-Bias Safe Operating Area



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Fig. 13. Maximum Transient Thermal Impedance

