STW43NM60ND
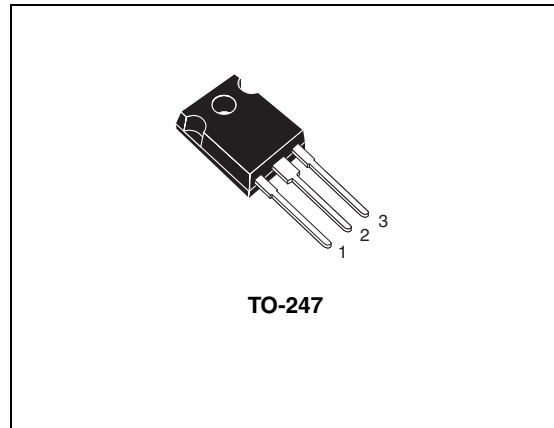
N-channel 600 V, 0.075 Ω, 35 A TO-247 FDmesh™ Power MOSFET (with fast diode)

Features

Type	V_{DSS} @ T_{JMAX}	$R_{DS(on)}$ max	I_D
STW43NM60ND	650 V	< 0.088 Ω	35 A

- The worldwide best $R_{DS(on)}$*area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities.

TO-247

Application

- Switching applications

Description

The FDmesh™ II series belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode.It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.
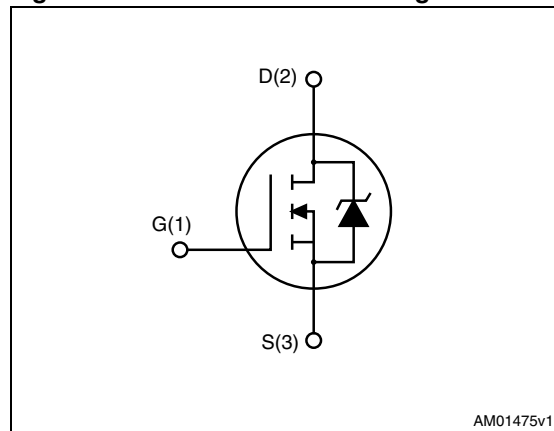
Figure 1. Internal schematic diagram

D(2)

G(1)

S(3)

AM01475v1

Table 1. Device summary

Order code	Marking	Package	Packaging
STW43NM60ND	43NM60ND	TO-247	Tube

Contents

1   Electrical ratings

Table 2.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\ °C$	35	A
I_D	Drain current (continuous) at $T_C = 100\ °C$	22	A
I_{DM} [1]	Drain current (pulsed)	140	A
P_{TOT}	Total dissipation at $T_C = 25\ °C$	255	W
dv/dt [2]	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1.   Pulse width limited by safe operating area

2. $I_{SD} \leq 35$ A, di/dt ≤ 600 A/µs, $V_{DD} = 80\%\ V_{(BR)DSS}$

Table 3.   Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.49	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 4.   Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	14	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\ °C$, $I_D=I_{AS}$, $V_{DD}=50$ V)	1000	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5.   On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125 °C			10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 17.5 A		0.075	0.088	Ω

Table 6.   Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} [1]	Forward transconductance	V_{DS}=15 V, I_D = 17.5 A	-	17	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	4300 250 25	-	pF pF pF
$C_{oss\ eq.}$ [2]	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	530	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 35 A, V_{GS} = 10 V, *(see Figure 15)*	-	145 18 80	-	nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	1.7	-	Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7.   Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300 V, I_D = 17.5 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 14)*	-	30 40 120 50	-	ns ns ns ns

Table 8.   Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} [1]	Source-drain current Source-drain current (pulsed)		-		35 140	A A
V_{SD} [2]	Forward on voltage	I_{SD} = 35 A, V_{GS} = 0	-		1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 35 A, di/dt = 100 A/µs V_{DD} = 100 V *(see Figure 16)*	-	190 1.6 17		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 35 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C *(see Figure 16)*	-	280 3.0 22		ns µC A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

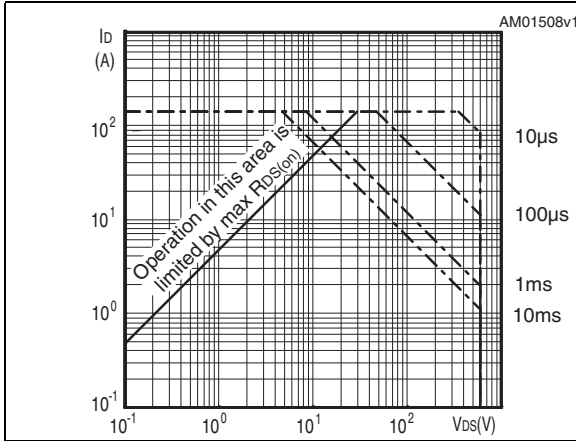## 2.1 Electrical characteristics (curves)

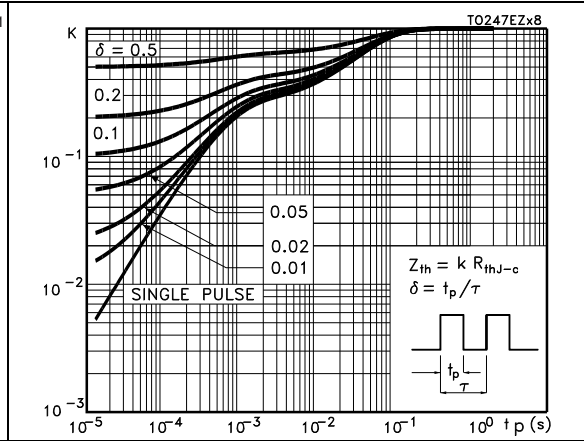**Figure 2. Safe operating area**

Figure 3. Thermal impedance
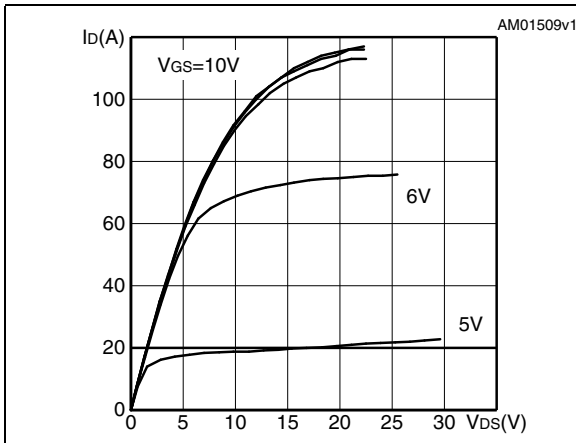

Figure 4. Output characteristics

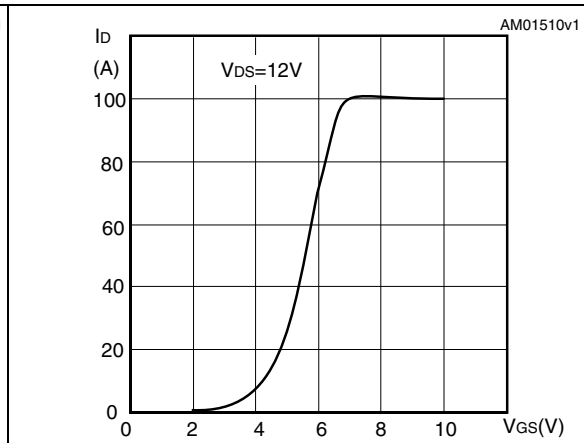**Figure 5. Transfer characteristics**

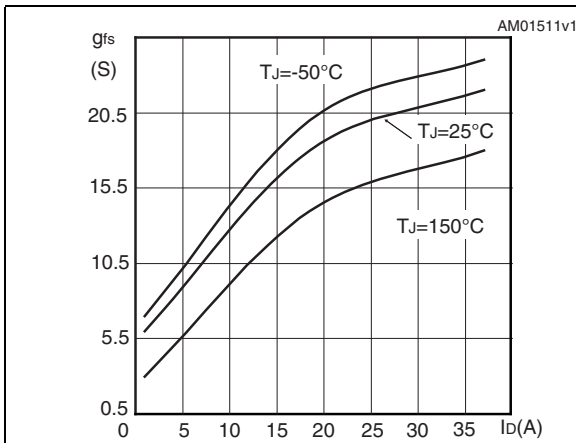**Figure 6. Transconductance**

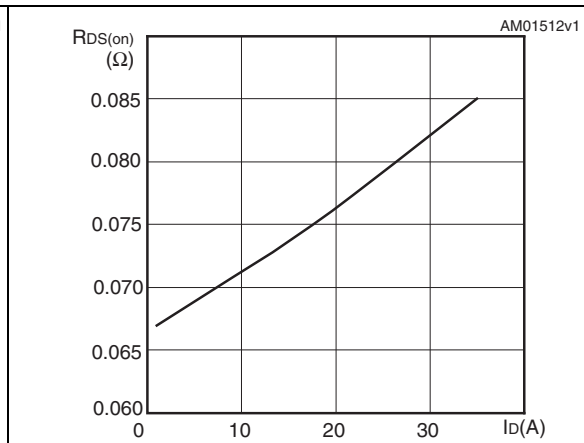**Figure 7. Static drain-source on resistance**

Figure 8.   Gate charge vs gate-source voltage

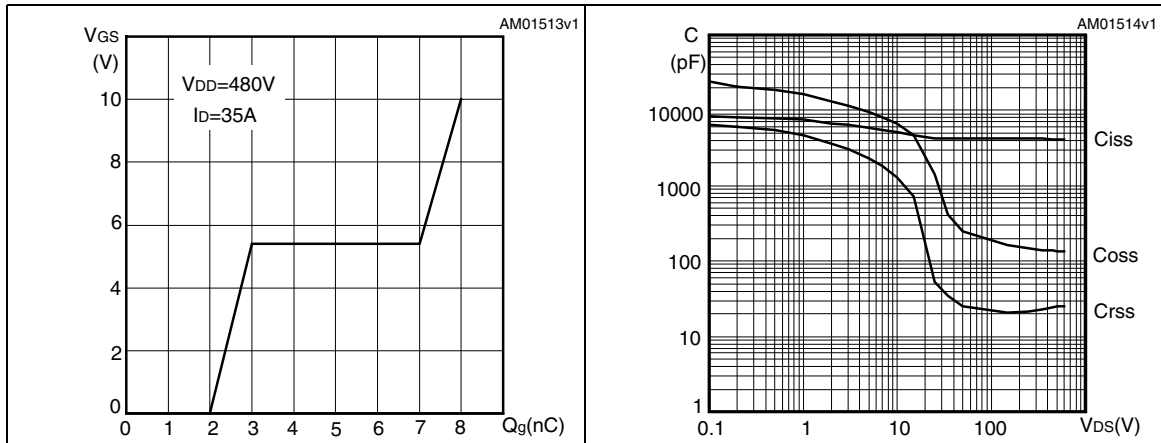**Figure 9.   Capacitance variations**

Figure 10. Normalized gate threshold voltage vs temperature
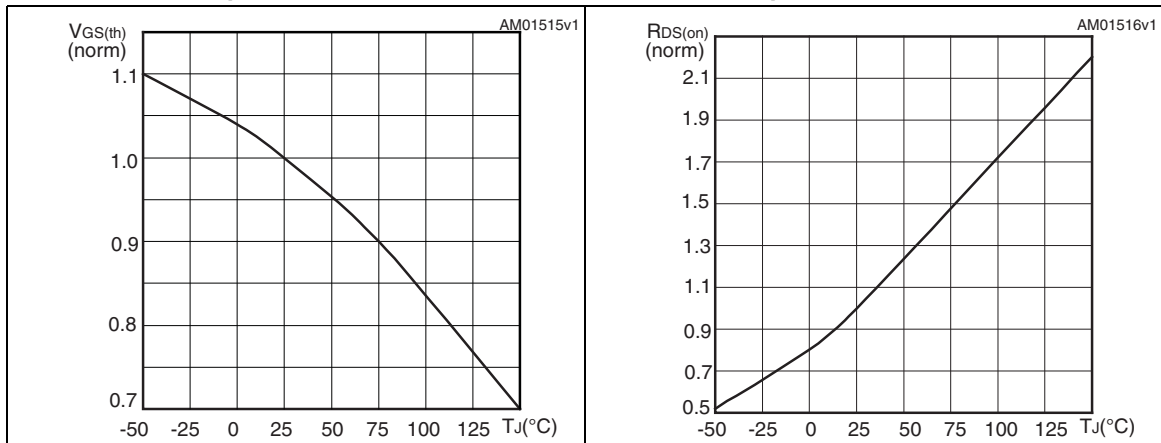

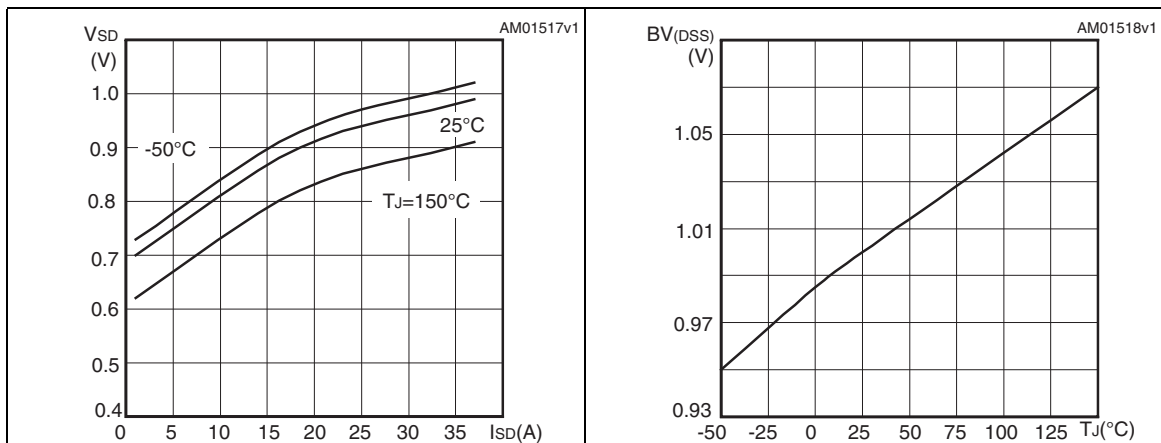**Figure 11. Normalized on resistance vs temperature**

Figure 12. Source-drain diode forward characteristics

Figure 13. Normalized B$_{VDSS}$ vs temperature

3 Test circuits

Figure 14. Switching times test circuit for resistive load
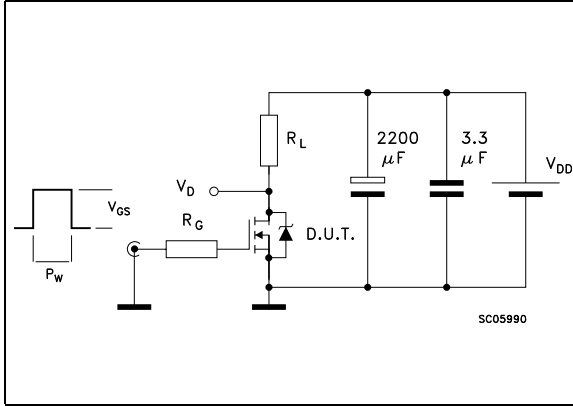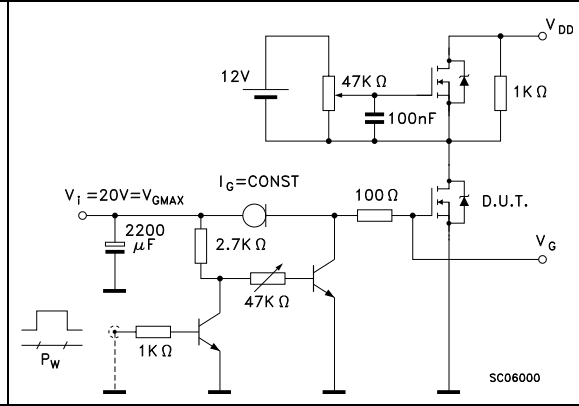

Figure 15. Gate charge test circuit

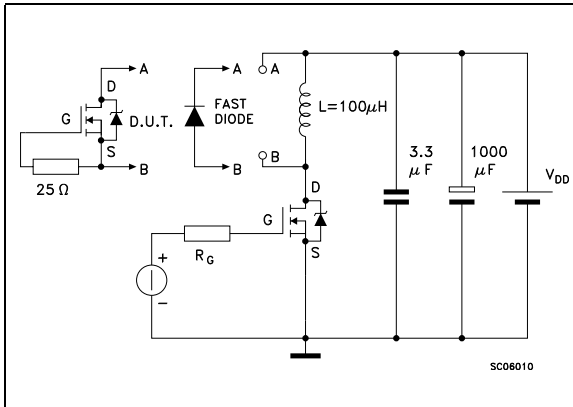**Figure 16. Test circuit for inductive load switching and diode recovery times**
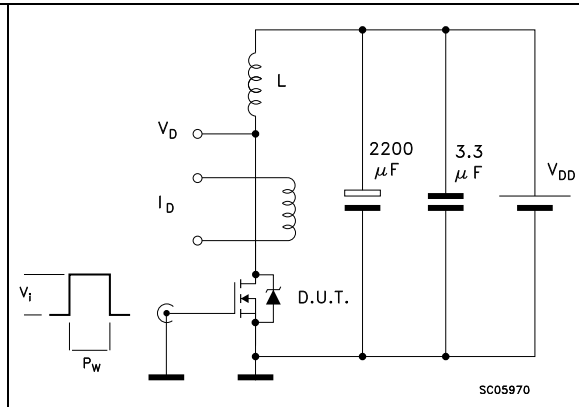

Figure 17. Unclamped inductive load test circuit

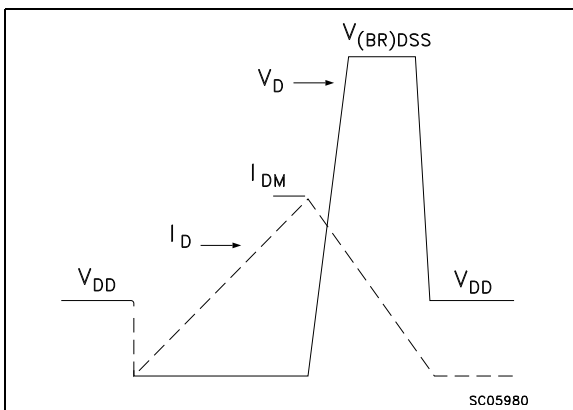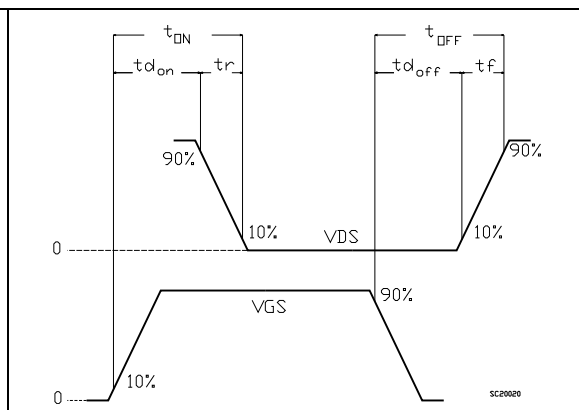**Figure 18. Unclamped inductive waveform**

Figure 19. Switching time waveform

4 Package mechanical data

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Table 9.   TO-247 mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 20.   TO-247 drawing

0075325_F

5 Revision history

Table 10.   Document revision history

Date	Revision	Changes
06-Feb-2008	1	First release
22-Jan-2009	2	Document status promoted from preliminary data to datasheet.
16-Feb-2010	3	*Figure 13: Normalized B$_{VDSS}$ vs temperature* has been corrected.
14-Feb-2011	4	I$_{DSS}$ value in *Table 5* has been corrected.

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