



# STF10N62K3, STI10N62K3 STP10N62K3

N-channel 620 V, 0.68  $\Omega$ , 8.4 A, TO-220, TO-220FP, I<sup>2</sup>PAK  
SuperMESH3™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STF10N62K3	620 V	< 0.75 $\Omega$	8.4 A <sup>(1)</sup>	30 W
STI10N62K3	620 V	< 0.75 $\Omega$	8.4 A	125 W
STP10N62K3	620 V	< 0.75 $\Omega$	8.4 A	125 W

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected

## Application

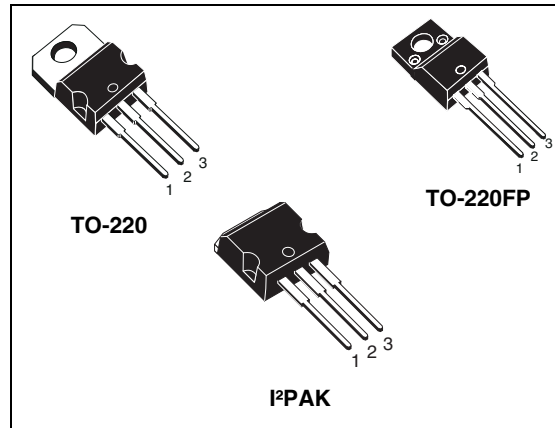
- Switching applications

## Description

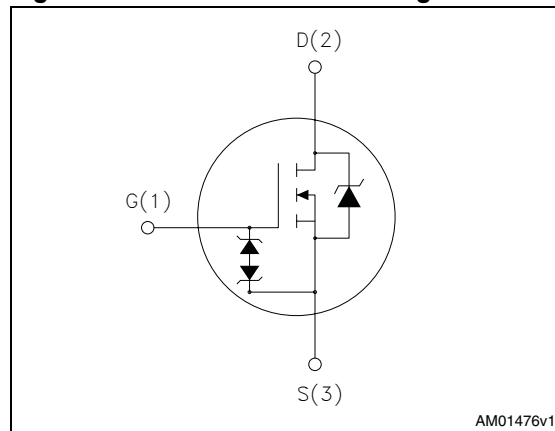
The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimized vertical structure. In addition to pushing on-resistance significantly down, special attention has been taken to ensure a very good dynamic performance coupled with a very large avalanche capability for the most demanding application.

**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STF10N62K3	10N62K3	TO-220FP	Tube
STI10N62K3	10N62K3	I <sup>2</sup> PAK	Tube
STP10N62K3	10N62K3	TO-220	Tube



**Figure 1. Internal schematic diagram**



## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Revision history</b> .....	<b>13</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, I <sup>2</sup> PAK	TO-220FP	
V <sub>DS</sub>	Drain source voltage	620		V
V <sub>GS</sub>	Gate-source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	8.4	8.4 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	5.2	5.2 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	33.6	33.6 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	125	30	W
I <sub>AR</sub>	Max current during repetitive or single pulse avalanche (pulse width limited by T <sub>JMAX</sub> )	8		A
E <sub>AS</sub>	Single pulse avalanche energy <sup>(3)</sup>	220		mJ
dv/dt <sup>(4)</sup>	Peak diode recovery voltage slope	12		V/ns
V <sub>ESD(G-S)</sub>	Gate source ESD (HBM C=100 pF, R=1.5 kΩ)	2500		V
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)		2500	V
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed

2. Pulse width limited by safe operating area

3. Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = I<sub>AR</sub>, V<sub>DD</sub> = 50 V

4. I<sub>SD</sub> ≤ 8.4 A, di/dt = 400 A/μs, V<sub>Peak</sub> < V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220, I <sup>2</sup> PAK	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.00	4.17	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5		°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300		°C

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	620			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> =125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A		0.68	0.75	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4 A	-	6	-	S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	1250 138 16	-	pF pF pF
C <sub>o(tr)</sub> <sup>(2)</sup>	Equivalent capacitance time related	V <sub>DS</sub> = 0 to 496 V, V <sub>GS</sub> = 0	-	56	-	pF
C <sub>o(er)</sub> <sup>(3)</sup>	Equivalent capacitance energy related	V <sub>DS</sub> = 0 to 496 V, V <sub>GS</sub> = 0	-	38	-	pF
R <sub>G</sub>	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	3.5	-	Ω
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 496 V, I <sub>D</sub> = 8 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 18</a> )	-	42 7.4 23	-	nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%
2. C<sub>oss eq.</sub> time related is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>
3. C<sub>oss eq.</sub> energy related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310 \text{ V}$ , $I_D = 4 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 17</a> )	-	14.5	-	ns
$t_r$	Rise time			15		ns
$t_{d(off)}$	Turn-off-delay time			41		ns
$t_f$	Fall time			31		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				33.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8 \text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 22</a> )	-	320		ns
$Q_{rr}$	Reverse recovery charge			2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			13		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 22</a> )	-	410		ns
$Q_{rr}$	Reverse recovery charge			2.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			14		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, I<sup>2</sup>PAK

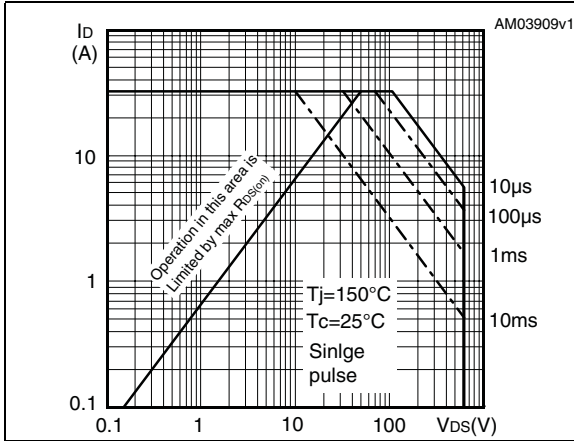


Figure 3. Thermal impedance for TO-220, I<sup>2</sup>PAK

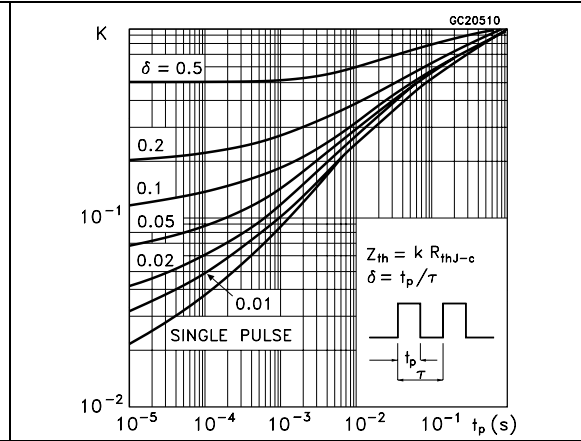


Figure 4. Safe operating area for TO-220FP

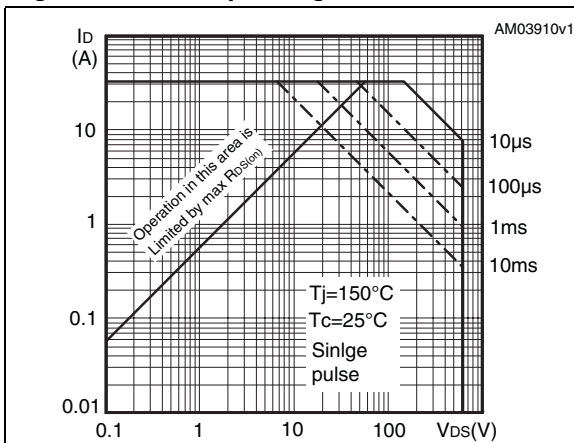


Figure 5. Thermal impedance for TO-220FP

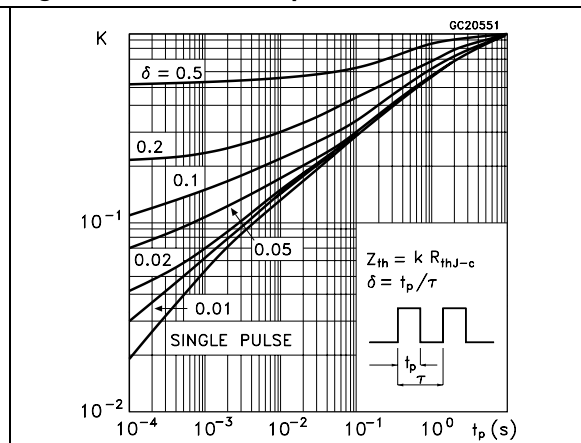


Figure 6. Output characteristics

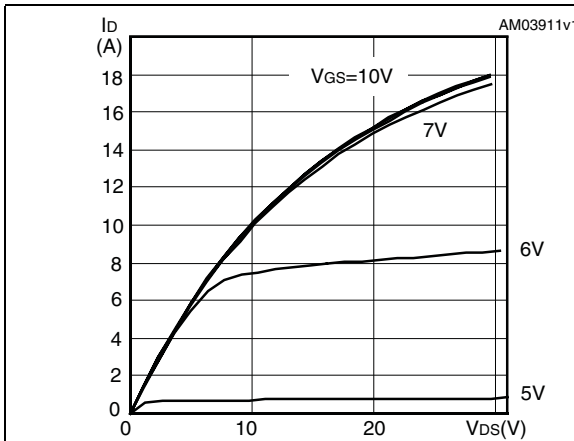
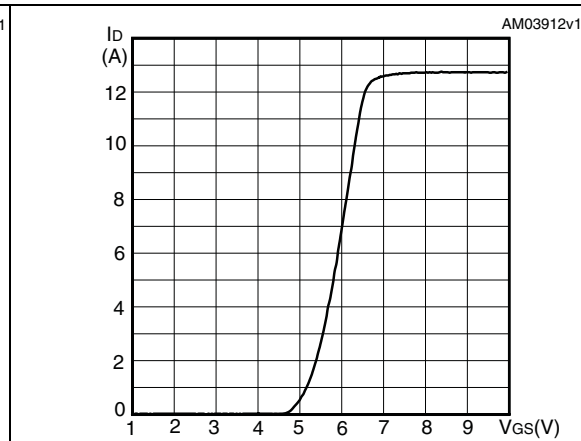
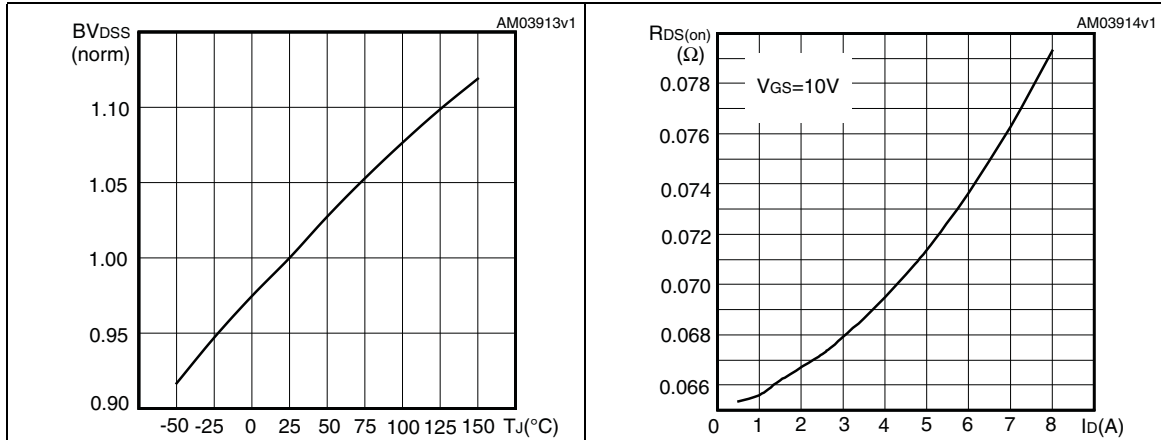


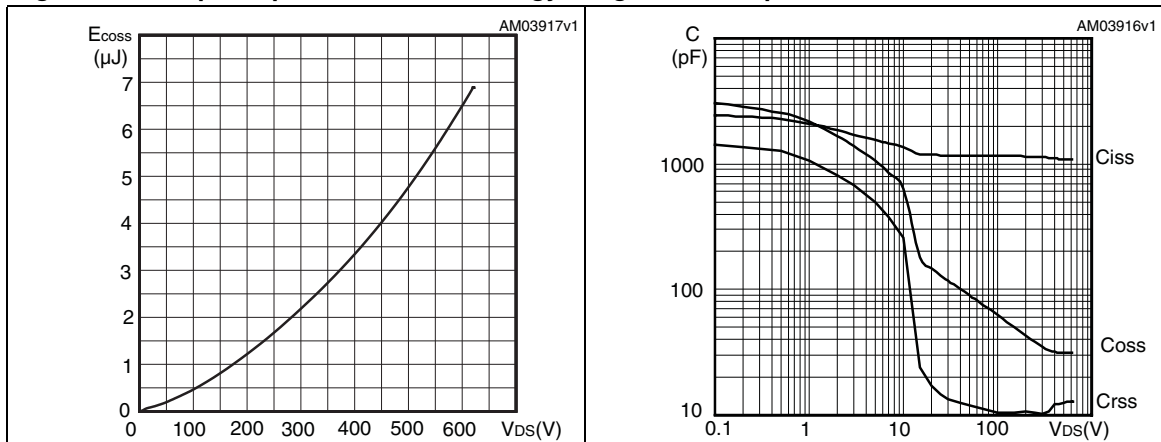
Figure 7. Transfer characteristics



**Figure 8. Normalized  $BV_{DSS}$  vs temperature** **Figure 9. Static drain-source on resistance**



**Figure 10. Output capacitance stored energy** **Figure 11. Capacitance variations**



**Figure 12. Gate charge vs gate-source voltage** **Figure 13. Normalized on resistance vs temperature**

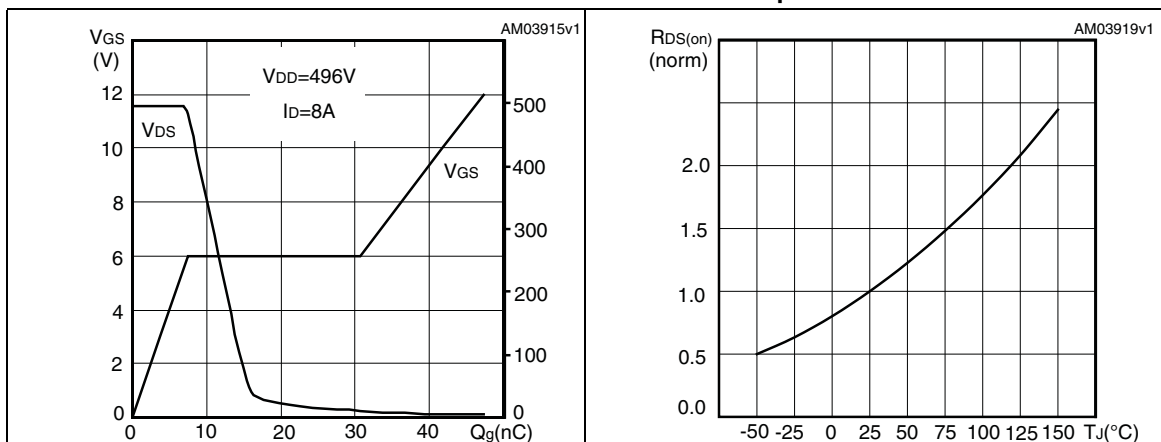


Figure 14. Normalized gate threshold voltage vs temperature

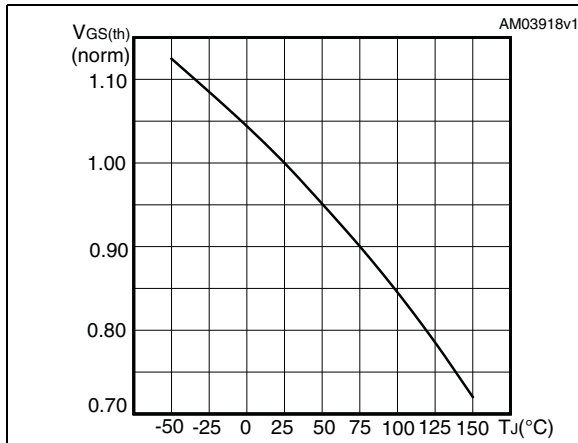


Figure 15. Maximum avalanche energy vs temperature

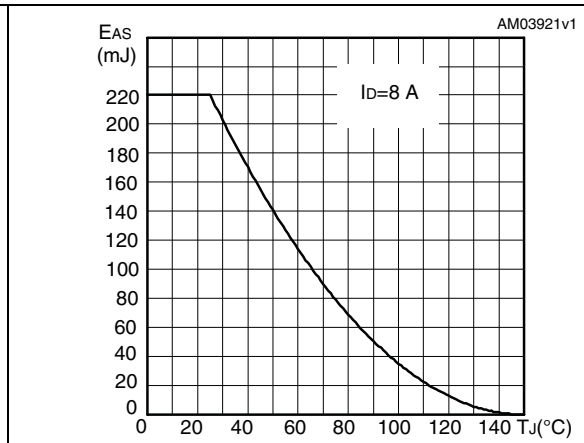
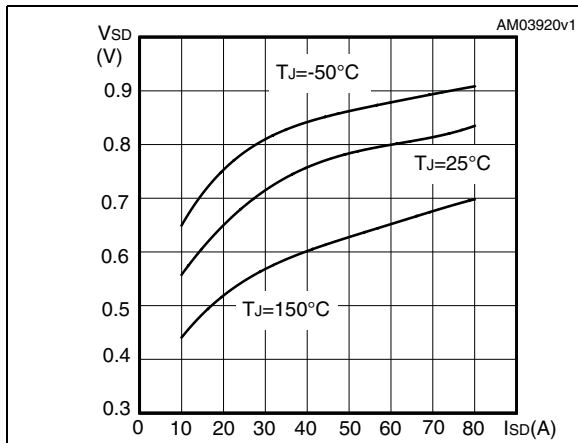


Figure 16. Source-drain diode forward characteristics





### 3 Test circuits

Figure 17. Switching times test circuit for resistive load

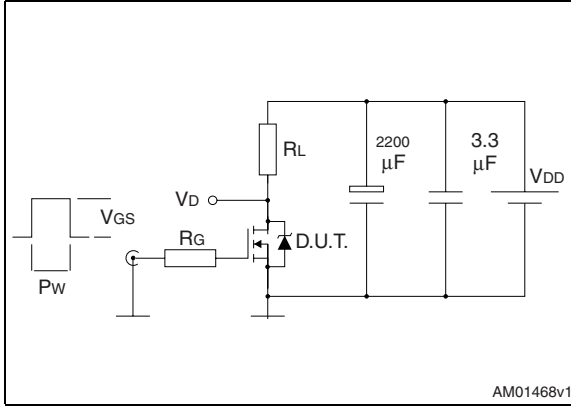


Figure 18. Gate charge test circuit

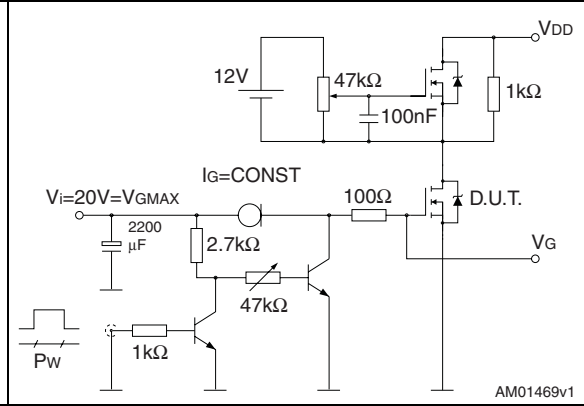


Figure 19. Test circuit for inductive load switching and diode recovery times

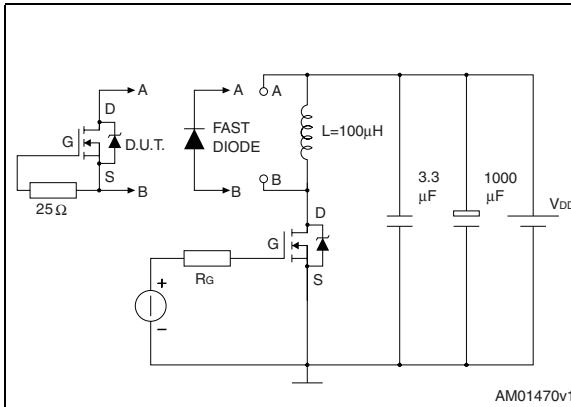


Figure 20. Unclamped inductive load test circuit

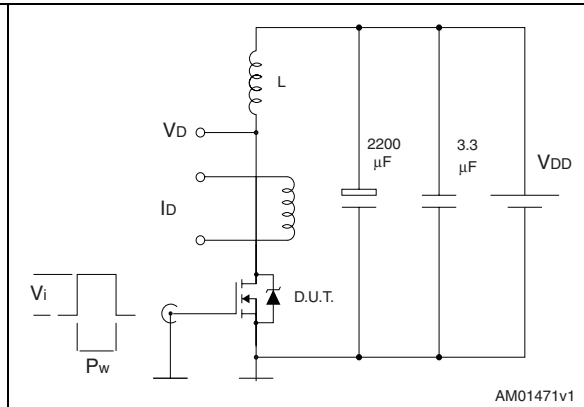


Figure 21. Unclamped inductive waveform

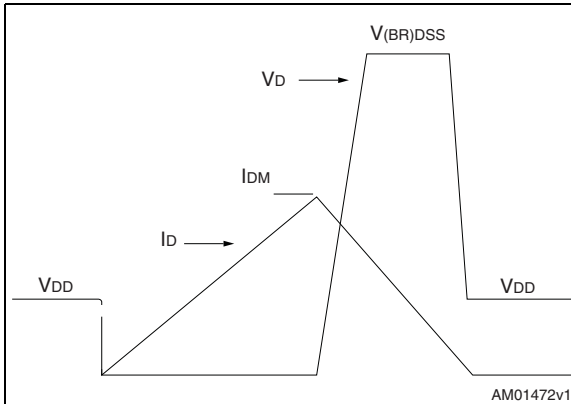
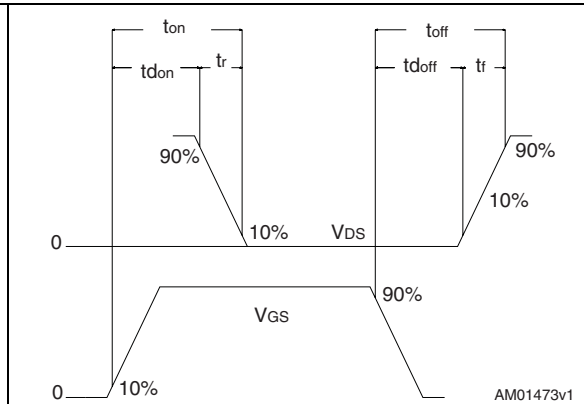


Figure 22. Switching time waveform

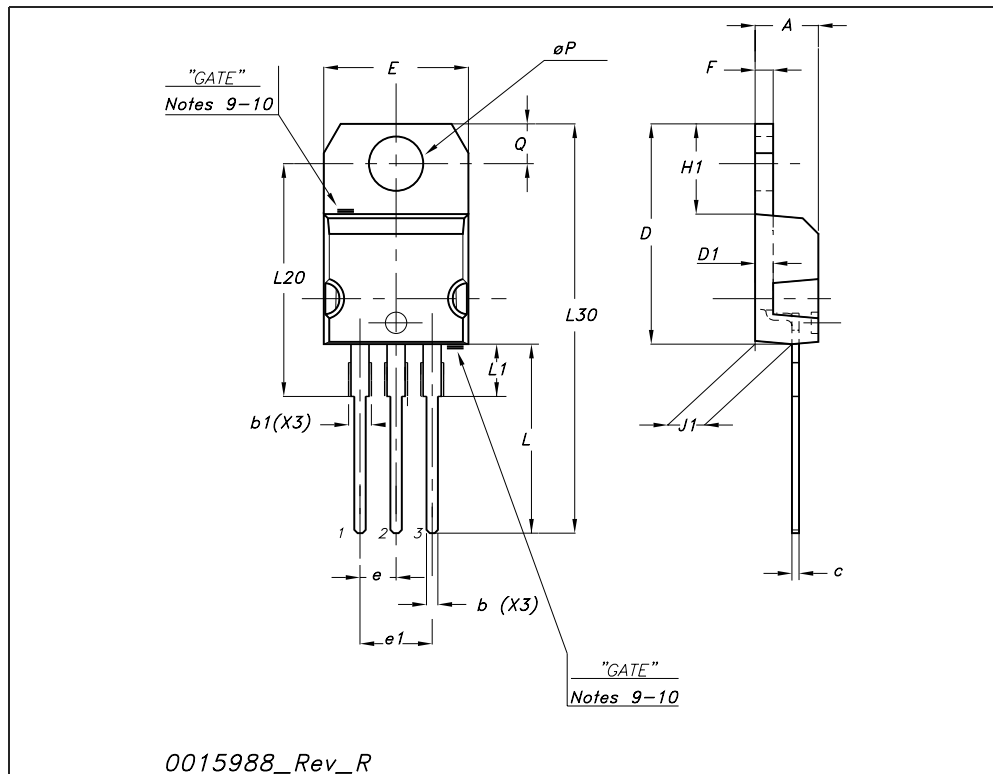


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

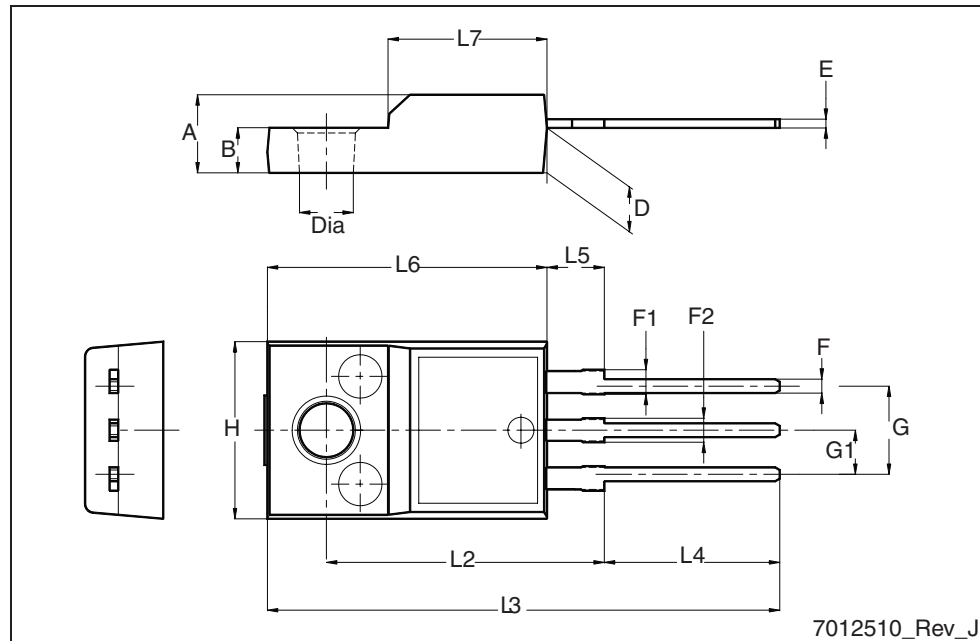
## TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



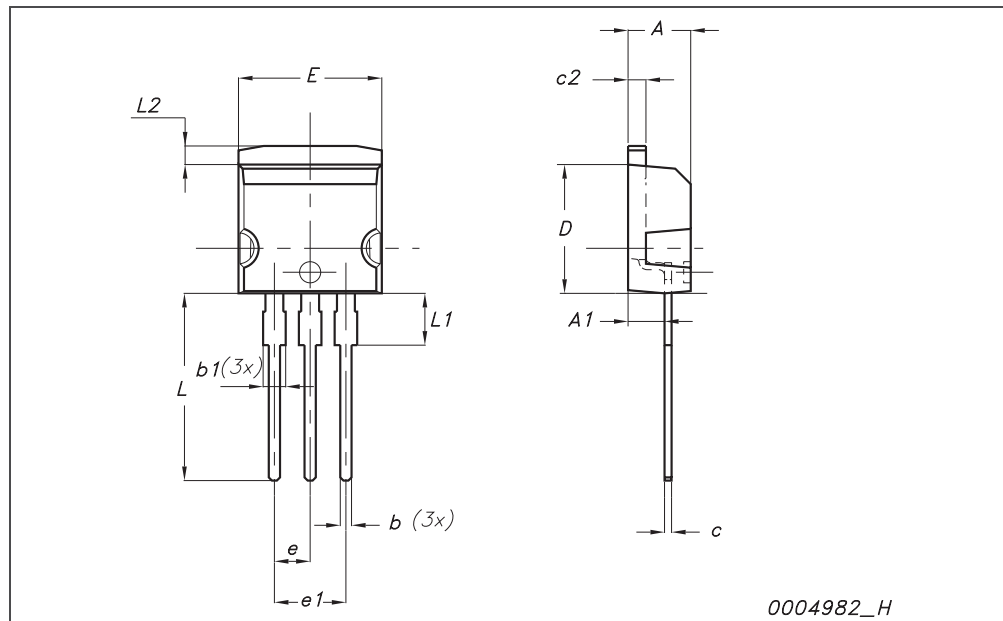
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



I<sup>2</sup>PAK (TO-262) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
08-Jun-2009	1	First release.
22-Jun-2009	2	Added new package, mechanical data: I <sup>2</sup> PAK

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2009 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

