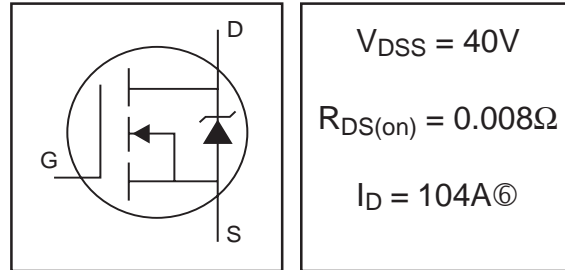


# IRL1104SPbF

# IRL1104LPbF

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRL1104S)
- Low-profile through-hole (IRL1104L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



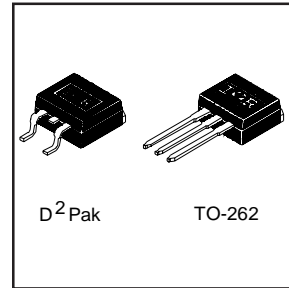
$V_{DS} = 40V$   
 $R_{DS(on)} = 0.008\Omega$   
 $I_D = 104A\text{⑥}$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRL1104L) is available for low-profile applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V\text{⑤}$	104⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V\text{⑤}$	74⑥	
$I_{DM}$	Pulsed Drain Current ①⑤	416	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.4	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	167	W
	Linear Derating Factor	1.1	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑤	340	mJ
$I_{AR}$	Avalanche Current①	62	A
$E_{AR}$	Repetitive Avalanche Energy①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient(PCB Mounted, steady-state)**	—	40	

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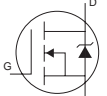
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07/19/04

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>⑤</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.008	W	V <sub>GS</sub> = 10V, I <sub>D</sub> = 62A <sup>④</sup>
		—	—	0.012		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 52A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	—	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	53	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 62A <sup>⑤</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	—	68	nC	I <sub>D</sub> = 62A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	24		V <sub>DS</sub> = 32V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	34		V <sub>GS</sub> = 4.5V, See Fig. 6 and 13 <sup>④⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	18	—		V <sub>DD</sub> = 20V
t <sub>r</sub>	Rise Time	—	257	—		I <sub>D</sub> = 54A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	32	—		R <sub>G</sub> = 3.6Ω, V <sub>GS</sub> = 4.5V
t <sub>f</sub>	Fall Time	—	64	—		R <sub>D</sub> = 0.4Ω, See Fig. 10 <sup>④⑤</sup>
L <sub>S</sub>	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C <sub>iss</sub>	Input Capacitance	—	3445	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1065	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	270	—		f = 1.0MHz, See Fig. 5 <sup>⑤</sup>

**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	104 <sup>⑥</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	416		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 62A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	84	126	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 62A
Q <sub>rr</sub>	Reverse Recovery Charge	—	223	335	nC	di/dt = 100A/μs <sup>④⑤</sup>
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 15V, starting T<sub>J</sub> = 25°C, L = 0.18mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 62A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 62A, di/dt ≤ 217A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRL1104 data and test conditions.
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

\*\* When mounted on 1" square PCB ( FR-4 or G-10 Material ).  
For recommended footprint and soldering techniques refer to application note #AN-994.

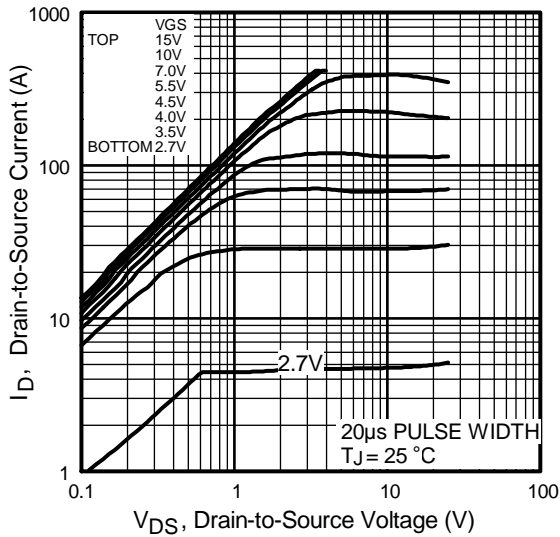


Fig 1. Typical Output Characteristics

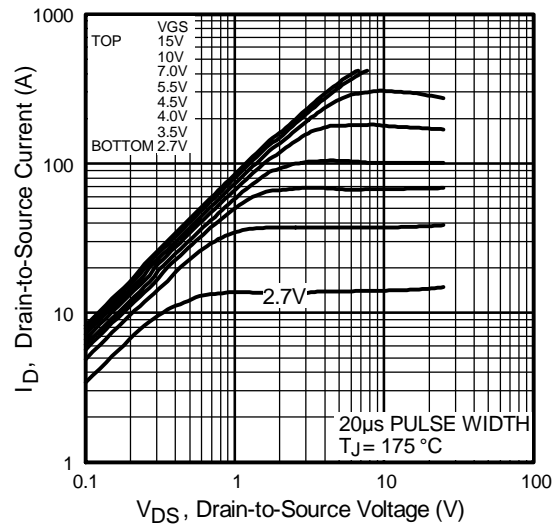


Fig 2. Typical Output Characteristics

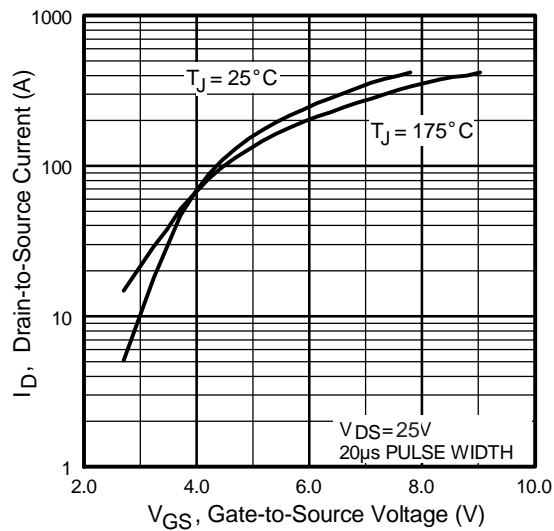


Fig 3. Typical Transfer Characteristics

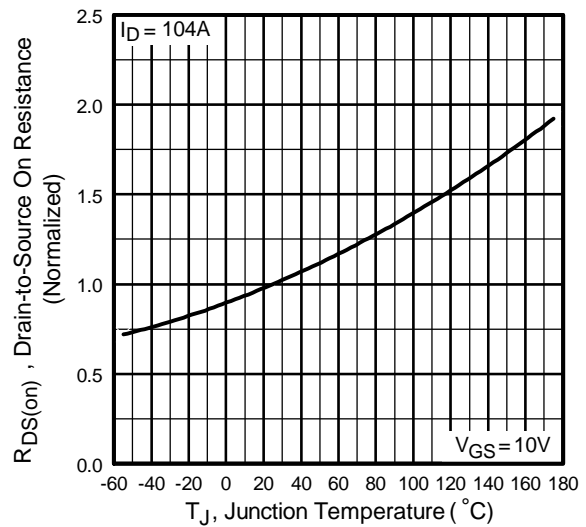


Fig 4. Normalized On-Resistance Vs. Temperature

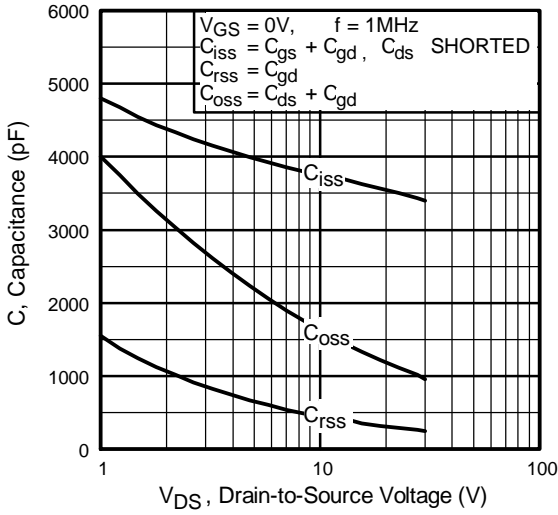


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

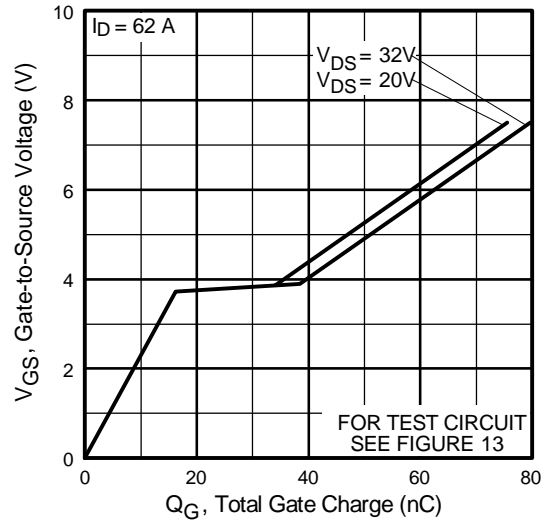


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

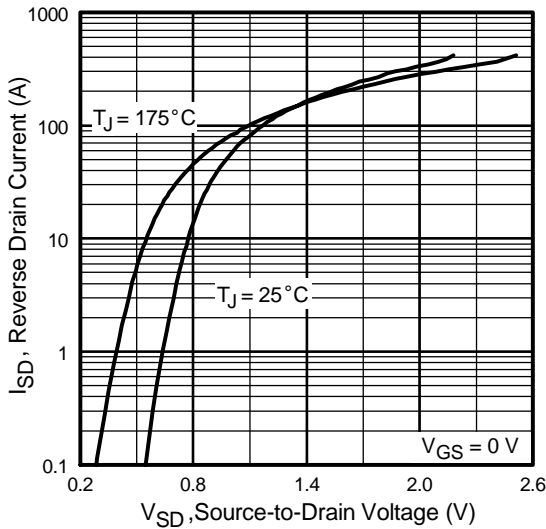


Fig 7. Typical Source-Drain Diode Forward Voltage

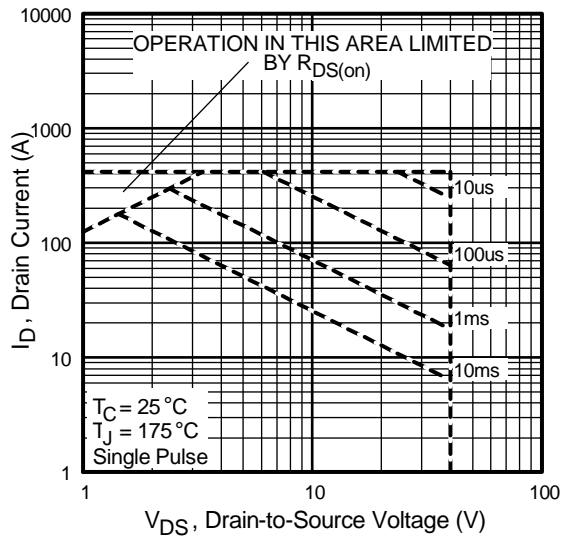


Fig 8. Maximum Safe Operating Area

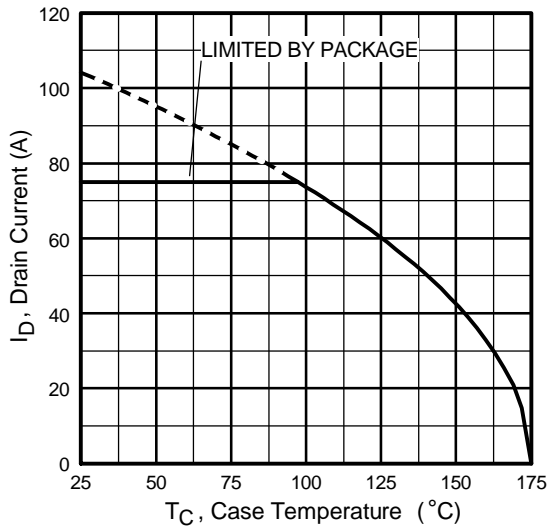


Fig 9. Maximum Drain Current Vs. Case Temperature

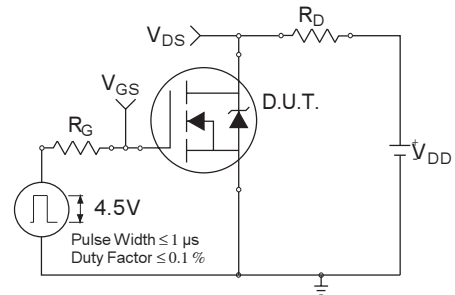


Fig 10a. Switching Time Test Circuit

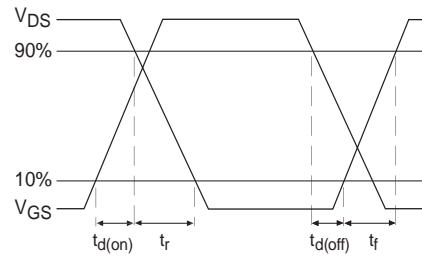


Fig 10b. Switching Time Waveforms

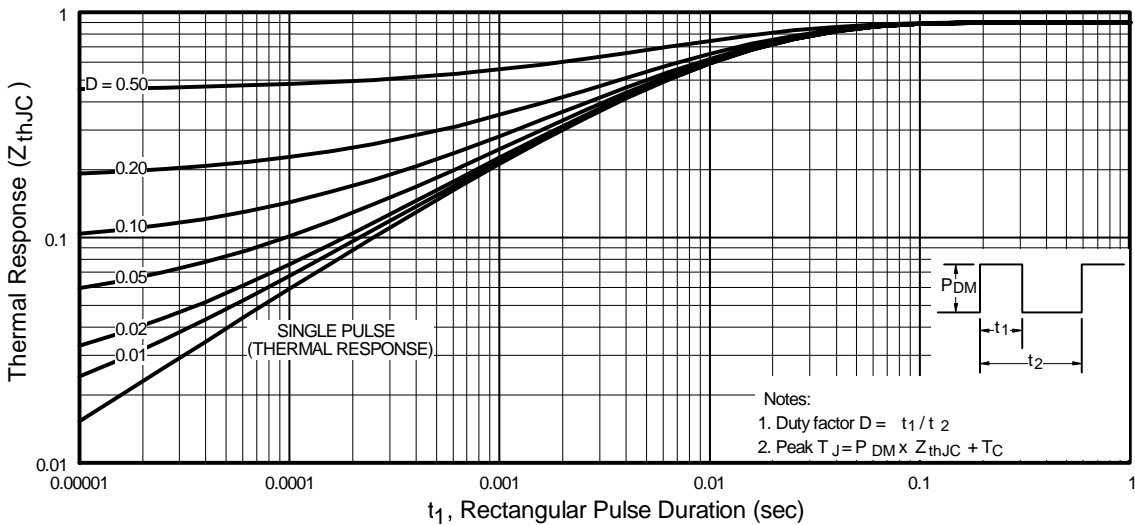


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

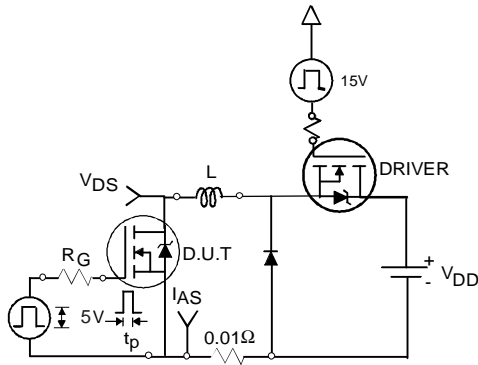


Fig 12a. Unclamped Inductive Test Circuit

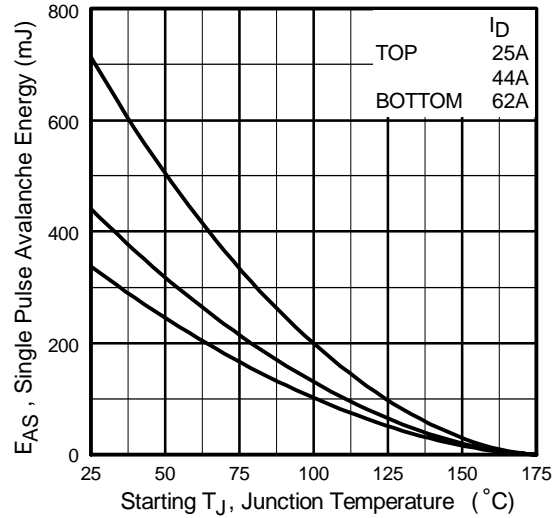


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

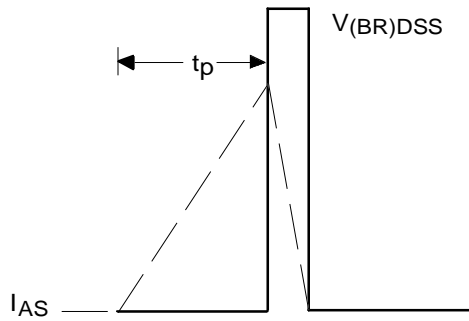


Fig 12b. Unclamped Inductive Waveforms

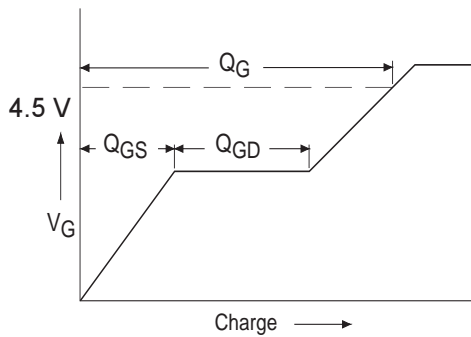


Fig 13a. Basic Gate Charge Waveform

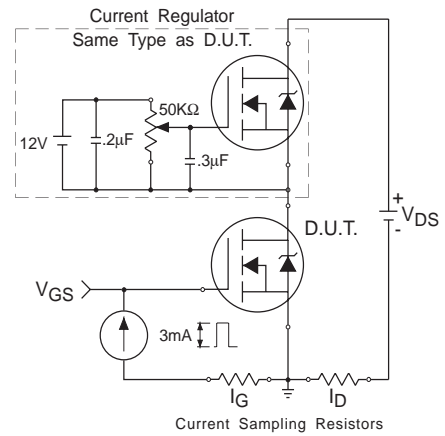
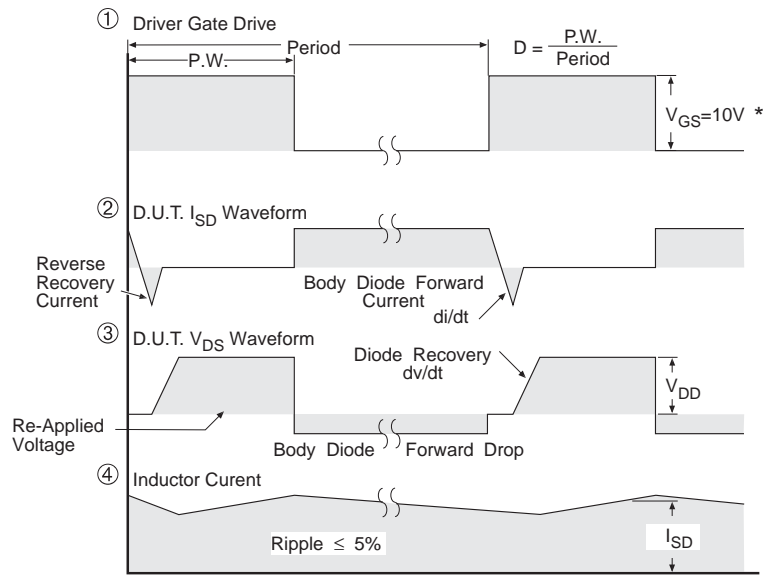
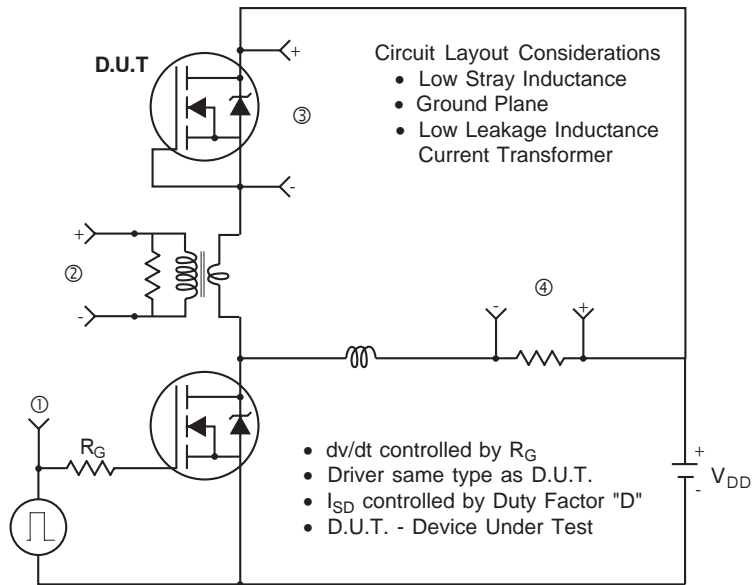


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

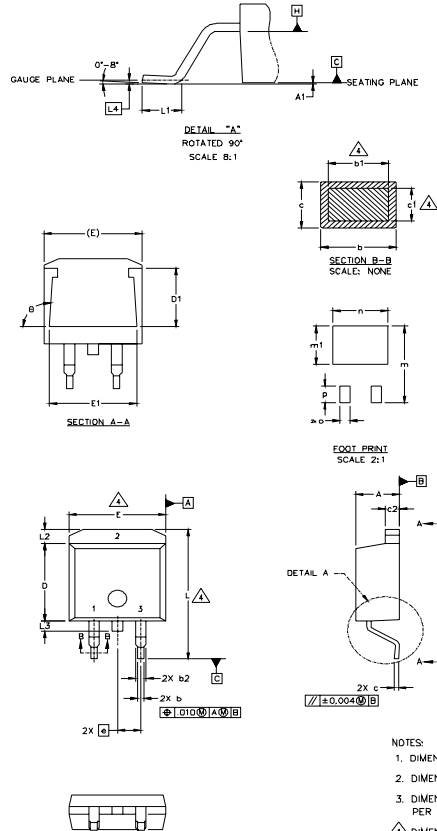
Fig 14. For N-Channel HEXFETS

# IRL1104S/LPbF

International  
**IR** Rectifier

## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	0.127		.005		
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33	.210			
E	9.65	10.67	.380	.420	3
E1	6.22	.245			
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2	1.65		.065		
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78	.700			
m1	8.89	.350			
n	11.43	.450			
o	2.08	.082			
p	3.81	.150			
theta	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

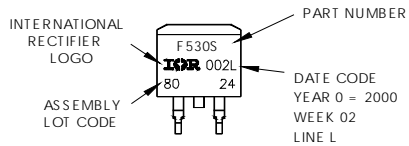
\* PART DEPENDENT.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [ .005" ] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

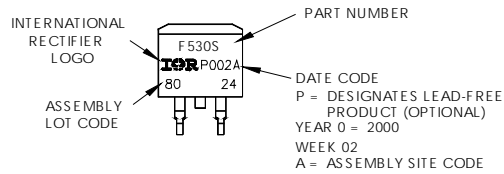
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"



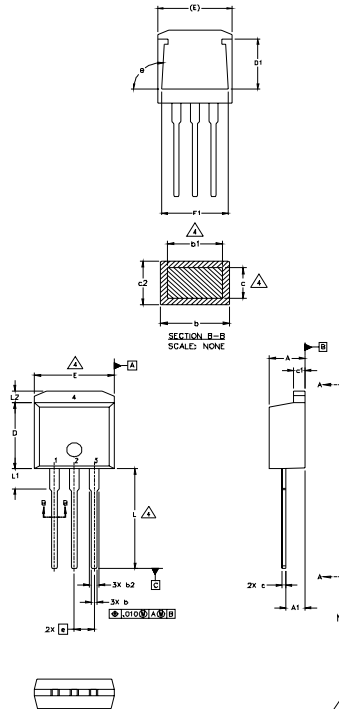
**OR**





TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

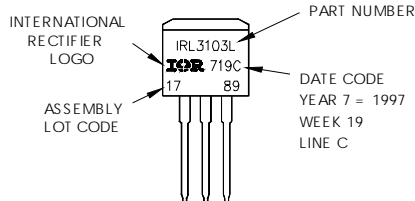
LEAD ASSIGNMENTS

HEXFET	IGBT
1.- GATE	1 - GATE
2.- DRAIN	2 - COLLECTOR
3.- SOURCE	3 - EMITTER
4.- DRAIN	

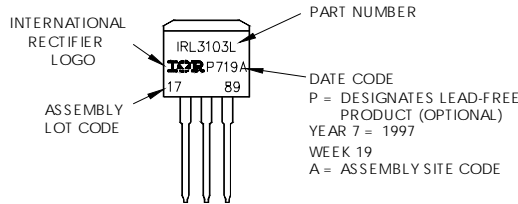
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
 Note: "P" in assembly line  
 position indicates "Lead-Free"



OR

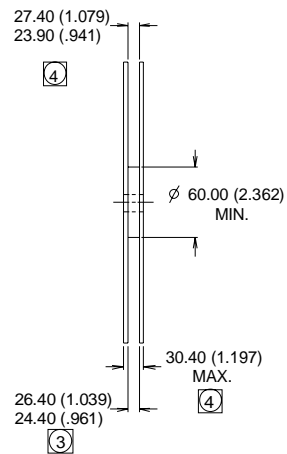
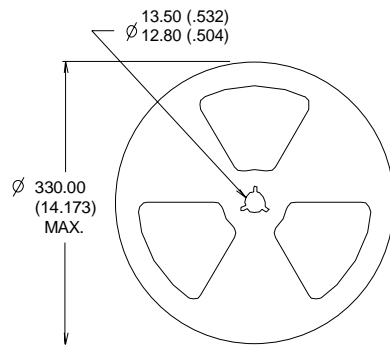
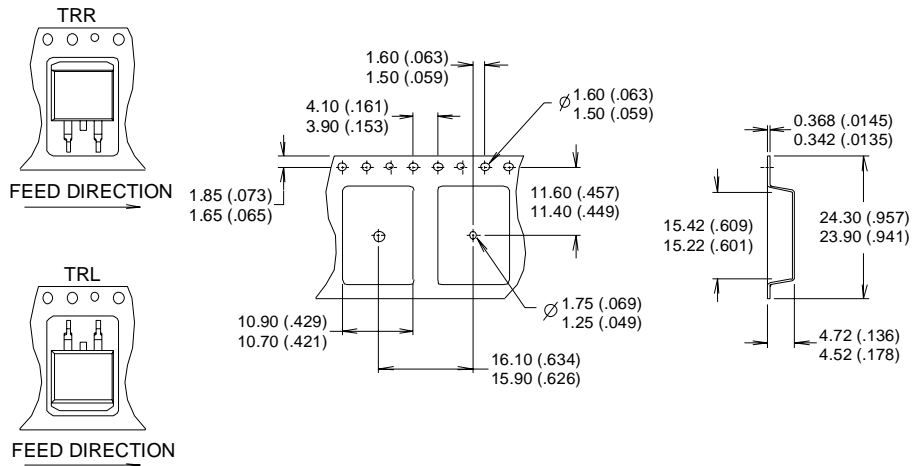


# IRL1104S/LPbF

International  
**IOR** Rectifier

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.

International  
**IOR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>